Symmetric Dual-Switch Converter

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***Abstract*—High step-up dc/dc converters are widely used in many industrial applications, especially in green energy power generation and uninterruptible power systems. The circuit configuration of a dual-switch high step-up dc/dc converter is very simple and the converter can achieve a high step-up voltage gain by operating in parallel charge and series discharge. However, this converter has a strict requirement of the parameter's consistency or it will lead to the high voltage stress of switches due to parasitic capacitance and inductor's resonance. Although passive lossless clamp circuit can be adopted to realize the voltage balance of switches in steady state, unbalance voltage still exists in dynamic state owing to an unsymmetrical structure. Therefore, this article proposed a dual-switch converter with symmetric topology, which can realize the voltage balance of switches and capacitors in both steady and dynamic states. According to the proposed converter, a prototype rated at 200 W has been established in the lab and the experimental results verify the accuracy of the analysis.**

***Index Terms*—High step-up voltage gain, symmetric, voltage balance.**

I. Introduction

BECAUSE of environmental problems, new clean energy sources have been developed rapidly. However, for some new energy power system, the output voltage of fuel cell system and photovoltaic system are relatively low. In order to inject these powers into the grid or to be used as uninterruptible power supplies, high-gain dc/dc converter is applied to convert low-voltage dc into high-level dc voltage [1]. However, it is hard to achieve both high-voltage conversion ratio and high efficiency at the same time with the traditional boost converter. High step-up dc/dc converters have been widely used [2], [3].

Various topologies have been developed to provide a high step-up with an extremely high turns ratio of the high-frequency transformer. However, high turns ratio may increase the leakage inductance of the transformer and lead to the voltage spike and high voltage stress of the power devices. Moreover, it also results in high-voltage stress and serious reverse recovery of secondary-side diodes [4]–[6]. Besides, those isolated converters have no advantage in the cost of implementation.

In the situations without the need of electrical isolation, non-isolated dc/dc converter has some advantages of simple electric energy conversion process, high efficiency, power density, and low cost because of no transformer [7]. In order to achieve high gain transformation, nonisolated high-gain dc/dc converters can be generalized as cascade type, coupled inductor type, and switched capacitor type. Cascade converters can get high gain by multistage power conversion. But the topologies are too complex and the power loss is high with multistage power conversion. Moreover, the problem of system instability and high-voltage stress across power devices still exist [8]–[13]. A number of coupled inductor-based high step-up converters have been developed to achieve the high voltage gain by increasing the turns ratio of the coupled inductor. However, the leakage inductance of the coupled inductor is inevitable, which may cause voltage spikes and high-voltage stress when the switch turns OFF. Various passive and active voltage clamping strategies which can suppress the voltage spike effectively and improve the efficiency significantly have been developed with additional cost of the components [14]–[18]. The number of capacitors and diodes also substantially increases along with the increase of the voltage gain ratio in the switched-capacitor-based converters. But working state of the converters is often accompanied by the problem of current spike, which not only increases current stress of the switches but also causes serious problems of EMI [19]–[21].

Yang *et al.* [22] present a nonisolated high-gain dual-switch converter that can realize the parallel charging and series discharging of two inductors through the synchronous ON–OFF of two switches S1 and S2. It has the advantages of simple structure, low switch voltage/current stress, and high voltage gain. However, in this topology, it is difficult to achieve consistency of the device parameters. So in actual situations, the resonance between switch junction capacitors and inductors can easily occur, which may cause the problem of unequal voltage across switches. Tang *et al.* [23] propose a passive lossless clamp for

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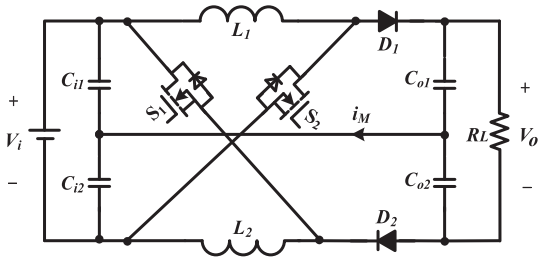

Fig. 1. Dual-switch high step-up dc/dc converter with symmetric topology.

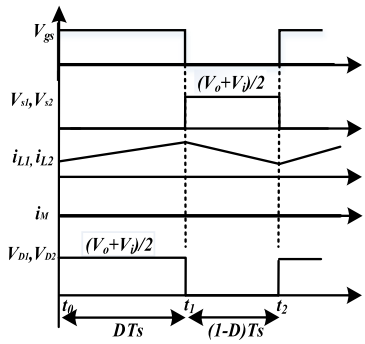

Fig. 2. Key waveforms of CCM operation.

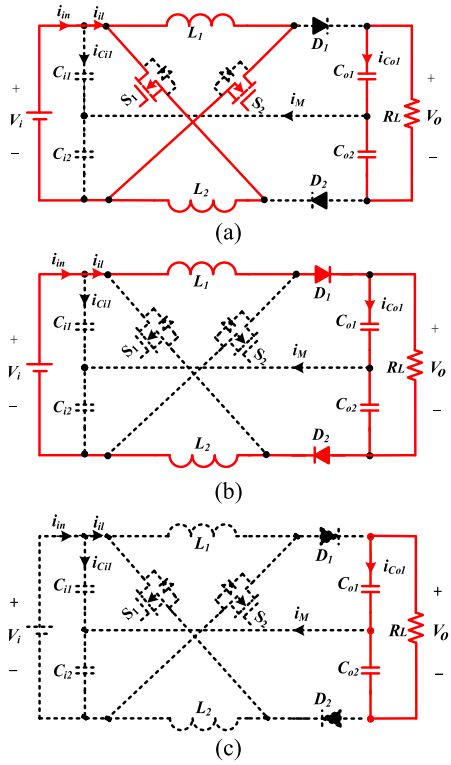

Fig. 3. Equivalent circuit of the converter.

dual-switch converter to suppress the resonance in steady state and balance the voltage stress across the switches. Due to the asymmetry of the circuit structure, it is hard to realize the balance of switches under dynamic operating conditions. As compared to the asymmetric structure, symmetric converters with balanced switching operation can reduce the common-mode conducted noise effectively [24].

This article presents a dual-switch high step-up dc/dc converter with symmetric topology. It can achieve voltage balance of switches under dynamic and steady conditions. At the same time, it has advantages like high voltage gain, low voltage stress on the components, and simple structure. The operational analysis under different working modes has been discussed and a prototype has been established in the lab. The simulation and experimental results are given to verify the analysis.

II. Operation Principle

As shown in Fig. 1, a dual-switch high step-up dc/dc converter with symmetric topology has been presented. The converter changes the connection of inductors L_1, L_2 by controlling the ON–OFF of switches S_1 and S_2 to get high-voltage gain. Because the voltage of capacitors cannot be changed suddenly, the voltage of S_2 is clamped by capacitors C_{o1}, C_{i2} and the voltage of S_1 is clamped by C_{o2} and C_{i1}. Owing to the symmetry of the structure, the converter can achieve voltage balance of switches both in steady and dynamic circumstances. The analyses of continuous conduction mode (CCM), discontinuous conduction mode (DCM), and boundary conduction mode (BCM) are being discussed.

A. Analysis of Operation Modes

Under CCM operation, Fig. 2 illustrates the key waveforms of the proposed converter. In order to facilitate the analysis, all the components are supposed to be ideal.

1) The input voltage V_i and output voltage V_o are constant.
2) $L_1 = L_2 = L$, $C_{i1} = C_{i2}$, $C_{o1} = C_{o2}$.
3) The capacitances of switches are ignored and the diodes are ideal.

According to key waveforms and equivalent circuits which are shown in Figs. 2 and 3, there are two main modes in CCM operation, which depends on the state of switching signal V_{gs}.

1) Mode 1 $[t_0, t_1]$: The equivalent circuit is shown in Fig. 3(a). The switches S_1, S_2 are turned ON and the diodes D_1, D_2 are turned OFF during this time interval. The inductors L_1, L_2 are charged by the input power V_i, and the current through inductors increases linearly. The voltage across the inductors can be expressed as

$$L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} = V_i \tag{1}$$

2) Mode 2 $[t_1, t_2]$: At t_1, diodes D_1, D_2 are turned ON, and the load is discharged by inductors L_1, L_2. The equivalent circuit is shown in Fig. 3(b). The voltages across the inductors are

$$\begin{cases} V_{L1} = V_{Ci1} - V_{Co1} \\ V_{L2} = V_{Ci2} - V_{Co2}. \end{cases} \tag{2}$$

Under DCM operation, according to the key waveforms of the converter shown in Fig. 4, Modes 1 and 2 are the same as CCM; the main difference is that there is no current flowing

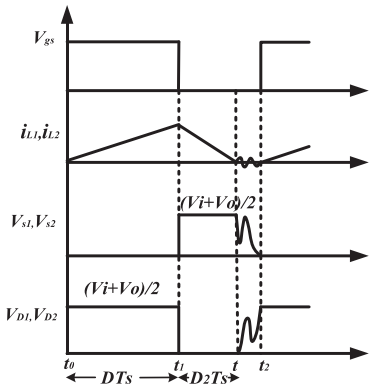

Fig. 4. Key waveform of DCM operation.

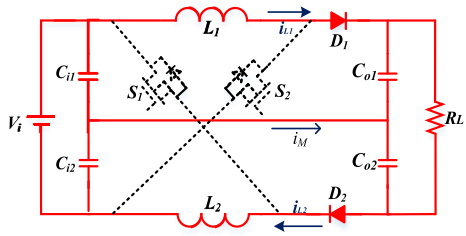

Fig. 5. Mode 2 in the condition of unbalanced inductors.

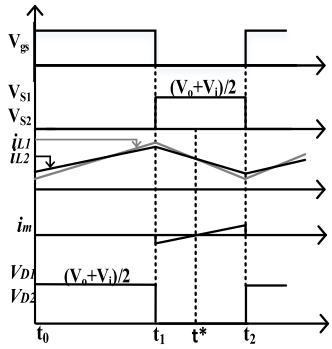

Fig. 6. Key waveform of the converter in the condition of unbalanced inductors.

in inductors after t'; as shown in Fig. 3(c), the load only gets charged by V_{CO1} and V_{CO2}.

B. CCM Operation With Unbalanced Inductors

Actually, it is difficult to keep the two inductors consistent and this article assumes that L_1 is less than L_2. As shown in Fig. 5, for CCM with unbalanced inductors, the main difference is that Mode 2 is different. During $t_1 - t^*$, the current flowing path is shown in Fig. 5 and the direction of i_M is from the output side to the input side; during $t^* - t_2$, the direction of i_M is from the input side to the output side. Fig. 6 illustrates the key waveforms of the converter in the condition of unbalanced inductors.

Under high frequency, the current in the middle line only affects the voltage ripple of the input and output capacitors, the voltage ripple is very small, and it has very little impact on the average voltage of the input and output capacitors. Therefore, the voltage balance of the input and output capacitors can be remained, and the voltage stress of the switches can be derived as

$$\begin{cases} V_{S1} = \frac{1}{2}(V_{Ci1} + V_{Co2}) = \frac{1}{2}(V_i + V_o) \\ V_{S2} = \frac{1}{2}(V_{Ci2} + V_{Co1}) = \frac{1}{2}(V_i + V_o). \end{cases} \tag{3}$$

III. Circuit Performance Analysis Under Steady State

A. Voltage Conversion Ratio

In order to simplify the analysis, assumptions are shown as follows. The values of capacitors C_{i1}, C_{i2}, C_{o1}, and C_{o2} are large enough, and input and output voltages are constant, so

$$\begin{cases} V_{Ci1} = V_{Ci2} = \frac{1}{2}V_i \\ V_{Co1} = V_{Co2} = \frac{1}{2}V_o. \end{cases} \tag{4}$$

According to the voltage-second balance on the inductors L_1, L_2

$$D \cdot V_i + (1 - D) \cdot (V_{Ci1} - V_{Co1}) = 0 \tag{5}$$

$$D \cdot V_i + (1 - D) \cdot (V_{Ci2} - V_{Co2}) = 0. \tag{6}$$

Simplifying (5) and (6), the voltage gain of the CCM operation is

$$G_{\mathrm{CCM}} = \frac{V_o}{V_i} = \frac{1 + D}{1 - D}. \tag{7}$$

B. DCM Voltage-Conversion Ratio and BCM

Under DCM operation, during the time when the switches are ON, the inductors' current increases, and its peak current is

$$i_{L1p} = i_{L2p} = \frac{V_i D T_s}{L}. \tag{8}$$

During the time when the switches are OFF, the inductors' current decreases, and its peak current is

$$i_{L1p} = i_{L2p} = \frac{(V_o - V_i) D_2 T_s}{2L} \tag{9}$$

where $D_2 T_s$ is the duration time of Mode 2.

From (8) and (9), D_2 can be derived as follows:

$$D_2 = \frac{2V_i}{V_o - V_i} D. \tag{10}$$

The output capacitor's average current is zero throughout the whole period, so

$$I_o = \frac{i_{L1p} D_2}{2} = \frac{V_o}{R_L}. \tag{11}$$

Substituting (8) and (10) into (11), G_{DCM} is derived as

$$G_{\mathrm{DCM}} = \frac{1}{2} + \sqrt{\frac{1}{4} + \frac{D^2}{\tau}} \tag{12}$$

where the time constant τ is defined as $\tau = L f_s / R_L$.

If the proposed converter operates in BCM, the voltage gains under CCM and DCM operation are equal. According to (7) and (12), the boundary-normalized inductor time constant can

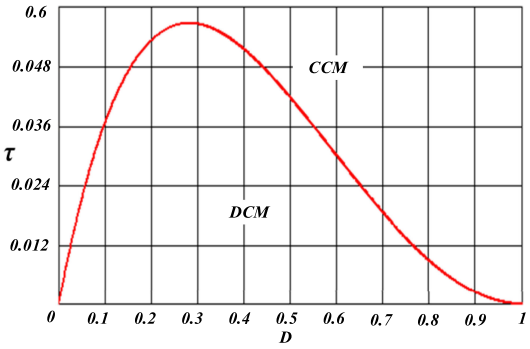

Fig. 7. Boundary condition of the proposed converter.

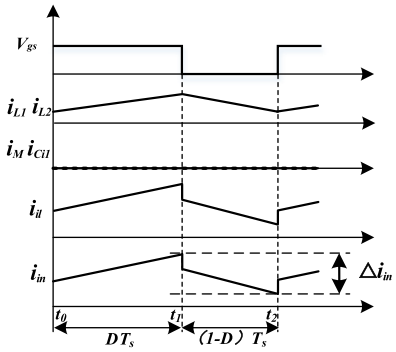

Fig. 8. Current waveforms of converter.

be derived as

$$\tau_B = \frac{D(1-D)^2}{2(1+D)}. \tag{13}$$

The boundary condition of the proposed converter is shown in Fig. 7. If τ is larger than τ_B, the proposed converter is operated in CCM.

C. Voltage and Current Stress of the Power Devices

According to the analysis of CCM operation modes, the voltage and current stress of power switches and diodes, respectively, are

$$V_{D1} = V_{D2} = V_{S1} = V_{S2} = \frac{1}{1+D} V_o. \tag{14}$$

$$\begin{cases} I_{S1} = I_{S2} = I_L + \Delta I_L = I_o + \frac{V_o(1-D)D}{2Lf_s(1+D)} \\ I_{D1} = I_{D2} = I_L + \Delta I_L = I_o + \frac{V_o(1-D)D}{2Lf_s(1+D)}. \end{cases} \tag{15}$$

The voltage stress of each power device is lower than the output voltage.

D. Input Current Ripple

All the components are supposed to be ideal, and L_1 is the same as L_2. Fig. 8 illustrates the current waveforms of converter. The current through inductors L_1, L_2 and the input capacitor C_{i1} can be expressed as

$$i_{L1} = i_{L2} = \begin{cases} I_L(t_0) + \frac{V_i}{L}(t-t_0) & t_0 \le t < t_1 \\ I_L(t_1) + \frac{V_i - V_o}{2L}(t-t_2) & t_1 \le t < t_2 \end{cases} \tag{16}$$

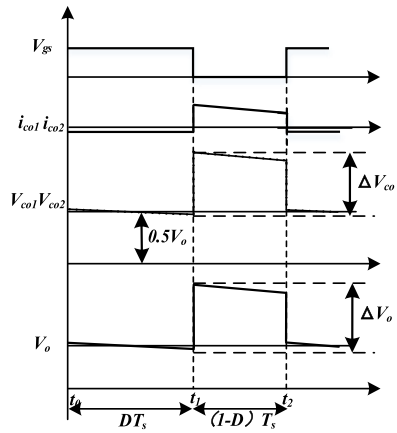

Fig. 9. Voltage waveforms of converter.

$$i_{ci1} = \frac{1}{2} i_M = 0. \tag{17}$$

Therefore, the input current can be achieved

$$i_{\text{in}} = \begin{cases} \frac{2V_o}{L(1+D)} - \frac{V_o(1-D)D}{f_s L(1+D)} + \frac{2V_o(1+D)}{L(1+D)}(t-t_0) & t_0 \le t < t_1 \\ i\frac{V_o}{L(1+D)} + \frac{V_o(1-D)D}{2f_s L(1+D)} - \frac{DV_o}{L(1+D)}(t-t_2) & t_1 \le t < t_2. \end{cases} \tag{18}$$

The ripple of input current can be expressed as

$$\Delta i_{\text{in}} = \frac{P_o}{V_o(1-D)} + \frac{3V_o(1-D)D}{2Lf_s(1+D)}. \tag{19}$$

E. Output Voltage Ripple

Considering that ESRs exist in the output capacitors, it has a big effect on the output voltage ripple. So, the analysis about output voltage ripple should consider ESRs (R_{co1} and R_{co2}) in the output capacitors, which is assumed equal to each other.

According to Fig. 9 and (8), the ripple of output voltage can be expressed as

$$\Delta V_o = \frac{2P_o D}{V_o f_s C_o} + \frac{D(1-D)T_s V_o R_{co}}{(1+D)L}. \tag{20}$$

F. Comparison With Boost Converters

As shown in Table I and Fig. 10, the proposed converter has a higher voltage gain and simpler structure than other boost converters. The voltage stress on the switches and diodes are also lower than these converters except the three-level boost converter. However, current stress on the switches and diodes is much lower than the three-level boost converter due to the parallel structure. Thus, performance of the proposed converter is superior to others.

IV. Design Considerations

In order to have a proper operation, the components of the proposed converter should be designed appropriately. There are

TABLE I
COMPARISON BETWEEN THE PROPOSED CONVERTER AND OTHER CONVERTERS

Parameter	Proposed converer	Three-level boost converter	Boost converter	Reference [25]	Reference [26]
Voltage	$\frac{1+D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{2D}{1-D}$
Vs-stress	$\frac{V_o}{1+D}$	$\frac{V_o}{2}$	V_o	V_o	$\frac{V_o}{2D}$
V_D-stress	$\frac{V_o}{1+D}$	$\frac{V_o}{2}$	V_o	V_o	$\frac{V_o}{2D}$
No of Switch	2	2	1	1	1
No of diode	2	2	1	2	2
No of inductor	2	2	1	2	2
No of capacitor	4	2	1	3	3
Is-stress	$\frac{\sqrt{D}}{1+D}I_{in}$	$\sqrt{D}I_{in}$	$\sqrt{D}I_{in}$	$\sqrt{D}I_{in}$	$\frac{\sqrt{D}}{1+D}I_{in}$
I_D-stress	$\sqrt{1-D}I_o$	$\sqrt{1-D}I_o$	$\sqrt{1-D}I_o$	$\sqrt{1-D}I_o$	$\sqrt{1-D}I_o$

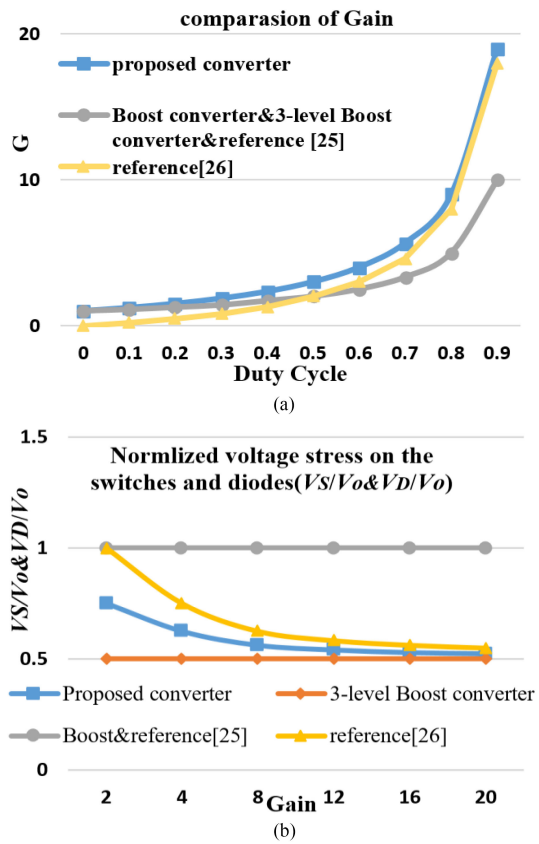

Fig. 10. Comparisons of the proposed converter with other converters. (a) Comparasion of gain. (b) Normalized voltage stress on the switches and diodes.

many disadvantages such as slow dynamic response, dependence on switching frequency, output power, and the value of the inductors. The proposed converter should be designed to operate under CCM condition. Therefore, the main equations to design the proposed converter in CCM operation are discussed here and validated by the experimental results in Section V.

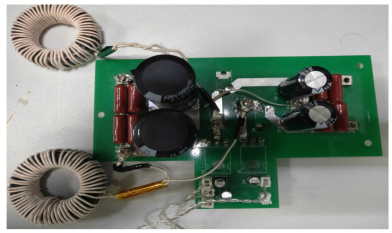

Fig. 11. Prototype of the proposed converter.

TABLE II
EXPERIMENTAL CONDITIONS

Components	Parameters
V_i (input voltage)	20-40V
V_o (output voltage)	200V
P_o (rated power)	200W
f_s (switching frequency)	50kHz
S_1,S_2 (switches)	IRFP250
D_1,D_2 (diodes)	SF24
L_1,L_2 (inductors)	240μH
C_{i1},C_{i2} (input capacitors)	1000μF/50V
C_{o1},C_{o2} (output capacitors)	470μF/250V&CBB2.3μF

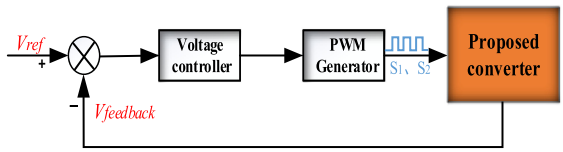

Fig. 12. Control strategy of the proposed converter.

A. Selection of Duty Cycle

According to (7), the converter duty cycle can be calculated as follows:

$$D = \frac{G-1}{G+1}. \tag{21}$$

B. Inductor Design

The current ripple of the inductors L_1 and L_2 are calculated by the same equation. The selection of the inductor depends on the inductor voltage (V_L), inductor ripple current $(\triangle i_L)$, switching frequency (f_s), and duty cycle (D). The voltage of the input inductance L_1 and L_2 is equal to V_i. Therefore, the inductance value of L_1 and L_2 can be expressed

$$L_1 = L_2 \geq \frac{V_i D T_s}{r i_L} \tag{22}$$

where $r = \triangle i_L / i_L$.

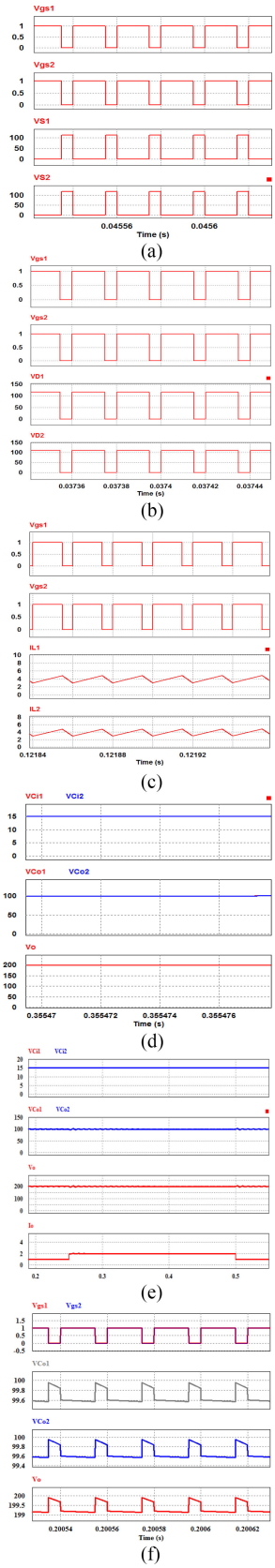

Fig. 13. Simulation waveforms of the proposed converter. (a) V_{gs1}, V_{gs2}, V_{S1}, V_{S2}. (b) V_{gs1}, V_{gs2}, V_{D1}, V_{D2}. (c) V_{gs1}, V_{gs2}, I_{L1}, I_{L2}. (d) V_{ci1}, V_{ci2}, V_{co1}, V_{co2}, V_o. (e) V_{ci1}, V_{ci2}, V_{co1}, V_{co2}, V_o in the transient condition. (f) V_{gs1}, V_{gs2}, $\triangle V_{co1}$, $\triangle V_{co2}$, $\triangle V_o$.

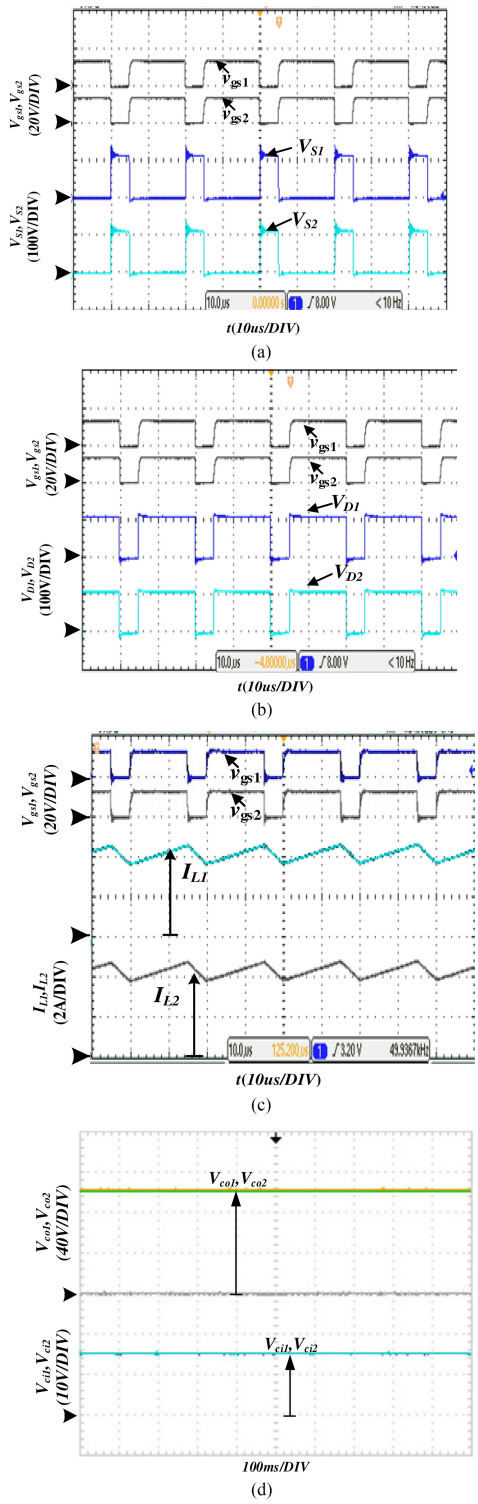

Fig. 14. Experiment waveforms of the proposed converter. (a) V_{gs1}, V_{gs2}, V_{S1}, V_{S2}. (b) V_{gs1}, V_{gs2}, V_{D1}, V_{D2}. (c) V_{gs1}, V_{gs2}, I_{L1}, I_{L2}. (d) V_{ci1}, V_{ci2}, V_{co1}, V_{co2}.

C. Capacitor Selection

The capacitor series equivalent resistance is considered null. The value of the output capacitor C_o depends on the output power of the converter P_o, output voltage V_o, voltage ripple $\triangle V_o$, and switching frequency f_s, which can be derived by using the

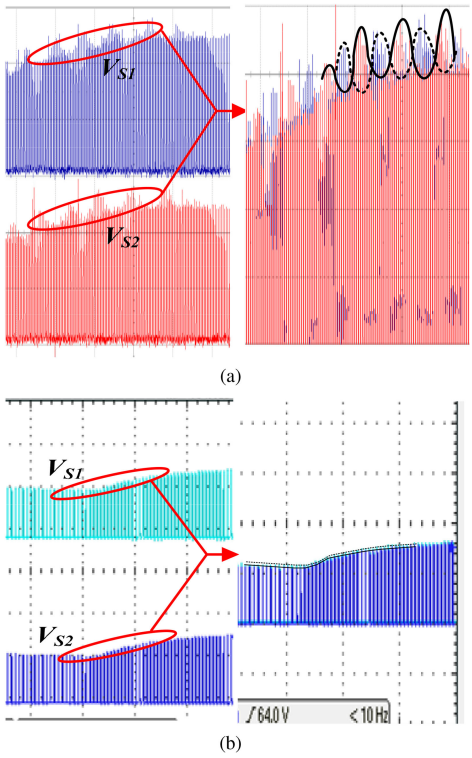

Fig. 15. Comparison of the switches' voltage waveforms. (a) Converters in [23]. (b) Proposed converter.

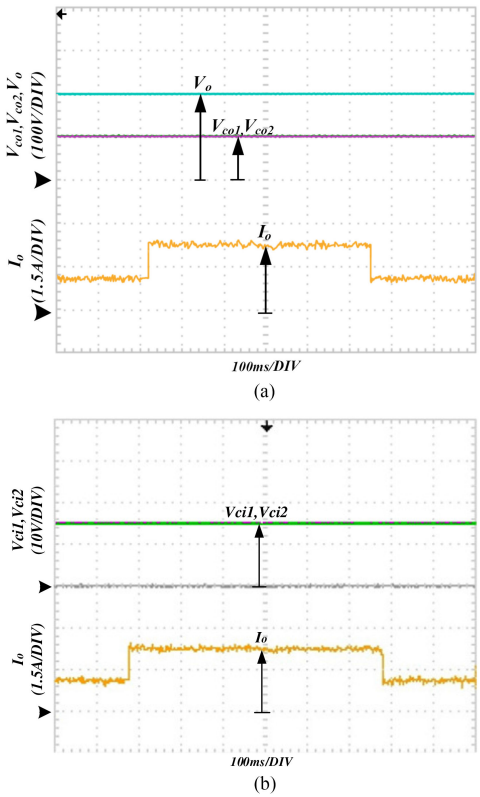

Fig. 16. Key waveforms in the dynamic state with sudden load change. (a) Waveforms of V_o, V_{co1}, and V_{co2}. (b) Waveforms of V_{ci1} and V_{ci2}.

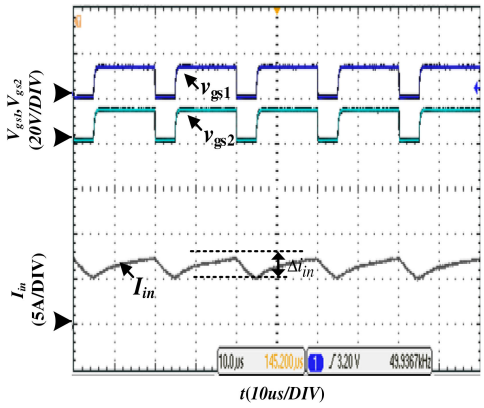

Fig. 17. Input current waveforms of converter when $V_i = 30$ V.

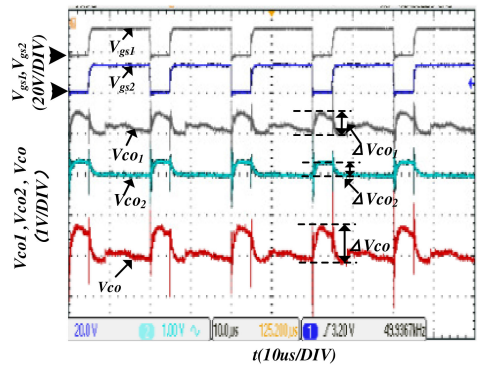

Fig. 18. Output voltage waveform of converter when $V_i = 30$ V.

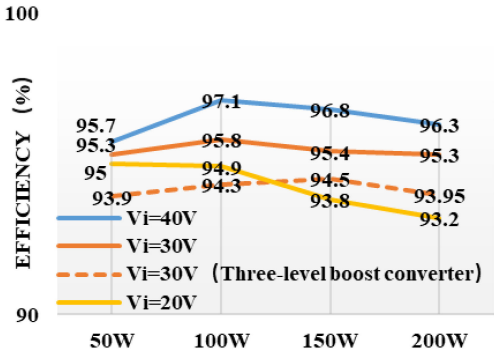

Fig. 19. Efficiency curves of different input voltage.

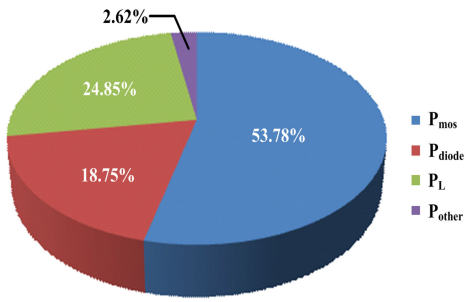

Fig. 20. Power loss of the proposed converter when $V_i = 30$ V, $V_o = 200$ V, and $P_o = 200$ W.

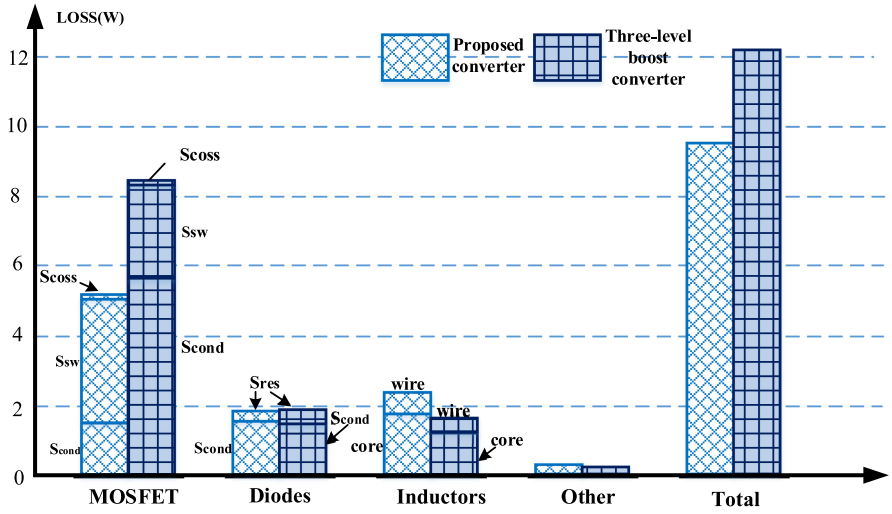

Fig. 21. Comparison of power loss between the proposed converter and three-level boost converter.

following equation:

$$C_o \geq \frac{(1-D)T_s I_o}{kV_o} \tag{23}$$

where $k = \triangle V_o / V_o$.

The output capacitor C_o concludes two capacitors C_{o1}, C_{o2}; the values of C_{o1} and C_{o2} are the same, and hence it can be expressed as

$$C_{o1} = C_{o2} \geq \frac{2(1-D)T_s I_o}{kV_o}. \tag{24}$$

V. Simulation and Experiment Results

In order to verify the precision of the analysis, some simulation and experiments have been conducted separately. Fig. 11 shows the power circuit, and the experimental conditions and parameters are shown in Table II.

The proposed converter has the ability to realize self-voltage balance on capacitors and switches. So, the proposed converter does not need complicated control logic. As shown in Fig. 12, the voltage V_o is controlled by the voltage controller with the reference voltage $V_{\rm ref}$ in the voltage loop. The corresponding PWM schemes are selected to generate the switching signals of S_1 and S_2.

The waveforms of simulation and experiment are listed below. The voltage waveforms of switches S_1, S_2 are shown in Figs. 13(a) and 14(a) when the input voltage is 30 V. Figs. 13(b) and 14(b) show the voltage waveforms of output diode, which are found to be the same. And the current waveforms of inductor are shown in Figs. 13(c) and 14(c), respectively, which are consistent with the theoretical analysis.

The simulation verification of the proposed converter is given on PSIM. And the structure is symmetric and parameters are totally same, and as shown in Fig. 13(d), the voltage stress on the input and output capacitors is the same. Fig. 14(d) shows the experimental waveforms of capacitors' voltage and output voltage; it is obvious that the performance of self-voltage balance is good in the steady state.

Fig. 15(a) illustrates the voltage waveforms of switches when the duty ratio changes suddenly, and the passive lossless clamp circuit is proposed by [23]. Because of its structural asymmetry, when duty ratio changes suddenly, the inequality voltage problem of switches S_1 and S_2 still exists. Fig. 15(b) shows the voltage waveforms of switches proposed in this article, and when the duty ratio changes suddenly, the voltage of the switches V_{S1} and V_{S2} are always the same, so two switches can still achieve good voltage balance.

Figs. 13(e) and 16 show the voltage waveforms of capacitors and output voltage when the load changes suddenly; as can be seen, the output current varied to twice and a half value immediately when the load changes, voltages of the all capacitors remain unchanged and keep balance in the transient condition.

The proposed converter can keep voltage balance on the switches when the duty cycle suddenly changes, and the voltage on all capacitors also remains balanced when the load suddenly changes. Thus, the proposed converter can achieve the voltage balance on the switches and capacitors; moreover, it has a good reliability and stability in the dynamic state.

Fig. 17 shows the experimental waveforms of the input current. And the actual input current ripple is consistent with the theoretical analysis. Fig. 18 shows the experimental waveforms of the output voltage. According to Fig. 9 and (20), the output voltage ripple is obtained by superimposing two output capacitors' voltage ripples. The experimental output voltage ripple is consistent with the simulation as shown in Fig. 13(f), which simulated in the rated condition with ESR.

Fig. 19 shows the efficiency curves; the efficiency curves are made by experimental measurement in the condition of $V_o =$ 200 V. The proposed converter shows a better efficiency performance than the three-level boost converter when $V_i = 30$ V.

Fig. 20 shows the power loss of the proposed converter when $V_i = 30$ V, $V_o = 200$ V, and $P_o = 200$ W, which consists of the loss of the switches, diodes, inductors, and other parts. And the losses in MOSFETs and inductors are collectively more than all other losses.

Due to symmetric and dual switches structure, the proposed converter is compared with the three-level boost converter. As shown in Table I, the number of components is similar except that the proposed converter has four capacitors, in the same working condition, $P_o = 200$ W, $f_s = 50$ kHz, $V_{\rm in} = 30$ V, and $V_{\rm out} = 200$ V. The power loss of two converters has been calculated, as shown in Fig. 21; the loss of switches $P_{\rm mos}$ include conduction loss ($S_{\rm cond}$), switching losses (S_{sw}), and capacitive losses $S_{\rm coss}$; and the losses of diodes mainly contain conduction losses ($S_{\rm cond}$) and reverse recovery losses ($S_{\rm res}$); and the losses of inductors are main on core and wire. Though the proposed converter has higher inductors loss, the conduction losses can be outstandingly reduced due to the lower current stress. Therefore, the proposed converter has a higher efficiency than the three-level boost converter.

VI. Conclusion

In this article, a dual-switch high step-up dc/dc converter with symmetric topology is proposed to solve the problem of dynamic voltage balance. And the performance of converter is also analyzed in detail. Considering the discontinuous input and output current, especially the step ripple across the filter capacitor, the improved design method to reduce the current ripple is still need to be developed. The converter has the following characteristics.

1) The proposed converter can keep low-voltage stress of the power devices and make the switches realize voltage balancing in both steady and dynamic states, which reduce the voltage stress effectively.
2) The structure of the proposed converter is simpler than most of high-voltage gain converters, and the voltage gain is also higher than other traditional converters.
3) As compared to asymmetric high-gain converters, balanced structure is utilized which is beneficial to reduce system EMI.
4) Based on maintaining the stress of switches invariant, the input current and output voltage ripples are low, which reduce the size of input and output filters. Besides, the highest efficiency of the proposed converter is about 97.1%.

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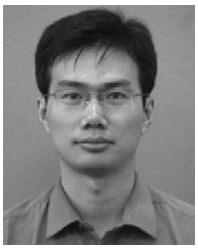

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