Strategy and Implementation of Harmonic-Reduced Synchronized SVPWM for High-Power Traction Machine Drives

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***Abstract*—High-power traction systems usually operate under low-switching-frequency conditions to avoid high switching losses. Synchronized space vector pulsewidth modulation (synchronized SVPWM) is an effective modulation method in low-switching-frequency modulation for its balanced harmonic performance and implementation complexity. A number of pulse pattern patterns in synchronized SVPWM are developed for application with different frequency ratios. In this article, the authors systematically analyzed the performance of pulse pattern and developed a harmonic-reduced pulse pattern selection strategy considering the influence of the modulation index. An implementation of synchronization SVPWM with strong universality is proposed, which includes a phase-locked loop (PLL) based synchronization method and pulse pattern transition strategy. The transition strategy can handle the transition for special-vector-sequence pulse patterns and over-modulation operation. The harmonic-reduced synchronized SVPWM strategy and its implementation are verified through simulations and experiments.**

***Index Terms*—Harmonic analysis, high-power motor drives, low switching frequency, over-modulation, synchronized SVPWM.**

NOMENCLATURE

f_r	Modulation reference frequency.
$f_{\text{sw0}}, f_{\text{sw}}$	Original and actual switching frequency.
N, P	Frequency ratio and pulse number.
$P(N, I^{+/-}_{\uparrow/\downarrow})$	Identifier of pulse pattern.
m	Length of space vector (normalized by $2V_{\text{dc}}/3$).
MI	Modulation index (normalized by $V_{\text{dc}}/2$).
e_f	Frequency measurement error.
T_{s0}, T_s	Original and actual sampling period.
φ_v, φ'_v	Original and transformed space vector phase.
φ'_e	Phase error of PLL synchronization.
φ_d	Phase delay of the modulation.
ω_e	Angular frequency of modulation reference.
$k_{P_1-P_2}$	Compensation factor of transition from pulse pattern P_1 to pulse pattern P_2.

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I. INTRODUCTION

IN HIGH-POWER machine drives, the switching frequency of inverters is usually restrained for lowering the switching loss [1]–[5]. For example, the switching frequency of the 530 kVA inverter on high-speed railway CRH1A is restricted to 1 kHz, and the electric locomotive HXD3 equips 1.2 MVA inverters with only 500 Hz switching frequency, but the frequency of these machines can reach up to 200 Hz [6]. Excessive switching loss will result in overheating of the IGBT modules. As an example, the loss and the maximum allowed heatsink temperature of high-power IGBT modules is shown in Fig. 1 [7], [8]. On IGBT module FZ1500R33HE3, when the switching frequency is 2 kHz, the loss on a single IGBT module reaches 5.38 kW, and the cooling system need to control the temperature of the heatsink under 60 °C. It is a heavy burden for the cooling system so that using lower switching frequency is necessary. However, in such low-switching-frequency circumstances, conventional PWM methods generate high harmonics and sub-harmonics [9], and the harmonics result in extra loss and vibrations [10], [11]. Both Permanent Magnet Synchronous Machines (PMSMs) and Induction Machines (IMs) face the same problem in low-switching-frequency operation.

Lots of research has been conducted in different aspects to ameliorate the performance of Pulse Width Modulation (PWM) methods under low-frequency-ratio conditions. In the first aspect, researchers try to improve the existing modulation methods and develop new modulation methods. The synchronized SVPWM synchronizes the modulation reference with the carrier and successfully reduces harmonics [9], [12]. In [13], the over-modulation strategy of synchronized sinusoidal pulsewidth modulation (SPWM) is proposed. Moreover, the specified harmonic elimination pulsewidth modulation (SHE-PWM) uses a mathematical method to calculate switching angles for canceling specified-order harmonics [14]. Optimal PWM is similar to SHE-PWM, but the switching angles are solved for minimizing current THD or copper loss of machines [15], [16].

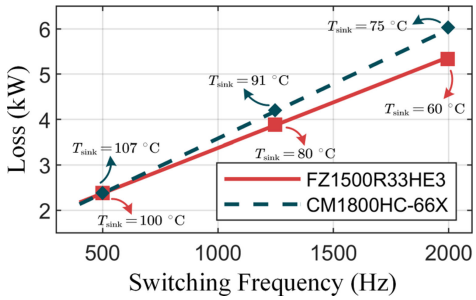


Fig. 1. Loss and the maximum allowed heatsink temperature of the IGBT modules. The loss is calculated with Collector-Emitter Voltage $V_{CE} = 1800$ V, Junction Temperature $T_j = 125$ °C, and sinusoidal phase current with amplitude $I_{phase} = 1200$ A.

The research in the second aspect focuses on the implementation and application of the modulation methods. Zhang *et al.* [17] optimize the current harmonics considering the saliency of IPMSM for metro traction application with the idea of optimal PWM. Lago *et al.* in [18] give general principles of optimal PWM in multi-level inverters. Diao *et al.* [19] realize a hybrid PWM strategy which combines synchronized SVPWM, SHE-PWM, and optimal PWM in a DSP-FPGA-based platform. In [13], [20], [21], researchers focus on realizing the fast-dynamic current-closed-loop control of high-power machines with low-switching-frequency modulation methods.

In high-power traction applications, e.g., locomotives, a fast-dynamic control can help to improve the punctuality, realize exact designated stop and crewless operation. Although optimal PWM can provide the best harmonic performance, it is based on the steady-state operation. Applying optimal PWM in field-oriented-control (FOC) drives requires a compensation for canceling dynamic modulation error, which increases the complexity of the system [20]. Another way of realizing fast-dynamic FOC with optimal PWM is by using trajectory control or predictive control [22]–[24]. Predictive controllers have the advantage of fast response, but it bears a much more substantial computational burden. Synchronized SVPWM has balanced performance and implementation complexity and does not generate dynamic modulation error when it is used with a conventional FOC controller. The only concern is that synchronized SVPWM has variable sampling frequency so that the stability and the performance of the current controller should be checked under different discretization frequencies. In this article, the authors select synchronized SVPWM as the research objective and try to improve its performance and implementation.

Synchronized SVPWM is first proposed by Narayanan *et al.* in [9], [12]. Researchers have added additional pulse patterns and an over-modulation strategy of synchronized SVPWM in [25], [26]. In early research, synchronized SVPWM is only applied in constant V/f control. The main problems of the application synchronized SVPWM in FOC drives are the realization of synchronization and the transition of pulse patterns. Different from V/f control conditions, the voltage command in FOC drives is not stable, which affects the realization of synchronized SVPWM. In [27], synchronized SVPWM is realized by adjusting the sampling period through a dead-beat controller. In [13], researchers implement the synchronized SPWM using FPGA. This implementation is based on the comparison between the sinusoidal reference and the triangle carrier so that only pulse patterns with frequency ratio $3k(k = 1, 3, 5 \ldots)$ can be realized, while there are other pulse patterns available.

High-power traction machines on locomotives will work in a wide speed range. Hence different pulse patterns of synchronized SVPWM should be applied. In [12], the researchers compared the performance of different pulse patterns in synchronized SVPWM and gave guidance on how to select pulse patterns with the best harmonic performance. However, in the later research, the pulse pattern selection did not follow the guidance [13], [21]. The authors think the reason might be that implementing kinds of pulse patterns increases the complexity of the system. In this article, the authors comprehensively consider the harmonic performance and develop the harmonic-reduced pulse patterns selection strategy according to the frequency ratio and the modulation index. A high-universality implementation of synchronized SVPWM is developed, which makes realizing the pulse pattern selection strategy have little effect on the complexity of the system.

The primary contribution of this article is that the authors provide a complete solution of synchronized SVPWM, which includes the over-modulation strategy, the pulse pattern selection strategy, and the complete implementation synchronized SVPWM. In the implementation, a flexible PLL-based synchronization method is developed, and a universal pulse pattern transition strategy considering special-vector-sequence pulse patterns and over-modulation operation is proposed. The proposed synchronized SVPWM strategy and implementation can collaborate with fast-dynamic FOC current controllers. The effectiveness of the proposed method is verified through simulations and experiments.

II. Principles of Synchronized SVPWM Including Over-Modulation

In this section, the principles and classification of synchronized SVPWM are discussed, and an over-modulation strategy is proposed. An essential characteristic of SVPWM is the ratio, N, between the original switching frequency, f_{sw0}, and the reference frequency, f_r. N defines the duration of the space vector and the number of space vectors in one reference period. The original switching frequency, f_{sw0}, means no strategy like bus-clamping that will change the switching frequency is employed

$$N = \frac{f_{sw0}}{f_r}. \tag{1}$$

Some strategies like the bus-clamping PWM (also known as discontinuous PWM, DPWM) can reduce actual switching frequency, f_{sw}. The ratio between f_{sw} and f_r is named pulse number P and is written as

$$P = \frac{f_{sw}}{f_r}. \tag{2}$$

In SVPWM, $V_1 - V_6$ represent the six active vectors, and V_0 and V_7 represent two zero vectors. Two types of space vectors in asymmetric sampling are rising-vector with sequence $V_0V_xV_yV_7$ and falling-vector with sequence $V_7V_yV_xV_0$.

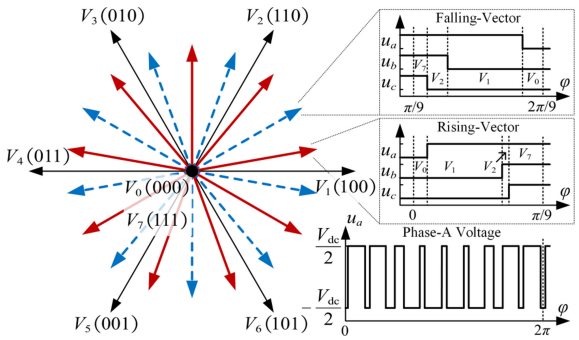


Fig. 2. Example of space vector distribution of pulse pattern $(P = 9, N = 9)$ in Mode I. Red solid arrows are rising-vectors and blue dashed arrows are falling-vectors.

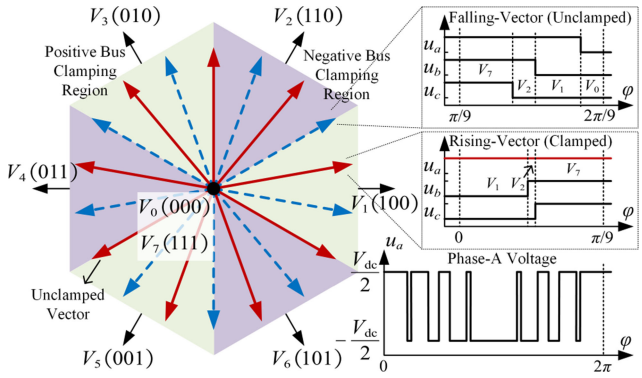


Fig. 3. Example of space vector distribution of pulse pattern $(P = 7, N = 9)$ in Mode II. The type of bus-clamping changes every $\pi/3$ to keep symmetry of the bus-clamping region.

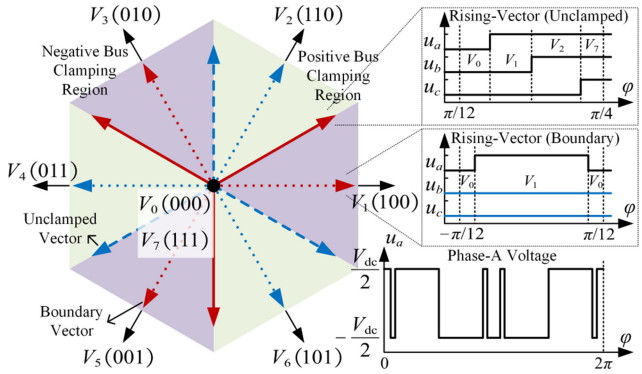


Fig. 4. Example of space vector distribution of pulse pattern $(P = 5, N = 6)$ in Mode III. The doted arrows are the boundary vectors.

A. Classification of Synchronized SVPWM

Synchronized SVPWM is a method to improve the performance of SVPWM in low-frequency-ratio conditions. In [9], the general idea of synchronized SVPWM is proposed. A fundamental requirement of synchronized SVPWM is keeping the symmetries of the voltage waveform. The symmetries include three-phase symmetry (TPS), half-wave symmetry (HWS), and quad-wave symmetry (QWS). The pulse patterns of synchronized SVPWM can be classified into three modes. In all modes, the distribution of vectors is symmetric to the angular-bisector of sectors.

Mode I is the synchronized conventional SVPWM. In this mode, no bus-clamping strategy is employed, and the positions of rising-vectors and falling-vectors can be exchanged. Hence, there are two pulse pattern realizations for a certain pulse number. An example of the space vector distribution and the corresponding phase voltage waveform with pulse pattern $(P = 9, N = 9)$ is illustrated in Fig. 2. Rising-vectors and falling-vectors are highlighted by different line types.

Mode II is the synchronized bus-clamping SVPWM, which uses DPWM to reduce the switching frequency. In bus-clamping regions, the vector sequence is $V_xV_yV_7/V_7V_xV_y$ or $V_0V_xV_y/V_xV_yV_0$. The type of bus-clamping region needs to be changed every 60° to keep symmetry. Vectors on the edges of the bus-clamping regions are unclamped vectors which are modulated by traditional vector sequence like $V_0V_xV_yV_7$. An example of modulation in Mode II with pulse pattern $(P = 7, N = 9)$ is shown in Fig. 3.

Mode III is the synchronized bus-clamping SVPWM with special vector sequence. Distinct from Modes I and II, there are vectors aligned with the six active vectors, which are named boundary vectors. The boundary vectors are modulated using special sequences $V_0V_xV_0$ or $V_7V_xV_7$. Therefore, at least one phase should switch twice in a sampling period. In avoiding extra switches, the vectors aligned with V_1, V_3, V_5 must be clamped to the negative bus, and vectors aligned with V_2, V_4, V_6 must be clamped to the positive bus. An example of this mode for pulse pattern $(P = 5, N = 6)$ is illustrated in Fig. 4. The boundary vectors are marked with dot lines.

The identifier

$$P\left(N, \text{mode}^{+/-}_{\uparrow/\downarrow}\right) \tag{3}$$

is used to distinguish different pulse patterns in the three modes. The superscript and subscript are defined as follows.

1) Superscript $+/-$ of mode:
   a) $+$ indicate that the modulation is clamped to the positive bus in phase range $[-\pi/6, \pi/6]$;
   b) $-$ indicate that the modulation is clamped to the negative bus in phase range $[-\pi/6, \pi/6]$.
2) Subscript $\uparrow$ / $\downarrow$ of mode:
   a) $\uparrow$ indicate that the pulse pattern start with a rising-vector in sector I;
   b) $\downarrow$ indicate that the pulse pattern start with a falling-vector in sector I.

For Mode I, there is no bus-clamping strategy. Therefore, the upper script is omitted. For Mode III, $\uparrow$ / $\downarrow$ represents the first edge of the boundary vector aligned with V_1. The available pulse patterns of Modes I, II, and III are listed in Table I.

TABLE I
AVAILABLE PULSE PATTERNS

Mode I	Mode II	Mode III
$3(3,\text{I}_\uparrow)/3(3,\text{I}_\downarrow)$	$7(9,\text{II}^+_\uparrow)$	$5(6,\text{III}^-_\uparrow)$
$9(9,\text{I}_\uparrow)/9(9,\text{I}_\downarrow)$	$11(15,\text{II}^-_\uparrow)$	$13(18,\text{III}^-_\uparrow)$
$15(15,\text{I}_\uparrow)/15(15,\text{I}_\uparrow)$	$15(21,\text{II}^+_\uparrow)$	
$21(21,\text{I}_\uparrow)/21(21,\text{I}_\downarrow)$	$19(27,\text{II}^-_\uparrow)$	

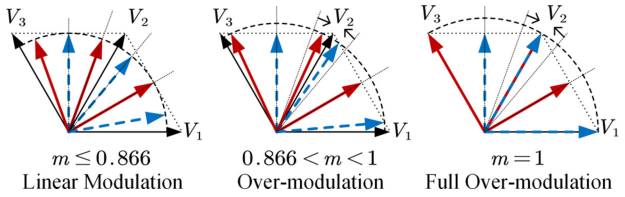


Fig. 5. Illustration of over-modulation. Vectors which are not the angular bisectors are shifted in the over-modulation region.

B. Over-Modulation of Synchronized SVPWM

For maximizing the utilization of bus voltage, the inverter will work in the over-modulation region. The over-modulation strategy proposed in [28] does not accommodate to low-frequency-ratio cases. In this article, a universal over-modulation strategy for all pulse patterns of synchronized SVPWM is adopted.

The over-modulation strategy is illustrated in Fig. 5 with pulse pattern $9(9, \mathrm{I}_{\downarrow})$. The length of the reference vector is defined as m which is also the radius of the reference trajectory circle. In the linear-modulation region that $m \leq 0.866$, all vectors keep unchanged. When $0.866 \leq m \leq 1$, the vectors which exceed the hexagon but are not on the angular-bisectors are moved to the intersection points. The lengths of the vectors on the angular-bisectors are reduced to 0.866 while the phases remain unchanged. When $m = 1$, the non-angular-bisector vectors are aligned with the six active vectors, and the synchronized SVPWM generates waveforms that are identical to six-step modulation waveforms. Therefore the modulation index (MI) reaches 1.27.

III. Pulse Pattern Selection Strategy Based on Performance Evaluation

The proposed pulse pattern selection strategy is based on the performance evaluations of pulse patterns. MI and harmonic performance of a pulse pattern are evaluated through Fourier Analysis. The amplitude of the nth order harmonic is calculated by

$$U_n = \left| \frac{1}{\pi} \int_0^{2\pi} u_a(\varphi) e^{-jn\varphi} \, d\varphi \right|, n = 0, 1, 2, \ldots, \quad (4)$$

in which u_a is the phase voltage. When $n = 1$, U_1 is the amplitude of the fundamental component which decides MI.

To reveal the absolute amplitude of the harmonic, Dc-Voltage-Normalized Weighted Total Harmonic Distortion (WTHD0) is used as the criteria for harmonic performance. The WTHD0 can be calculated by

$$\mathrm{WTHD0} = \frac{\sqrt{\sum_{n=2}^{\infty} \frac{1}{n^2} U_n^2, n \neq 3k, k = 1, 2, 3 \ldots}}{\frac{1}{2} V_{\mathrm{dc}}} \quad (5)$$

in which U_n is the amplitude of the nth order voltage harmonic. The $3k$ order harmonics are not included in the calculation because the TPS cancels all these harmonics in line voltage.

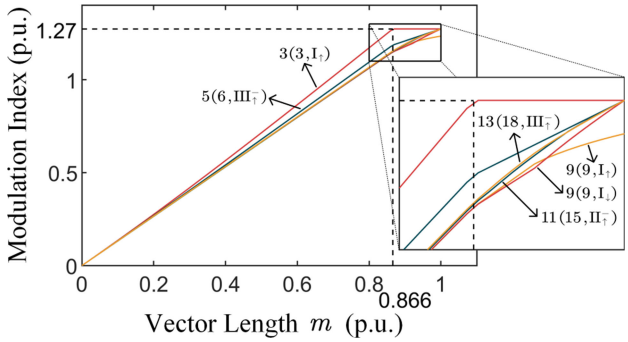


Fig. 6. Modulation index of different pulse patterns including the over-modulation region.

A. Modulation Index

Under low-frequency-ratio conditions, MI of synchronized SVPWM is different from conventional SVPWM. The relationship between the m and MI is revealed in Fig. 6. In the linear-modulation region that $m < 0.866$, the maximum MI of $3(3, \mathrm{I}_{\uparrow})$, $5(6, \mathrm{III}_{\uparrow}^{-})$, and the others is 1.273, 1.186, and 1.153, respectively. Hence, for $3(3, \mathrm{I}_{\uparrow})$, with the increase of m, the modulation can naturally transit to six-step modulation. Other pulse patterns reach higher MI through the over-modulation strategy. For pulse patterns in which the vector located at $\varphi = 90^{\circ}$ is a rising vector, the maximum modulation index cannot reach 1.27. Hence, $9(9, \mathrm{I}_{\downarrow})$ should be adopted instead of $9(9, \mathrm{I}_{\uparrow})$ in the over-modulation region. For pule patterns that $P \geq 15$, this phenomenon is unapparent.

The non-linear relationship between m and MI can be linearly approximated. In the linear-modulation region that $m \leq 0.866$, the relationship is

$$\mathrm{MI} \approx \begin{cases} 1.470m, & P = 3(3, \mathrm{I}_{\uparrow}) \\ 1.370m, & P = 5(6, \mathrm{III}_{\uparrow}^{-}) \\ 1.331m, & \text{others} \end{cases} \quad (6)$$

and in the over-modulation region that $0.866 < m \leq 1$, the relationship is

$$\mathrm{MI} \approx \begin{cases} 1.273, & P = 3(3, \mathrm{I}_{\uparrow}) \\ 1.186 + 0.649(m - 0.866), & P = 5(6, \mathrm{III}_{\uparrow}^{-}) \\ 1.153 + 0.897(m - 0.866), & \text{others}. \end{cases} \quad (7)$$

It should be noticed that (7) does not cover $9(9, \mathrm{I}_{\uparrow})$ and $7(9, \mathrm{II}_{\uparrow}^{-})$.

B. Harmonic Performance

The harmonic performance of pulse patterns is compared in Fig. 7. For the pulse patterns that have the same pulse number, the difference in harmonic performance is not significant except for $3(3, \mathrm{I}_{\uparrow})$ and $3(3, \mathrm{I}_{\downarrow})$. The pulse pattern $3(3, \mathrm{I}_{\uparrow})$ has better harmonic performance and is included in this figure. Different from the general idea that pulse pattern with a higher pulse number generates lower harmonics, the harmonic performance is also related to MI. For example, $15(21, \mathrm{II}_{\uparrow}^{+})$ provides better harmonic performance under high modulation index conditions,

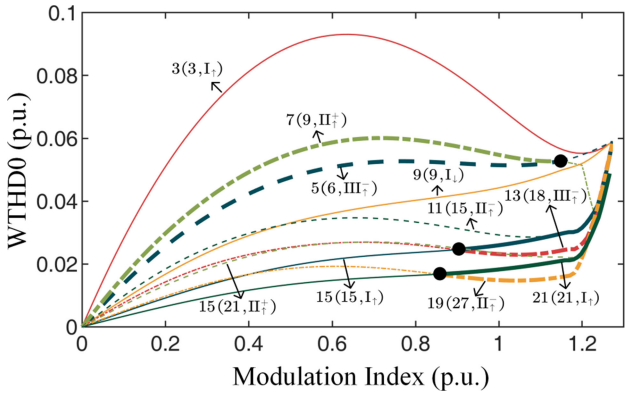


Fig. 7. Comparison of WTHD0 over different pulse patterns.

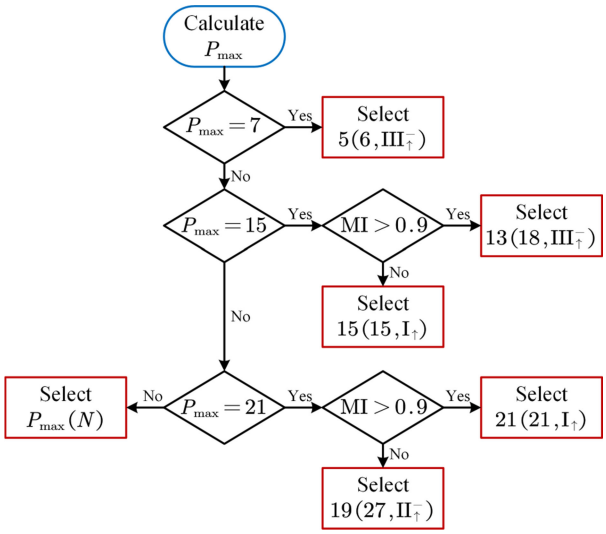


Fig. 8. Flow chart of selecting pulse pattern.

and $15(15,\mathrm{I}_{\uparrow})$ provides better harmonic performance under low modulation index conditions.

C. Strategy of Pulse Pattern Selection

Based on the above discussion on modulation index and harmonic performance, a strategy that selects the pulse pattern according to machine frequency and MI can be built. The strategy can lower harmonic distortion of synchronized SVPWM. The procedure of pulse pattern selection is illustrated in Fig. 8, and the results are shown in Fig. 9. In Fig. 8, the maximum allowed pulse number is represented by $P_{\max}$ which satisfies

$$P_{\max} \leq \frac{f_{\mathrm{sw,max}}}{f_e}, P_{\max} \in \{3,5,7,9,11,13,15,19,21\} \quad (8)$$

and $P_{\max}(N)$ represents the pulse pattern whose pulse number equals $P_{\max}$. Although $7(9,\mathrm{II}_{\uparrow}^{-})$ provides better harmonic performance than $9(9,\mathrm{I}_{\downarrow})$ and $5(6,\mathrm{III}_{\uparrow}^{-})$ in a part of the overmodulation region, the section in MI is too narrow to apply a different pulse pattern. Hence, the pulse pattern $7(9,\mathrm{II}_{\uparrow}^{-})$ is deprecated.

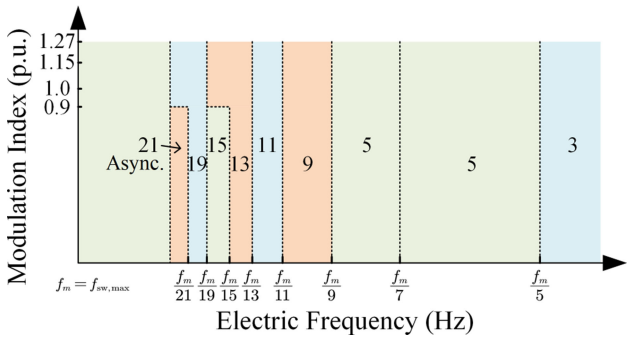


Fig. 9. Relationship among MI, election frequency and pulse pattern in proposed pulse pattern selection strategy.

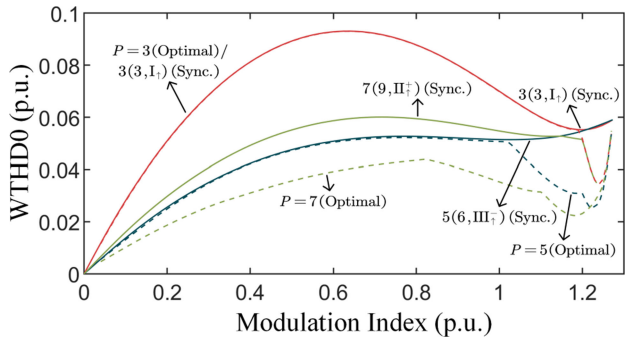


Fig. 10. Comparison of WTHD0 between synchronized SVPWM pulse patterns and Optimal PWM pulse patterns. The solid lines are the WTHD0 of synchronized SVPWM and the dashed lines represent the WTHD0 of Optimal PWM.

D. Performance Comparison With Optimal PWM

Optimal PWM is a technique that minimizes the harmonic distortion of low-frequency-ratio operation. The performance comparison of synchronized SVPWM and optimal PWM is demonstrated in Fig. 10. As an optimal method, optimal PWM provides the least harmonic distortion. However, the harmonic-reduced pulse pattern selection strategy narrows the performance gap between synchronized SVPWM and optimal PWM due to the usage of $5(6,\mathrm{III}_{\uparrow}^{-})$, compared with the synchronized SVPWM strategy adopted in other research [13], [21]. Besides, the biggest advantage of synchronized SVPWM over optimal PWM is the balance between harmonic performance and implementation complexity. Although optimal PWM in flux trajectory control or predictive control can provide better performance than synchronized SVPWM, the implementation of the controller is much more complex than synchronized SVPWM based FOC controller [20], [24]. Applying optimal PWM in FOC controller will face difficulties like the dynamic modulation error and the fundamental current extraction, while synchronized SVPWM does not have these difficulties.

IV. Implementation of Synchronized SVPWM for Machine Drives Using PLL

Synchronized SVPWM has already been adopted in machine control systems, like the constant V/f control of induction machines. However, for the control approaches with fast

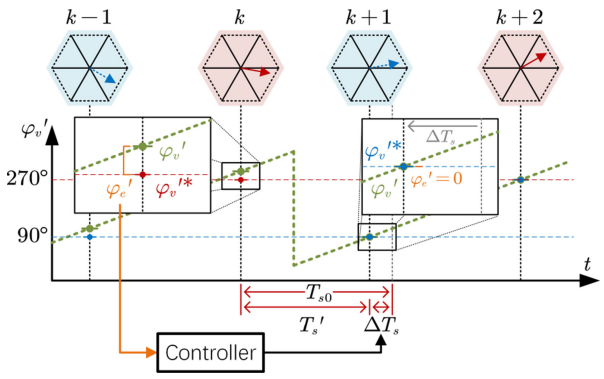


Fig. 11. Synchronization process of the modulation. The sampling period is adjusted from T_{s0} to T_s' in the kth sampling period.

dynamics like FOC, the output of the current controller may change rapidly. The traditional implementation of synchronized SVPWM could not track a fast dynamic input. Besides, synchronization should not bring modulation errors that could affect the performance of the current controller.

In this section, an implementation of synchronized SVPWM using PLL is developed for FOC machine drives. This implementation is based on authors' previous research in [29], but can synchronize pulse patterns in Mode III. The proposed implementation uses a PLL to synchronize the sampling with the reference. Compared with other implementations of synchronized SVPWM in [13], [21], the PLL-based implementation is more universal, which covers more pulse patterns and is more flexible to work under different conditions.

A. Design of the Synchronization With PLL

The PLL works by comparing the sampled voltage space vector phase with the synchronized vector phase and adjusting the sampling period to control the phase of the following sampled vector. The adjustment is on the base of the sampling frequency which is calculated by N and f_r. In Figs. 2–4, every synchronized vector has a fixed phase. This relationship can be simplified using the phase mapping

$$\varphi_v' = \mathrm{Mod}(N\varphi_v, 2\pi) \tag{9}$$

in which φ_v is the vector phase, and $\mathrm{Mod}(x, y)$ is the function to calculate the remainder of x/y. With (9), it is possible to uniformly handle the same type of vectors with different phases. For example, in $9(9, \mathrm{I}_\downarrow)$, the desired phase of a rising vector is $(\varphi_v = -10° + i \times 40°, i = 1, 2, 3, \ldots)$, and the transformed phase of a rising-vector will be $\varphi_v' = 270°$. Accordingly, the transformed phase of a falling-vector will be $\varphi_v' = 90°$. Hence, we only need to handle the transformed phase without considering the actual phase of a vector. For pulse patterns in Mode III, φ_v' of synchronized vectors is $0°$ and $180°$.

The synchronization process of $9(9, \mathrm{I}_\downarrow)$ is depicted in Fig. 11. The sampling period is adjusted according to the phase error φ_e between the desired vector phase $\varphi_v'^*$ and the transformed sampled vector phase φ_v'. The modulation reference frequency f_r is assumed a constant. The frequency ratio is N so that the ideal sampling frequency is $2Nf_r$. At the kth sampling, the

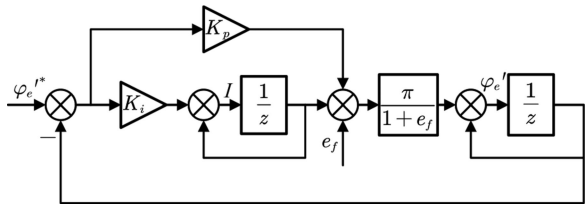


Fig. 12. Block diagram of the PLL implemented in z domain.

transformed vector phase is $\varphi_v'(k)$. It is reasonable to suppose that the frequency measurement error e_f exists. Therefore, the actual sampling frequency is $2Nf_r(1 + e_f)$. $\varphi_v'^*(k)$ is assumed $270°$ at this sampling moment and will be $90°$ at the next sampling moment. The sampling period adjustment is $\Delta t_{\mathrm{pu}}(k)$ so that the kth sampling period becomes

$$T_s'(k) = T_{s0}(1 + \Delta t_{\mathrm{pu}}(k)) = \frac{1 + \Delta t_{\mathrm{pu}}(k)}{2Nf_r(1 + e_f)} \tag{10}$$

in which T_{s0} is the unadjusted sampling period. The difference between $\varphi_v'^*$ and φ_v' at sampling k is

$$\varphi_e'(k) = \varphi_v'^*(k) - \varphi_v'(k) = 270° - \varphi_v'(k). \tag{11}$$

At the $(k+1)^{th}$ sampling, the transformed vector phase becomes

$$\begin{aligned}\varphi_v'(k+1) &= \varphi_v'(k) + 360° \times T_s(k) N f_r \\ &= \varphi_v'(k) + \frac{180°(1 + \Delta t_{\mathrm{pu}}(k))}{1 + e_f}.\end{aligned} \tag{12}$$

Hence, the phase error becomes

$$\begin{aligned}\varphi_e'(k+1) &= \varphi_v'^*(k+1) - \varphi_v'(k+1) \\ &= 270° - \varphi_v'(k) - \frac{180°(\Delta t_{\mathrm{pu}}(k) - e_f)}{1 + e_f}.\end{aligned} \tag{13}$$

As a result, Δt_{pu} can control the phase error as well as the sampled phase of space vectors. A PI controller is put in place to generate Δt_{pu}.

The block diagram of the PLL is shown in Fig. 12. In the analysis, the frequency measurement error e_f is assumed a constant. The discrete state-space model of the PLL system is

$$\begin{bmatrix} I(k+1) \\ \varphi_e'(k+1) \end{bmatrix} = \begin{bmatrix} 1 & -K_i \\ \dfrac{\pi}{e_f + 1} & 1 - \dfrac{\pi K_p}{e_f + 1} \end{bmatrix} \begin{bmatrix} I(k) \\ \varphi_e'(k) \end{bmatrix} + \begin{bmatrix} K_i & 0 \\ \dfrac{\pi K_p}{e_f + 1} & \dfrac{\pi}{e_f + 1} \end{bmatrix} \begin{bmatrix} \varphi_e'^* \\ e_f \end{bmatrix} \tag{14}$$

where $\varphi_e'^*$ is the reference of the synchronization error which will always be 0, and K_p and K_i are the gains of the PI controller. The state of the integrator is represented by I. The stable point at $[-e_f, \varphi_e'^*]$ means the phase offset φ_e' will track the reference without steady-state error.

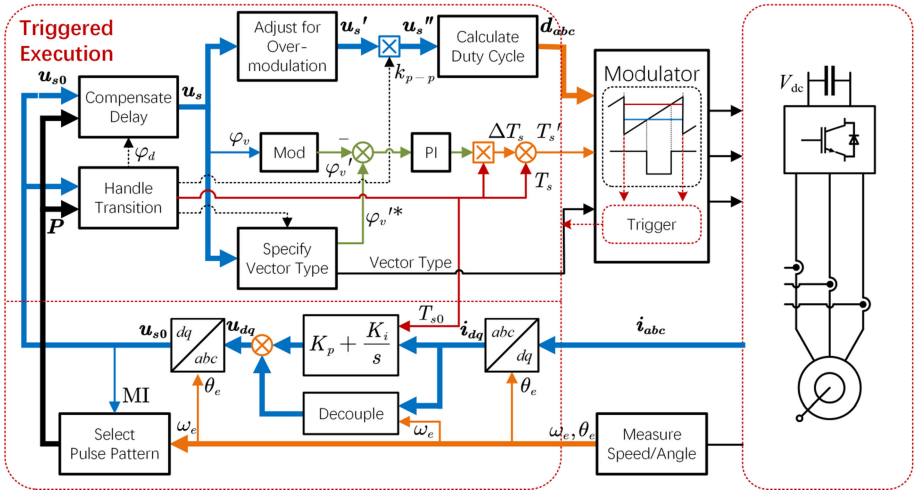


Fig. 13. Proposed implementation block diagram of the FOC drive with synchronized SVPWM.

B. Stability Analysis and PLL Gain Design

When the frequency measurement error, e_f, is regarded as a constant, the PLL is a discrete linear system, and the distribution of the system poles determines the system's stability. The system poles can be found by solving the characteristic equation

$$|z\boldsymbol{I} - \boldsymbol{G}| = 0 \tag{15}$$

in which $\boldsymbol{G}$ is the state transition matrix in (14). The solution of (15) gives the system poles

$$z = \frac{\pm\sqrt{-4\pi e_f K_i - 4\pi K_i + \pi^2 K_p^2} + 2e_f - \pi K_p + 2}{2e_f + 2}. \tag{16}$$

For a stable system, the poles must distribute inside the unit circle. In order to simplify the stability criteria, the locations of poles are verified under two different conditions under which both poles are real and both poles are complex. In the calculation, the frequency measurement error is usually small so that it is reasonable to assume $-1 < e_f < 1$. The simplified results give the stable conditions as well as the range of the PI gains

$$0 < K_i < \frac{4e_f + 4}{\pi} \wedge K_i < K_p < \frac{4e_f + \pi K_i + 4}{2\pi}. \tag{17}$$

In practice, higher K_p brings faster converge speed, but makes the PLL more sensitive to interference. Besides, slower adjustment on the sampling period helps reduce the influence of modulation on the current controller. Hence, it is important to find a balance in tuning the parameters of PLL under the guidance of (17). The tunable synchronization speed is an advantage of the proposed PLL-based synchronization method, which makes the proposed method appropriate for different conditions.

C. Implementation of Synchronized SVPWM

The flowchart demonstrating the implementation of synchronized SVPWM is shown in Fig. 13. The output of the PI controller affects the next sampling moment as well as the triggered execution of the synchronization process. Hence, φ_v is controlled by the output of the PI controller, and a PLL is formed through this feedback. In the proposed implementation, a traditional current controller can be used. In this figure, the current controller is a PI controller with feed-forward decoupling, but using other current controllers like complex vector controller is also possible. Retaining the structure of traditional current control is an advantage of synchronized SVPWM. However, the current controller is also executed by the trigger, and the trigger frequency will change in synchronized SVPWM. Hence, the performance of the current controller under different discretization frequency should be verified. The details of delay compensation and transition handling will be discussed in the next section. The dashed arrows only take effect when pulse pattern transition happens.

V. Pulse Pattern Transition Strategy Considering Over-Modulation Operation

For the application of synchronized SVPWM in variable frequency drives, the pulse pattern needs to change according to the electric frequency of machines. In this section, a pulse pattern transition strategy of synchronized SVPWM is proposed, which can also work in over-modulation operation. The strategy guarantees a smooth transition between different pulse patterns. Together with the PLL-based synchronization method, an implementation of synchronized SVPWM is fully constructed for fast-dynamic FOC PMSM drives under low-frequency-ratio conditions.

A. Time Delay Compensation in the Modulation

In the transition of pulse patterns, the modulation time delay is critical. Delays inevitably exist in digital platforms. Improper handling of delays will degrade the performance of the machine control system. In the case of the synchronous frame current regulator, the time delay is accompanied by the frame rotation [30].

While the rotating speed of the synchronous frame can be regarded as a constant in a short time, the error can be compensated by rotating the reference voltage space vector. The

delay between the ideal modulation reference and the sampled one is $T_s/2$. Due to the limitations of hardware, the sampled modulation reference can only be output in the next sampling period, which generates a delay with the duration T_s. Hence, the length of the total delay is $3T_s/2$. In low-frequency-ratio conditions, the delay will cause a significant phase error. The phase error can be calculated using N as

$$\varphi_d = 1.5T_s\omega_e = \frac{3\pi}{2N} \tag{18}$$

in which ω_e is the rotating speed of the synchronous frame. φ_d should be added to the phase of the sampled modulation reference to cancel the phase error of the space vector. In the synchronization of modulation, the compensated space vector phase should also be used. With the compensation, the phase of output voltage matches the input of the modulation.

B. Pulse Pattern Transition Strategy

The pulse pattern transition strategy contains two targets. The first target is to make sure the modulation keeps synchronized. The second target is to avoid working point change and dynamics in transitions.

The first target can be achieved by transition timing. Assuming that the pulse pattern changes from $P_1(N_1)$ to $P_2(N_2)$ at sampling k, for keeping the modulation synchronized, the end phase of $P_1(N_1)$ must be continuous to the start phase of $P_2(N_2)$. At the end of the sampling period $k-1$, the output voltage phase is

$$\varphi_{\text{end}}(N_1) = \varphi_v^*(N_1) + \frac{\pi}{2N_1} \tag{19}$$

in which φ_v^* is the phase of the synchronized space vector. For keeping the first vector after the transition is in the synchronized position, the output voltage phase of sampling k should be

$$\varphi_{\text{start}}(N_2) = \varphi_v^*(N_2) - \frac{\pi}{2N_2}. \tag{20}$$

Hence, to make sure the modulation is synchronous after the transition, $\varphi_{\text{end}}(N_1)$ must equal $\varphi_{\text{start}}(N_2)$, which leads to

$$\varphi_v^*(N_2) - \varphi_v^*(N_1) = \frac{\pi}{2N_1} + \frac{\pi}{2N_2}. \tag{21}$$

By verifying the vector distribution of pulse patterns, the transition timing can be divided into three cases.

Case 1: $P_1(N_1)$ and $P_2(N_2)$ are both in modulation Mode I or II. In this case, the vectors that satisfy (21) exist. Specifically, the last vector in a sector and the first vector in the next sector always satisfy (21). The transition process is depicted in Fig. 14. The delay is considered in the transition. Because of the change in the sampling period, there is a distinct phase delay compensation at sampling k, which is

$$\varphi_d(k) = \frac{\pi}{N_1} + \frac{\pi}{2N_2}. \tag{22}$$

Case 2: $P_1(N_1)$ is in Mode I or II, and $P_2(N_2)$ is in Mode III. In this case, no vectors satisfy (21). Hence, the transition timing should be adjusted. We handle the problem by adding a transition vector, which is generated by dividing the sampling period of the boundary vector in Mode III. The transition vector is modulated

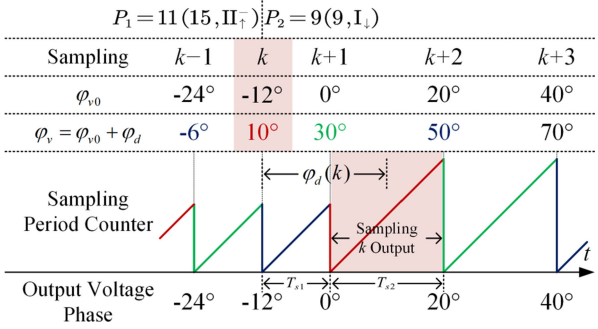


Fig. 14. Example of pulse pattern transition process from $11(15,\text{II}_\uparrow^-)$ to $9(9,\text{I}_\downarrow)$.

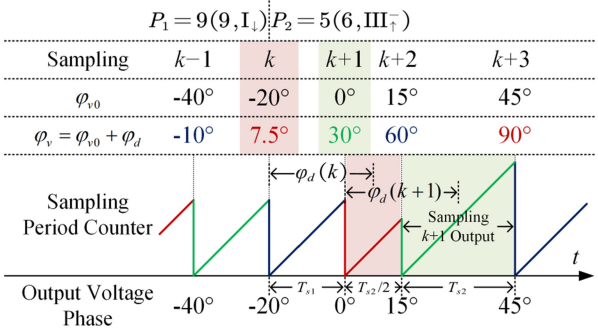


Fig. 15. Example of pulse pattern transition from $9(9,\text{I}_\downarrow)$ to $5(6,\text{III}_\uparrow^-)$. The vector calculated at the instant k is the transition vector with sampling period $T_{s2}/2$.

in Mode III with the duration of $T_{s2}/2$. The transition process also happens when the modulation reference is crossing the sector boundary, as shown in Fig. 15. In the figure, the transition vector with $\varphi_v(k) = 7.5°$ ensures the next space vector is located on the synchronized position. The specific delay compensation in the transition is

$$\varphi_d(k) = \frac{\pi}{N_1} + \frac{\pi}{4N_2}, \varphi_d(k+1) = \frac{\pi}{N_2}. \tag{23}$$

Case 3: $P_1(N_1)$ is in Mode III, and $P_2(N_2)$ is in Mode I or II. In this case, the transition is the inverse of the transition in case 2 and is not discussed in detail.

The second step of pulse pattern transition is to avoid working point change and dynamics in transitions. The pulse pattern transition should make the machine change from one steady state to another without affecting the working point. The same working point means that the steady-state fundamental current should be the same. When the stator resistance is ignored, the same steady-state fundamental current is equal to the same steady-state stator flux, and analyzing the stator flux is more convenient. To ensure the machine is in steady-state after pulse pattern transition, the steady-state actual current of the two pulse pattern at the transition point should be the same. Similarly, the equal steady-state actual current can be converted to the equal steady-state actual stator flux. Hence, the steady-state fundamental flux and steady-state actual flux of different pulse patterns should be calculated to ensure the equality.

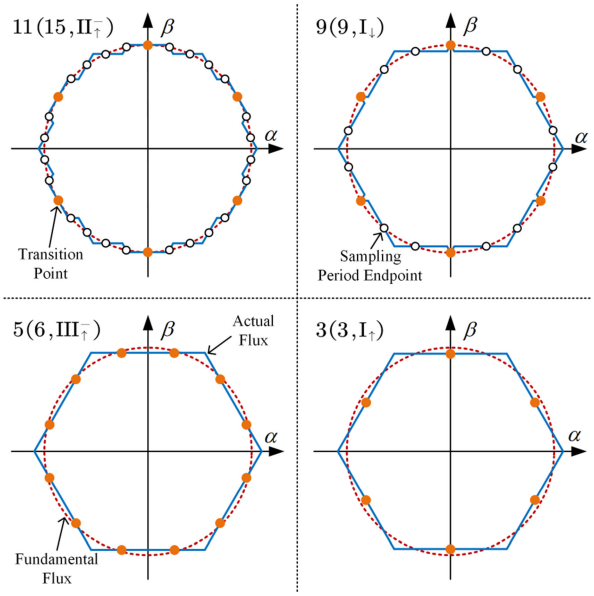


Fig. 16. Flux trajectories of pulse patterns $11(15, \mathrm{III}_{\uparrow}^{-})$, $9(9, \mathrm{I}_{\downarrow})$, $5(6, \mathrm{III}_{\uparrow}^{-})$ and $3(3, \mathrm{I}_{\uparrow})$. The endpoint of sampling period is the position of stator flux when a sampling period ends.

The steady-state fundamental stator flux, $\boldsymbol{\psi}_{\mathbf{fund}}$, is related to MI. When the stator resistance is ignored, $\boldsymbol{\psi}_{\mathbf{fund}}$ can be calculated as

$$\begin{aligned}\boldsymbol{\psi}_{\mathbf{fund}} &= \int \frac{1}{2}\mathrm{MI} \cdot V_{\mathrm{dc}} e^{j\omega_e t}\, dt \\ &= \frac{1}{2j\omega_e}\mathrm{MI} \cdot V_{\mathrm{dc}} e^{j\omega_e t} + C_0. \end{aligned} \tag{24}$$

In steady-state operations, the center of the fundamental flux trajectory is located at the origin, and the amplitude of $\boldsymbol{\psi}_{\mathbf{fund}}$, as well as the radius of the flux trajectory circle, is

$$|\boldsymbol{\psi}_{\mathbf{fund}}| = \frac{1}{2\omega_e}\mathrm{MI} \cdot V_{\mathrm{dc}}. \tag{25}$$

The steady-state actual stator flux, $\boldsymbol{\psi}_{\mathbf{act}}$, is different from the fundamental flux. For $P(N)$ in the linear-modulation region, the steady-state stator flux at the end of every sampling period forms an N-regular-polygon with the edge length

$$\begin{aligned}|\boldsymbol{\psi}_{\mathbf{edge}}| &= m\frac{2}{3}V_{\mathrm{dc}}T_s \\ &= \frac{2\pi}{3N\omega_e} m V_{\mathrm{dc}}. \end{aligned} \tag{26}$$

The amplitude of $\boldsymbol{\psi}_{\mathbf{act}}$ at the vertex of the polygon can be calculated from the geometric relationship as

$$|\boldsymbol{\psi}_{\mathbf{act}}| = \frac{\sin\left(\frac{\pi}{2} - \frac{\pi}{2N}\right)}{\sin\left(\frac{\pi}{N}\right)} \frac{2\pi}{3\omega_e N} m V_{\mathrm{dc}}. \tag{27}$$

Based on the above calculation, $\boldsymbol{\psi}_{\mathbf{fund}}$ and $\boldsymbol{\psi}_{\mathbf{act}}$ of different pulse patterns can be plotted as shown in Fig. 16. The transition points selected in transition timing are specially marked in this figure. The relationship between $|\boldsymbol{\psi}_{\mathbf{fund}}|$ and $|\boldsymbol{\psi}_{\mathbf{act}}|$ at the transition point can be carried out through the modulation

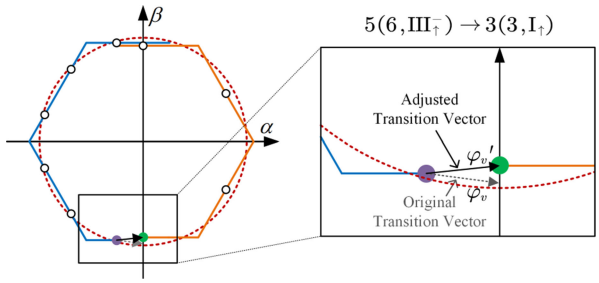


Fig. 17. Flux trajectory of the transition from $5(6, \mathrm{III}_{\uparrow}^{-})$ to $3(3, \mathrm{I}_{\uparrow})$.

index property of different pulse patterns in (6) and (7). In the linear-modulation region, the relationship is

$$\frac{|\boldsymbol{\psi}_{\mathbf{act}}|}{|\boldsymbol{\psi}_{\mathbf{fund}}|} \approx \begin{cases} 0.950, & 3(3, \mathrm{I}_{\uparrow}) \\ 0.984, & 5(6, \mathrm{III}_{\uparrow}^{-}) \\ 1.007, & 9(9, \mathrm{I}_{\downarrow}) \\ 1.0, & \text{others.} \end{cases} \tag{28}$$

For pulse patterns that $P \geq 9$, $|\boldsymbol{\psi}_{\mathbf{fund}}|$, and $|\boldsymbol{\psi}_{\mathbf{act}}|$ can be regarded as the same, which means $\boldsymbol{\psi}_{\mathbf{act}}$ is naturally continuous at the transition points, and the machine will naturally go into the steady state after transitions. No adjustment is needed for the transition between these pulse patterns. However, for the transition into and out of pulse patterns $3(3, \mathrm{I}_{\uparrow})$ and $5(6, \mathrm{III}_{\uparrow}^{-})$, transition vectors need to be adjusted to make sure the machine steps into the steady state. The adjustment on the transition vector is exampled in Fig. 17.

The adjustment factor can be calculated by comparing the demanded transition vector with the original transition vector. For the transition from $5(6, \mathrm{III}_{\uparrow}^{-})$ to $3(3, \mathrm{I}_{\uparrow})$, the vector adjustment factor is

$$\begin{aligned} k_{5-3} &= \frac{\boldsymbol{\psi}_{\boldsymbol{v}}'}{\boldsymbol{\psi}_{\boldsymbol{v}}} \\ &= \frac{0.950|\boldsymbol{\psi}_{\mathbf{fund,3}}|e^{j270^\circ} - 0.984|\boldsymbol{\psi}_{\mathbf{fund,5}}|e^{j255^\circ}}{0.5|\boldsymbol{\psi}_{\mathbf{edge,5}}|e^{-j7.5^\circ}} \\ &= 1.000e^{j7.74^\circ}. \end{aligned} \tag{29}$$

Other transition factors can be calculated in the same way. In the linear-modulation region, the transition vector needs to be adjusted only in these four cases

$$\begin{cases} k_{3-5} = 1.000e^{-j7.74^\circ} \\ k_{9-5} = 1.024e^{j4.89^\circ} \\ k_{5-9} = 1.024e^{-j4.89^\circ}. \end{cases} \tag{30}$$

In the over-modulation region, the relationship between $|\boldsymbol{\psi}_{\mathbf{fund}}|$ and $|\boldsymbol{\psi}_{\mathbf{act}}|$ is more complicated. Due to the shift of vectors in the over-modulation region, the vectors in an electric period no longer form an N-regular-polygon. Hence, (27) cannot be used to calculate $|\boldsymbol{\psi}_{\mathbf{act}}|$ in this case. Nevertheless, the flux trajectory of vectors in each sector is still symmetric, which can be utilized in the calculation of $|\boldsymbol{\psi}_{\mathbf{act}}|$, as demonstrated in Fig. 18. For $9(9, \mathrm{I}_{\downarrow})$, $|\boldsymbol{\psi}_{\mathbf{act}}|$ can be calculated as

$$|\boldsymbol{\psi}_{\mathbf{act}}| = |\boldsymbol{v_1}T_s + \boldsymbol{v_2}T_s + \boldsymbol{v_3}T_s| \tag{31}$$

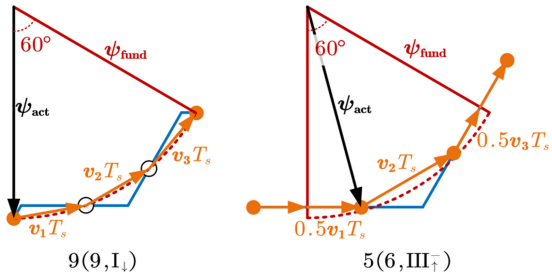


Fig. 18. Illustration of the calculation of $|\psi_{act}|$ in over-modulation operation.

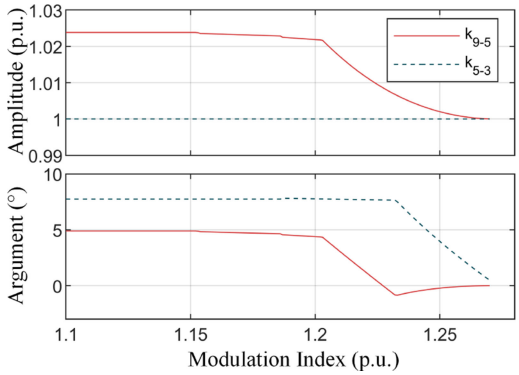


Fig. 19. Transition factor in over-modulation operation.

in which v_1, v_2, and v_3 are the vectors after the adjustment of the over-modulation strategy. For $5(6, \mathrm{III}_\uparrow^-)$, the transition point is not on the axis of symmetry of flux trajectory, hence $|\psi_{act}|$ in this pulse pattern should be calculated as

$$|\psi_{act}| = \Big| |0.5v_1T_s + v_2T_s + 0.5v_3T_s| e^{-j90^\circ} + |0.5v_1T_s| \Big|. \quad (32)$$

When $|\psi_{act}|$ is carried out, the rest step of calculating the transition factor is similar to linear-modulation occasions. The transition adjustment should be based on the transition vector after the over-modulation adjustment. The results of the transition factor calculation in over-modulation operation are illustrated in Fig. 19. For the transitions from $3(3, \mathrm{I}_\uparrow)$ to $5(6, \mathrm{III}_\uparrow^-)$ and $5(6, \mathrm{III}_\uparrow^-)$ to $9(9, \mathrm{I}_\downarrow)$, we only need to use the conjugate of the plotted transition factors.

C. Implementation of Transition Strategy

The logic to implement the pulse pattern transition strategy is demonstrated in Fig. 20. The transition strategy works like a state machine and it moves one step forward in the flowchart in each time of execution. If the conditions to start the transition are satisfied, one of the three branches will be executed according to the current and the next pulse pattern, otherwise, the strategy loops at the start flag. The conditions to start the transition include the following.

1) The target pulse pattern is different from the current one.
2) The voltage vector is located at the synchronized position which is one sampling period before the transition point.

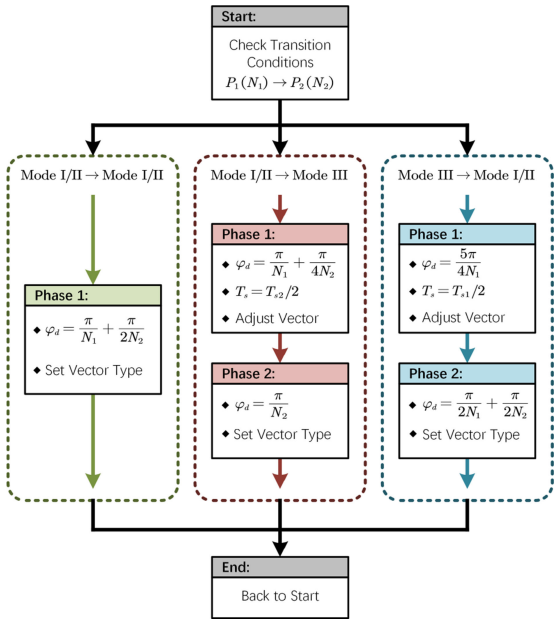


Fig. 20. Logic to implement the pulse pattern transition strategy.

TABLE II
MACHINE PARAMETERS

Parameter	Symbol	Scaled-down PM Machine	Full-scale PM Machine
DC Voltage	V_{dc}	200 V	800 V
Rated power	P_N	1.5 kW	120 kW
Rated Torque	T_N	9.6 N · m	760 N · m
Rated Current	I_N	10 A	340 A
Rated frequency	f_N	100 Hz	120 Hz
Number of pole pairs	P	5	4
Stator phase resistance	R_s	0.273 Ω	0.029 Ω
Stator d-axis Inductance	L_s	2.25 mH	0.96 mH
Stator q-axis Inductance	L_s	2.25 mH	1.44 mH

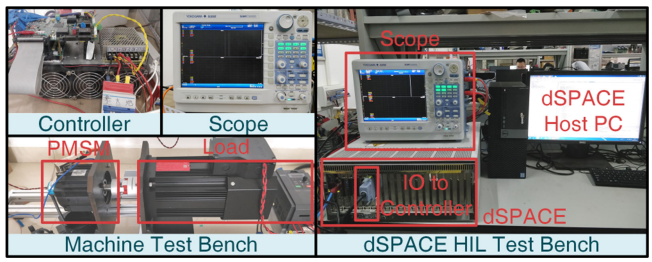


Fig. 21. Photos of scaled-down experiment test bench and HIL experiment platform.

In Fig. 20, the four types of actions that change φ_d, change T_s, set vector type and adjust transition vector are corresponding to the four outputs of the transition handling block in Fig. 13.

VI. Simulations and Experiments

Scaled-down experiments and full-scale hardware-in-loop (HIL) experiments are conducted to verify the effectiveness of the proposed strategy. The parameters of the two machines are shown in Table II. The machine drive in the scaled-down experiment is implemented using a microcontroller TI

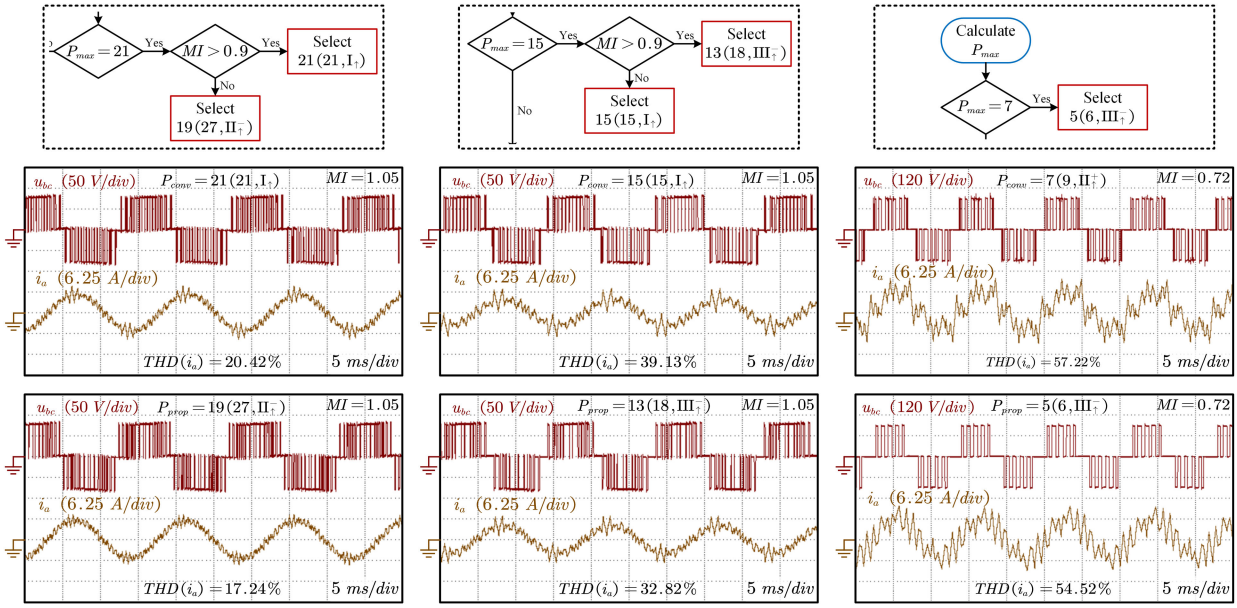


Fig. 22. Experimental harmonic performance of pulse patterns selected by the proposed strategy and the comparison with traditional strategy.

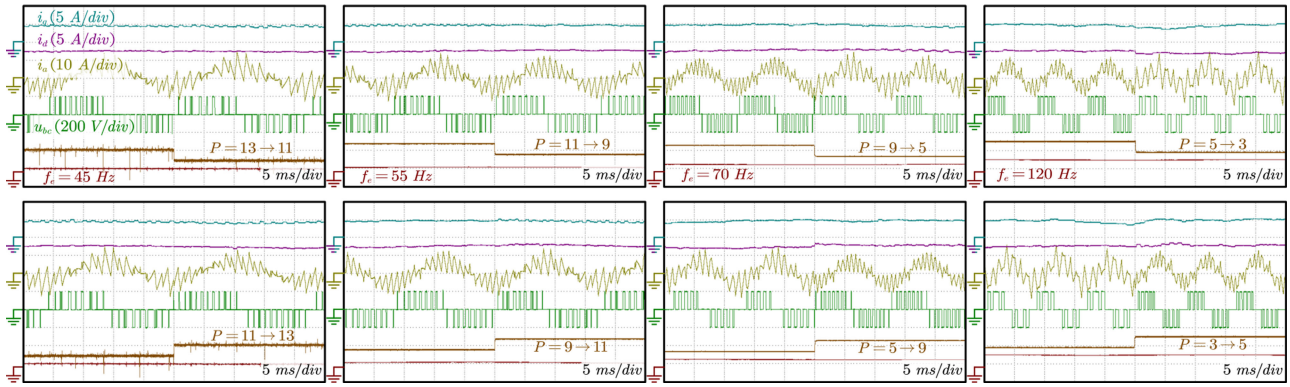


Fig. 23. Experimental results of pulse pattern transition in linear-modulation region. The machine works in torque mode and speed is controlled by the loading machine.

TMS320F28335, and the HIL experiment is based on dSPACE DS1007. Fig. 21 contains photographs of the machine test bench and HIL devices. The machine controller contains a speed regulator and a current regulator. i_d and i_q are outputted by the controller using a D/A converter.

A. Scaled-Down Simulations and Experiments on a 1.5-kW PMSM

In the scaled-down simulations and experiments, the tested machine is not intended for low-switching-frequency operation. Hence, the current harmonic distortion is relatively high.

Fig. 22 represents the harmonic reduction of the proposed pulse pattern selection strategy compared with the conventional one. In this experiment, the proposed strategy replaces the traditional pulse patterns $P = 21, 15, 7$ (with the subscript cnov) with pulse patterns $P = 19, 13, 5$ (with the subscript prop) in specified cases and reaches the current harmonic distortion reduction in 15.57%, 16.12%, and 4.7%, respectively.

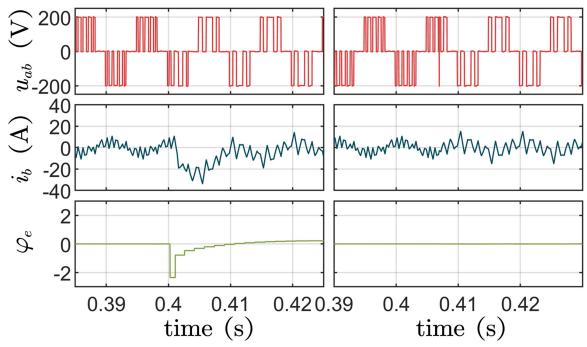


Fig. 24. Simulation waveform of pulse pattern transition without the proposed strategy (left) and with the proposed strategy (right).

Fig. 23 shows the experimental results of pulse pattern transitions in the linear-modulation region. No current oscillation occurs in the transition, and the modulation keeps synchronized. Since the pulse pattern transition without the proposed strategy

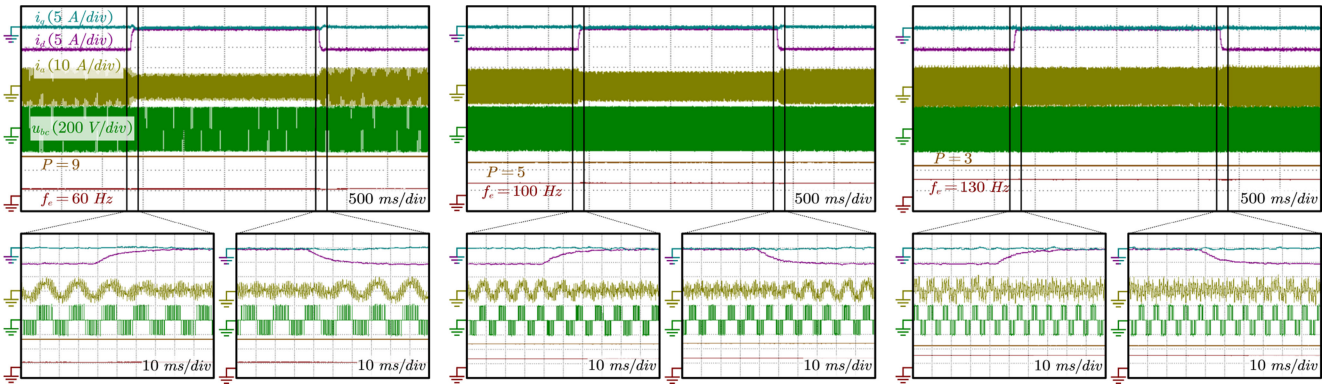


Fig. 25. Results of the current step-change experiments. The machine works in speed control mode.

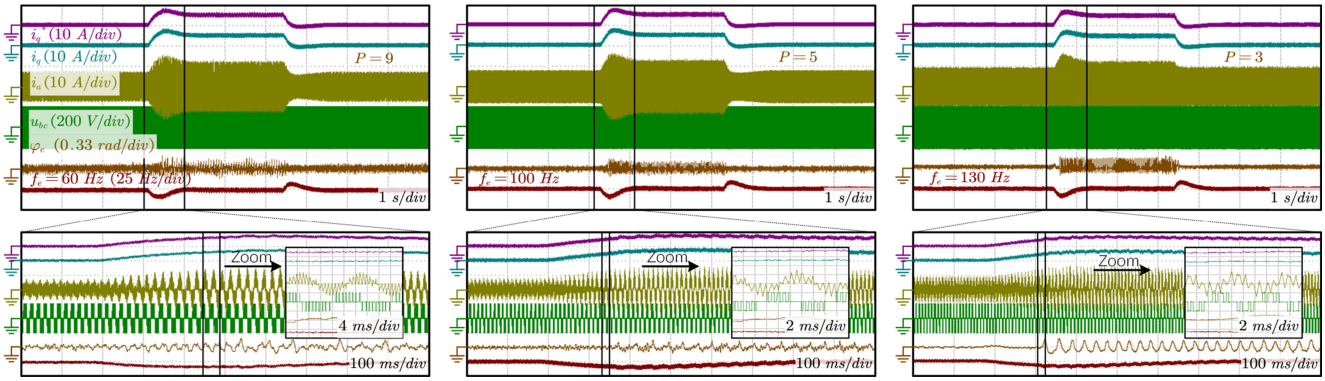


Fig. 26. Results of the loading and unloading experiments. The machine works in speed control mode.

will trigger the over-current protection of the test bench, a detailed transition strategy comparison result is demonstrated in Fig. 24 with the simulation results. The transition timing and transition vector adjustment ensure that the machine works in a steady state after the transition.

The reactions of the controller to current reference step changes in the FOC control system with proposed synchronized SVPWM implementation are shown in Fig. 25. A step-change in i_d^* is applied and the controller shows satisfactory dynamic performance. Also, a good decoupling ability of current control is verified, no apparent oscillation exists in i_q when the command of i_d changes.

The results of step loading and unloading experiments are shown in Fig. 26. In the experiments, the controller works in speed control mode, and the load machine controls the torque. The experiments are carried out in different pulse patterns with the load changes from 0 to 6 N·m. To show the performance of PLL in the dynamics, φ_e is plotted in the figure. The current controller quickly tracks the current reference, and the synchronized SVPWM works correctly in all conditions. Because the phase mapping (9) will amplify the noise, φ_e in pulse pattern $3(3, \mathrm{I}_{\uparrow})$ is more stable than in $9(9, \mathrm{I}_{\downarrow})$. An increase in the ripple of φ_e can be observed after loaded. The reason is that the load torque is unstable, which causes about 3-Hz speed ripples and affects the accuracy of the PLL. In spite of this, the synchronization error of the PLL is less than 5°.

Fig. 27 demonstrates the effectiveness of the over-modulation strategy. In the experiments, the bus voltage is reduced to 100 V for testing over-modulation operation. The machine accelerates from 80 to 100 Hz and enters over-modulation operation, then decelerate to 80 Hz and exits over-modulation operation. The modulation is able to transit to six-step modulation with the proposed over-modulation strategy. The synchronization is not affected by the over-modulation strategy. The i_d decreases in the acceleration because of the intervention of the flux-weakening controller.

Fig. 28 contains the experimental waveforms of pulse pattern transition in over-modulation operation. In these experiments, the machine accelerates to 100 Hz and enters the over-modulation region, then the pulse pattern changes. After 0.5 s, the machine decelerates to 80 Hz and returns to the linear-modulation region. The pulse pattern transition strategy works fine with the proposed transition strategy in over-modulation operation, and the modulation always keeps synchronized.

The results of the speed dynamic experiment are shown in Fig. 29. The machine accelerates from 35 to 135 Hz in about 0.5 s using the proposed pulse pattern selection strategy. The used pulse patterns are shown in Fig. 29(a). The proposed implementation of synchronized SVPWM shows superior performance in the speed dynamic test.

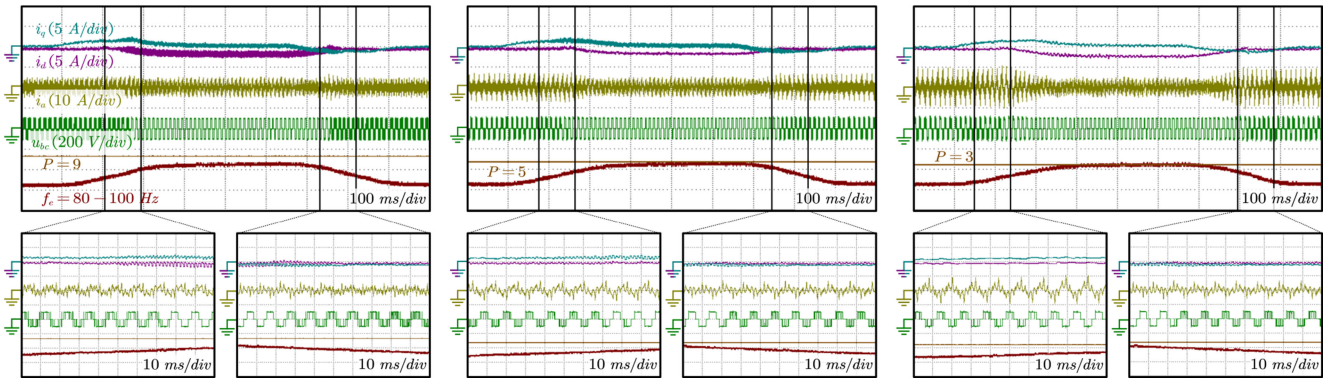


Fig. 27. Experimental results of over-modulation in synchronized SVPWM. The machine works in speed control mode and bus voltage is reduced to 100 V.

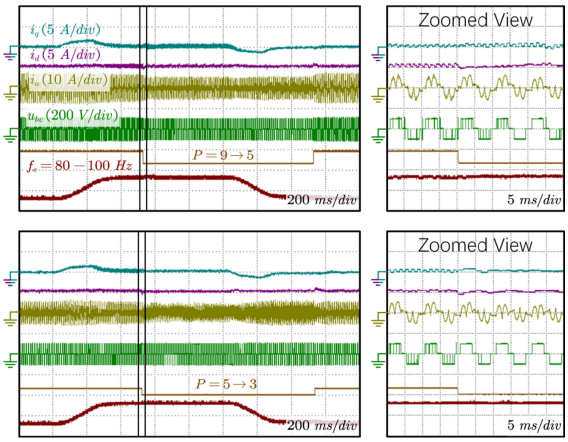
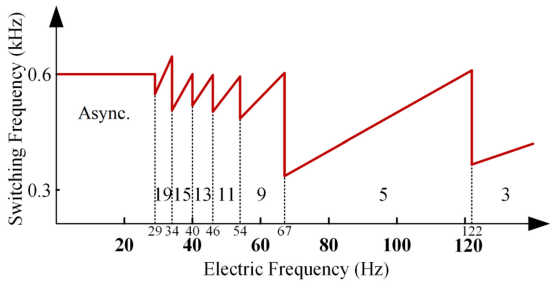


Fig. 28. Experimental results of pulse pattern transition in over-modulation operation. The machine works in speed control mode and the bus voltage is reduced to 100 V.



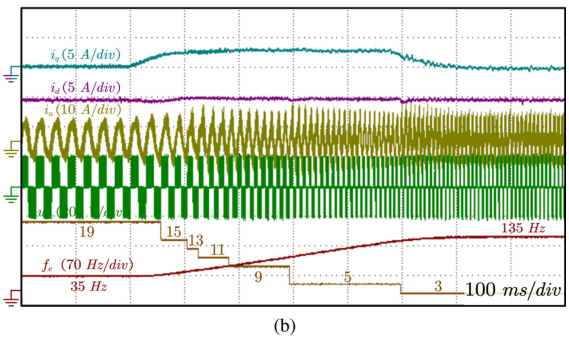
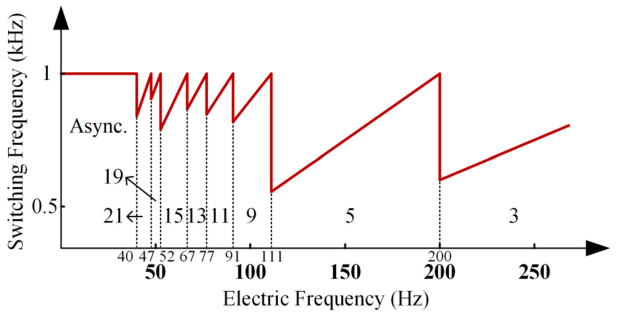


Fig. 29. Experimental results of speed dynamic test on the test bench. (a) Pulse patterns and the corresponding switching frequencies. (b) Experimental waveform.



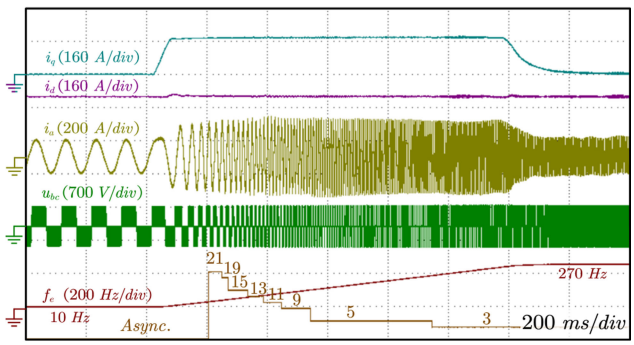


Fig. 30. Experimental results of speed dynamic test in HIL. (a) Pulse patterns and the corresponding switching frequencies. (b) Experimental waveform.

B. Full-Scale HIL Experiments on a 120 kW PMSM

The full-scale HIL experiments aim at simulating the working condition of traction applications and conducting a comprehensive test of the proposed strategies. The results of the speed-dynamic experiment are shown in Fig. 30. The machine accelerates from 10 to 270 Hz in about 1 s. The pulse patterns are selected according to the proposed strategy, and the switching frequency curve is shown in Fig. 30(a). The controller shows satisfactory performance in tracking the current reference. The pulse pattern transits from asynchronous SVPWM to $3(3, \mathrm{I}_{\uparrow})$ during the acceleration. The PLL synchronizes the modulation well in speed dynamics, and the pulse pattern transition brings no negative influence on the performance of the current controller.

VII. Conclusion

In this article, the authors take MI into consideration while selecting pulse patterns of synchronized SVPWM. It is verified that the pulse pattern selection strategy can reduce harmonic distortion. For applying synchronized SVPWM, a complete implementation of synchronized SVPWM is developed, which includes a PLL-based synchronization method and a pulse pattern transition strategy. The transition strategy accommodates to transitions of special pulse patterns and the operation in the over-modulation region. The proposed implementation permits the synchronized SVPWM to track fast-dynamic modulation reference without degrading the performance of the current control loop in both linear-modulation operation and over-modulation operation. The experiments verified the effectiveness of the implementation in all kinds of working conditions. Harmonic-reduced synchronized SVPWM strategy is preferred in high-power drives under low-switching-frequency conditions.

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