Letters

Single Pulse Unclamped-Inductive-Switching Induced Failure and Analysis for 650 V p-GaN HEMT

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***Abstract*—This letter firstly reveals the single pulse unclamped-inductive-switching (UIS) withstanding physics and failure mechanism for p-GaN high electron mobility transistor (HEMT) with Schottky type gate contact. Unlike silicon/silicon carbide (Si/SiC)-based devices, the p-GaN HEMT withstands the surge current from load inductor by storing the energy into the output capacitance of the device, rather than dissipating the energy by avalanche process. To describe the UIS process, physics-based models are proposed. Also, by the simulations and de-cap/de-layer experiments, the failure mechanism is presented as a different manner compared with Si/SiC-based devices. The high voltage during the UIS process introduces high electric field near the drain contact, which leads to the inverse-piezoelectric effect, then bringing the rise-up of the leakage current and high power dissipation. As a result, the region near drain contact is burned by thermal runaway. Moreover, it is demonstrated that higher bus voltage and larger load inductance will increase the UIS-induced failure risk, while the gate resistance, turn-OFF gate voltage and ambient temperature exhibit little influences upon the UIS withstanding capability of the device.**

***Index Terms*—Failure physics, p-GaN high electron mobility transistor (HEMT), unclamped-inductive-switching (UIS).**

I. Introduction

ENHANCEMENT-MODE power GaN high electron mobility transistors (HEMTs) have been applied to power electronic systems with the trend of rapid increase [1]–[4]. Among the structures realizing HEMT normally-OFF, the p-GaN gate structure with Schottky type gate contact can be the most competitive one since it maintains the significant advantages of pure HEMT and relatively low gate leakage current. The performances of modern power electronic systems have been improved to meet the requirements of development by using p-GaN HEMTs [5]–[7]. However, the reliability issues are always the obstacles before p-GaN HEMTs can be widely used in products [8]–[11]. When applied to power electronic systems with inductive loads or parasitic components in the circuits, the p-GaN HEMT may suffer from unclamped-inductive-switching (UIS) stress. During the UIS, the energy stored in the inductors will transfer into the switching device. For silicon/silicon carbide (Si/SiC) power devices, the avalanche process dissipates the energy from inductor and the voltage drop on the device is clamped at a certain value. However, there is almost not avalanche process in the p-GaN HEMT and not voltage clamping, leading to high failure risk. Unfortunately, there are few investigations on the UIS withstanding capability of the p-GaN HEMT. In [12]–[15], it was concluded that the UIS withstanding capability of p-GaN HEMT was dependent on the gate leakage current. Also, there was a conclusion that the capability was related to the capacitive charging process for ohmic gate p-GaN HEMT and normally-on HEMT [16]–[18]. Generally, these papers only focused on the withstanding phenomena, the physical mechanism analysis for the UIS-induced failure of p-GaN HEMTs was lacked.

With the help of physics-based models, de-cap/de-layer solutions, and technology computer-aided design (TCAD) simulations on Silvaco platform, this letter firstly reveals the comprehensive withstanding physics and failure mechanism of p-GaN HEMT with Schottky type gate contact under single pulse UIS condition. Moreover, the influences of the UIS test conditions including bus voltage (V_{bus}), load inductance (L_{load}), turn-off gate resistance ($R_{\mathrm{g_off}}$), turn-off gate voltage ($V_{\mathrm{gs_off}}$), and ambient temperature are discussed.

II. Experiment Setups and Withstanding Physics

Fig. 1(a) shows the cross-section diagram of the device under test (DUT) from GaN System Inc. (GS66504B) [19], the rated drain current and voltage are 15A and 650V, respectively. The gate contact is Schottky type. Fig. 1(b) and (c) show the test circuit and test board for the single pulse UIS investigation, respectively. The DUT is driven by an isolated gate driver (Si8271) together with a 6-V isolated dc power supply. The $R_{\mathrm{g_off}}$ is 25 Ω, the gate voltage (V_{gs}) is a single pulse voltage (V_{pulse}) with amplitude of 6 V (0–6 V), the L_{load} is 3 mH and the V_{bus} is 50V.

The typical measured and simulated waveforms of the DUT under UIS condition are presented in Fig. 2. The used simulation

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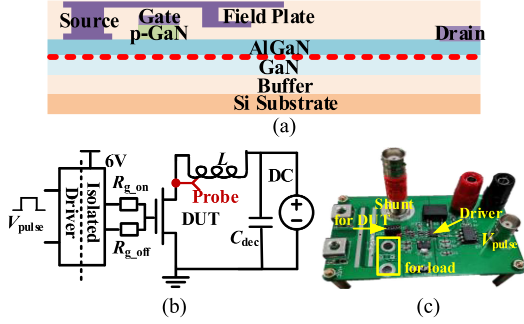

Fig. 1. (a) Cross-section diagram of the DUT. (b) Topology of the test circuit. (c) Test board.

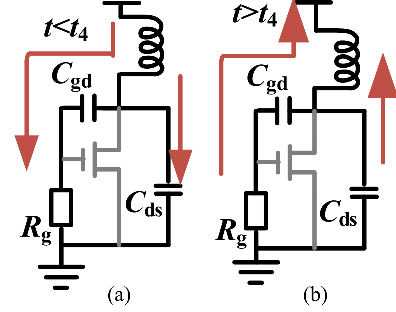

Fig. 3. (a) Energy transferring process before t_4. (b) Energy transferring after t_4.

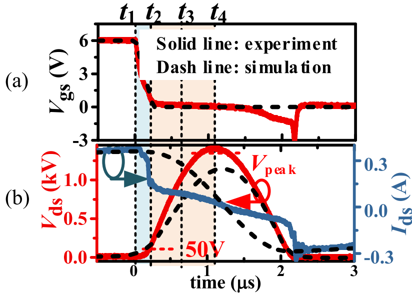

Fig. 2. Typical waveforms of the UIS. (a) *V*gs. (b) *V*ds and *I*ds.

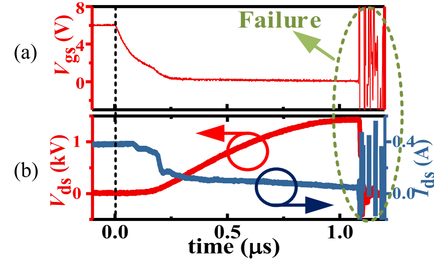

Fig. 4. Waveforms when failure happens. (a) V_{gs}. (b) V_{ds}&I_{ds}.

platform is Silvaco Atlas. The incomplete ionization model is used for Mg-dopant simulation, other key models named *GaNsat.n*, *selb*, *lat.temp*, *consrh*, *auger*, *albrct.p*, *ten.piezo*, and *calc.strain* are used for static and mix-mode simulations [20]. The UIS conditions for simulations are set as the same with the experiments. It is noted that the simulated values of typical static electrical parameters in this letter have been calibrated and approximately match the measured values. The small differences for UIS waveforms, as shown in Fig. 2, may result from the inevitable parasitic components in the practical test boards, however, these differences will not influence the conclusions. At the moment t_1, the DUT begins to turn off, the channel resistance begins to increase and the drain current (I_{ds}) decreases. Then the V_{bus} begins to charge the output capacitance ($C_{\mathrm{oss}} = C_{\mathrm{gd}}+C_{\mathrm{ds}}$) of the DUT, and the drain to source voltage (V_{ds}) reaches the V_{bus} at the moment t_2. Once the V_{ds} is higher than V_{bus}, such as the moment t_3, the energy stored in the load inductor is transferring to the C_{oss}, as shown in Fig. 3(a). At the moment t_4, all the energy stored in inductor has transferred to the C_{oss} and the V_{ds} reaches the highest value (V_{peak}), which introduces the risk of failure. After t_4, the energy in C_{oss} begins to transfer back into inductor and the negative displacement current appears, as shown in Fig. 3(b), which differs from Si/SiC devices. For Si/SiC devices, the energy from inductor is dissipated by avalanche process, and nearly no energy transfers back to the inductor, moreover, the V_{ds} is clamped to a certain value.

According to the physics, the energy transferring process can be modeled. Since the process after t_4 is opposite of that before t_4, only the models before t_4 are presented as follows:

$$E_1 = 0.5 I_{load}^2 L_{load} \tag{1}$$

$$E_2 = \int_0^{V_{bus}} V_{ds} \left(\int_0^{V_{bus}} C_{oss}(V_{ds}) dV_{ds} \right) dV_{ds} \tag{2}$$

$$E_3 = \int_{t_1}^{t_4} I_{ds} V_{ds} dt \tag{3}$$

$$E_4 = \int_0^{V_{peak}} V_{ds} \left(\int_0^{V_{peak}} C_{oss}(V_{ds}) dV_{ds} \right) dV_{ds} \tag{4}$$

$$E_4 = E_1 + E_2 - E_3 \tag{5}$$

where I_{load} is the maximum load current. E_1 is the energy stored in L_{load}. E_2 is the initial energy in C_{oss} charged by V_{bus}. E_3 is the switching energy loss between t_1 and t_4. E_4 is the energy stored in C_{oss} at t_4, the value of which at failure moment reflects the UIS withstanding capability of the p-GaN HEMT and is determined by the V_{peak}.

III. Results and Discussions

According to the withstanding physics, the V_{ds} cannot be clamped due to the lack of avalanche process and reaches a high voltage. When the I_{ds} reaches 0.4A with $V_{\mathrm{bus}} = 50$ V, $L_{\mathrm{load}} = 3$ mH, the V_{peak} reaches 1400 V and the DUT is destroyed, as seen in Fig. 4. Based on (1)–(5), the calculated E_1 is about 240 μJ, E_2 is about 1 μJ, E_3 is about 55 μJ, the UIS energy E_4 is about 186 μJ. In [21] and [22], the calculated UIS energies of the Si device and SiC device with similar operating voltage/current levels were about 68 and 112 mJ, respectively. Clearly, compared with the Si/SiC devices with the same ratings, the p-GaN HEMT withstands much lower UIS surging energy. To understand the failure mechanism, the mix-mode TCAD simulations have been carried out. Fig. 5 shows the lattice temperature (T_{lat}) distributions at the four moments during the UIS process, t_1 to t_4 in

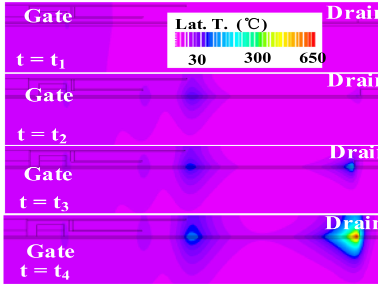

Fig. 5. Mix-mode simulations results of T_{lat} distributions ($t_1 - t_4$).

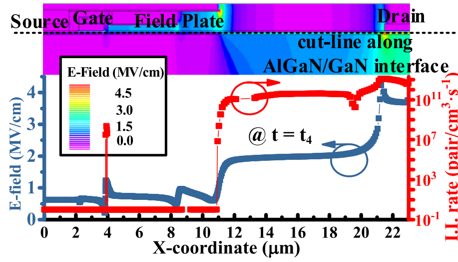

Fig. 6. Simulations results of E-field and I.I. rate distributions along the AlGaN/GaN interface when the V_{ds} reaches V_{peak} during the UIS process.

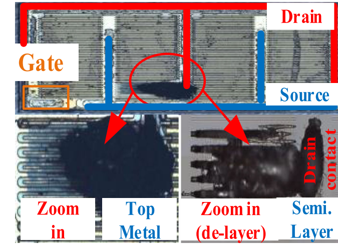

Fig. 7. Failure point validation by de-cap and de-layer experiments.

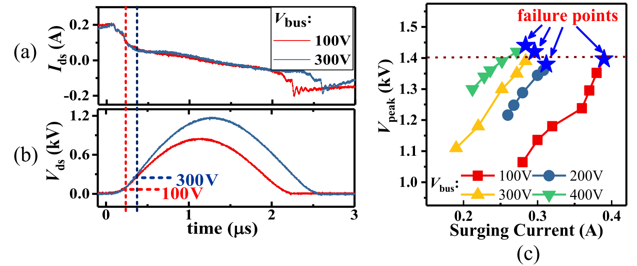

Fig. 8. Influences of V_{bus} on the UIS withstanding capability. (a) I_{ds} curves. (b) V_{ds} curves. (c) V_{peak} with I_{load} increases.

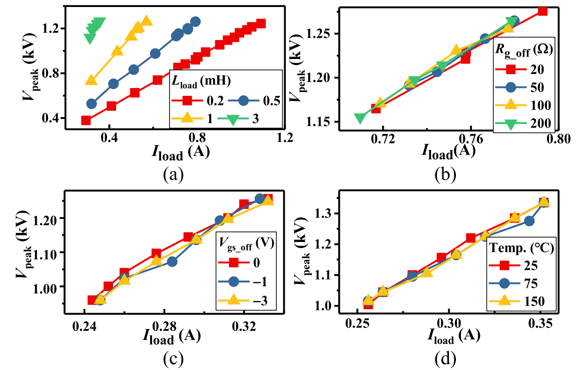

Fig. 9. Influences of (a) L_{load}, (b) external $R_{\mathrm{g_off}}$, (c) $V_{\mathrm{gs_off}}$, and (d) ambient temperature on the UIS withstanding capability.

Fig. 2. At t_4, the T_{lat} also reaches the peak value, indicating the highest failure risk during the UIS process.

The distributions of electric field (E-field) and impact ionization (I.I.) generation rate at t_4 along the AlGaN/GaN interface are also given, both the peak values appear near drain contact, as presented in Fig. 6. It is noted that the I.I. rate ($<1\times10^{15}$ pairs/cm$^3\cdot$s^{-1}) is largely lower than that in Si/SiC devices ($>1\times10^{23}$ pairs/cm$^3\cdot$s^{-1}) [23], which verifies that there is almost not avalanche process in p-GaN HEMT. In [24], it was presented that the avalanche-induced latch-up of parasitic bipolar-junction-transistor (BJT) for the Si device was widely confirmed when concerning its UIS failure. For the SiC device, the built-in potential of SiC pn junction is so high that the latch-up of parasitic BJT cannot be triggered easily. In [22] and [25], it was indicated that the UIS failure of the SiC device directly resulted from the avalanche-induced thermal runaway. Clearly, the failure of p-GaN HEMT may be not due to the weak avalanche. Meanwhile, the E-filed near gate is relatively low, indicating that the gate is well protected by the specially designed field plates. However, the inverse-piezoelectric effect may appear under the extremely high E-field near the drain, which creates dislocations (defects) and leads to the rise-up of the leakage current [26]. As a result, the heat can be induced by the power of high leakage current under high voltage bias, finally destroying the device. In short, the inverse-piezoelectric effect under high E-field under drain contact may be the dominating reason for the failure.

Further de-cap and de-layer experiments have been carried out to verify the failure mechanisms, and the results are presented in Fig. 7. The phenomenon at top metal layer indicates that the burning originates from the drain contact. When de-layering to the semiconductor layer, the most serious burning is observed at drain contact. Combining the above simulation results, it can be considered that there is thermal runaway after the leakage rise-up, so that the severe burning occurs near drain contact.

Comprehensive investigations on the influences of working conditions upon the single pulse UIS withstanding capability of p-GaN HEMT are meaningful for the device users. Fig. 8 shows the influences of different V_{bus} with the same I_{load}. As seen in Fig. 8(a) and (b), the larger the V_{bus} is, the higher the peak V_{ds} reaches, which results from that the C_{oss} stores larger energy at higher V_{bus}, as (1)–(5) described. Moreover, as shown in Fig. 8(c), the failure happens when the V_{ds} reaches near 1400 V. Differently, the V_{ds} under UIS condition for Si/SiC devices is clamped to a certain value and cannot reach too high. As discussed above, the failure is dependent on the E-field, which originates from the V_{peak}. Considering the manufacturing process, it is reasonable that the V_{peak} is a little different among the DUTs. Statistically, the failure voltages are the same for the experimental devices with different V_{bus}.

Moreover, the influences of L_{load} on the UIS withstanding capability are also investigated. As shown in Fig. 9(a), lower

$L_{\rm load}$ leads to lower $V_{\rm peak}$ at the same $I_{\rm load}$, because the lower $L_{\rm load}$ stores less energy and brings less energy into the $C_{\rm oss}$, as modeled above. Also, the influences of the $R_{\rm g_off}$, the $V_{\rm gs_off}$, and the ambient temperature are investigated, as shown in Fig. 9(b) to (d). With different $R_{\rm g_off}$ and $V_{\rm gs_off}$, the barrier height of the Schottky metal/p-GaN junction may be different. However, since the reverse-biased p-GaN/AlGaN/GaN diode maintains most of the drain to gate voltage drop during the UIS process, the barrier height of the Schottky metal/p-GaN junction can be neglected. As a result, the $R_{\rm g_off}$ and the $V_{\rm gs_off}$ have little influences on the UIS withstanding capability of p-GaN HEMT. Finally, at high temperatures, as investigated in [27], the $C_{\rm oss}$ changes little, thus the $V_{\rm peak}$ cannot be influenced by the ambient temperature when the $C_{\rm oss}$ has stored the same energy, as presented in Fig. 9(d).

According to the failure mechanisms and influences of test conditions described above, smaller $I_{\rm load}$ and $L_{\rm load}$ should be effective to prevent the $V_{\rm peak}$ from reaching a high value when concerning the UIS withstanding capability of p-GaN HEMT. On the other hand, alleviating the E-field near drain by adding drain field plate or introducing a p-type buried layer under the drain is also the effective way to improve the single pulse UIS withstanding capability of p-GaN HEMT.

IV. Conclusion

Comprehensive single pulse UIS withstanding physics and failure mechanism of p-GaN HEMT with Schottky gate contact are firstly presented in this letter. Due to the lack of avalanche process, both the UIS withstanding physics and failure mechanism of p-GaN HEMT are different from Si/SiC devices. The UIS energy is stored in the $C_{\rm oss}$ rather than dissipated by the avalanche process. High E-field during the UIS process is introduced near drain contact, which enhances the inverse-piezoelectric effect and induces defects under the drain, leading to the rise-up of the leakage current and high power dissipation. Finally, the device is destroyed by the thermal runaway. Moreover, according to the established models and experiments, higher $V_{\rm bus}$ and larger $L_{\rm load}$ increase the UIS-induced failure risks, while the $R_{\rm g_off}$, $V_{\rm gs_off}$ and ambient temperature exhibit little influences. To improve the UIS withstanding capability, some methods to reduce the drain peak E-field during the UIS process are suggested.

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