Simplified Predictive Duty Cycle Control of Multilevel Converters With Internal Identical Structure

Dehong Zhou, *Member, IEEE*, Zhongyi Quan, *Member, IEEE*, and Yunwei Li, *Fellow, IEEE*

***Abstract*—Classical finite control set model predictive control of multilevel converters faces two major limitations: heavy computation burden and low steady-state performance. On the other hand, the internal paralleled or cascaded identical structure is extensively employed in multilevel converters as the voltage level increases. Taking advantage of the internal identical structure in multilevel converters, a simplified predictive duty cycle control method for multilevel converters is proposed in this article. First, a series of switching pairs with the identical structure are modeled as a virtual switching state, and the number of the corresponding voltage vectors can be significantly reduced. Then, a least-square optimization problem is formulated to calculate the duty cycles for optimal output current tracking using these virtual voltage vectors. The output current quality is enhanced due to the employment of the interleaved output voltage stage with phase-shifted pulsewidth modulation. As the number of voltage vectors is significantly reduced, the computation burden is drastically reduced. The proposed method can be applied in various multilevel topologies with internal identical structures. Simulation and experimental results on the multilevel converters with internal cascaded/paralleled identical cells are presented to verify the good performance and application value of the proposed method.**

***Index Terms*—Capacitor voltage balance, circulating current suppression, internal cascaded/paralleled multilevel converter, model predictive control (MPC), phase-shifted pulsewidth modulation (PWM).**

I. Introduction

MULTILEVEL converters have been widely applied in grid-tied inverters [1], energy storage systems [2], medium voltage motor drive systems [3], and so on [4], thanks to their advanced benefits of better output voltage quality, reduced switching losses, lower dv/dt, and so on. Among the existing multilevel converters, neutral-point-clamped (NPC) [5], [6], flying capacitor (FC) [7], cascaded H-bridge (CHB) [8] multilevel converters are classical multilevel topologies that are the most widely used in the industry for various applications.

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Dehong Zhou is with the School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China (e-mail: dehong1@ualberta.ca).

Zhongyi Quan and Yunwei Li are with the Department of Electrical and Electronic Engineering, University of Alberta, Edmonton, AB T6G 2R3, Canada (e-mail: zquan@ualberta.ca; yunwei.li@ualberta.ca).

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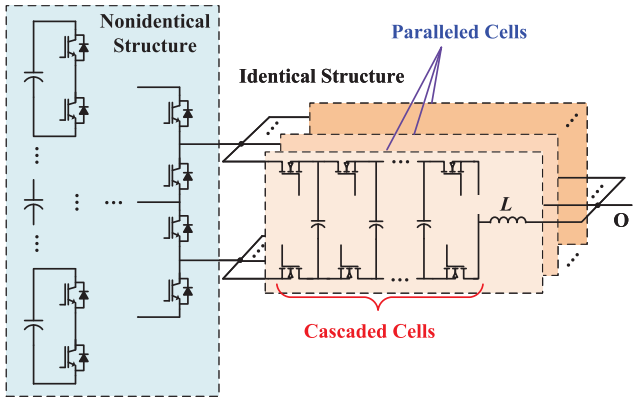

Fig. 1. Multilevel converters with internal cascaded and paralleled cells.

In order to increase the voltage levels, a large number of multilevel converter topologies are studied and investigated in the literature [9]–[14]. Among these topologies, the ones with fully or partially cascaded or paralleled cells, as illustrated in Fig. 1, have been identified as the most promising topologies for practical applications, owing to the advantages such as simple structure, scalability, and possible hybrid utilization of semiconductors [15], [16].

Although flexible adoption of cascaded/paralleled cells in multilevel converters provides attractive features in cost, volume, and efficiency, the control complexity is increased that should be considered. Generally, multiple control objectives, such as FC balance, circulating current suppression, dc-link voltage balance, and output current control, should be achieved simultaneously when the number of voltage levels becomes large.

To achieve the multiple-objective control in the multilevel converter, the linear system theory-based multiple proportional integral (PI) or proportional resonant (PR) loops with pulsewidth modulation (PWM), may be a possible choice. However, multiple PI loops lead to tedious tuning work, and the interactions of the different PI/PR loops may lead to poor control performance. In addition, proper modulation strategy is also required to map the desired voltage reference to gating signals. Carrier-based PWM, such as phase-shifted PWM [17], level-shifted PWM [18], is a widely accepted method with a simple

implementation process. However, the dc voltage utilization rate of these methods is only 87% compared to that of the space-vector PWM (SVPWM) scheme. Zero-sequence voltage injection, which is complicated due to the redundant switching state within each phase, has to be implemented to increase its dc voltage utilization rate. On the other hand, SVPWM is a much more complex modulation scheme in comparison with the carrier-based one. The SVM hexagon diagram is divided into a huge number of triangle sectors, and every possible switching sequence in each sector is calculated in consideration of the neutral voltage balance [19].

Model predictive control (MPC) can realize the optimal control of multiple objectives, and it has been attracting growing interest due to its merits such as fast dynamic response, straightforward realization, and easy inclusion of nonlinear constraints [20]–[25].

However, classical finite control set MPC gets the optimal switching state by an exhaustive searching approach. When the number of available switching state is large, it may be impractical to implement the classical MPC with the state-of-art microprocessor. This is particularly true for multilevel converters with high-voltage levels, because the number of available switching states is increasing exponentially with the number of voltage levels [26], [27]. In addition, the multiple additional constraints, such as dc-link capacitor balance, circulating current suppression, FC balance, will also increase the calculation amount of the classical MPC. In summary, time-consuming computation is an obstacle that limits the application of the conventional MPC, especially when considering that more and more multilevel converters are employed in low voltage applications where power density needs to be high, e.g., modern aircraft [28]. In these applications, the high switching frequency as well as high fundamental frequency make the computational burden issue even more challenging.

Extensive research efforts have been devoted to reducing the computation burden of MPC [23], [29]–[32]. A computationally efficient MPC, which decoupled the control of internal capacitor voltage balance from the cost function by an external voltage sorting algorithm, was proposed in [29]. This scheme increased the complexity and reduced the control option to $2N+1$ voltage levels. Hexagon candidate region and triangle candidate region preselection methods were proposed to reduce the computation burden of an NPC inverter [30]. When applied to the multilevel converters with higher voltage levels, the reduced computational burden was not significant. Two state machines with strict commutation path restrictions were proposed to reduce the computational burden of a five-level ANPC [23]. As only limited commutation paths were available in each sampling period, the sampling period should be short enough to achieve satisfactory performance, which imposes a very high requirement on the computational power of the controller. Moreover, as the voltage level increases, the design of the state machines would be complicated. Some other reduced computational burden MPC methods were achieved by reducing the number of feasible switching states using preselecting methods [31], [32]. However, a certain number of switching states are still required to optimize all the control objectives simultaneously, and the preselecting methods may lead to inferior output performance.

On the other hand, MPC undergoes no PWM process and outputs only one switching state during the entire sampling period. The output staircase waveforms are noninterleaved as all the switching states will update at the same time. Therefore, the output voltage quality of the multilevel converter is not fully explored.

To fully explore the output voltage quality of the multilevel converter, and reduce the computational complexity of the classical MPC, this article presents a simplified predictive duty cycle control method to avoid the exhaustive evaluation process of all the switching state and improve the steady-state performance by taking advantage of the internal identical cells in multilevel converters. The optimal duty cycles are calculated by output current tracking error minimization and applied by the phase-shifted PWM (PS-PWM). The weighting factors are eliminated by the control flexibility provided by the duty cycle. Simulation and experimental results on the multilevel converter with internal cascaded/paralleled identical cells are presented to verify the excellent performance and application value of the proposed method.

II. Multilevel Converters With Identical Cells

The identical cells are widely employed in multilevel converters thanks to their advanced benefits of modularity, flexible expandability, ease of assembling, and so on. Among them, modular multilevel converter (MMC) [34] and CHB [35] converter, consisting of pure identical cells, are the classical multilevel converters. Nowadays, many non-MMCs have been proposed for various applications due to their flexibility and combined benefits of different topologies. However, as the voltage level increases, identical cells are partially employed in these converters.

The identical cells in the multilevel converter are subdivided into functionally identical cells and physically identical cells. The functionally identical cells do not have the same physical structure. But the switching state action in each cell leads to the same phase voltage change in the total output. The typical multilevel converter with functionally identical cells is shown in Fig. 2(a). The physically identical cells are the ones that have the same physical structure, and their switching state action leads to the same phase voltage change in the total output. The typical topology with physically identical cells is shown in Fig. 2(b). The functionally/physically identical structure is widely employed in the multilevel converter. The typical examples of topologies with internal identical cells are five-level active-NPC (ANPC) converters [16], dual-FC ANPC converters [36], multilevel converters with parallel modularity [37], some hybrid clamped multilevel converters [9], etc.

Two typical topologies presented in Fig. 2 are investigated as case studies to validate the proposed predictive control method. One is the $2N+1$ level internal cascaded multilevel converter (ICMC), and the other is the $2N+1$ level internal parallel multilevel converter (IPMC). As presented in Fig. 2 (a), ICMC

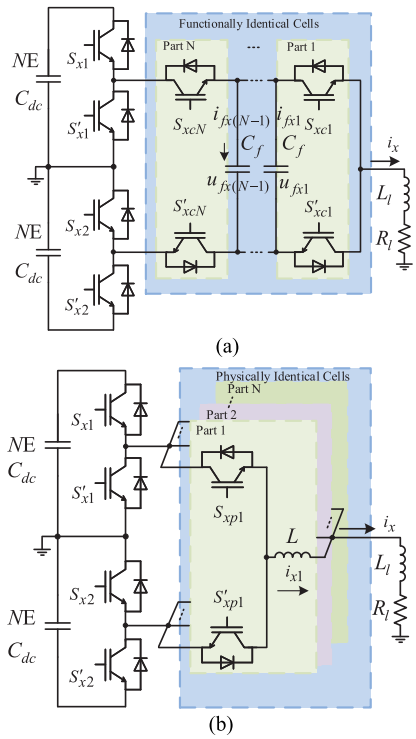

Fig. 2. Identical cells in multilevel converters. (a) Structure of a 2*N* + 1-level ICMC [33]. (b) Structure of a 2*N* + 1-level IPMC [15].

can be considered as N cascaded-connected two-level cells combined with an NPC topology. For simplicity, the dc-link capacitor voltage and FC capacitor voltage are assumed to be balanced. The N cascaded-connected two-level cells can be considered as functionally identical cell, where the output voltage of each cell is identical, where "ON" state of S_{xcn} ($x \in \{a, b, c\}$, $n \in \{1, 2, \ldots, N\}$) will insert E to the terminal and "OFF" state of S_{xcn} will insert zero voltage to the terminal, E is the voltage across each cell. L_l is the load inductor, and R_l is the load resistor.

As presented in Fig. 2(b), IPMC can be considered as N parallel-connected two-level cells combined with an NPC topology. The N parallel-connected two-level cells can be considered as physically identical cell, where each cell is identical and the "ON" state of S_{xpn} will insert E to the terminal and "OFF" state of S_{xpn} will insert zero voltage to the terminal, E is $\frac{1}{2N}$ of the dc-link voltage. L is the internal inductor.

III. Simplified Model of ICMC/IPMC

The mathematic models of ICMC and IPMC are introduced in this section.

A. Model of the Functionally Identical Cell in ICMC

The circuit configuration of a single-phase ICMC is shown in Fig. 2(a), where S_{x1}, S'_{x1}, S_{x2}, and S'_{x2} require N switches connected in series or high-voltage switches to bear a higher voltage, which is N time of S_{xcn} and S'_{xcn} ($n \in \{1, 2, \ldots, N\}$), N is the number of the identical cells in ICMC. S_{x1} and S_{x2} requires the same switching signals. i_x are the output current.

TABLE I
Simplified Switching State of ICMC and IPMC

	S_{x1}/S_{x2}	S_{vx}	u_{xo}
V_0	0	0	$-NE$
V_1	0	1	-0
V_2	1	0	0
V_3	1	1	NE

L_l and R_l are the load inductance and resistance, respectively. The voltages across the dc-link capacitors are equal to NE.

The FC voltage u_{fxn} ($n \in \{1, 2, \ldots, N-1\}$) is set to nE in cell n. Thus, voltage across cell n is equal to

$$u_{\text{ccn}} = nE - (n-1)E = E. \tag{1}$$

As shown in (1), the voltage across the switching pair in cell n is equal to E. Therefore, the cascaded identical cell in ICMC can be regarded as functionally identical cell.

The total output phase voltage of the identical cell in ICMC can be expressed as

$$u_{xo} = \frac{\sum_{n=1}^{N}(u_{\text{ccn}} t_x)}{T_s} = \frac{NEt_x}{T_s} \tag{2}$$

where t_x is the desired optimal duty cycle for the identical cells.

B. Model of the Physically Identical Cell in IPMC

The circuit configuration of a single-phase IPMC is shown in Fig. 2(b), where S_{x1}, S'_{x1}, S_{x2}, and S'_{x2} bear the same voltage as those of S_{xpn} and S'_{xpn} ($n \in \{1, 2, \ldots, N\}$), N is the number of the identical cells in IPMC.

The voltage across cell n of the IPMC can be denoted as

$$u_{pcn} = NE. \tag{3}$$

As shown in (1), the voltage across the switching pair in cell i is the same and equal to NE. Therefore, the paralleled identical cell in IPMC can be regarded as physically identical cell.

The total output phase voltage of the identical cell in IPMC can be expressed as

$$u_{xo} = \frac{\sum_{n=1}^{N}(u_{ccn} t_x)}{T_s} = \frac{NEt_x}{T_s}. \tag{4}$$

C. Simplified Model of ICMC/IPMC

As shown in (2) and (4), the identical cell in ICMC can be regarded as the functionally identical cell while the identical cell in IPMC can be considered as the physically identical cell. By considering the identical structure in ICMC/IPMC as a virtual switching state, the number of the switching combinations of the multilevel converter can be significantly reduced.

As shown in Table I, the number of switching states can be reduced to four switching states in each phase. S_{x1}/S_{x2} is always operated as the fundamental frequency to reduce the switching losses. The duty cycle of the virtual switching state should be determined to generate the gate signals for each switching pairs. In the three-phase condition, there are $4^3 = 64$ virtual voltage vectors.

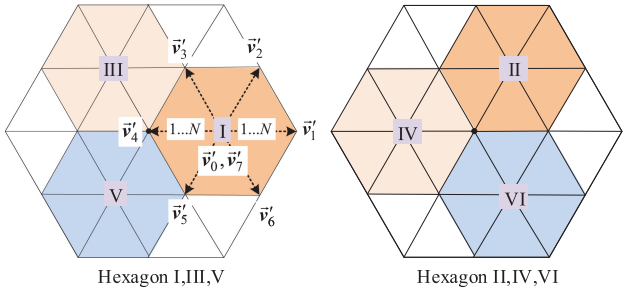

Fig. 3. Virtual voltage vectors for ICMC and IPMC.

To further simplify the system model, the number of switching states can be further reduced by classifying the voltage vector into two groups: S_{x1}/S_{x2} and S_{vx}. As S_{x1}/S_{x2} should operate at the fundamental switching frequency to reduce the switching loss, their gating signals can be determined first using finite control set MPC. After the determination of S_{x1}/S_{x2}, then the optimal duty cycles of the S_{vx} are calculated and applied by PS-PWM to achieve optimal current tracking.

According to the switching state selection of S_{x1}/S_{x2}, the voltage vectors can be categorized into six small hexagons, as shown in Fig. 3. In each hexagon, the number of the virtual voltage vector is only eight. Six voltage vectors lie in the vertex of the hexagon, while two of them lie in the center of the hexagon. By selecting the optimal vectors in the small hexagon and calculating the duty cycles for those virtual voltage vectors, the computational burden of the proposed predictive controller can be reduced.

IV. Proposed Predictive Duty Cycle Control

For simplicity, the dc-link capacitor voltage and FC capacitor voltage are assumed to be balanced. As analyzed in Section III, the system model can be simplified by taking advantage of the functionally/physically identical cell in the multilevel converter. Although the ICMC and the IPMC have the same mathematic model in output current control, the two types of topologies have different internal dynamic requirements. FC voltage balance should be guaranteed in the ICMC while circulating current suppression should be guaranteed in the IPMC. In this section, the proposed predictive duty cycle control with PS-PWM of ICMC and IPMC will be presented, respectively. The proposed method includes two parts: switching state selection of the nonidentical cell and optimal duty cycle generation for the identical cell.

A. Switching State Selection of the Nonidentical Cell

The cascaded-connected or high-voltage switch S_{x1}/S_{x2} is nonidentical cells and can operate at fundamental switching frequency to reduce the switching loss.

The switching states of the nonidentical cell can be selected by evaluating the cost function defined as follows:

$$J = \left(i_\alpha^* - i_\alpha(k+1)\right)^2 + \left(i_\beta^* - i_\beta(k+1)\right)^2. \tag{5}$$

TABLE II
Voltage Vector for Small Hexagon Selection

voltage vectors $\boldsymbol{v}$	Switching states $(S_{a1}S_{b1}S_{c1})$	Hexagon h
$\boldsymbol{v}_1 = \frac{NE}{3}$	(100)	1 (I)
$\boldsymbol{v}_2 = \frac{NE}{6} + j\frac{\sqrt{3}NE}{6}$	(110)	2 (II)
$\boldsymbol{v}_3 = -\frac{NE}{6} + j\frac{\sqrt{3}NE}{6}$	(010)	3 (III)
$\boldsymbol{v}_4 = -\frac{NE}{3}$	(011)	4 (IV)
$\boldsymbol{v}_5 = -\frac{NE}{6} - j\frac{\sqrt{3}NE}{6}$	(001)	5 (V)
$\boldsymbol{v}_6 = \frac{NE}{6} - j\frac{\sqrt{3}NE}{6}$	(101)	6 (VI)

The current at $k+1$ instant in the ICMC/OPMC can be predicted as

$$\boldsymbol{i}(k+1) = \boldsymbol{i}(k) + \frac{(\boldsymbol{v} - \boldsymbol{i}R_{eq})T_s}{L_{eq}} \tag{6}$$

where $\boldsymbol{i} = i_\alpha + ji_\beta$ is the output current vector and $\boldsymbol{v} = v_\alpha + jv_\beta$ is the converter voltage vector. L_{eq} and R_{eq} are the load inductance and resistance, respectively. $L_{eq} = L_l$ and $R_{eq} = R_l$ in the ICMC, whereas $L_{eq} = \frac{L}{N} + L_l$ and $R_{eq} = R_l$ in the IPMC.

As analyzed in Section III, the switching state can be determined by determining the hexagon. In order to simplify the calculation process, only the voltage vector lies in the center of the hexagon is utilized to evaluate the cost function. The voltage vector with the minimum cost function value will achieve the best current tracking performance, and its corresponding hexagon will be selected. As long as the desired hexagon is selected, the switching state of the nonidentical cell can be determined. The voltage vectors, their corresponding hexagons and switching states are presented in Table II.

B. Optimal Duty Cycle Generation for Internal Identical Cell

After switching states of S_{x1}/S_{x2} are determined, the available space vector diagram is narrowed into a small hexagon. For example, if hexagon I is selected, the available hexagon and the corresponding eight voltage vectors can be plotted out in the left figure in Fig. 3. By considering the identical cells as a virtual switching state, the computational burden of MPC can be reduced significantly.

The proposed method for the optimal duty cycle generation includes three steps: virtual voltage vector selection, optimal duty cycle calculation for the selected virtual voltage vector, and the duty cycle application to each switching pair in the identical cell. The implementation details of the three steps are clarified in the following text.

1) Virtual Voltage Vector Selection: Generally, two voltage vectors lie in the vertex of the hexagon together with two zero voltage vectors lie in the center of the hexagon are always selected to generate the seven-segment PWM [38], [39] in two-level converters. In the selected hexagon, a similar principle can be applied.

In the first step, the two adjacent virtual switching states should be selected. The virtual voltage vector $\boldsymbol{v}'$ in the vertex of

the hexagon can be calculated using the six basic voltage vectors shown in Table I

$$\boldsymbol{v}_i' = \boldsymbol{v}_i + \boldsymbol{v}_h \tag{7}$$

where the subscript $i, (i \in \{1, 2, \ldots, 6\})$ is the index of voltage vector number in the vertex of the hexagon. $h, (h \in \{1, 2, \ldots, 6\})$ is the selected hexagon. It should be noted that voltage vector in the center of the selected hexagon represents two switching combination of $(S_{va}S_{vb}S_{vc})$, that are (000) and (111). Here, (000) is denoted as $\boldsymbol{v}_0'$, and (111) is denoted as $\boldsymbol{v}_7'$.

Here, the two virtual voltage vectors will be selected using the same cost function (5). The current is predicted by substituting $\boldsymbol{v}'$ into $\boldsymbol{v}$ in (6). The cost function value, when $\boldsymbol{v}_i'$ is substituted, is denoted as J_i.

To selected the two adjacent virtual voltage vectors simultaneously, the cost function can be defined as

$$g_i = J_i + J_{i+1}, i \in \{1, 2, \ldots, 6\} \tag{8}$$

where $J_7 = J_1$. By evaluating (8), the two adjacent virtual voltage vectors with minimum cost function value will be selected for duty cycle calculation. After the optimization process, two adjacent optimal virtual vectors will be selected, which are denoted as $\boldsymbol{v}_{o1}$ and $\boldsymbol{v}_{o2}$.

2) Optimal Duty Cycle Calculation: The optimal duty cycle is obtained based on the current tracking error minimization. The slopes of the output current when applying selected virtual voltage $\boldsymbol{v}_{o1}$ and $\boldsymbol{v}_{o2}$ can be expressed as

$$\boldsymbol{s}_1 = \frac{1}{L_{eq}}(\boldsymbol{v}_{o1} - \boldsymbol{i}R_{eq}) \tag{9}$$

$$\boldsymbol{s}_2 = \frac{1}{L_{eq}}(\boldsymbol{v}_{o2} - \boldsymbol{i}R_{eq}) \tag{10}$$

where $\boldsymbol{s}_1 = s_{\alpha 1} + js_{\beta 1}$ and $\boldsymbol{s}_2 = s_{\alpha 2} + js_{\beta 2}$.

Moreover, the current slope of the voltage vector lie in the center of the hexagon can be obtained as

$$\boldsymbol{s}_0 = \frac{1}{L_{eq}}(\boldsymbol{v}_h - \boldsymbol{i}R_{eq}) \tag{11}$$

where $\boldsymbol{s}_0 = s_{\alpha 0} + js_{\beta 0}$.

The predicted output currents at the end of the control period can be expressed by

$$\boldsymbol{i}_\alpha(k+1) = \boldsymbol{i}_\alpha(k) + s_{\alpha 1}t_1 + s_{\alpha 2}t_2 + s_{\alpha 0}(T_s - t_1 - t_2) \tag{12}$$

$$\boldsymbol{i}_\beta(k+1) = \boldsymbol{i}_\beta(k) + s_{\beta 1}t_1 + s_{\beta 2}t_2 + s_{\beta 0}(T_s - t_1 - t_2) \tag{13}$$

where t_1 and t_2 are the optimal duty cycle for virtual voltage vectors $\boldsymbol{v}_{o1}$ and $\boldsymbol{v}_{o2}$, respectively. $T_s - t_1 - t_2$ is the duty cycle for virtual voltage vector $\boldsymbol{v}_h$.

Then, the errors between the reference and the predictive current in (5) can be represented using (12) and (13)

$$\varepsilon_\alpha = \tilde{i}_\alpha + s_{\alpha 1}t_1 + s_{\alpha 2}t_2 + s_{\alpha 0}(T_s - t_1 - t_2) \tag{14}$$

$$\varepsilon_\beta = \tilde{i}_\beta + s_{\beta 1}t_1 + s_{\beta 2}t_2 + s_{\beta 0}(T_s - t_1 - t_2) \tag{15}$$

where $\tilde{i}_\alpha = i_\alpha^* - i_\alpha(k)$ and $\tilde{i}_\beta = i_\beta^* - i_\beta(k)$.

The cost function (5) can be rewritten as

$$J = \varepsilon_\alpha^2 + \varepsilon_\beta^2. \tag{16}$$

To obtain the minimized output current tracking errors, a least square optimization problem is formulated to calculate the optimal duty cycles. The optimal values of t_1 and t_2 in (12) and (13) should satisfy the minimum value conditions

$$\frac{\partial J}{\partial t_1} = 0; \frac{\partial J}{\partial t_2} = 0. \tag{17}$$

The solution of (17) is given by the following. Therefore, the optimal duty cycle for current tracking can be obtained by

$$t_1 = \frac{(s_{\beta 2} - s_{\beta 0})\tilde{i}_\alpha + (s_{\alpha 0} - s_{\alpha 2})\tilde{i}_\beta + (s_{\alpha 2}s_{\beta 0} - s_{\alpha 0}s_{\beta 2})T_s}{(s_{\beta 2} - s_{\beta 0})s_{\alpha 1} + (s_{\beta 0} - s_{\beta 1})s_{\alpha 2} + (s_{\beta 1} - s_{\beta 2})s_{\alpha 0}} \tag{18}$$

$$t_2 = \frac{(s_{\beta 0} - s_{\beta 1})\tilde{i}_\alpha + (s_{\alpha 1} - s_{\alpha 0})\tilde{i}_\beta + (s_{\beta 1}s_{\alpha 0} - s_{\beta 0}s_{\alpha 1})T_s}{(s_{\beta 2} - s_{\beta 0})s_{\alpha 1} + (s_{\beta 0} - s_{\beta 1})s_{\alpha 2} + (s_{\beta 1} - s_{\beta 2})s_{\alpha 0}} \tag{19}$$

$$t_0 = T_s - t_1 - t_2. \tag{20}$$

The duty cycles for $\boldsymbol{v}_0'$ and $\boldsymbol{v}_7'$ are equally distributed and assigned to $t_0/2$. Therefore, the optimal duty cycles t_1, t_2 are saturated to $[0, T_s]$. If $t_1 + t_2 > T_s$, the optimal duty cycles t_1, t_2 are saturated to $\bar{t}_1 = \frac{t_1}{t_1+t_2}T_s$ and $\bar{t}_2 = \frac{t_2}{t_1+t_2}T_s$.

3) Duty Cycle Calculation for Each Identical Cell: After duty cycles for the virtual voltage vectors are determined, the duty cycle for each identical cell can be determined. The identical cells are considered as a whole during the duty cycle calculation. The total output phase voltage can be represented using (2) or (4).

The voltage across each cell is only E, and the duty cycles of all the identical cells are applied with the same duty cycles t_x. As the total output voltage of each phase is equal to the sum of all the identical cells, the total output voltage can be obtained as

$$u_{xo} = \frac{NEt_x}{T_s}. \tag{21}$$

In this way, each identical cell is applied with the same duty cycle. The applied voltage is equal to the optimal voltage in (2) or (4), indicating that the proposed predictive control method meets the voltage-second balance principle.

As the duty cycle of each switching pair is determined, the output current quality can be further improved due to the interleaved switching manner achieved by the PS-PWM, as shown in Fig. 4. In the proposed method, the carrier period is set to T_s, and the duty cycle for each identical cell is set to t_s. The duty cycle for each identical cell is updated at the valley point of the carrier. The update frequency for each cell is $\frac{T_s}{N}$. The carrier signals are triangular waves with phase-shifted by $\frac{360^o}{N}$.

C. DC-Link Voltage Balance

Other than the output current control, the dc-link capacitor voltage balance should be guaranteed for the stable operation of the ICMC/IPMC. The capacitor voltage difference $\tilde{u}_{\mathrm{dc}}$ can be

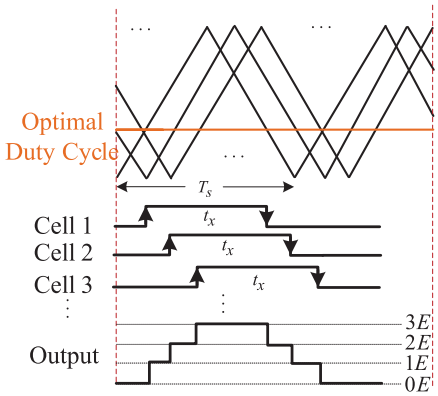

Fig. 4. Schematic diagram of the implementation of the PS-PWM for the identical cells.

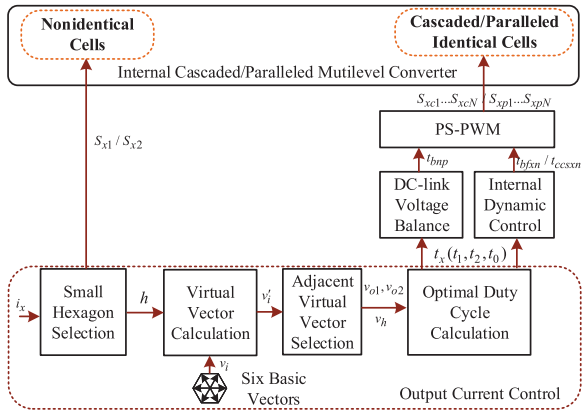

Fig. 5. Control diagram of the proposed predictive duty cycle control method of ICMC/IPMC.

expressed as

$$\frac{d\tilde{u}_{\rm dc}}{dt} = \frac{1}{C_{\rm dc}} i_{\rm NP} \tag{22}$$

where $\tilde{u}_{\rm dc} = u_{\rm dc1} - u_{\rm dc2}$, $u_{\rm dc1}$ and $u_{\rm dc2}$ are the capacitor voltages of the two dc-link capacitors. $i_{\rm NP}$ is the current of the neutral point. The dc-link capacitor voltage balance can be achieved by controlling $i_{\rm NP}$.

As well known, the switching state of $(S_{a1}S_{a2}S_{a3})$ is determined, and no control flexibility is available. Therefore, the dc-link voltage balance is achieved by adjusting the duty cycle of the switching state of $(S_{va}S_{vb}S_{vc})$. The switching states (000) and (111) of $(S_{va}S_{vb}S_{vc})$ contribute to the same effect on the output current control, however, the opposite effect for the dc-link voltage balance [17]. That is, (111) will introduce a positive neutral current while (000) will introduce a negative neutral current.

Therefore, dc-link voltage balance can be achieved by adjusting the duty cycle of the redundant virtual voltage vector without affecting of the output current control. The injecting duty cycle can be calculated as

$$t_{bnp} = k_{bnp}(\Delta u^*_{\rm dc} - \tilde{u}_{\rm dc}) \tag{23}$$

where $\Delta u^*_{\rm dc}$ is the reference of the dc-link voltage offset, which is always set to 0. k_{bnp} is a proportional control parameter to adjust the balance of the dc-link capacitor voltage.

Taking the dc-link capacitor voltage and FC capacitor voltage balancing into consideration, the duty cycle for each identical cell can be represented as

$$t_{x1} = t_x + t_{bnp}. \tag{24}$$

D. Internal Dynamic Control

The control diagram of the proposed predictive duty cycle control method of ICMC/IPMC is shown in Fig. 5. As shown in the figure, in addition to output current control and the dc-link capacitor voltage balance, internal dynamic control is also mandatory for stable operation of the multilevel converter, such as FC voltage control in ICMC and circulating current suppression in IPMC.

1) FC Voltage Control in ICMC: FC voltage control is necessary in the ICMC for its reliable operation. The duty cycle for each identical cell can be slightly adjusted for FC voltage balance. As long as the sum of the duty cycle for each identical cell is the same, the output current control will not be affected.

The average FC current at identical cell n in a carrier period is

$$i_{fxn} = (t_{xc(n+1)}t_{xcn})i_x. \tag{25}$$

where $t_{xc(n+1)}$ and t_{xcn} are the duty cycle of identical cell $n+1$ and n of phase x, respectively.

For the output current control, the duty cycle for each identical cell is set to the same value. That is, $t_{xc(n+1)} = t_{xcn} = t_x$, which means the FC voltage is naturally balanced. However, due to the system parameter mismatch and harsh environmental conditions, FC voltage may deviate from its reference value, and the FC voltage balance scheme is still required.

As n and $n+1$ cell are functionally identical cells, the balance of FC capacitor voltage can be achieved by adjusting the duty cycles of S_{xcn} and $S_{xc(n+1)}$. As long as the sum of the duty cycles of S_{xcn} and $S_{xc(i+1)}$ remains unchanged, the output voltage will not be affected. The duty cycle applied for FC voltage balance can be denoted as

$$t_{bfxn} = k_{bfc}\text{sgn}(i_x)(u^*_{fn} - u_{fxn}) \tag{26}$$

where $u^*_{fn} = nE$ is the reference for FC capacitor voltage. $\text{sgn}(*)$ is a sign function that extracts the sign of a real number. k_{bfc} is a positive coefficient to adjust the balance of the FC capacitor voltage.

Taking (24) into consideration, the FC capacitor voltage balance can be achieved by adjusting the duty cycle to S_{xcn} and $S_{xc(n+1)}$. As a result, the duty cycle for

$$t_{xcn} = \begin{cases} t_x + t_{bnp} - t_{bfx1}, n = 1 \\ t_x + t_{bnp} - t_{bfx(n+1)} + t_{bfxn}, 1 < n < N \\ t_x + t_{bnp} + t_{bfx\rm N}, n = N. \end{cases} \tag{27}$$

As shown in (27), the sum of the duty cycles of the identical cells remains unchanged, the output voltage will not be affected by the FC voltage balance.

TABLE III
SYSTEM PARAMETERS

Parameters	Simulation	Experiment
DC bus voltage: U_{DC}	1500 V	160 V
Load resistance: R_l	48 Ω	9.6 Ω
Load inductance (ICMC): L_l	3 mH	1 mH
Load inductance (IPMC): L_l	3 mH	0 mH
Internal inductance: L	3 mH	3 mH
DC bus capacitance:C_{DC}	1500 μF	1500 μF
Output frequency: f_o	60 Hz	60 Hz
Flying capacitance: C	50 μF	50 μF
Sampling frequency: f_s	10kHz	10kHz
Number of identical cells: N	3	2
Dead time:		1.5 μs

2) Circulating Current Suppression in IPMC: Circulating current suppression is necessary for the reliable operation of the IPMC. The duty cycle for each identical cell can be slighted adjusted for the circulating current suppression. As long as the sum of the duty cycle for each identical cell is the same, the output current control will not be affected. The circulating current is generated by the voltage differences among the identical cells. Since the average voltage of each cell is the same, the circulating current is naturally balanced with the PS-PWM scheme.

However, due to the system parameter mismatch and harsh environmental conditions, the circulating current may become very large. Thus, the circulating current suppression scheme is still required. For simplification, the circulating current is suppressed by adjusting the duty cycle between the cells whilst the sum of the applied duty cycle remains unchanged.

The internal circulating current can be calculated as

$$i_{cxn} = i_{xn} - \frac{i_x}{N}. \tag{28}$$

The duty cycle for the circulating current suppression of each identical cell can be calculated as

$$t_{ccsxn} = k_{ccs}(i_c^* - i_{cxn}) \tag{29}$$

where i_c^* is the reference of the internal circulating current, which is always set to 0. k_{ccs} is a positive coefficient to suppress the circulating current. As shown in (29), the sum of the duty cycles of the identical cells remains unchanged, the output voltage will not be affected by the circulating current suppression.

Taking (24) into consideration, the circulating current suppression can be achieved by adjusting the duty cycle to S_{xpn}. As a result, the duty cycle for each identical cell can be rewritten as

$$t_{xpn} = t_x + t_{bnp} + t_{ccsxn}. \tag{30}$$

As shown in (30), the sum of the duty cycles of the identical cells remains unchanged, the output voltage will not be affected by the circulating current suppression.

V. SIMULATION RESULTS

In order to show the performance of the proposed predictive duty cycle control method, simulation studies have been carried out in MATLAB/Simulink environment. The parameters of the system are shown in Table III. The effectiveness of the proposed predictive controller to generate output voltages, regulated load currents, and capacitor voltage balance is analyzed during both steady-state and transient interval.

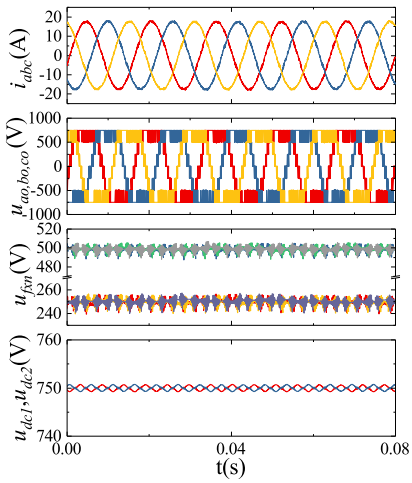

Fig. 6. Steady-state control performance of the proposed predictive duty cycle control of ICMC. For each figure-set, from top to down bottom are load current, output voltage, FC voltage, and dc-link capacitor voltage.

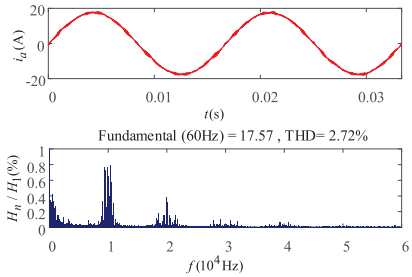

Fig. 7. Current FFT results of the ICMC. From top to bottom, waveforms are the load current and its spectrum.

A. Internal Cascaded Multilevel Converter

The steady-state performance of the ICMC, regulated by the proposed predictive duty cycle control method, is investigated. The output power is set to 30 kW. The steady-state performance regulated by the proposed predictive controller with PS-PWM at 10 kHz sampling frequency is illustrated in Fig. 6. The carrier period is set to NT_s to achieve a constant switching frequency of 10 kHz. It can be seen that the load current is well regulated with the help of the proposed method and the ICMC operates stably with balanced dc-link and FC capacitor voltages. Three FC voltages u_{fx2}, in Fig. 2(a), are balanced at $\frac{u_{\rm dc}}{3} = 500$ V, the other three capacitor voltages u_{fx1} in Fig. 2(a) are balanced at $\frac{u_{\rm dc}}{6} = 250$ V. The dc-link voltage is balanced at $\frac{u_{\rm dc}}{2} = 750$ V. As the number of the identical cells is three, the voltage u_{ao} is a seven-level output.

In order to further present the steady-state performance, the harmonic spectra of the load current of the ICMC are presented in Fig. 7. The load current total harmonic distortion (THD) of the proposed method is 2.72%. By using the proposed predictive duty cycle control method with PS-PWM, the switching frequency can be constant. The current harmonics concentrate on

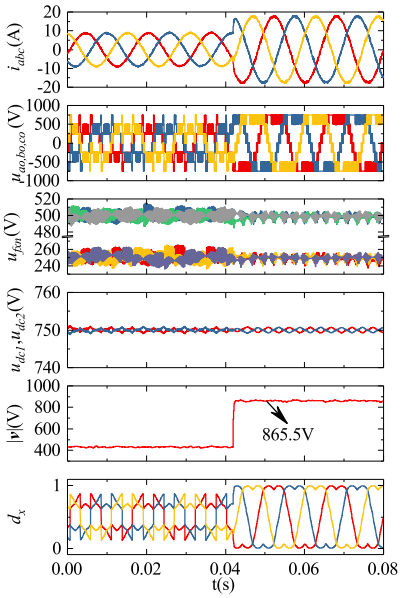

Fig. 8. Transient-state control performance of the ICMC. From top to bottom, waveforms are load current, output voltage, FC voltage, dc-link capacitor voltage, magnitude of the output voltage vector, and equivalent output duty cycles.

the 10 kHz, which are in accordance with the equivalent switching frequency. This brings some benefits to the design of filters.

The dynamic response of the ICMC is evaluated in Fig 8. The output current reference is stepped changed from 15 to 30 kW at 0.04 s. It can be seen that the ICMC is stable during large operation point step changes. As shown in the results, the transient response of the proposed method is very fast, indicating that the advantage of fast dynamic response. As shown Fig 8, the magnitude of the output voltage vector can reach the maximum output voltage magnitude of the SVM, where 865.5 V $\approx U_{\rm dc}/\sqrt{3}ig = 866$ V. In this condition, the equivalent duty cycles of each phase $d_x = \frac{S_{x1}}{2} + \frac{t_x}{2}$ are saddle waveforms, which are the same with SVM. Thus, the dc-utilization of the proposed predictive duty cycle control method is comparable with that of SVM.

B. Internal Parallel Multilevel Converter

The steady-state performance of the IPMC, regulated by the proposed predictive duty cycle control method, is investigated. The output power is set to 30 kW. The steady-state performance regulated by the proposed method with PS-PWM at 10 kHz sampling frequency is illustrated in Fig. 9. The carrier period is set to NT_s to achieve a constant switching frequency of 10 kHz. It can be seen that the load current is well regulated with the help of the proposed method, and the IPMC operates stably with balanced dc-link and suppressed internal circulating current. All the low-frequency circulating currents are suppressed around 0 A. The high-frequency circulating currents are generated due to the interleaved PWM, which cannot be suppressed by the controller. Due to the interleaved operation of the internal parallel cells, the equivalent seven-level output voltage is achieved.

In order to further present the steady-state performance, the harmonic spectra of the load current of the IPMC are presented in

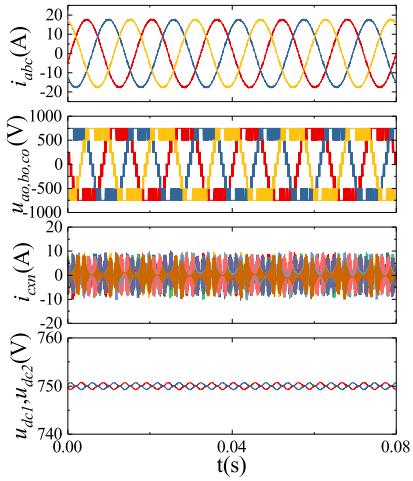

Fig. 9. Steady-state control performance of the IPMC. For each figure-set, from top to down bottom are load current, output voltage, circulating current, and dc-link capacitor voltage.

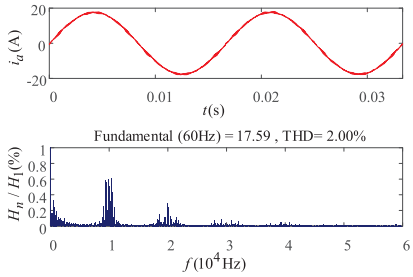

Fig. 10. Current FFT results of the proposed predictive duty cycle control of the IPMC. From top to bottom, waveforms are the load current and its spectrum.

Fig. 10. The load current THD of the proposed method is 2.00%. By using the proposed predictive duty cycle control method with PS-PWM, the switching frequency can be constant. The current harmonics concentrate on the 10 kHz, which are in accordance with the equivalent switching frequency.

The dynamic response of the IPMC is evaluated in Fig 11. The output current reference is stepped changed from 15 to 30 kW at 0.04 s. It can be seen that the IPMC is stable during large operation point step changes. The dc-link voltage balance is not affected, and the low-frequency circulating currents are suppressed around 0 during the transient, proving the effectiveness of the proposed method for the IPMC. As shown in the results, the transient response of the proposed method is very fast, indicating that the advantage of fast dynamic response. As shown Fig 8, the magnitude of the output voltage vector can reach the maximum output voltage magnitude of the SVM, where 865.5 $V \approx U_{\rm dc}/\sqrt{3} = 866$ V. In this condition, the equivalent duty cycles of each phase $d_x = \frac{S_{x1}}{2} + \frac{t_x}{2}$ are saddle waveforms, which are the same with SVM. Thus, the dc utilization of the proposed duty cycle control method is comparable with that of SVM.

VI. Experimental Results

Apart from the simulation study, the proposed predictive duty cycle control method with PS-PWM is experimentally tested on a downscaled ICMC/IPMC, where the experimental setup is

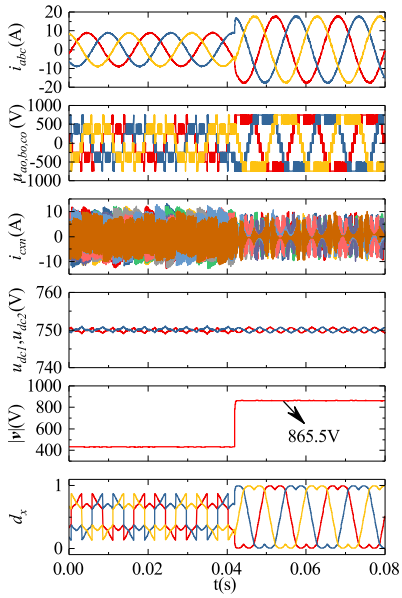

Fig. 11. Transient-state control performance of the proposed MPC of the IPMC. From top to bottom, waveforms are load current, output voltage, circulating current, dc-link capacitor voltage, magnitude of the output voltage vector, and equivalent output duty cycles.

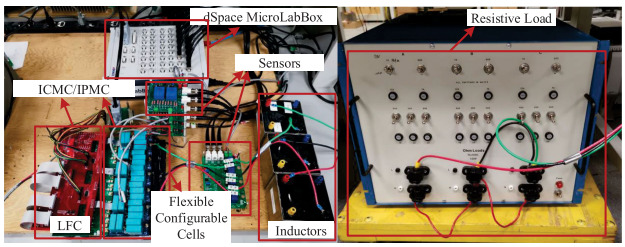

Fig. 12. Experimental setup.

illustrated in Fig. 12. In the prototype, the flexibly configurable cells are adopted. The prototype can be configured to ICMC or IPMC. A dSPACE MicroLabBox DS1202 was adopted to implement the digital control, and a slave Xilinx was applied to generate the gate signals for each switch, implement the analog-to-digital conversion. S_{x1}/S_{x2} was implemented by insulated-gate bipolar transistors (IGBTs) (Infineon IKQ50N120CT2), while the S_{xcn}/S_{xpn} was implemented by GaN devices (GaN Systems GS66516). In the following tests, all the variables are directly measured by current and voltage probes. The number of internal identical cells is two in the experimental test. As well known, the one-step delay between the commanding voltage and the applied voltage exists in the digital implementation of the MPC [40]. In this article, the compensation method proposed in [40] is also adopted to compensate for the one-step delay. In order to show the superiority of the proposed predictive duty cycle control, the experimental results of the PR controller of the ICMC/IPMC [17], [37] with PS-PWM are also presented as a benchmark.

One of the major limitations of the classical MPC is the heavy computation burden, which is exponentially related to the number of switching states in each phase. For the number of internal identical cells is two, the number of switching states is

TABLE IV
COMPUTATIONAL BURDEN COMPARISON

	ICMC	IPMC
Proposed method	$10.6\mu s$	$9.52\mu s$
PR controller	$10.16\mu s$	$10.2\mu s$

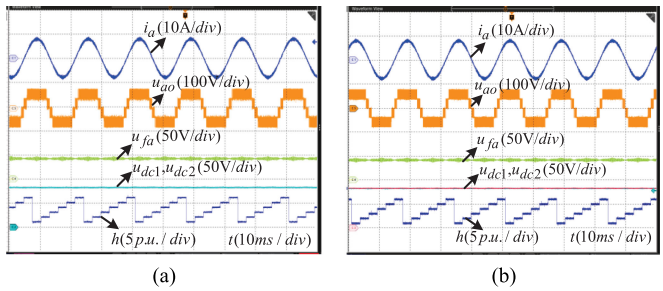

Fig. 13. Steady-state control performance of ICMC for (a) proposed method, and (b) PR controller. For each figure-set, from top to down bottom are load current, output voltage, FC voltage, dc-link capacitor voltage, and selected hexagon h.

eight. Then, the number of control variable predictions and cost function evaluation required need to be calculated is $8^3 = 512$. In the proposed method, the number of control variable prediction and cost function evaluation is independent of the number of internal identical cells and is only six. Taking the multilevel converter with two internal identical cells as an example, the percentage of computational burden reduction of the proposed predictive duty cycle control method in comparison with that of the classical MPC can be simply calculated as $1 - \frac{6}{512} = 98.8\%$. For the multilevel converter with a higher number of internal identical cells, the computational burden reduction will be even higher. According to our test using the dSpace profiler 3.8, it takes 10.6 μs and 9.52 μs to implement the proposed predictive duty cycle control method for ICMC and IPMC with two internal identical cells, respectively. The computational burden of the PR controller is also included as a comparison. As presented in Table IV, the computational burden of the proposed methods are almost the same as that of the PR controller. As the PR controller is not a computationally expensive control method, the comparative computational burden of the proposed method with the PR controller indicates its computational efficiency.

A. ICMC

1) Steady-State Performance: The experimental results of the proposed predictive duty cycle control method and the PR controller for the ICMC with two cascaded identical cells are presented to validate the effectiveness of the proposed method. The steady-state performance of the proposed predictive duty cycle control and the PR control of ICMC is presented in Fig. 13. The carrier frequency f_c in both methods is set to 5 kHz. The sampling point is set to both the top and bottom of each carrier, resulting in an equivalent switching frequency of 10 kHz. The FC voltages are balanced at around $u_{\rm dc}/4 = 40$ V, and dc-link capacitor voltages are balanced at around $u_{\rm dc}/2 = 80$ V. The output voltage u_{ao} is with five stages. The selected hexagon number switches smoothly, indicating the low-frequency operation of S_{x1}/S_{x2} is achieved in both methods. As shown, the

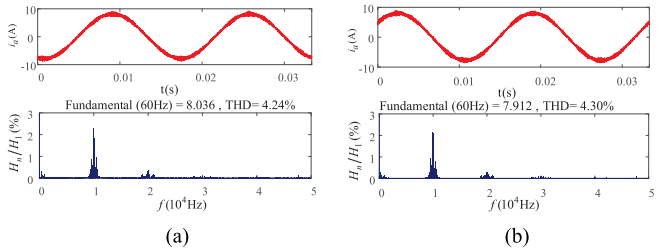

Fig. 14. Current FFT results of ICMC for (a) proposed method, and (b) PR controller. From top to bottom, waveforms are the load current and its spectrum.

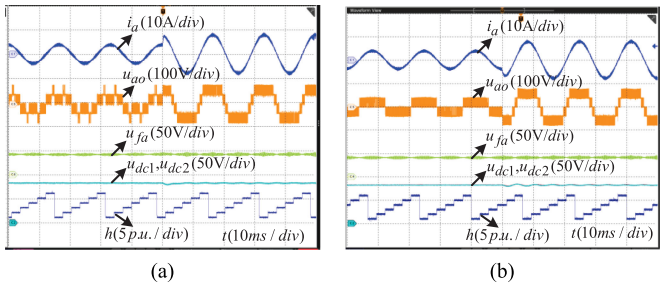

Fig. 15. Transient-state control performance of ICMC for (a) proposed method, and (b) PR controller. From top to bottom, waveforms are load current, output voltage, FC voltage, dc-link capacitor voltage, and selected hexagon h.

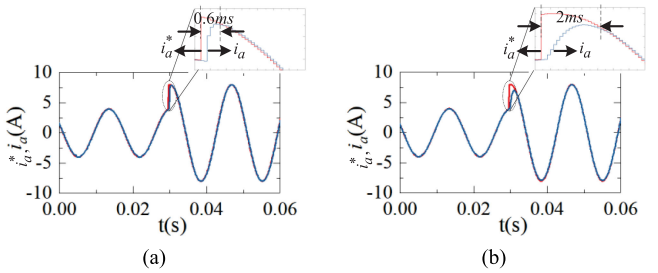

Fig. 16. Zoomed output current tracking performance of ICMC for (a) proposed method, and (b) PR controller.

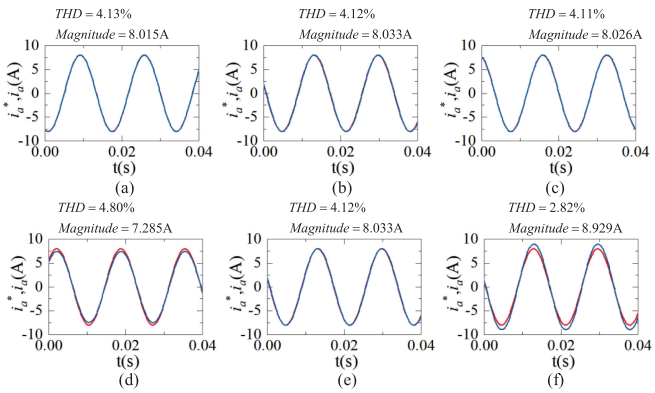

Fig. 17. Performance assessment under parameter variations for proposed predictive control of ICMC.

stable operation of the ICMC can be achieved with the proposed method. To further present the steady-state performance, the phase "a" current harmonic spectra of the proposed predictive duty cycle control and the PR control of the ICMC are presented in Fig. 14. The data was sampled using an oscilloscope at the 1 MHz sampling rate and analyzed using MATLAB. The current THD of the proposed method is 4.24%, while that of the PR controller with PS-PWM is 4.3%. The current harmonics are similar to each other and are concentrated at around 10, 20, and 30 kHz, indicating the constant switching frequency at 10 kHz is achieved, and the output current quality of the proposed method is comparative with that of the linear controller with PS-PWM.

2) Dynamic Performance: Other than the steady-state performance tests, the dynamic performance of the proposed method of ICMC is also tested and presented in Fig. 15. During the dynamic performance, the current reference is changed from 4 to 8 A at 0.05 ms. It can be seen that both methods of the ICMC with two cascaded identical cells are stable during the large operation point step changes. The FC voltages and dc-link capacitor voltages are balanced during the dynamic. The number of the selected hexagon switches smoothly even during the dynamic, indicating the fundamental-frequency operation even during current reference step changes. The transient response of the proposed method of the ICMC is faster than that of the PR controller, indicating that the advantage of the fast dynamic response in the MPC is maintained. To clearly show the dynamic performance of the two controllers of the ICMC, zoomed waveforms in discrete-time scale during the load current reference stepped change from 4 to 8 A are presented in Fig. 16. As shown in the figure, it takes only 0.6 ms to reach its reference in the proposed controller while it takes 2 ms to reach its reference in the PR controller, indicating the fast response in the step-change of the current reference.

3) Performance Assessment Under Parameter Variation: As a model-based control algorithm, system parameters are utilized for the switching state selection and duty-cycle calculation. Therefore, the performances of the proposed method of the ICMC under load inductance and resistance variations are tested. The testing scenarios are: the load filter inductance (L_{eq} is the control parameter, and L_0 is the accurate value) is changed to 50% and 150% of the measured (accurate) values; The load filter resistance (R_{eq} is the control parameter, and R_0 is the accurate value) is changed to 90% and 110% of the measured (accurate) values. Phase "a" and its reference are collected and compared with the situation where measured parameter value is used. The results have been illustrated in Fig. 17.

As can be seen from Fig. 17, the inductance varies from 50% and 150% while the THD and tracking errors of current are almost not affected. Note that, the errors induced in the measurement of the inductor are within the range of 10% in practical cases. It can be noticed that the performance is almost not affected within this range. These results show that the proposed method is not sensitive to inductance variations.

On the other hand, the resistance varies from 90% and 110% while the tracking errors of current are significant. Although such a variation range has not driven the system into instability, performance degradations are seen. This will suggest an effective parameter robust solution (e.g., online parameter estimations, online voltage measurements) is desirable when

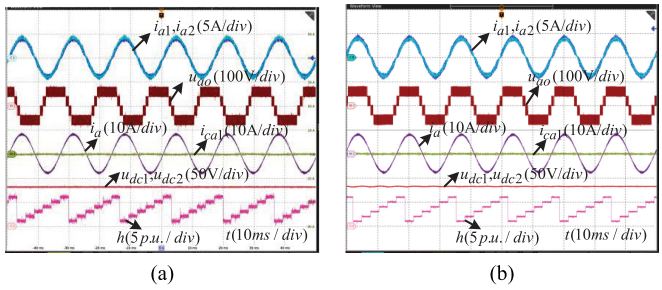

Fig. 18. Steady-state control performance of IPMC for (a) proposed method, and (b) PR controller. For each figure-set, from top to down bottom are parallel cell current, output voltage, load current and circulating current, dc-link capacitor voltage, and selected hexagon h.

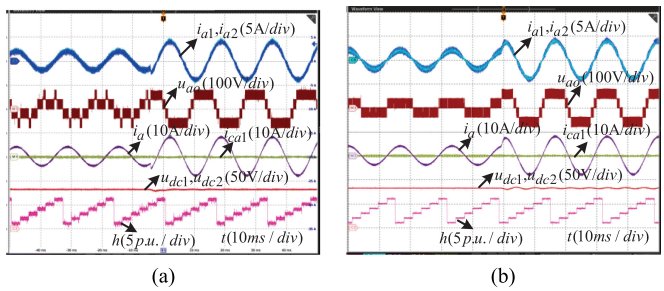

Fig. 20. Transient-state control performance of IPMC for (a) proposed method, and (b) PR controller. From top to bottom, waveforms are parallel cell current, output voltage, load current and circulating current, dc-link capacitor voltage, and selected hexagon h.

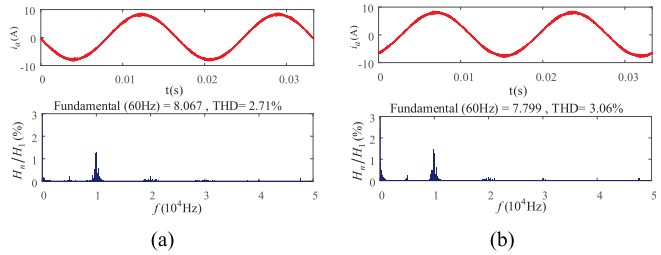

Fig. 19. Current FFT results of IPMC for (a) proposed method, and (b) PR controller. From top to bottom, waveforms are the load current and its spectrum.

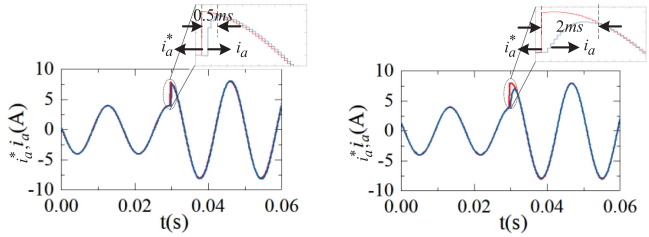

Fig. 21. Zoomed output current tracking performance of IPMC for (a) proposed method, and (b) PR controller.

the proposed method is applied, which is one of our research interests in the near future.

B. IPMC

The experimental results of the proposed predictive control method and the PR controller for the IPMC with two internal parallel cells are also tested and presented in Fig. 18. The carrier frequency and the sampling point is set to the same as that of the ICMC to achieve an equivalent switching frequency of 10 kHz. As shown in both methods, the dc-link capacitor voltages are balanced at around $u_{\rm dc}/2 = 80$ V. The low-frequency circulating current is suppressed around 0 A, resulting in a balanced output current between each parallel cell, that is, i_{a1} has the same magnitude with i_{a2}. The output voltage u_{ao} is with five stages due to the interleaved operation of the internal parallel cells. The selected hexagon number switches smoothly, indicating the low-frequency operation of S_{x1}/S_{x2} is achieved. To further present the steady-state performance, the phase "a" current harmonic spectra of the proposed method and the PR controller for the IPMC are presented in Fig. 19. The data was sampled using an oscilloscope at the 1 MHz sampling rate and analyzed using MATLAB. The phase "a" current THD is 2.71% while that of the PR controller is 3.06%. The current harmonics of both methods are concentrated at around 10, 20, and 30 kHz, indicating the constant switching frequency at 10 kHz is achieved, and the proposed method can achieve the comparative output current quality with that of the linear controller with PS-PWM.

1) Dynamic Performance: The dynamic performance of the proposed method of IPMC is presented in Fig. 20. During the dynamic performance, the current reference is changed from 4 to 8 A at 0.05 ms. It can be seen that both methods of the IPMC with two parallel cells are stable during the large operation point step changes. The low-frequency internal circulating current is suppressed, and dc-link capacitor voltages are balanced during the dynamic. The number of the selected hexagon switches smoothly even during the dynamic, indicating the fundamental-frequency operation even during current reference step changes. The transient response of the proposed method of the IPMC is very faster than that of the PR controller, indicating that the advantage of the fast dynamic response in the MPC is maintained. To clearly show the dynamic performance of the two controllers of the IPMC, zoomed waveforms in discrete-time scale during the load current reference stepped change from 4 to 8 A are presented in Fig. 21. As shown in the figure, it takes only 0.5 ms to reach its reference in the proposed controller while it takes 2 ms to reach its reference in the PR controller, indicating the fast response in the step-change of the current reference.

2) Performance Assessment Under Parameter Variation: The performances of the proposed predictive duty cycle control of the IPMC under load inductance and resistance variations under the same scenarios as those of the ICMC are tested. As can be seen from Fig. 22, the inductance varies from 50% and 150% while the THD and tracking errors of current are almost not affected. Note that, the errors induced in the measurement of the inductor are within the range of 10% in practical cases. It can be noticed that the performance is almost not affected within this range. These results show that the proposed method is not sensitive to inductance variations.

On the other hand, the resistance varies from 90% and 110% while the tracking errors of current are significant. Although

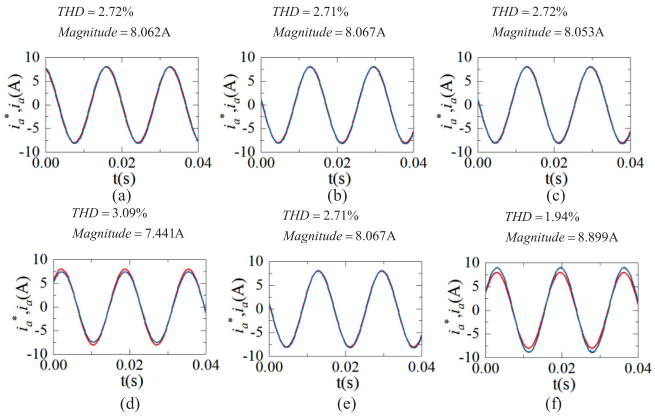

Fig. 22. Performance assessment under parameter variations for proposed predictive control of IPMC.

such a variation range has not driven the system into instability, performance degradations are seen. This will suggest an effective parameter robust solution (e.g., online parameter estimations, online voltage measurements) is desirable when the proposed method is applied, which is one of our research interests in the near future.

C. Discussion

According to the above results for both ICMC and IPMC, it can be concluded that the proposed method can achieve a similar current quality with that of the PR controller with PS-PWM. As a model-based optimal controller, the proposed controller can provide a much faster dynamic than that of the post-error-based PR controller. On the other hand, multiple-loop PI or PR controller parameters should be carefully tuned to achieve satisfactory steady and dynamic performance. However, in the proposed predictive controller, thanks to the employment of the optimization method, the current control is parameter-tuning free.

Furthermore, the freedom of the adjustable duty cycle is fully explored in the proposed method. The dc-link voltage is regulated by adjusting the duty cycles between (000) and (111) of $(S_{va}S_{vb}S_{vc})$. The FC voltage balance or circulating current suppression is achieved by adjusting the duty cycles between the identical cells. Therefore, the objective or constraint is excluded from the cost function. Therefore, the tuning effort for weighting factors is avoided, and the optimization solver is simplified. This is also considered as an advantage of the proposed predictive controller.

VII. Conclusion

A simplified predictive duty cycle control scheme is proposed for multilevel converters with the internal identical structure to reduce the computation burden and improve the steady-state performance in this article. By formulating a novel mathematic model, where a series of switching pairs with the identical structure are modeled as a virtual switching state, the number of the corresponding voltage vectors for cost function evaluation can be significantly reduced. The optimal current tracking can be achieved by the formulated least-square optimization problem. The output current quality is enhanced due to the employment of the interleaved output voltage stage with PS-PWM. Simulation and experimental results on the multilevel converters with the internal cascaded/paralleled identical cells are presented to verify the good performance and application value of the proposed method. The proposed predictive duty cycle control method is an attractive alternative method for the multilevel converter with the identical structure where a reduced computational burden and an enhanced current control performance are required.

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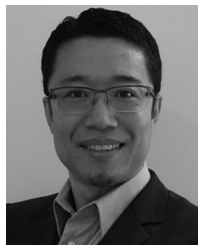
Dehong Zhou (Member, IEEE) received the B.Sc. and Ph.D. degrees in control science and engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2012 and 2016, respectively.

From 2016 to 2018, he was a Postdoctoral Research Fellow with Nanyang Technological University, Singapore. From 2018 to 2020, he was a Postdoctoral Fellow with University of Alberta, Edmonton, AB, Canada. Since 2020, he has been a Faculty Member with the School of Automation Engineering, University of Electronic Science and Technology of China. His research interests include power electronics and motor drives.

Zhongyi Quan (Member, IEEE) received the B.Eng. degree from Tianjin University, Tianjin, China, in 2010, the M.Sc. degree from Beihang University, Beijing, China, in 2013, and the Ph.D. degree in electrical engineering in from the University of Alberta, Edmonton, AB, Canada, in 2013.

From October 2019 to November 2019, he was a Visiting Research Fellow with the Institute for Power Generation and Storage Systems, E.ON Energy Research Center, RWTH Aachen University, Germany. He is currently a Postdoctoral Fellow at the University of Alberta. His current research interests include design of high density and high efficiency power converters for applications such as renewable energy, electric vehicles, and other energy efficient equipment.



Yunwei (Ryan) Li (Fellow, IEEE) received the B.Sc. degree in electrical engineering from Tianjin University, Tianjin, China, in 2002, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2006.

In 2005, he was a Visiting Scholar with Aalborg University, Denmark. From 2006 to 2007, he was a Postdoctoral Research Fellow with Ryerson University, Toronto, ON, Canada. In 2007, he also worked with Rockwell Automation, Canada, before he joined University of Alberta, Edmonton, AB, Canada. Since then, he has been with University of Alberta, where he is currently a Professor. His research interests include distributed generation, microgrid, renewable energy, high power converters, and electric motor drives.

Dr. Li serves as an Editor-in-Chief for the IEEE TRANSACTIONS ON POWER ELECTRONICS LETTERS. Prior to that, he was an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON SMART GRID, and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He was the recipient of the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society in 2013, and the Second Prize Paper Award of IEEE TRANSACTIONS ON POWER ELECTRONICS in 2014. He is listed as a Highly Cited Researcher by the Web of Science Group.