Modular Interline DC Power Flow Controller

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***Abstract*—DC power flow controller (DCPFC) is regarded as an effective technology to improve the active power distribution capability in a complex dc grid. Among different types of DCPFCs, the interline dc power flow controller (IDCPFC) can realize multiline power flow control functions in a complex dc grid. In this article, a modular multiline IDCPFC has been proposed via a transformerless structure. Specifically, the *n*-line IDCPFC can actively control (*n*−1)-line power flow based on the theoretical analysis. The proposed technology is analyzed in detail, including topology, operation principle, and control strategy. As a case study, a three-line IDCPFC is implemented in this article. Both simulation and experimental results are obtained to show that the proposed IDCPFC can effectively control multiline power flows under various conditions.**

***Index Terms*—Extension methodology, multiline interline dc power flow controller, multiline power flow control, multiterminal HVDC system.**

NOMENCLATURE

DCPFC	dc power flow controller.
IDCPFC	Interline dc power flow controller.
HVDC	High-voltage dc system.
MTDC	Multiterminal HVDC system.
VSC	Voltage source converter.
SAVS	Series adjustable voltage source.
MDCPFC	Multiport DCPFC.
CDCPFC	Composite DCPFC.
VSC*i*	*i*th VSC ($i = 0,1,2,\ldots,n$).
Bus*i*	DC slack bus of VSC*i* ($i = 0,1,2,\ldots,n$).
V_i	DC voltage of bus*i* ($i = 0,1,2,\ldots,n$).
P_i	Output power of VSC*i* ($i = 1,2,\ldots,n$).
P_0	Input power of VSC0.
V_{ci}	DC voltage of equivalent voltage source in series with line*i* ($i = 1,2,\ldots,n$).
R_i	Equivalent resistor of line*i* ($i = 1,2,\ldots,n$).
I_i	DC current of line*i* ($i = 1,2,\ldots,n$).
I_0	Input dc current of VSC0.
$R_{i(i+1)}$	Equivalent resistor of the line from bus*i* to bus($i+1$) ($i = 1,2,\ldots,n-1$).
$I_{i(i+1)}$	DC current of the line from bus*i* to bus($i+1$) ($i = 1,2,\ldots,n-1$).
i_L	DC current of inductor *L*.
D_i	Duty cycle for substate *i* ($i = 1,2,\ldots,n$).
ΔV_{ci}	Voltage ripple of V_{ci} ($i = 1,2,\ldots,n$).

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I. INTRODUCTION

IN RECENT years, with the rapid development of large-scale renewable energy based power generation and grid integration, high-voltage dc system (HVDC) and multiterminal HVDC system (MTDC) projects based on voltage source converter (VSC) technology have gained more and more attention in both academies and industry [1]–[6]. In a dc grid, the power flow of each dc line is only passively determined by the terminal voltage and the line resistance. Hence, for a given dc grid, the power flow distribution can only be controlled by adjusting the line resistance and the terminal dc voltages [7]–[9]. For a complex multiline dc grid, the precise dc power flow control cannot be realized for all the individual lines by only adjusting the output power of VSCs [10]–[12]. Therefore, the dc power flow control is a challenge in a complex dc grid.

The concept of dc power flow controller (DCPFC) has been introduced to realize the active and precise power flow control in dc grid. DCPFC can be divided into the resistance and voltage types [13]. The series variable resistance, as a typical resistance-type DCPFC, is equivalent to an adjustable resistance inserted into the dc line [14]. The utilization of resistance-type DCPFC leads to larger line resistance, and with the shortcomings of unidirectional power flow adjustment and higher line losses. According to the topology, the voltage-type DCPFC can be categorized into four subtypes: the dc transformer, the series adjustable voltage source (SAVS), the multiport DCPFC (MDCPFC), and the interline dc power flow controller (IDCPFC). The dc transformer and SAVS, with the bidirectional power flow adjustment capability, are equivalent to a series adjustable voltage source embedded into the dc line. The differences between them are as follows: the dc transformer has complex design, and has to withstand the system-level voltage. This is because its input and output sides are connected to positive and negative transmission lines

of different voltage levels [15], [16]. The SAVS with the supply of external power are embedded into positive or negative polarity line, and can therefore have lower voltage and power levels [17], [18].

On the other hand, the MDCPFC and IDCPFC can be utilized to exchange the power among multiple adjacent lines. With a complex topology including the multiphase ac coupling transformer and MMC structure, the MDCPFC has been studied to realize two lines' active power flow control for a three-terminal dc grid scenario [19].

The IDCPFC, with the transformerless structure, has lower power requirement and therefore low cost [20]. Two-line IDCPFC, equivalent to two dc voltage sources inserted into two lines respectively, transfers partial energy from one line to the other line [21], [22]. This kind of IDCPFC has larger voltage and current ripples because of two equivalent voltage sources which are frequently put into operation and bypassed in two lines. To decrease the ripples and have the capability of reversing the power flow, improved IDCPFCs have been proposed in [23] and [24], where the energy buffer is replaced by the inductor and coupling inductors.

Unfortunately, because of the power conservation of two-line IDCPFC, all existing two-line IDCPFCs can only control the power flow of the one line actively, while the power flow of the other line is determined passively [25].

For multiline dc systems, the active power flow control of multiple lines using DCPFC is required. This is realized through the collaborative control of VSC stations and DCPFCs [26]–[29]. In [25] and [30], the composite DCPFC (CDCPFC) with external dc voltage source or auxiliary circuit is presented to realize two lines' active power flow control in dc grid.

A three-line IDCPFC has also been developed from two-line IDCPFC for multiterminal dc grid. The proposed topology can be applied to three dc lines with the unidirectional power flow directions [31]. Developed three-line IDCPFC topologies are proposed to be applied to three dc lines with bidirectional power flow directions [32], [33]. Again, these methods only have the ability of active power flow control of a single line. In theory, a three-line IDCPFC has the potential to actively control two lines' power flow [34]. However, the active multiple dc power flow control ability of multiline IDCPFC has not yet been well studied in literature.

Therefore, in future complex dc system, there is a big improvement space and an urgent methodology demand to enhance multiple dc power flow control capability for multiline IDCPFC.

In this article, under the theoretical analysis of proposed methodology, n-line IDCPFC can control $(n-1)$-line power flow actively, whose power flow control ability is exploited enough. A general operation principle of multiline IDCPFC is given to fully explore the potential of dc power flow control. A universal extension methodology of multiline IDCPFC via a nontransformer structure is detailed, including extension topology, operation principle, and control strategy. Coupling inductor is chosen as energy buffer for less voltage and current ripples and the capability of coping with bidirectional power flows. Three-line IDCPFC is taken as an example to utilize the methodology for demonstration. The simulation and experiment results of three-line IDCPFC proved the multiline power flow control ability of proposed extension methodology under various conditions with a good application prospect.

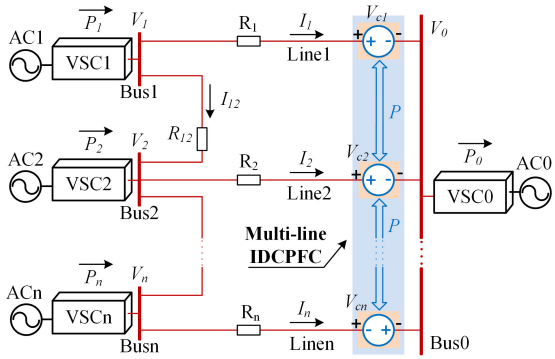

Fig. 1. General structure of $(n+1)$-terminal VSC–HVDC system with an n-line IDCPFC installed.

II. Equivalent Model of Multiline IDCPFC

The equivalent model of the proposed multiline IDCPFC is given in Fig. 1. The proposed multiline IDCPFC can fully explore the maximum active dc power flow control potential.

A. Equivalent Model of Multiline IDCPFC

As shown in Fig. 1, an n-line IDCPFC (blue part) is inserted into the $(n+1)$-terminal VSC–HVDC system. It is noted that VSC1, VSC2, …, VSCn are operated in the constant power mode, delivering power P_1, P_2, …, P_n to the $(n+1)$-terminal VSC–HVDC system. VSC0 is operated in the constant voltage mode to provide a slack bus dc voltage V_o.

The proposed modular IDCPFC can be adopted in a dc bus terminal connected to multiple lines, such as Buso in Fig. 1. The n-line IDCPFC is equivalent to n voltage sources (V_{c1}, V_{c2}, …, V_{cn}) in series with n dc lines (line 1, line 2, …, line n), whose dc power flows are regarded as the control targets of n-line IDCPFC. Energy exchange happens among these equivalent voltage sources.

B. Potential Analysis of Multiple DC Power Control

According to Fig. 1, the general dc power flow (1) of each controlled dc line can be obtained as follows:

$$V_i - V_{ci} - V_0 = I_i R_i,\ i = 1, 2, \ldots, n. \tag{1}$$

The general dc power flow (2) of each uncontrolled dc line can be obtained as follows:

$$V_i - V_{i+1} = I_{i(i+1)} R_{i(i+1)}, i = 1, 2, \ldots, (n-1) \tag{2}$$

where $R_{i(i+1)}$ is the equivalent resistor of the line from bus$i$ to bus$(i+1)$ (i = 1,2,…,$n-1$); and $I_{i(i+1)}$ is the dc current of the line from bus$i$ to bus$(i+1)$ (i = 1,2,…,$n-1$).

Equation (3) is the power conservation equation of VSCs with constant output power (VSC1, VSC2, …, VSCn) and can be

obtained as follows:

$$\begin{cases} P_1 = V_1(I_1 + I_{12}) \\ P_i = V_i(I_i + I_{i(i+1)} - I_{(i-1)i}), i = 2, 3, \ldots, (n-1) \\ P_n = V_n(-I_{(n-1)n} + I_n). \end{cases} \quad (3)$$

Equation (4) is the power conservation equation of multiline IDCPFC.

$$\sum_{i=1}^{n} V_{ci} I_i = 0 \quad (4)$$

while the multiline IDCPFC efficiency is assumed to be 100%.

The total number of above system-level constraint equations is $3n$.

For a given $(n+1)$-terminal VSC–HVDC system, the corresponding output power of each VSC (P_1, P_2, …, P_n), the dc-side voltage V_0 of VSC0, and the resistance of each dc line (R_1, R_2, …, R_n, R_{12}, R_{23}, …, $R_{(n-1)n}$) can be represented as constants. Thus, the total number of system-level constants is equal to $3n$.

The total number of all system-level unknowns is thus equal to $(4n-1)$, including the voltage V_1, V_2, …, V_n, V_{c1}, V_{c2}, …, V_{cn} and the current I_1, I_2, …, I_n, I_{12}, I_{23}, …, $I_{(n-1)n}$.

For these $(4n-1)$ unknowns that exist in the $(n+1)$-terminal VSC–HVDC system, if $(n-1)$ unknowns are determined, the other $3n$ unknowns can be solved by $3n$ constraint equations. Thus, $(n-1)$ unknown electrical parameters of this system represent mathematically the maximum controlled space. That is, for such a $(n+1)$-terminal VSC–HVDC system with n-line IDCPFC, as shown in Fig. 1, the maximum number of active dc power flow control targets should be $(n-1)$, which is the maximum control ability. In other words, the power flow of $(n-1)$ lines can be controlled actively, while the last one power flow is determined passively.

For an instance of three-line IDCPFC, the maximum number of actively controlled lines is two, whereas the number of passively controlled lines is one.

III. Modular Multiline IDCPFC

The proposed modular multiline IDCPFC that can satisfy the previously discussed requirements is presented in this section.

A. Modular Topology

Here, the two-line IDCPFC topology of [24] is adopted to construct the universal modular approach.

1) Integrated Structur: As shown in Fig. 2(a), a generalized n-line IDCPFC topology consists of one "energy buffer" and n "Parts" (i.e., Part 1, Part 2, …, Part n) embedded into n dc lines. Bus a, bus b, and bus 0 build energy exchange paths between energy buffer and Parts. For Part i ($i = 1, 2, \ldots, n$), the ports p_i, a_i, b_i, and c_i are connected with line i, bus a, bus b, and bus 0, respectively. The positive reference direction of each electrical quantity can be referred to as in Figs. 2 and 4.

If $n = 2$, the extension topology, two-line IDCPFC, is same as that in [24]. The specific topology analyses of energy buffer and Part are described as follows.

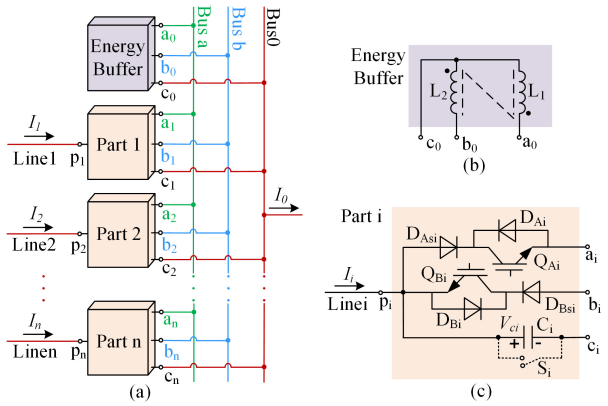

Fig. 2. Topology of modular multiline IDCPFC. (a) Integrated structure. (b) Energy buffer. (c) Part i.

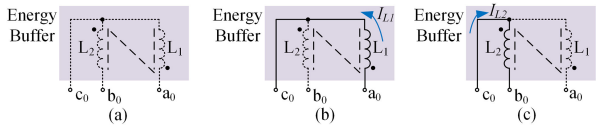

Fig. 3. Modes of Energy Buffer. (a) Mode 1 (bypass mode). (b) Mode 2 (exchange mode in positive power flow direction). (c) Mode 3 (exchange mode in negative power flow direction).

2) Energy Buffer: Energy buffer can be regarded as the inner energy intermediary of an extended IDCPFC. Here, the coupling inductor [25] (L_1 and L_2) is chosen as an energy buffer, whose merits are low current ripples and the ability to cope with power flow reversal. Its three modes are detailed as follows.

Mode 1: Bypass mode

While the multiline IDCPFC is bypassed, energy buffer is also bypassed, as shown in Fig. 3(a).

Mode 2: Positive direction exchange mode

While multiline IDCPFC works, energy buffer always works with every Part in turn, which means energy exchange happens between one selective Part and energy buffer. If the power flow direction of selective Part is positive, L_1 of coupling inductor works is as shown in Fig. 3(b).

Mode 3: Negative direction exchange mode

Similarly, if the power flow direction of selective Part is negative, L_2 of coupling inductor works is as shown in Fig. 3(c).

Energy buffer also can be represented with capacitor [21] and inductor [23] as required. Different energy buffers mean different assorted Parts with different technical characteristics.

3) Part: Parts of universal topology transform the transmission lines to build the bridge for transmission lines and energy buffer.

The internal topology of Part i ($i = 1, 2, \ldots, n$) consists of one capacitor (C_i) inserted in series with line i, one bypass switch (S_i), two IGBTs (Q_{Ai} and Q_{Bi}), two antiparallel diodes (D_{Ai} and D_{Bi}), and two series diodes (D_{Asi} and D_{Bsi}). Bypass switch is the bidirectional switch that consists of two IGBTs in parallel. Its four modes are detailed as follows.

Mode 1: Bypass mode

While S_i is turned ON, Part i is shorted as shown in Fig. 4(a), that is, line i has no access to multiline IDCPFC.

Mode 2: Normal mode

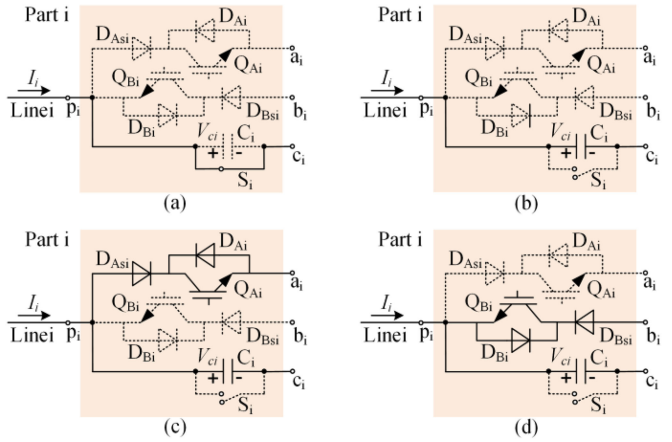

Fig. 4. Modes of Part. (a) Mode 1(bypass mode). (b) Mode 2(normal mode). (c) Mode 3(exchange mode in positive power flow direction). (d) Mode 4(exchange mode in negative power flow direction).

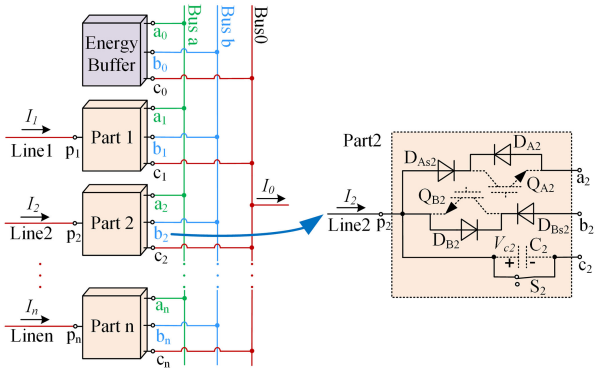

Fig. 5. Part 2 fault action of *N*-line IDCPFC.

When S_i is turned off, C_i is inserted in line i, equivalent to a voltage source in series with line i. The port c_i is connected with bus0 of VSC0, whereas the port p_i is connected with line i. It is V_{ci} that alters the power flow of line i. In this mode, no energy exchange happens between line i and energy buffer.

Mode 3: Exchange mode in positive power flow direction

For the positive power flow direction, Q_{Ai} is turned on when energy exchange happens between line i and energy buffer.

Mode 4: Exchange mode in negative power flow direction

For the negative power flow direction, Q_{Bi} is turned on when energy exchange happens between line i and energy buffer.

This type of Part can cope with power flow reversal because of the switch between modes 3 and 4.

Note: Fault action of Part

1) If Part i is broken, both Q_{Ai} and Q_{Bi} turn off. The two sets of antiparallel diodes separate Part i from bus a and bus b.
2) At the same time, the switch S_i will turn on to separate Part i from line i. In other words, the faulty Part i is cut off from dc grid and modular IDCPFC.

For instance, as shown in Fig. 5, if Part 2 is broken and then separated from the grid and the proposed IDCPFC, the N-line IDCPFC will perform the function as $(N-1)$-line IDCPFC to control $(N-1)$ lines' power flows except line 2, whose power flow ability is still partially maintained.

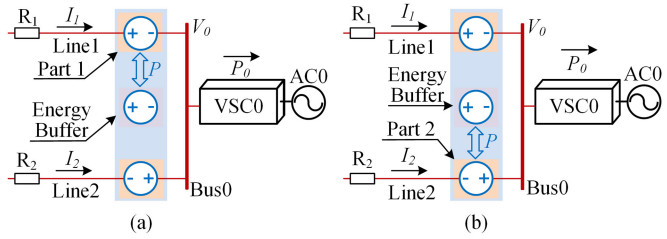

Fig. 6. Inner working rule of IDCPFC in three-terminal HVDC system. (a) Substate1. (b) Substate 2.

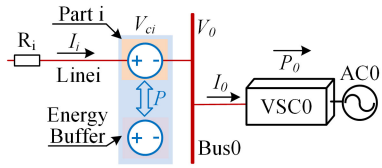

Fig. 7. Inner operation principle of *N*-line IDCPFC (substate *i*).

4) Bus: As shown in Fig. 2(a), there are two inner common buses (i.e., bus a and bus b) in a multiline IDCPFC.

Bus a serves as the energy exchange path between energy buffer and Part i when power flow direction of line i is positive. Inversely, bus b serves as the energy exchange path between energy buffer and Part i when power flow direction of line i is negative. It is noted that bus 0, connected to the port c_i of Part i, is the dc terminal Bus of VSC0. Only single inner bus (bus a or bus b) will work, while multiline IDCPFC is put into operation.

Thus, which mode of energy buffer and Part i will work depends on the power flow direction of line i.

B. Operation Principle

The operation principle of all existing two-line IDCPFCs is same, as shown in Fig. 6. Two equivalent voltage sources of Parts 1 and 2 are in series with lines 1 and 2. Parts 1 and 2 take turns in exchanging energy with energy buffer during their substates. By energy buffer, the partial energy is transferred between two lines to realize dc power flow control.

Similarly, the operation principle of n-line IDCPFC can be obtained. For n-line IDCPFC, the energy exchange paths take turns working between energy buffer and every Part by switches' turning on and off, which means n substates and n loops in a single switching cycle. Every Part would participate in energy exchange with energy buffer during its own substate of single duty cycle, as shown in Fig. 7.

When $S_1, S_2, \ldots, S_n$ are turned on, $C_1, C_2, \ldots, C_n$ are shorted, bypassing the multiline IDCPFC. Considering different kinds of power flow directions of transmission lines, there are many power flow conditions based on the number of lines. For detailed analysis of operation principle, two typical conditions of three-line IDCPFC are taken as an example. The specific operations cased are shown in Figs. 8 and 9.

Condition 1: I_1, I_2, and I_3 are all in positive direction.

In this case, I_1 and I_2 are controlled to be decreased actively, while I_3 is controlled to be increased passively. That is, the equivalent positive dc voltage sources are in series with

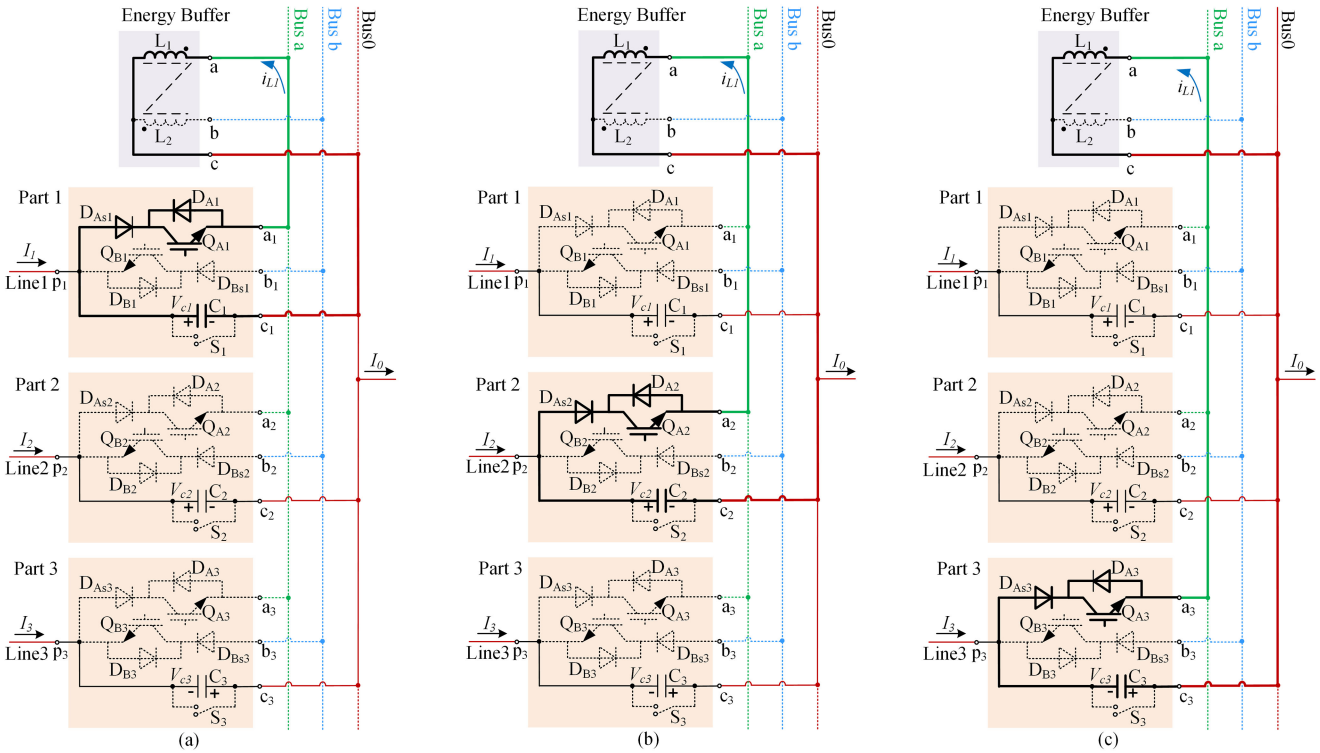

Fig. 8. Operation principle of three-line IDCPFC (condition 1). (a) Substate 1. (b) Substate 2. (c) Substate 3.

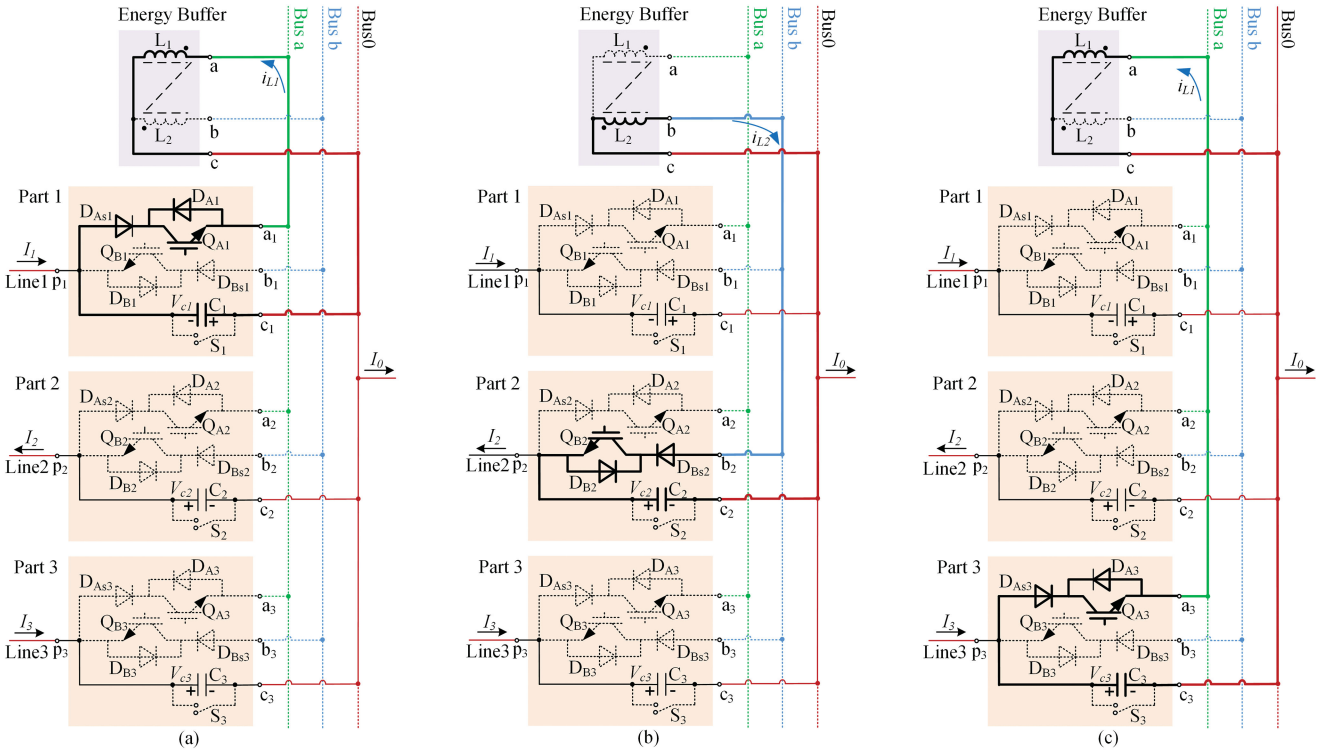

Fig. 9. Operation principle of three-line IDCPFC (condition 2). (a) Substate 1. (b) Substate 2. (c) Substate3.

lines 1 and 2, while the equivalent negative dc voltage source is in series into line 3 (Voltage directions of C_1, C_2, and C_3 are shown in Fig. 8.).

If there is no energy exchange path between Part and energy buffer, both V_{c1} and V_{c2} will continue increasing, whereas V_{c3} continues decreasing. Therefore, in order to keep the balance of V_{c1}, V_{c2}, and V_{c3}, there is an urgent need for energy exchange paths between the capacitors and energy buffer.

The whole switching cycle can be divided into three substates during steady operation, as shown in Fig. 8, whose brief sketch is as follows.

1) Substate 1, first Q_{A1} is turned ON, energy exchange path C_1–D_{Asi}–D_{A1}–L_1 is formed between Part 1 and energy buffer, as shown in Fig. 8(a). The energy is shifted from C_1 to L_1, and i_{L1} is increased linearly for the duration of this substate.
2) Substate 2, Q_{A1} is turned OFF/ Q_{A2} is turned ON, then energy exchange path C_2–D_{As2}–Q_{A2}–L_1 is formed between Part 2 and energy buffer, as shown in Fig. 8(b). The energy is shifted from C_2 to L_1, and i_{L1} is increased linearly for the duration of this substate.
3) Substate 3, Q_{A2} is turned OFF/ Q_{A3} is turned ON, then energy exchange path C_3–D_{As3}–Q_{A3}–L_1 is formed between Part 3 and energy buffer, as shown in Fig. 8(c). The energy is shifted from L_1 to C_3, and i_{L1} is decreased linearly for the duration of this substate.

When Q_{A3} is turned OFF and Q_{A1} is turned ON, another switching cycle begins. In this condition, only L_1 of $L_1 \| L_2$ works, while L_2 is out of work because the power flow direction of three lines is positive. Q_{A1}, Q_{A2}, and Q_{A3} are complementary to each other, whereas Q_{B1}, Q_{B2}, and Q_{B3} are always in the OFF state, which means Q_{A1}, Q_{A2}, and Q_{A3} need to be controller.

Condition 2: I_1 and I_3 are in positive direction/ I_2 is in negative direction.

In this case, I_1 and I_2 are controlled to be increased actively, while I_3 is controlled to be decreased passively. That is, the equivalent positive dc voltage sources are in series into line 1 and line 2, while the equivalent negative dc voltage source is in series into line 3 (Voltage directions of C_1, C_2, and C_3 are shown in Fig. 9.).

If there is no energy exchange path between Part and energy buffer, both V_{c1} and V_{c2} will continue to decrease, while V_{c3} continues to increase. Therefore, in order to keep the balance of V_{c1}, V_{c2}, and V_{c3}, there is an urgent need for energy exchange paths between the capacitors and energy buffer.

The whole switching cycle can be divided into three substates during steady-state operation, as shown in Fig. 9, whose brief sketch is as follows.

1) Substate 1, first Q_{A1} is turned on, energy exchange path C_1–D_{Asi}–D_{A1}–L_1 is formed between Part 1 and energy buffer, as shown in Fig. 9(a). The energy is shifted from L_1 to C_1, and i_{L1} is decreased linearly for the duration of this substate.
2) Substate 2, Q_{A1} is turned OFF/ Q_{A2} is turned ON, then the energy exchange path L_2–D_{Bs2}–Q_{B2}–C_2 is formed between Part 2 and energy buffer, as shown in Fig. 9(b). During the duration of this substate, the energy of L_1 is transferred to L_2 because of the coupling inductance. The energy is shifted from L_2 to C_2,and i_{L2} is decreased linearly for the duration of this substate.
3) Substate 3, Q_{A2} is turned OFF/Q_{A3} is turned ON, then energy exchange path C_3–D_{As3}–Q_{A3}–L_1 is formed between Part 3 and energy buffer, as shown in Fig. 9(c). During the duration of this substate, L_2's energy is transferred to L_1 for the coupling inductance. The energy is shifted from C_3 to L_1, and i_{L1} is increased linearly for the duration of this substate.

When Q_{A3} is turned OFF and Q_{A1} is turned ON, another switching cycle begins. By coupling inductance, some energy of C_3 is transferred to C_1 and C_2 to increase I_1 and I_2. Q_{A1}, Q_{B2}, and Q_{A3} are complementary to each other, whereas Q_{B1}, Q_{A2}, and Q_{B3} are always in the OFF state, which means Q_{A1}, Q_{B2}, and Q_{A3} need to be controlled.

According to the analysis above, during one substate, it is assumed that the energy exchange path forms between Part i and energy buffer, while the other Parts disconnect from energy buffer. This three-line IDCPFC has 49 kinds of operation conditions, including the bypass mode, to meet the different power flow directions and control targets.

The summary table of conditions 1 and 2 is given in Table I. The specific switching action rules based on specific operation conditions are given as follows.

1) The mode that Parts and energy buffer work in is determined by the dc power flow direction. There will be an energy exchange path between Part i and energy buffer.
2) While the dc power flow of line i is in the positive direction during one substate, the energy buffer works in mode 2; while the dc power flow of line i is in the negative direction during one substate, the energy buffer works in mode 3.
3) While the dc power flow of line i is in the positive direction, Part i works in mode 3 (Q_{Ai} is controlled); while dc power flow of line i is in the negative direction, Part i works in mode 4 (Q_{Bi} is controlled).
4) If Part j ($j \neq i$) participates in energy exchange during one duty cycle, Part j works in mode 2. If Part j ($j \neq i$) does not participate in energy exchange during one duty cycle, Part j works in mode 1. That is, a given n-line IDCPFC can achieve the function of k-line IDCPFC ($k = 1,2,\ldots,n$).

Note: An n-line IDCPFC can achieve the function of k-line IDCPFC ($k = 1,2,\ldots,n$). If some lines that do not participate in energy exchange between lines, their Parts work in mode 1.

C. Multitarget Control Strategy

For n-line IDCPFC, n substates in a single duty cycle need to be controlled independently. Define duty cycles for n substates as $D_1, D_2, \ldots, D_n$, respectively.

The general control strategy for n-line IDCPFC is shown in Fig. 10. It can be seen that the control strategy consists of two parts: the front part is used to generate transition waveforms (PWM1, PWM2, …, PWMn); the back part is used to generate switching signals (CH1, CH2, …, CHn).

TABLE I
SUMMARY OF CONDITIONS 1 AND 2

$I_1/I_2/I_3$ direction	$I_1/I_2/I_3$ control targets	$V_{c1}/V_{c2}/V_{c2}$ polarity	Controlled switching device	Sub-state	Mode of Part 1	Mode of Part 2	Mode of Part 3	Mode of Energy Buffer	Condition
+/+/+	↓/↓/↑	+/+/-	Q_{A1}, Q_{A2}, Q_{A3}	Sub-state1	mode3	mode2	mode2	mode2	1
				Sub-state2	mode2	mode3	mode2	mode2	
				Sub-state3	mode2	mode2	mode3	mode2	
+/-/+	↑/↑/↓	-/-/+	Q_{A1}, Q_{B2}, Q_{A3}	Sub-state1	mode3	mode2	mode2	mode2	2
				Sub-state2	mode2	mode4	mode2	mode3	
				Sub-state3	mode2	mode2	mode3	mode2	

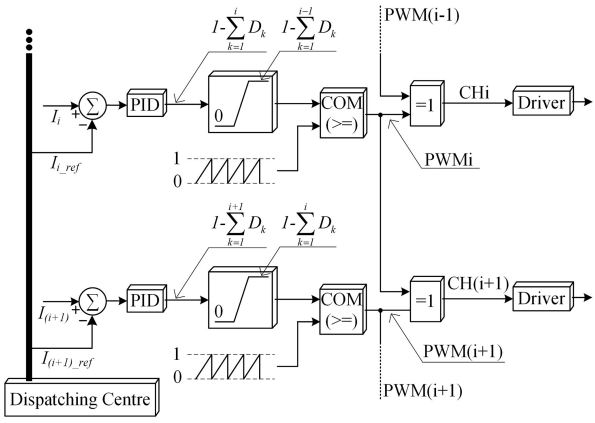

Fig. 10. Universal control strategy of multiline IDCPFC.

Current reference value I_{i_ref} of line i is compared with the actual current value I_i of line i. The difference obtained by PID regulator is compared with sawtooth carrier to generate PWM*i*. It is noted that the difference obtained is limited by "dynamic limit value" to obtain complementary switching signals. Particularly, defining PWM*n* is low level (0), PWM0 is high level (1). CH*i* is generated with XOR gate by PWM($i-1$) and PWM*i* rather than comparing their duty cycles and carrier waveform traditionally.

Condition 1 of three-line IDCPFC (referring to Fig. 8) is taken as an example to demonstrate detailed control strategy.

Suppose the currents I_1 and I_2 of Line 1 and 2 are control targets, that is, I_1 and I_2 are controlled actively, while I_3, the current of Line 3, is controlled passively. As shown in Fig. 11, two control targets are completely decoupling without constraint on each other. In Fig. 11(a), the upper limit of output limiter unit for PID unit is determined by $1-D_1$, whose equivalent mathematical constraints (1) is as follows:

$$\text{s.t.} \begin{cases} 0 \le D_i \le 1 i = 1, 2, 3 \\ D_1 + D_2 + D_3 = 1. \end{cases} \tag{5}$$

The generation process of three complementary signals (CH1, CH2, and CH3) in a single switching cycle is detailed in Fig. 11(b). CH1, CH2, and CH3 are the control signals of Q_{A1}, Q_{A2}, and Q_{A3}, respectively in condition 1.

D. Characteristics Analysis

Also, condition 1 of three-line IDCPFC (referring to Fig. 8) is taken as an example to prove the general character equation.

Set the duty cycle of Q_{A1} as D_1, Q_{A2} as D_2, Q_{A3} as D_3 ($D_1 + D_2 + D_3 = 1$). While the current of coupling inductance is continuous, (6) can be obtained by the principle of voltage-second balance as

$$V_{c1} D_1 T_s + V_{c2} D_2 T_s - V_{c3} D_3 T_s = 0 \tag{6}$$

where T_s is the switching cycle.

While the voltages of C_1, C_2, and C_3 are continuous, according to charge conservation, (7)–(9) can be obtained as

$$(I_1 - I_L) D_1 T_s + I_1 (1 - D_1) T_s = 0 \tag{7}$$

$$(I_2 - I_L) D_2 T_s + I_2 (1 - D_2) T_s = 0 \tag{8}$$

$$(I_3 - I_L) D_3 T_s + I_3 (1 - D_3) T_s = 0 \tag{9}$$

where I_L is the average inductor current.

When the equations above are simplified, we can obtain

$$I_1 = D_1 I_L \tag{10}$$

$$I_2 = D_2 I_L \tag{11}$$

$$I_3 = D_3 I_L. \tag{12}$$

The duty cycles D_1, D_2, and D_3 have a linear relationship with the corresponding line current, which indicates that D_i can control the current of line i. Also, (10)–(12) are the average model of three-line IDCPFC. According to (6) and (10)–(12), we can obtain

$$V_{c1} I_1 + V_{c2} I_2 - V_{c3} I_3 = 0 \tag{13}$$

$$I_L = I_1 + I_2 + I_3. \tag{14}$$

Equation (13) is the charge conservation of three-line IDCPFC, while the efficiency is 100%. The ripple formulas of V_{c1}, V_{c2}, V_{c3}, and I_L can be derived as

$$\begin{cases} \Delta V_{c1} = (I_2 + I_3) I_1 T_s / C_1 I_L \\ \Delta V_{c2} = (I_1 + I_3) I_2 T_s / C_2 I_L \\ \Delta V_{c3} = (I_1 + I_2) I_3 T_s / C_3 I_L \\ \Delta I_L = I_3 V_{c3} T_s / (I_1 + I_2 + I_3) L. \end{cases} \tag{15}$$

As seen in Fig. 12, three-line IDCPFC has four function areas and the analysis is detailed as follows.

1) When $D_1 + D_2 + D_3 = 1$, the controller performs the function as three-line IDCPFC (the power flows of two lines are controlled actively, while the other one is controlled passively), as indicated by the triangle ABC.

TABLE II
DETAILS OF FUNCTION AREAS

CASE	MATHEMATICS LAYER		PHYSICAL LAYER		BYPASS SWITCH		NUMBER OF CONTROLLED LINES	
	ALGEBRAIC MEANING	GEOMETRIC MEANING	CONTROLLED LINE	BYPASS LINE	ON	OFF	ACTIVE	PASSIVE
1	$D_1+D_2+D_3=1$	①ΔABC	Line1, Line2, Line3	----	----	S_1, S_2, S_3	2	1
2	$D_1+D_2=1\&D_3=0$	② L_{AB}	Line1, Line2	Line3	S_3	S_1, S_2	1	1
3	$D_1+D_3=1\&D_2=0$	③ L_{AB}	Line1, Line3	Line2	S_2	S_1, S_3	1	1
4	$D_2+D_3=1\&D_1=0$	④ L_{BC}	Line2, Line3	Line1	S_1	S_2, S_3	1	1

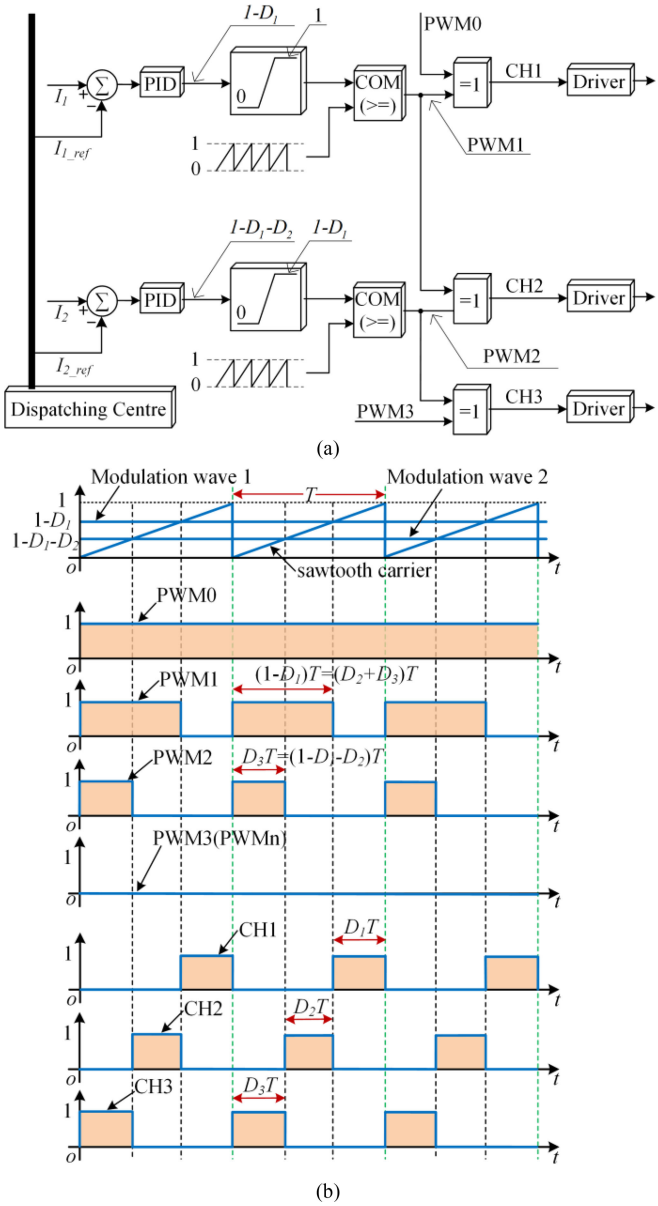

Fig. 11. Control strategy of three-line IDCPFC. (a) Block diagram. (b) Switch signals in one case.

2) When ($D_1 + D_2 = 1$ & $D_3 = 0$) or ($D_1 + D_3 = 1$ & $D_2 = 0$) or ($D_2 + D_3 = 1$ & $D_1 = 0$), the controller performs the function as three-line IDCPFC (the power flow of one line is controlled actively, while the other one is controlled passively), as indicated by the lines 2, 3, and 4.

The specific details are listed in Table II including the controlled lines and controlled switches.

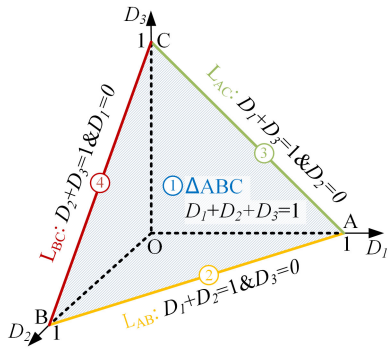

Fig. 12. Functional area of three-line IDCPFC.

Similarly, for the multiline IDCPFC, the general character equations are given as follows:

$$\sum_{i=1}^{n} V_{ci} D_i T_s = 0 \tag{16}$$

where V_{ci} is the average voltage of capacitor.

While the voltage of C_i is continuous, according to charge conservation, (17) can be obtained

$$I_i = D_i I_L i = 1, 2, \cdots, n \tag{17}$$

where I_L is the average inductor current. The duty cycle D_i has a linear relationship with the line current, which indicates that D_i can control the current of lines.

According to (16) and (17), we can obtain

$$\sum_{i=1}^{n} V_{ci} I_i = 0. \tag{18}$$

Equation (18) is the charge conservation of multiline IDCPFC, while the efficiency is 100%. Similarly, the ripple formula of the capacitor voltage V_{ci} and the inductor current I_L can be derived as

$$\begin{cases} \Delta V_{ci} = \left(\sum_{i=1}^{n} I_i - I_i\right) I_i T_s / C_i \sum_{i=1}^{n} I_i \\ \Delta I_L = T_s \sum_{i=1}^{n} |I_i V_{ci}| / 2L \sum_{i=1}^{n} I_i. \end{cases} \tag{19}$$

The main parameters of modular IDCPFC are designed by the rate values (obtained by the desired power flow range and the system equations) and ripple requirements above.

IV. SIMULATION VERIFICATION

In order to verify the validity and accuracy of proposed extension methodology, an equivalent four-terminal HVDC system model is built in MATLAB/SIMULINK environment, as seen in Fig. 13. A three-line IDCPFC is taken as an example to verify the methodology in this four-terminal VSC–HVDC system.

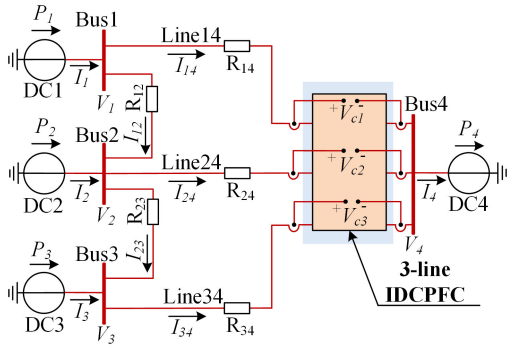

Fig. 13. Simulation model of a four-terminal VSC–HVDC system.

The detailed information of the simulation cases are listed in the following:

1) For the symmetry and convenience of analysis, only the positive polarity transmission lines of dc grid are considered.
2) VSC1,VSC2, and VSC3 work as constant power sources, delivering 300,120, and 60 MW to the four-terminal VSC–HVDC system, respectively.
3) VSC4 that works in constant voltage mode ($V_4 = 150$ kV) outputs system power.
4) The three-line IDCPFC is installed beside the bus 4 of VSC4. The capacitors C_1, C_2, and C_3 are in series with the line 14, line 24, and line 34, respectively.
5) The transmission line parameters are provided in Table III.
6) Parameter calculation:
   1) According to the power flow control range request, the rated values I_{14}, I_{24}, and I_{34} are 1.5, 1.8, and 1.6 kA, respectively.
   2) By the system power flow equation [1]–[4], the rated values V_{c1}, V_{c2}, and V_{c3} are 5, 5, and 12 kV, respectively.
   3) The switching frequency is set as 2 kHz.
   4) Set the $\Delta V_{c1}/V_{c1}$, $\Delta V_{c2}/V_{c2}$, $\Delta V_{c3}/V_{c3}$, and $\Delta I_L/I_L = 20\%$. By the ripple (19), C_1, C_2, C_3, and L ($L = L_1 = L_2$) are calculated mathematically as 0.52, 0.57, 2.24, and 1.86 mH, respectively. Thus, C_1, C_2, C_3, and L are set as 0.6, 0.6, 2.4, and 2 mH, respectively.

$$\begin{cases} I_{12} = \frac{V_1 - V_2}{R_{12}} \\ I_{23} = \frac{V_2 - V_3}{R_{23}} \\ I_{14} = \frac{V_1 - V_4 - V_{c1}}{R_{14}} \\ I_{24} = \frac{V_2 - V_4 - V_{c2}}{R_{24}} \\ I_{34} = \frac{V_3 - V_4 - V_{c3}}{R_{34}} \\ P_1 = (I_{12} + I_{14})V_1 \\ P_2 = (I_{23} + I_{24} - I_{12})V_2 \\ P_3 = (I_{34} - I_{23})V_3. \end{cases} \tag{20}$$

According to Fig. 13, the power flow equations of system are given by (20). According to system equations, the initial steady-state currents I_{14}, I_{24}, and I_{34} of lines 24 and 34 can be calculated as 1.0, 1.1, and 1.0 kA, respectively.

TABLE III
TRANSMISSION LINE PARAMETERS

Parameter	LINE12	LINE23	LINE14	LINE24	LINE34
Distance/km	250	500	500	500	250
Resistance/Ω	2.5	5	5	5	2.5

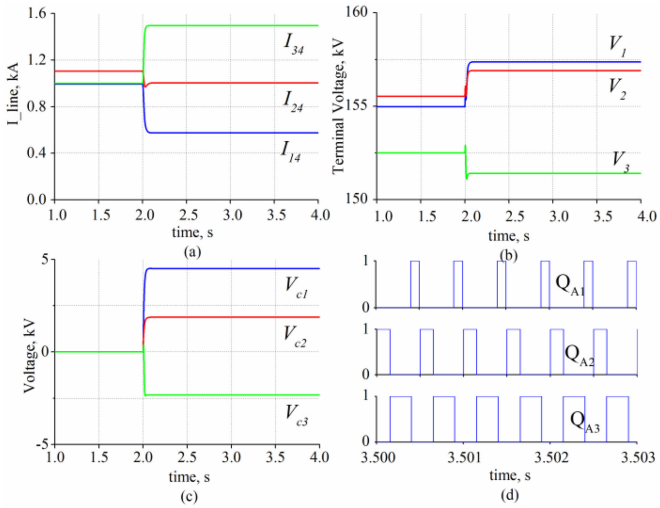

Fig. 14. Simulation results of startup. (a) I_{14}, I_{24}, and I_{34}. (b) V_1, V_2, and V_3. (c)V_{c1}, V_{c2}, and V_{c3}. (d) Q_{A1}, Q_{A2}, and Q_{A3}.

A. Startup of Three-Line IDCPFC

In this simulation, the three-line IDCPFC is bypassed in initial state (i.e., $t = 0$–2 s). At $t = 2$ s, the three-line IDCPFC obtains instructions to control the currents I_{24} and I_{34} of lines 24 and 34, whose reference values are 1 and 1.5 kA, then the three-line IDCPFC is started up.

The simulation waveforms of the entire startup process are given in Fig. 14. It can be seen in Fig. 14(a) that the line currents quickly respond when the three-line IDCPFC is put into operation (red curve corresponding to I_{24}; blue curve corresponding to I_{14}; and green curve corresponding to I_{34}). The terminal voltage curves of VSCs are shown in Fig.14(b). The voltage curves of V_{c1}, V_{c2}, and V_{c3} are shown in Fig. 14(c). The capacitor voltages V_{c1}, V_{c2}, and V_{c3} reach 4.5, 1.88, and -2.33 kV, respectively, after the quick transient process. The complementary switching signal waveforms are shown in Fig. 14(d). It can be found from Fig. 14 that the simulation results of startup process meet the theoretical analysis, which proves the validity of the proposed working principles.

B. Active Control of One Line's Power Flow

In this simulation, the three-line IDCPFC is first set to work in the steady state (I_{24} and I_{34} are controlled to reach 1 and 1.5 kA, respectively). At $t = 2$ s, the three-line IDCPFC is instructed to change the current reference value of I_{24} from 1 to 0.5 kA, while I_{34} keeps unchanged.

The whole simulation results in this case are shown in Fig. 15. The waveforms of three controlled lines' power flows are shown in Fig. 15(a). The current I_{24} of line 24 is decreased from 1 to

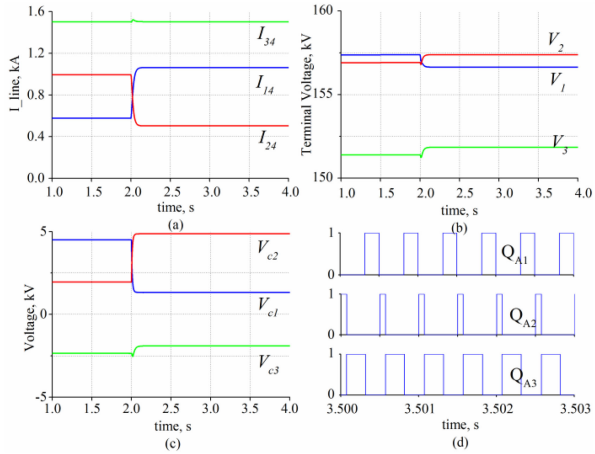

Fig. 15. Simulation results of one line's active control. (a) I_{14}, I_{24}, and I_{34}. (b) V_1, V_2, and V_3. (c)V_{c1}, V_{c2}, and V_{c3}. (d) Q_{A1}, Q_{A2}, and Q_{A3}.

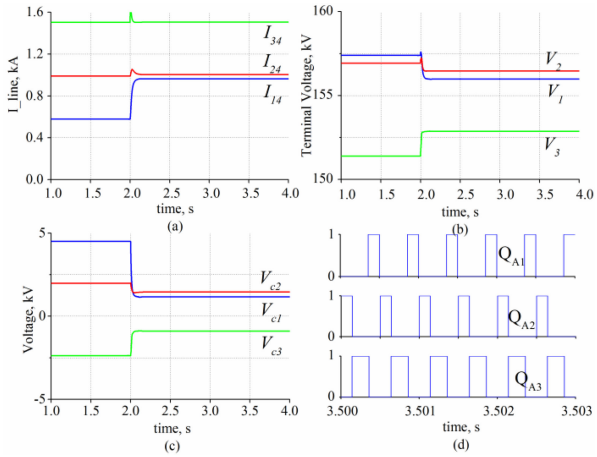

Fig. 16. Simulation results of VSC power output change. (a) I_{14}, I_{24}, and I_{34}. (b) V_1, V_2, and V_3. (c)V_{c1}, V_{c2}, and V_{c3}. (d) Q_{A1}, Q_{A2}, and Q_{A3}.

0.5 kA, while the current I_{34} of line 34 keeps 1.5 kA after quick transient process.

And, the current I_{14} of line14 is increased from 0.57 to 1.06 kA. The terminal voltages V_2 and V_3 of VSC2 and VSC3 reach 157.38 and 151.84 kV, respectively, as seen in Fig. 15(b). As shown in Fig. 15(c), the capacitor voltages V_{c1}, V_{c2}, and V_{c3} are 1.32, 4.87, and -1.92 kV, respectively. It can be seen from Fig. 15 that the simulation results, which are consistent with the theoretical analysis, verify the ability in active power flow control of two lines.

C. Response to Disturbance

In this simulation, the three-line IDCPFC is first set to work in the steady state (I_{24} and I_{34} are controlled to reach 1 and 1.5 kA, respectively). At $t = 2$ s, the output power of VSC3 is set to rise quickly from 60 to 120 MW (a step change), while VSC1 and VSC2 output powers keep unchanged. For the three-line IDCPFC, the control reference values of both I_{24} and I_{34} keep unchanged. As shown in Fig. 16(a), it can be seen that the power flows of controlled line have rapidly returned to the desired current values after the short transient process of

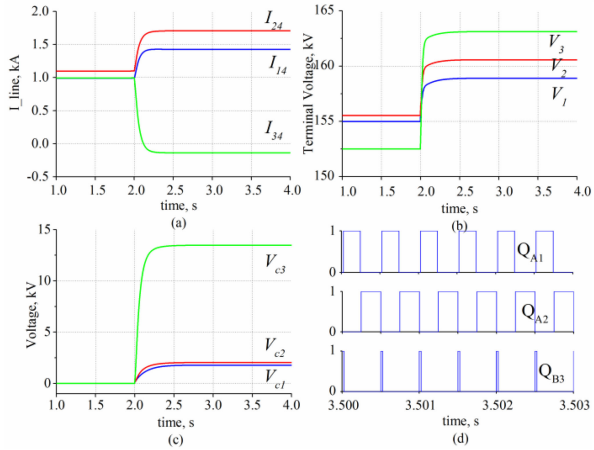

Fig. 17. Simulation results of power flow reversal. (a) I_{14}, I_{24}, and I_{34}. (b) V_1, V_2, and V_3. (c)V_{c1}, V_{c2}, and V_{c3}. (d) Q_{A1}, Q_{A2}, and Q_{A3}.

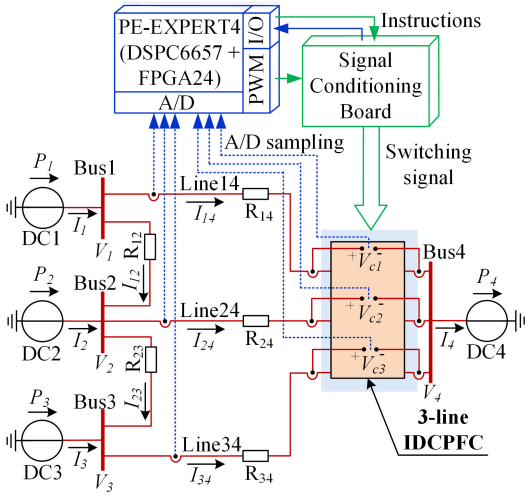

Fig. 18. Four-terminal dc grid experimental platform.

about 0.12 s. As shown in Fig. 16(b) and (c), it can be seen that after about 0.12 s, VSC terminal voltages $V_1/V_2/V_3$ and the capacitor voltages $V_{c1}/V_{c2}/V_{c3}$ return to their steady-state values. The voltages V_{c1}, V_{c2}, and V_{c3} reach 1.16, 1.45, and -0.90 kV, respectively, after transient process.

The whole simulation results show that in the event of sudden disturbances (e.g., VSC output power jumps), the proposed multiline IDCPFC control strategy has good performance of fast responding and accurate regulation.

D. Power Flow Reversal

This simulation is used for verifying the capability of coping with power flow reversal process of line 34. The three-line IDCPFC is bypassed and the current $I_{34} = 1$ kA before I_{34} reverses. At $t = 2$ s, the three-line IDCPFC is instructed to control I_{24} and I_{34} with current reference values of 1.7 and -0.14 kA, respectively. The simulation results of the whole process are shown in Fig. 17.

According to Fig. 17(a), the direction of I_{34} in line 34 is changed from the positive direction to the negative direction

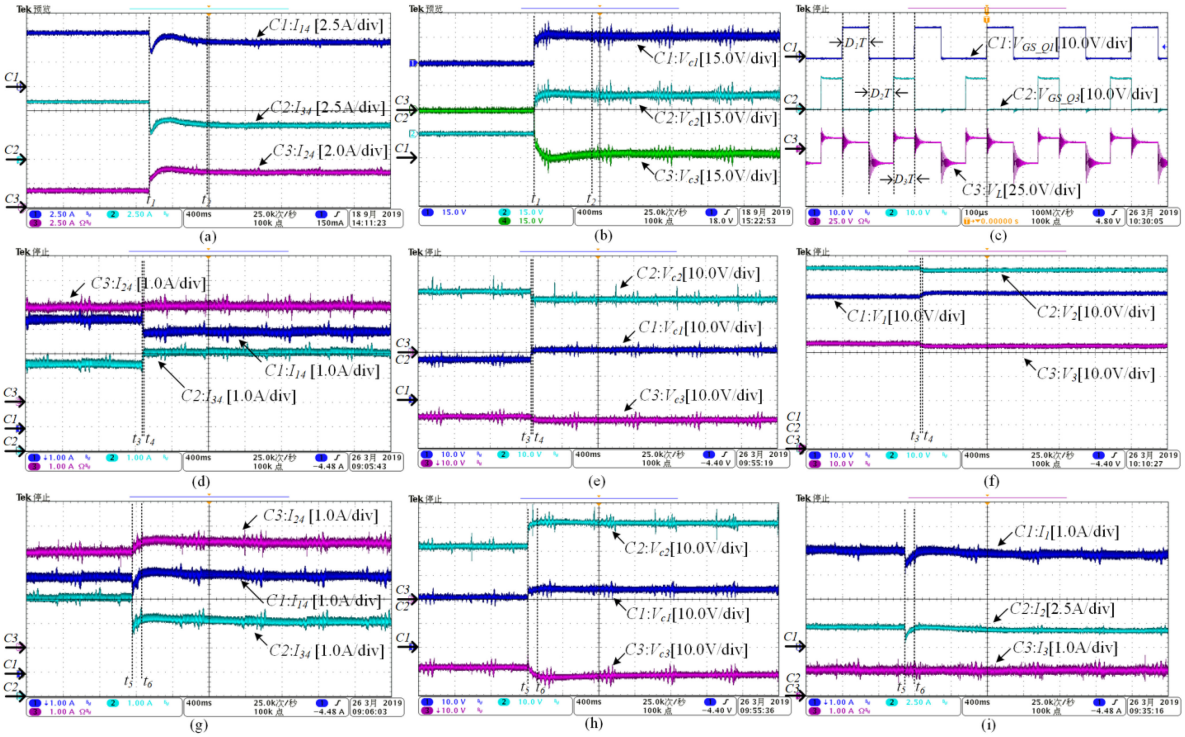

Fig. 19. Experiment waveforms. (a) Startup: the currents I_{14}, I_{24}, and I_{34}. (b) Startup: the voltages V_{c1},V_{c2}, and V_{c3}. (c) Startup: the voltages V_L, driver signal $V_{GS\cdot Q1}$, and $V_{GS\cdot Q3}$ after t_2. (d) Increasing I_{34}: the currents I_{14}, I_{24}, and I_{34}. (e) Increasing I_{34}: the voltages V_{c1}, V_{c2}, and V_{c3}. (f) Increasing I_{34}: the voltages V_1, V_2, and V_3. (g) Increasing I_{24}: the currents I_{24}, I_{14}, and I_{34}. (h) Increasing I_{24}: the voltages V_{c1}, V_{c2}, and V_{c3}. (i) Increasing I_{24}: the currents I_1, I_2, and I_3.

and the direction of I_{24} of line24 keeps unchanged, thereby indicating that the three-line IDCPFC can cope with power flow reversal scene. In Fig. 17(b), the terminal voltages $V_1/V_2/V_3$ of VSC1, VSC2, and VSC3 rise to 158.89, 160.57, and 163.11 kV, respectively. In Fig. 17(c), V_{c1}, V_{c2}, and V_{c3} are 1.77, 2.03, and 13.46 kV, respectively, which meets the requirements of the power flow reversal.

V. Experiment Verification

In order to verify the correctness and rationality of extension multiline IDCPFC topology proposed in this article, a down-scale experimental platform has been built in the laboratory. The four-terminal monopole architecture of experiment system is shown in Fig. 18 for reference, which is consistent with the simulation system in Fig. 13. Detailed information of the experiment system is listed as follows.

1) The proposed control strategy of multiline IDCPFC is accomplished in the PE-Expert4™ controller.
2) The output power P_1, P_2, and P_3 of three constant power sources DC1, DC2, and DC3 is 300, 500, and 50 W, respectively. The voltage V_4 of constant voltage source DC4 is 30 V.All sources are represented by Chroma DC Power Supply and pCUBE™ power supplies.
3) The line resistances $R_{14} = 5.5\ \Omega$, $R_{24} = 5.5\ \Omega$, and $R_{34} = 11\ \Omega$.

Based on the experimental platform, the typical experiment verifications on active dc power flow control function in two selective lines are carried out, and the corresponding waveforms are given in Fig. 19.

A. Experiment Study I (Startup of Three-Line IDCPFC)

The experimental waveforms are shown in Fig. 19(a)–(c) when the three-line IDCPFC has been activated. Before t_1, the initial steady-state currents I_{14}, I_{24}, and I_{34} of lines 14, 24, and 34 reach 5.2, 2.1, and 6.4 A, respectively. At t_1, the control instructions are sent to control the currents I_{24} and I_{34} of lines 24 and 34 to reach 4 and 3.5 A simultaneously. It takes about 800 ms for the controlled currents to reach steady-state value at t_2, and the capacitor voltages V_{c1} and V_{c2} rise from zero to 17.7 V and 25.5 V, whereas V_{c3} falls from zero to -26.6 V. The steady-state waveforms of driver signal $V_{GS\cdot Q1}$, $V_{GS\cdot Q2}$, and voltage V_L after t_2 are shown in Fig. 19(c), which are consistent with the theoretical analysis of proposed working principles and control strategy.

B. Experiment Study II (Active Control of the One Line's Power Flow While Keeping the Other One Unchanged)

Fig. 19(d)–(f) show the experimental waveforms of adjusting the current I_{14}, while keeping the current I_{24} unchanged. At t_3, a control instruction is sent to control the current I_{14} to reach 4 A. Within the period of 40 ms, the current I_{24} maintains at 4 A quickly after slight fluctuations and the current I_{14} reaches 4 A at t_4. The capacitor voltages V_{c1} and V_{c2} rise from zero to 21.7 and 21.9 V while, V_{C3} falls from zero to -28.3 V. The terminal voltages V_1, V_2, and V_3 with small changes are shown in Fig. 19(f).

Fig. 19(g)–(i) show the experimental waveforms of changing I_{34}, while keeping I_{14} unchanged. At t_5, a control instruction is sent to control the current I_{34} to reach 3.0 A. Within the

period of 110 ms, the current I_{14} maintains at 4.0 kA after slight fluctuations. The transient waveforms of dc source currents I_1, I_2, and I_3 from t_5 to t_6 are shown in Fig. 19(i).

VI. Conclusion

This article presents the general structure of multiline interline dc power flow controller and its maximum multiple dc power flow control potential is analyzed. For n-line IDCPFC, the power flow ability is exploited enough to control $(n-1)$-line power flow actively. A universal extension methodology of multiline IDCPFC is detailed in this article. The core of extension methodology, operation principle, and control strategy is detailed and analyzed. A simulation model and an experiment platform are built for verification. The conclusions are as follows.

1) For a single n-line interline dc power flow controller, the maximum number of dc power flow control targets is $(n-1)$. Specifically, the maximum $(n-1)$-line power flow can be controlled actively, while only one-line power flow is determined passively.
2) The proposed modular approach including topology, operation principle, and control strategy is detailed to precisely construct and analyze multiline interline dc power flow controller.
3) The proposed multiline interline dc power flow controller is suitable for situation with different power flow directions. For n-line interline dc power flow controller, the active control of $(n-1)$ lines power flow can be achieved.
4) The proposed multitarget control strategy can regulate the duty ratios within multiple substates in one duty cycle, by which the multiple control targets are completely decoupled.
5) Multiline interline dc power flow controller might have extensive applications in future dc grid scenarios, such as complex MTDC system and dc distribution network.
6) The modular approach also can be used as a guide to extend many existing IDCPFCs to fully excavate maximum dc power flow control ability.

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