# Letters

# Improving Surge Current Capability of SiC Merged PiN Schottky Diode by Adding Plasma Spreading Layers

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***Abstract*—In this article, a novel structure design concept [plasma spreading layer (PSL)] is introduced into silicon carbide (SiC) merged PiN Schottky (MPS) diode to improve the surge current capability. Compared to the isolated P+ island design in traditional MPS diode, the P+ islands in the proposed new structure are connected by the P+ plasma spreading layers which can spread bipolar current from P+ islands to the other parts of the device during the surge pulse. Therefore, the effective conducting area of the device is increased and the energy dissipation capability can be improved. In this article, 1.2-kV SiC MPS diodes with two types of plasma spreading layers are designed and fabricated. Their forward characteristics and surge current capability are compared to traditional stripe cell and hexagonal cell designed MPS diodes. The experimental results show that, with the help of the plasma spreading layers, a 20% increase of energy dissipation capability is achieved by the new structure design, which results in a 10% improvement of the surge current capability.**

***Index Terms*—Device design, diode, reliability, SiC, surge current.**

## I. Introduction

The forward characteristics of MPS diodes can be divided into two regimes: unipolar current conduction at relatively low forward voltage, and bipolar current conduction at high forward voltage [1], [2]. When the anode voltage reaches the threshold voltage of the Schottky junction, a current of majority carriers starts flowing through the device. When the anode voltage is further increased beyond a certain value which is the case for surge condition, the inherent pn junction formed by the P+ regions will be turned ON and minority carriers will be injected into the semiconductors on the two sides of the junction, thus, plasma of electrons and holes will cause a significant conductivity modulation in the bulk of MPS diodes. In this case, the surge current is mainly conducted by the pn junction instead of the Schottky junction.

Although the commercial products are technologically mature, and the reliability data has been reported to be good enough for old generations, new generation products based on the wafer thinning technology are facing greater challenges as the chip size is shrunk significantly. Therefore, new device technology advancements are still in need for SiC diodes to improve the reliability along with the continuous size/cost reduction. Surge current capability is one of the main aspects of reliability for a diode. Early work on SiC MPS diodes reported that the ratio of P+ area to Schottky area is a decisive parameter that controls the electrical behavior of MPS diodes [3], [4]. However, the layout types and the P+ region designs are also found to have great impacts on the surge current capability of MPS diodes. For example, in some studies, alternative variants of contact topography and layout design were considered to obtain a better tradeoff relation between the forward voltage drop at nominal current and surge current capability [5], [6]. In these studies, the P+ area percentage and the pn junction turn-ON voltage is deemed as the key factors that determine the surge current capability of the MPS diodes. However, they do not consider the unbalanced current distribution in each unit cell which contains both pn junction and Schottky junction. In addition, for a MPS diode structure which contains two types of P+ regions (narrow and wide ones), only wide P+ regions can be turned ON as the pn junction turn-ON voltage of the narrow one is much higher. This can aggravate the unbalance of current distribution. When the minority carriers are injected into the N-drift region and diffuse across the bulk region, the lateral plasma spreading process is essential for current sharing. How much the bipolar current can spread from the wide P+ area to the other parts can determine the effective conducting area during the surge pulse. If the surge current can be distributed within the whole device active area, the energy dissipation and surge current capability of the device can be improved. To solve this issue, a novel structure design concept, plasma spreading layer is introduced in this article.

## II. Simulation Study and Device Design

The schematic view of the typical SiC MPS diode cell structures are shown in Fig. 1, where Fig. 1(a) and (b) show stripe and hexagonal cell design, respectively. These two type cell designs are implemented in commercial SiC diode products. The MPS

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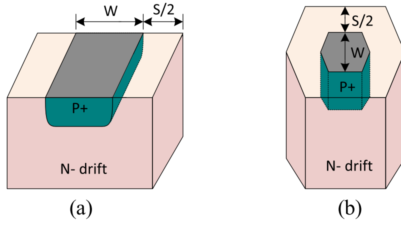


Fig. 1. Two typical cell structures of SiC MPS diode. (a) Stripe cell. (b) Hexagonal cell. These two type cell designs are implemented in commercial SiC diode products.

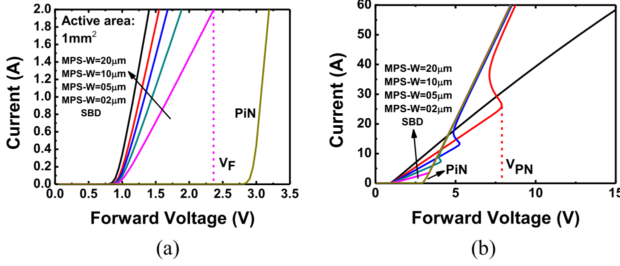


Fig. 2. Simulated forward I–V characteristics of stripe cell designed MPS diodes with $S = 2$ $\mu$m and varied $W$ designs from 2 $\mu$m to 20 $\mu$m. (a) Low current regime. (b) High current regime.

cell is formed by a P+ implant under the surface of the N-type drift layer and an Ohmic contact is placed on the P+ surface. The pn junction between the P+ region and the N-type drift layer can be turned ON at a certain forward voltage (named pn junction turn-ON voltage, $V_{PN}$) and conduct current in high current mode. The pn junction turn-ON voltage has great effects on the bipolar conduction capability. The lower pn junction turn-ON voltage, the lower power dissipated by the device when conducting a high current. While the forward voltage drop $V_F$ is usually used as the index to evaluate the device conduction performance in normal operation, the pn junction turn-ON voltage can be used as the precursor for surge capability assessment in device design stage. As shown in Fig. 1, the width of the P+ region and the Schottky region in the MPS cell are designated as $W$ and $S$, respectively. The two structural parameters are carefully designed in the following to obtain an optimized MPS diode design for each type of cell structure.

### *A. Simulation Study of SiC MPS Diodes*

Simulation studies of MPS diodes based on SILVACO software are carried out. The doping concentration and thickness of the drift layer used in simulation are $8 \times 10^{15}$ cm$^{-3}$ and 12 $\mu$m, respectively. The device active area is 1 mm$^2$.

For the stripe cell design as shown in Fig. 1(a), the simulated forward I-V characteristics of MPS diodes are shown in Fig. 2, where Fig. 2(a) and (b) show the I-V characteristics in low current regime (up to 2A) and high current regime (up to 60 A), respectively. The MPS diodes have the same $S$ (20 $\mu$m) design and different $W$ designs (2, 5, 10, and 20 $\mu$m). The I-V curves of a pure SBD diode and a PiN diode are also plotted as references. It is shown from Fig. 2(a) that the MPS diode behaves like a pure Schottky diode in the low current regime. With an increasing P+ width ($W$), device forward voltage drop ($V_F$) at

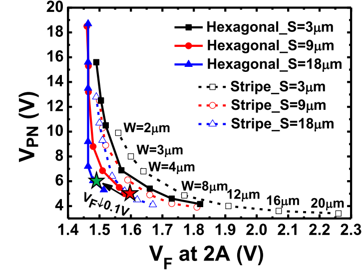


Fig. 3. Tradeoff relation between the forward voltage drop $V_F$ at 2A and pn junction turn-ON voltage $V_{PN}$ from the forward I–V simulation results of MPS diodes with stripe cell design and hexagonal cell design.

2A is also increased as the Schottky area percentage is declined. In high current regime in Fig. 2(b), when the voltage bias exceeds the pn junction turn-ON voltage $V_{PN}$, the I-V curves become sharper due to the minority carrier injection and the conductivity modulation effect. Different from the case of $V_F$, the pn junction turn-ON voltage $V_{PN}$ is decreased with an increasing $W$.

As the $V_F$ and $V_{PN}$ are the two key indexes for MPS diodes, they are extracted and summarized in Fig. 3. In addition, the hexagonal cell is also simulated, the $V_F$ and $V_{PN}$ results of which are summarized in Fig. 3 as well. Obviously, a trade-off relation between the $V_F$ and $V_{PN}$ can be observed. The design objective of the MPS diode is to find a proper group of structural parameters of the wide P+ region width ($W$) and spacing ($S$) to achieve a low $V_F$ and a low $V_{PN}$ at the same time. It can be concluded that $W = 14$ $\mu$m with $S \geq 15$ $\mu$m is the optimal design for the stripe cell structure, and the optimal design for hexagonal cell structure is $W = 16$ $\mu$m with $S \geq 15$ $\mu$m. The optimal hexagonal cell structure can outperform stripe cell structure as it can achieve a 0.1 V lower $V_F$, which is desirable to reduce the ON-state power loss of the device.

### *B. New Structure Design With Plasma Spreading Layers*

With the guidance of the simulation study, 1.2 kV/2A SiC MPS diode designs are performed for the two type cell structures, stripe cell and hexagonal cell. Fig. 4(a) shows the layout design (Design A) of stripe cell structure ($W = 14$ $\mu$m, $S = 16.5$ $\mu$m). Different from the simulation structure, multiple JBS cells with narrow P+ stripes are inserted into the P+ spacing of the MPS cell to enhance the electric field shielding effect and to reduce the leakage current in reverse blocking mode. The width of the narrow P+ stripes ($P$) are fixed at 1.5 $\mu$m and the spacing between two adjacent narrow P+ stripes is fixed at 3 $\mu$m.

Fig. 4(b) shows the layout design (Design B) of hexagonal cell structure ($W = 16$ $\mu$m, $S = 16.5$ $\mu$m). Similarly, the narrow P+ rings are added around the P+ islands to enhance the electric field shielding effect in reverse blocking mode.

To check the unbalanced current distribution existed in the MPS diode structure, the current density distribution in one unit cell in high current conduction condition is simulated and the results are shown in Fig. 5. It is shown that the wide P+ region conducts the most current while the Schottky region shares a little and the pn junction formed by the narrow P+ region is completely closed. The lateral current spreading from the bulk region under the wide P+ region to the other parts is limited.

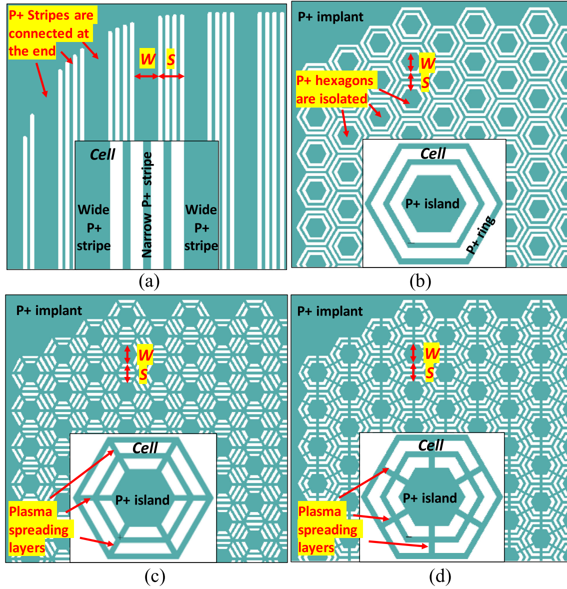


Fig. 4. Schematic view of different MPS diode structures. (a) Stripe cell design (Design A). (b) Hexagonal cell design without plasma spreading layers (Design B). (c) Hexagonal cell design with P+ diagonal lines added as the plasma spreading layers (Design C). (d) Hexagonal cell design with P+ cross lines added as the plasma spreading layers (Design D).

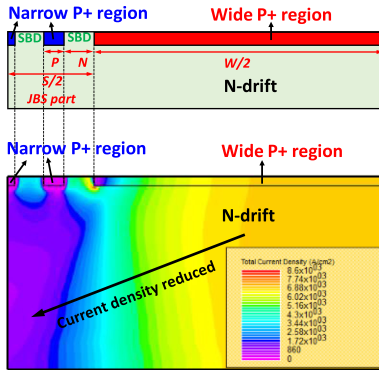


Fig. 5. Simulated current density distribution of the MPS diode structure in Fig. 4(b). The average current density is 6000 A/cm$^2$ corresponding to a 60 A surge current for the 1 mm$^2$ device size.

In order to spread the bipolar current laterally and increase the effective conducting area, P+ type plasma spreading layers are added to the hexagonal layout as shown in Fig. 4(c) and (d). They can provide interconnection for the P+ islands and narrow P+ rings. The number of cells in Design B-D are the same while it is different in Design A.

## III. Device Fabrication and Characterization

Based on the device designs in Section II, four kinds of 1.2 kV/2A MPS diodes are fabricated. There is no special treatment in the fabrication process for the MPS diode with PSL structure, as the P+ plasma spreading layers can be formed by the same implantation process with the P+ hexagonal islands in active region and the P+ rings in termination region. The active area is 1 mm$^2$. The fabricated devices are packaged, then electrical characterizations are performed. The measured

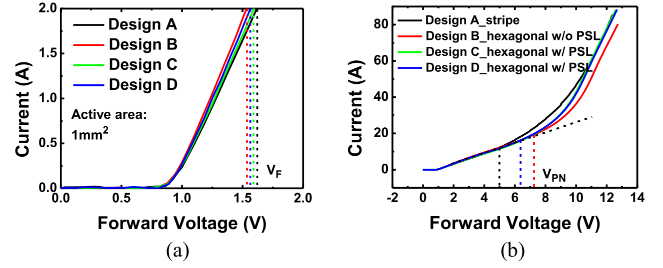


Fig. 6. Experimental results of forward I–V characteristics of the four SiC MPS diodes. (a) Low current regime. (b) High current regime.

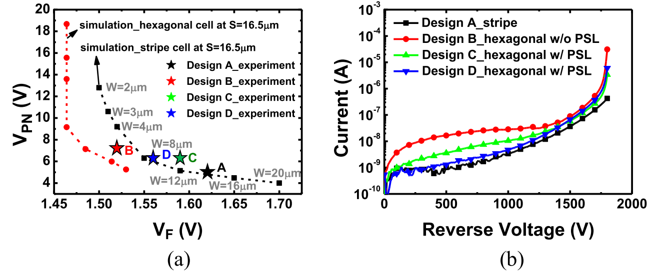


Fig. 7. (a) Experimental results of $V_F$ and $V_{PN}$ for the four SiC MPS diodes and their comparison with simulation results. (b) Experimental results of reverse I–V characteristics of the four SiC MPS diodes.

forward I-V characteristics of the four SiC MPS diodes are shown in Fig. 6, where Fig. 6(a) and (b) show the I-V curves in low current regime and high current regime, respectively. The forward voltage of hexagonal cell designs (Design B-D) are lower than that of the stripe cell design (Design A). From Fig. 6(b), the pn junction activation can be observed in the high current regime.

The experimental results of $V_F$ and $V_{PN}$ are extracted and compared with the simulation results in Fig. 7(a). Design A has the optimal stripe cell design with $W = 14$ $\mu$m and $S = 16.5$ $\mu$m, and the experimental result of Design A is consistent with the simulation results. On the other hand, Design B has the optimal hexagonal cell design with $W = 16$ $\mu$m and $S = 16.5$ $\mu$m, and the experimental result is very close to the simulation result except for the slightly larger $V_{PN}$ (6 V increased to 7 V). The $V_F$ of Designs A, B, C, and D are 1.62, 1.52, 1.59, and 1.56 V, respectively. Design A (the stripe design) shows the highest $V_F$. Designs C and D (the hexagon designs with PSL) show a little higher $V_F$ when compared to Design B (the hexagon design without PSL), as extra P+ areas (plasma spreading layers) are added in the layout.

The experimental results of the reverse I-V characteristics of the four SiC MPS diodes are shown in Fig. 7(b). Thanks to the JBS cell designs with narrow Schottky width (3 $\mu$m) and the enhanced electric field shielding effects, the four MPS diodes all show very low leakage current (<0.1 $\mu$A at 1200 V).

## IV. Surge Current Capability and Analysis

After the static characterization, single pulse surge current tests are carried out on the four SiC MPS diodes to analyze and compare the surge current capability of the diodes. As shown

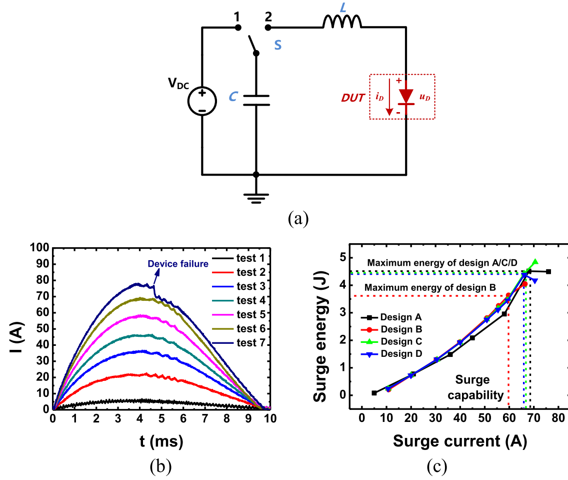


Fig. 8. (a) Schematic view of the test circuit. (b) Current waveforms of single pulse surge current tests for Device A. (c) Summary of energy $E_{surge}$ at different surge currents for the four SiC MPS diodes.

in Fig. 8(a), a half-sinusoidal current pulse with a pulse width of 10 ms is generated by the resonant circuit consisting of the capacitor and the inductor. The current peak amplitude of the current pulse can be adjusted by the DC voltage. During each test, current pulse is applied on the device while the device voltage and current waveforms are recorded. The peak current amplitude is increased gradually until the device fails. Fig. 8(b) show the current waveforms of Design A diode. The peak surge current is increased up to 75 A from test 1 to 7. At the last test (test 7), the current waveform shows a collapse at $t = 4.7$ ms. This represents the occurrence of the device failure. Similarly, device Design B undergoes several surge tests and get failed at a surge current of 65 A. For device Design C and D, they get failed at surge current of ~70 A.

The energy dissipation can be calculated from the current and voltage waveforms. The summary of surge energy at different surge current for the four MPS didoes are shown in Fig. 8(c). The last point of the plot corresponds to the device failure for each diode. And, the surge current at the second last test point can be regarded as the surge current capability. It is shown that device Design B has the lowest surge current capability (65A), and devices Designs A, C, and D have relatively higher surge capability (between 65 and 70 A). In addition, the maximum surge energy before failure can be extracted from the plot in Fig. 8(c). The maximum energy the device can safely dissipate is only 3.63 J for device Design B, while other three devices can dissipate 24% higher energy without device failure (~4.5 J). When comparing Designs C and D, they show minor difference for the surge energy dissipation and surge capability, which means that the different configuration of plasma spreading layers (i.e., P+ cross lines or diagonal lines) has minor effects on the surge current capability.

To analyze the effect of plasma spreading layers on the surge current capability of the MPS didoes, more diodes with different P+ ratios for each design group (stripe cell design, hexagonal cell design without PSL, and hexagonal cell design with PSL)

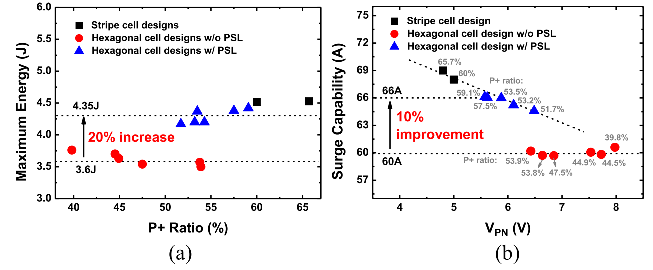


Fig. 9. (a) Summary of maximum energy that device can safely dissipate during surge current test for the three design groups. (b) Dependence of surge current capability of SiC MPS diodes on the pn junction turn-ON voltage $V_{PN}$.

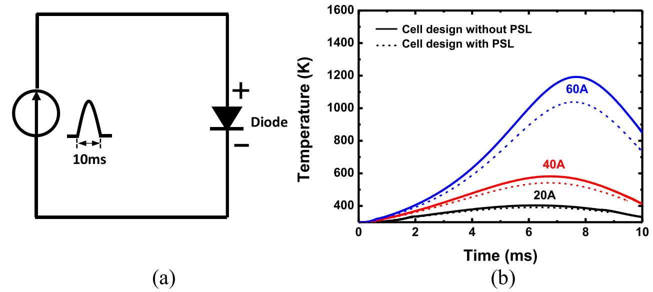


Fig. 10. (a) Setup of the single pulse surge current simulation, a half-sinusoidal pulse current source is connected to the diode. (b) Simulation results of the junction temperature transients during the surge pulse for the cell design without PSL and the cell design with PSL.

are fabricated and tested. The maximum energy from the surge current test results for each design group are summarized and plotted versus P+ ratio in Fig. 9(a). It is shown that the maximum energy for the group of non-PSL hexagonal cell design is the lowest, which is only 3.6 J. For the groups of stripe cell design and hexagonal cell design with PSL, the maximum energy that can be safely dissipated by the device is improved by 20% (~4.35 J).

The root cause of the device failure under surge current conditions is the highest junction temperature inside the device. It has been reported that the aluminum pad was melted when the surge current exceeded the maximum which is defined as the surge current capability [7]. The simulation of single pulse surge current is carried out to demonstrate the junction temperature difference under the same load current with different cell designs. As shown in Fig. 10(a), a half-sinusoidal pulse current source with pulse width of 10 ms is connected to the diode. The current amplitude is set the same (20, 40, and 60A) for the cell design without PSL and the cell design with PSL. The two cell designs have the same P+ region width ($W$) and spacing ($S$) parameters. The simulation results of the junction temperature transients during the surge pulse are shown in Fig. 10(b). It is shown that the peak junction temperature of the cell with PSL is lower than that of the cell without PSL under the same surge current. When the surge current is increased from 20 to 40 and 60A, the highest junction temperature difference between the two cell designs are 12, 40, and 155K, respectively.

With the help of the plasma spreading layers, the bipolar current conducted through the wide P+ region (i.e., wide P+ stripes or hexagonal P+ islands) during the surge pulse can spread through the interconnection between the P+ stripes / islands. For the stripe cell design, the P+ stripes are connected at the end [see Fig. 4(a)], which means all the P+ stripes are connected in a network which is equivalent to plasma spreading layers. The unbalanced current distribution and localized heating can be alleviated. Thus, the junction temperature is decreased with the same current condition. In other word, the new structure needs more surge energy dissipation to gain the same junction temperature. Therefore, the maximum energy of the new designs can be improved by ~20% by adding the PSL.

Fig. 9(b) summarizes the surge current capability for the three design groups. Different P+ ratio design results in different pn junction turn-ON voltage. It is shown that, the higher P+ ratio is designed, the lower $V_{PN}$ is obtained for each group. A decreased $V_{PN}$ can result in a slight increase of surge current capability for the groups of stripe cell design and hexagonal cell with PSL. As the maximum energy is almost the same for these devices, the lower $V_{PN}$ can contribute to a lower maximum voltage/energy dissipation and thus a higher surge current capability can be achieved. For the non-PSL hexagonal cell design group, $V_{PN}$ has minor impacts on the surge current capability. On the other hand, the stripe cell design exhibits the highest surge current capability (~69 A) among the three groups. However, hexagonal cell is preferable for MPS diode design as it features a lower $V_F$ [see Fig. 7(a)]. By adding PSL, due to the 20% improvement in maximum allowed energy, the hexagonal cell can obtain a surge current capability (66 A) 10% higher than the traditional non-PSL hexagonal cell design (60 A), which is close to that of the stripe cell design.

As discussed in Section III, PSL bring the degradation of $V_F$ for the normal current conduction operation [see Fig. 7(a)]. However, if the PSL structure is optimized, i.e., designing cross lines instead of diagonal lines and reducing PSL numbers, the degradation of $V_F$ can be minimized. Therefore, an improved tradeoff between the $V_F$ and surge current capability is achieved for SiC MPS diode with the proposed new structure.

## V. Conclusion

In this article, a novel structure design concept (plasma spreading layers, PSL) is introduced into the SiC MPS diode which can significantly improve the surge current capability. While the existed technology only focuses on the contact topography and layout design to get a balance between the forward voltage drop and surge current capability, this study put emphasis on the improvement of bipolar current spreading and the energy dissipation capability. The proposed concept can provide a new method for the device designer to achieve a better tradeoff relation between the device forward voltage drop at nominal current and surge capability. In this article, 1.2-kV SiC MPS diodes with two types of plasma spreading layers are designed and fabricated, their forward characteristics and surge current capability are compared to traditional stripe cell design and hexagonal cell design. The results show that a 20% increase of maximum allowed energy is achieved by the new structure design, which results in a 10% improvement of the surge current capability.

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