Impedance-Based Analysis of Digital Control Delay in Grid-Tied Voltage Source Inverters

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***Abstract*—Digital control delay is studied as one of the leading factors causing instability in grid-tied voltage source inverter (VSI) systems. However, how this delay affects the small-signal output impedance of the VSI and how the change in impedance shape further influences the system stability are still not clear. This article, for the first time, thoroughly analyzes the impact of delay on the *dq*-frame output impedance of the VSI operating in both the single current loop control mode and the dual-loop control mode. It is found that when delay is considered, a distinct magnitude drop and a phase rise always exist at the high-frequency area of the impedance, which is named the "impedance trough." By studying the *dq*-frame output impedance of the VSI, the origin of the impedance trough, and its analytical relationships with the current loop dynamics, voltage loop dynamics, and delay values are unveiled. Meanwhile, the influence of the impedance trough on the stability of the grid-tied VSI system under these two control modes is evaluated through *d–d* channel impedance matching and generalized Nyquist criterion (GNC). It is demonstrated that the joint effects of delay and control parameters result in the impedance mismatch between the grid and the VSI, which is the root cause of high-frequency oscillations in the grid-tied system. Finally, experimental results verify the analysis.**

***Index Terms*—Delay effects, impedance, inverters, stability.**

I. Introduction

DIGITAL control is increasingly applied in modern power electronic converters due to its superior capability to operate a complex algorithm, the possibility of reprogramming, and the reliability against ambience variations compared with the traditional analog control [1], [2]. However, in a digital control system, there inherently exists a time delay originated from analog-to-digital (AD) conversion, digital processor computation, and pulsewidth-modulated (PWM) generation [3]. For symmetrical-regular modulation, there lasts one carrier cycle T_s from the sampling instant to the update instant [4]. And the zero-order hold (ZOH) effect keeps the duty ratio constant after the update, which approximates to half T_s [5], thereby the total delay value $T_{\rm del}$ is widely accepted to be $1.5T_s$ [6].

Time delay would introduce a phase lag into the control loop of the converter [7], which tends to reduce the phase margin (PM) of the control loop and the control bandwidth, degrading system control performance [8]. Thereby, solutions to reduce the time delay have been proposed. The most direct way is to apply the asymmetrical modulation with double update, and then $T_{\rm del}$ is reduced to $0.75T_s$ [9]. In addition, due to the improvement of the microprocessor, AD conversion and computation durations are reduced dramatically, and a reduced computation delay method is proposed by shifting the sampling instant to the update instant [10]. As the computational delay decreases, the accuracy of the PWM modulation becomes more important. Recently it has been reported that there exists a deviation between the *s*-domain ZOH model and actual *z*-domain model. To improve the accuracy of *s*-domain model, a compensation strategy is proposed [11].

In recent years, studies on the delay effect have shifted to the stability analysis of current control of grid-tied voltage source inverters (VSIs) with *LCL* filters [12]–[15]. In [12], a discrete *z*-domain small-signal model of the inverter with delay effects is derived to predict the stability of the current controller. In [13], a concept of critical *LCL* filter resonance frequency, which equals one-sixth of the sampling frequency ($f_s/6$) is introduced. And it documents that if the resonance frequency is exactly equal to $f_s/6$, the system will always be unstable regardless of the capacitor current feedback coefficient. Zou *et al.* [14] and Wang *et al.* [15] compare the delay effects on the converter-side and grid-side current feedback control of *LCL* filters, and then obtain the stable range of time delay. Overall, it could be seen that current works on the delay effect are mainly based on the system loop gain, which analyze the influences of phase lag on the current control loop.

Although the system loop gain-based method is available to accurately assess the stability of the grid-tied VSI system, the impedance-based approach, which was originally introduced for the design of input filters in dc–dc converters [16], provides a more convenient tool to analyze the ac grid-tied system stability [17], [18]. Over the past decades, impedance-based stability analysis of grid-tied VSI systems has been a research concern, mainly focusing on factors such as the *LCL* filter resonance in current control [19]–[22], multiple converters and weak-grid condition [23]–[26], phase-locked loop (PLL) [27]–[29], and dc-link voltage loop dynamics [30]. The influences of PLL dynamics on VSI output impedance shape and system stability

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are analyzed in the $\alpha\beta$-frame [27] and the *dq*-frame [28], [29], respectively. In [30], the influence of dc-link dynamics on the VSI *dq*-frame output admittance is evaluated. However, how digital control delay impacts the impedance shape and how a change in the impedance shape is related to the system stability are not clear yet.

A few research works have studied the influences of digital control delay from the perspective of the impedance-based method. Via the passivity-based analysis, it is revealed in [31] and [32] that time delay constitutes a frequency-dependent term in the VSI total output admittance, which could make the total admittance have a negative real part. This negative real part will introduce a negative damping effect into the system, resulting in system instability. In [33], the delay effect on the grid-tied photovoltaic (PV) system is analyzed by establishing a single-input single-output (SISO) impedance model. And it is verified that as delay increases, the system stability margin declines. However, these works to study the delay effect are all based on the equivalent SISO model, which assumes the original three-phase system symmetrical and balanced by neglecting the dynamics of PLL and dc link. Admittedly, this assumption is feasible since the impact of delay is located around the high-frequency area, but the SISO model is not an accurate description of the original multi-input multi-output system after all. Thus, it is still necessary to establish a *dq*-frame or an $\alpha\beta$-frame impedance model when considering PLL and dc-link voltage loop.

Interestingly, in quite a few of the above-listed papers on VSI impedance modeling with delay, it is observed from the predicted models and measured results that a sudden magnitude drop and a phase rise always exist at around one-sixth switching frequency of the output impedance [20], [21], [27]–[29]. Nevertheless, these works hardly notice this phenomenon, let alone link it to the delay effect. This phenomenon is first pointed out in a recent publication that examines the impacts of delay on the VSI sequence impedance [34]. It indicates that as the delay value increases, the magnitude drop and phase rise deteriorate. The relation between the impedance shape change and the system stability is also shown. But this article presents the phenomenon and analyzes system stability only through parametric case studies, which lacks in-depth qualitative investigations (e.g., the origin, frequency location, variation rules to control parameters, etc.). Meanwhile, as delay varies, it is unclear whether the instability of the system is due to the standalone inverter or the impedance mismatch. Besides, so far, the analysis of delay effect on the impedance shape and system stability in the *dq*-frame is still absent.

To cope with these issues, the main contributions of this article are summarized as follows.

1) The origin and frequency characteristic of the impedance magnitude drop and the phase rise phenomenon, (i.e., the impedance trough) are thoroughly illustrated.
2) The joint effects of delay and control parameters on the *dq*-frame output impedance in both the single current loop control mode and the dual-loop control mode with outer dc-link voltage control are clarified.
3) The impacts of the delay-caused impedance trough on the stability of the grid-tied VSI system in these two control modes are evaluated. More specifically, the root cause of the high-frequency oscillations is unveiled.

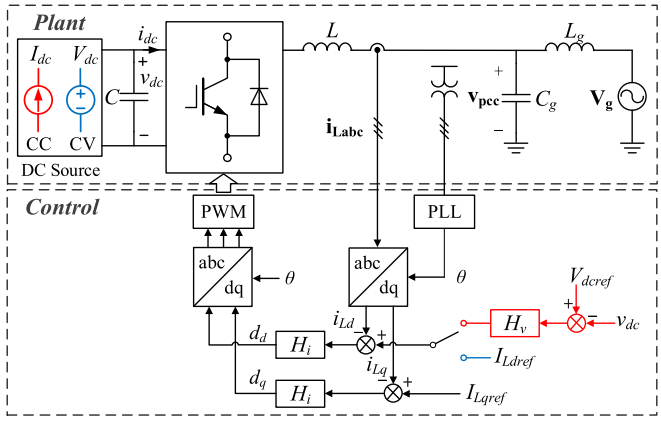


Fig. 1. Single-line equivalent circuit and control system of a three-phase VSI with constant dc voltage source or current source input.

TABLE I
MAIN PARAMETERS OF THE STUDIED VSI

Symbol	Description	Value (p.u.)
P	Active power	2 kW (1)
Q	Reactive power	0 Var (0)
V_g (rms)	Grid voltage (phase-to-phase)	110 V, 50Hz (1, 1)
V_{dc}	DC voltage	400 V (3.61)
C	DC-link capacitor	1500 μF (0.35)
L	Inverter output inductor	3.5 mH (0.18)
L_g	Grid inductor	1.75 mH (0.09)
C_g	Grid capacitor	15 μF (35.09)
T_s	Sampling period	100 μs (0.005)
f_s	Switching frequency	10 kHz (200)
$k_{ip}+k_{ii}/s$	PI controller of current loop	0.1+10/s
$k_{vp}+k_{vi}/s$	PI controller of voltage loop	1+10/s
$k_{pllp}+k_{plli}/s$	PI controller of PLL	0.5+50/s

This article is organized as follows. In Section II, the *dq*-frame impedances of VSI with and without delay are compared, and the impedance trough is introduced. The origin and the characteristics of the trough are illustrated in Section III. Section IV discusses the joint effect of delay and control parameters on the VSI output impedance shape in both single current loop and dual-loop control modes. In Section V, the impacts of the impedance trough and grid impedance on system stability are analyzed. The experimental results are presented in Section VI. Finally, Section VII concludes this article.

II. SYSTEM STUDIED AND ITS OUTPUT IMPEDANCE

In this article, a three-phase, two-level VSI operating in the single current loop control mode and the dual-loop control mode with dc-link voltage control is studied. A single-line equivalent circuit of the grid-tied system is depicted in Fig. 1, and the parameters are listed in Table I. The dc link of the VSI is supplied by a bulk capacitor C in parallel with either a constant dc voltage source $V_{\rm dc}$ or a constant dc current source $I_{\rm dc}$, which corresponds

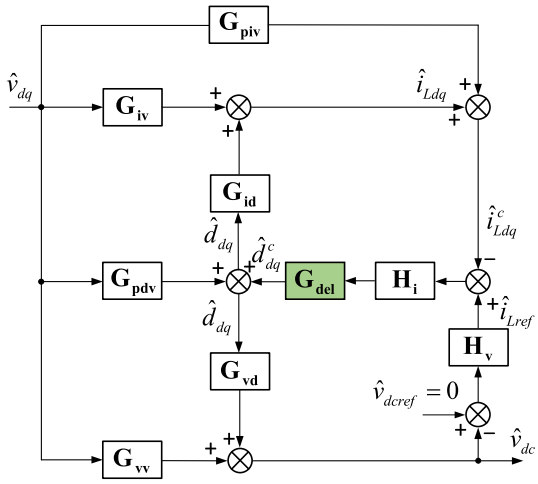


Fig. 2. Small-signal model of VSI in the dual-loop control mode.

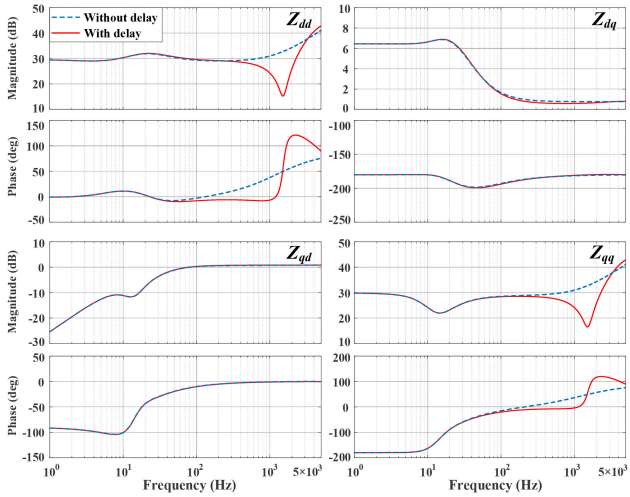


Fig. 3. Comparison of VSI output impedance with and without delay in the dual-loop control mode.

to the two control modes, respectively. Through an output filter inductor L, the ac side of the VSI is connected to a weak grid with an L–C type grid impedance. The inverter-side current is controlled in the dq-frame, and the phase signal is generated via PLL. For the dual-loop control mode, d-axis current reference is generated by the dc voltage loop. In both the voltage loop and the current loop, simple proportional-integral (PI) regulators are adopted, which are denoted by H_v and H_i, respectively.

The dq-frame small-signal model of the VSI with PLL and dc-link dynamics, which has already been well-established in existing publications [24], [28], is redrawn in Fig. 2. This model is composed by the open-loop power stage, the inner current control loop, and the outer voltage loop. In Fig. 2, a superscript "c" is added to distinguish the variables in the control system from those in the power stage. All of the transfer functions are in a second-order matrix form, of which the specific expressions could also be referred to in [24] and [28]. Among them, $\mathbf{G_{iv}}$ denotes the open-loop output impedance of inverter, $\mathbf{G_{vv}}$ is the open-loop transfer function from ac voltage to dc voltage, $\mathbf{G_{vd}}$ indicates the transfer function from duty ratio to dc voltage, $\mathbf{G_{id}}$ represents the transfer function from duty ratio to the inductor current, and $\mathbf{G_{piv}}$ and $\mathbf{G_{pid}}$ denote the relations between the inductor current and duty ratio in the control system and the ac voltage in the power stage, respectively. Besides, $\mathbf{G_{del}}$ is the digital control delay matrix, which is expressed as

$$\mathbf{G_{del}} = \begin{bmatrix} e^{-T_{\mathrm{del}}s} & 0 \\ 0 & e^{-T_{\mathrm{del}}s} \end{bmatrix}. \tag{1}$$

From Fig. 2, the output admittance of the VSI can be deduced as

$$\mathbf{Y_o} = (\mathbf{I} + \alpha \mathbf{G_{del}} \mathbf{H_i})^{-1} [\mathbf{G_{iv}} - \alpha (\mathbf{G_{del}} \mathbf{H_i} \mathbf{H_v} \mathbf{G_{vv}} - \mathbf{G_{pdv}} + \mathbf{G_{del}} \mathbf{H_i} \mathbf{G_{piv}})] \tag{2}$$

where $\alpha = \mathbf{G_{id}}(\mathbf{I} + \mathbf{G_{del}} \mathbf{H_i} \mathbf{H_v} \mathbf{G_{vd}})^{-1}$.

And then, by performing an inversion on (2), the dq-frame output impedance is obtained

$$\mathbf{Z_o} = \mathbf{Y_o}^{-1}. \tag{3}$$

The Bode diagrams of VSI output impedance $\mathbf{Z_o}$ with and without delay are compared in Fig. 3. It could be observed that in Z_{dd} and Z_{qq}, when delay is considered, a distinct magnitude drop and a phase rise appear at around 1 kHz. This phenomenon is just like a trough from the shape of the impedance magnitude, which thereby is named impedance trough. However, in Z_{dq} and Z_{qd}, the impedance trough does not exist since delay plays a dominant role in the d-axis and the q-axis current control loops, whereas it has little impact on the coupling terms.

Fig. 3 reveals that the impacts of digital control delay are located in the high-frequency area, whereas PLL only influences the low-frequency segment of Z_{qq}. Hence, the dynamics of PLL could be neglected herein. In this case, the output impedance could be simplified, which is defined as follows:

$$\mathbf{Z_{ov}} = (\mathbf{G_{iv}} - \alpha \mathbf{G_{del}} \mathbf{H_i} \mathbf{H_v} \mathbf{G_{vv}})^{-1} (\mathbf{I} + \alpha \mathbf{G_{del}} \mathbf{H_i}). \tag{4}$$

For the single current loop control mode VSI, the output impedance is defined as follows:

$$\mathbf{Z_{oc}} = \mathbf{G_{iv}}^{-1} (\mathbf{I} + \mathbf{G_{id}} \mathbf{G_{del}} \mathbf{H_i}). \tag{5}$$

III. Origin and Characteristics of Impedance Trough

Mathematically, delay $G_{\mathrm{del}} = e^{-T_{\mathrm{del}}s}$ is an exponential function with a constant modulus of 1 and a varied phase angle. The Bode plot of G_{del} is shown in Fig. 4(a), of which the magnitude is 0 dB and the phase declines linearly as the frequency increases. In addition, the characteristic of G_{del} could be more intuitively illustrated by means of complex plane representation. As shown in Fig. 5(a), delay G_{del} is intrinsically a clockwise rotating unit circle with a radius of 1. As frequency increases, the phase of the circle gradually declines.

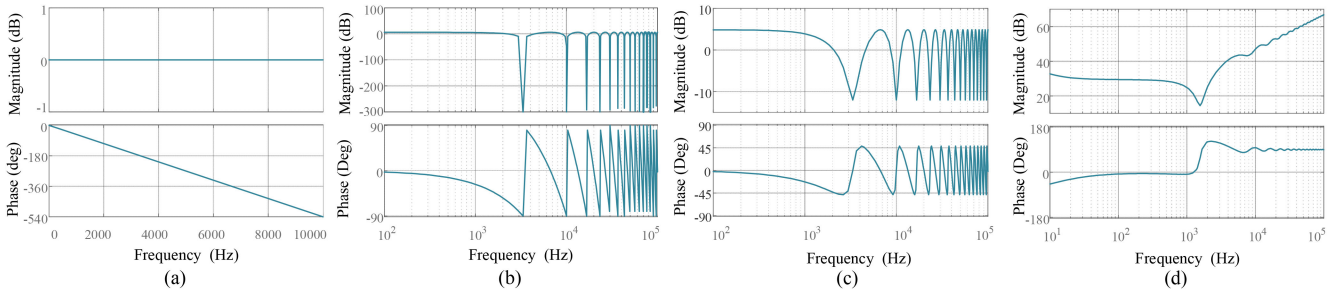


Fig. 4. Bode plot of (a) $G_{\rm del}$ in linear frequency axis, (b) G_1, (c) G_2, and (d) *d–d* channel impedance Z_{dd_c} of VSI with single current loop.

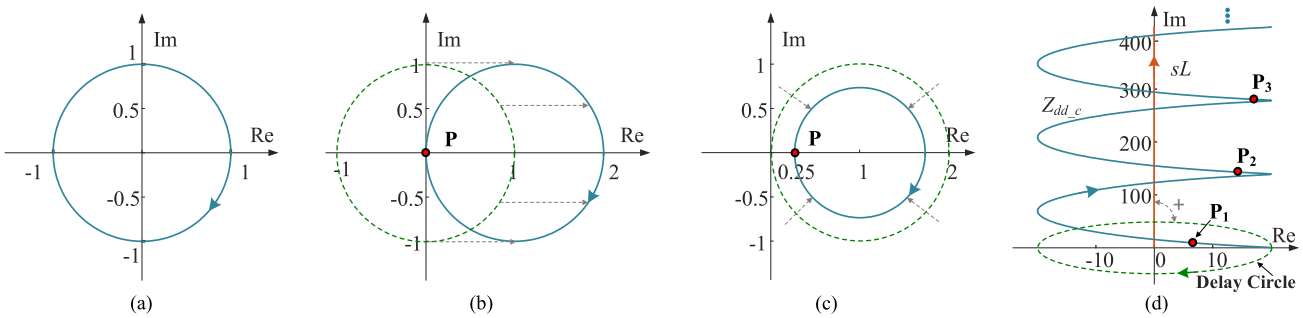


Fig. 5. Complex plane representation of (a) $G_{\rm del}$, (b) G_1, (c) G_2, and (d) *d–d* channel impedance Z_{dd_c} of VSI with single current loop.

The loop gain of the inner current control loop in Fig. 2 is

$$\mathbf{T_{cl}} = \mathbf{G_{id}} \mathbf{G_{del}} \mathbf{H_i}. \tag{6}$$

In (6), the relationship between $\mathbf{G_{del}}$ and the other two transfer functions is direct multiplication. Thus, delay could only bring phase lag into the current control loop.

Nevertheless, in the expression of VSI output impedance (2), (4), (5), $\mathbf{G_{del}}$ is not only multiplied with other plants, but it is also added to an identity matrix $\mathbf{I}$ with a constant of 1 in the main diagonal. Importantly, the following analyses are based on the elements in the main diagonal of the matrixes.

Once $G_{\rm del}$ is added to a constant 1, it becomes

$$\begin{aligned} G_1 &= 1 + e^{-T_{\rm del} s} \\ &= 1 + \cos\left(\omega T_{\rm del}\right) - j \sin\left(\omega T_{\rm del}\right). \end{aligned} \tag{7}$$

From (7), it could be seen that G_1 is a frequency-dependent and periodic function. And as long as

$$\omega T_{\rm del} = (2k+1)\,\pi, \quad k = 0, 1,\ 2 \ldots \tag{8}$$

$G_1 = 0$. The Bode plot of G_1 is depicted in Fig. 4(b). It could be seen that a sharp magnitude drop occurs periodically, and the phase rises abruptly from –90° to 90° at this frequency point. This could be more vividly presented via the complex plane representation of G_1 in Fig. 5(b), which is a unit circle centered on (1, *j*0) point. Whenever the curve rotates to the origin point *P*, the modulus decreases to zero, and the phase jumps abruptly from –90° to 90°. The frequency at point *P* is exactly the solution to (8), which is defined as follows:

$$\omega_p = \frac{2k+1}{T_{\rm del}}\pi, \quad k = 0, 1, 2 \ldots. \tag{9}$$

If $G_{\rm del}$ is not only in sum with a constant but also in multiplication with an arbitrary constant λ, then $G_{\rm del}$ becomes

$$G_2 = 1 + \lambda e^{-T_{\rm del} s} \tag{10}$$

and the minimum value of G_2 becomes $1 - \lambda \cdot \mathrm{sgn}(\lambda)$. For example, if λ equates to 0.75, then the minimum value is 0.25. It can be seen from the Bode plot of G_2 in Fig. 4(c) that there exists a similar periodic magnitude drop as in G_1, whereas the lower limit of the drop is countable to be –12 dB. The complex plane representation of G_2 is also a circle centered on the (1, *j*0) point, whereas the radius of the circle is reduced to 0.75. In Fig. 5(c), throughout the circle, point *P* owns the minimum modulus value 0.25, and whenever the curve rotates through point *P*, the modulus first decreases and then increases, posing a trough. The minimum modulus value of 0.25 exactly corresponds to the lower limit of 12 dB in Fig. 4(c).

From the analyses of G_1 and G_2, once $G_{\rm del}$ is added to a constant, then both the magnitude and phase of the Bode plot will change significantly, instead of a simple phase lag. Further analysis of the VSI output impedance in (4) and (5) reveals that in addition to the simple sum operation with constants, operations with *s*-functions and a matrix inversion for $G_{\rm del}$ also exist. In order to mathematically explain the origin of the impedance trough, it is necessary to obtain the analytical expression of the impedance first.

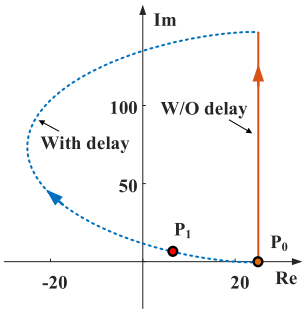


Fig. 6. Comparison of Z_{dd_c} with and without delay in the complex plane.

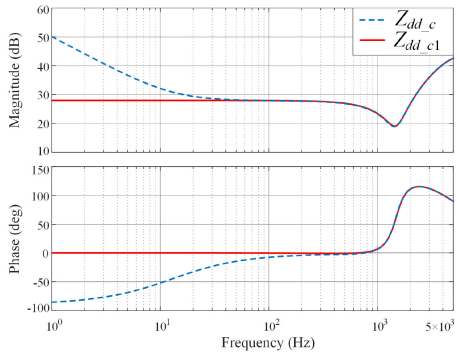


Fig. 7. Impact of the integral operator k_{ii}/s on *d–d* channel impedance Z_{dd_c}.

To ensure a more intuitive understanding of the origin of the impedance trough, the analysis starts from the simpler single current control mode VSI impedance $\mathbf{Z_{oc}}$. The *d–d* channel element of $\mathbf{Z_{oc}}$ is defined as Z_{dd_c}, of which the analytical expression is deduced as follows:

$$Z_{dd\_c} = sL + V_{\rm dc}\left(k_{ip} + \frac{k_{ii}}{s}\right)e^{-T_{\rm del}s}. \tag{11}$$

It could be observed from the Bode plot of Z_{dd_c} in Fig. 4(d) that although gradually attenuating, a magnitude drop and phase rise phenomenon still periodically emerge. This is exactly the impedance trough defined above. According to (11), Z_{dd_c} is composed of a passive term inductor sL, and the active term that contains delay. In the complex plane, sL is a straight-line on the imaginary axis with a 90° angle, and the active term approximates to a circle since the integral operator will be small enough as frequency increases. Combining the straight line sL and the "delay circle," Z_{dd_c} becomes the periodic arches rotated counterclockwise by 90°, as shown in Fig. 5(d).

On each arch, there always exists one point closest to the origin, which is labeled as P_n (n denotes the order of the period). The point P_n corresponds exactly to the bottom point of each impedance trough in the Bode plot in Fig. 4(d). When the curve passes through P_1, the modulus of the curve first decreases sharply, then increases, and the phase increases from near 0° to larger than 90° in a short frequency range. However, as frequency increases, when the curve reaches to P_2 and P_3, the changes in magnitude and phase gradually become slight.

It is worth mentioning that the accuracy of the small-signal linearization method is guaranteed only up to half-switching frequency. Hence, only the first impedance trough in Fig. 4(d) and the point P_1 in Fig. 5(d) are valid.

Fig. 6 further illustrates the effect of delay on the impedance by comparing Z_{dd_c} with and without delay. If delay is not considered, then the curve is a straight-line just shift to the right with a distance of $V_{\rm dc}k_{ip}$, and the point closest to the origin $\rm P_0$ is exactly the starting point. If delay is taken into account, then the curve will bend due to the delay circle, and the point closest to the origin moves to P_1.

IV. Parameter Analysis for the Impedance Trough

In this section, the joint effects of delay and control parameters on the output impedance of VSI in both single current loop and dual-loop control modes are elaborated.

A. Single Current Loop Control Mode

In (11), it could be seen that for Z_{dd_c}, the radius of the delay circle is closely related to the control parameters k_{ip} and k_{ii}, whereas the rotating speed is determined by delay time $T_{\rm del}$. However, the impact of the integral operator k_{ii}/s is weak, since the integral operator dominates in the low-frequency area, whereas the trough is located in the high-frequency area. Thus, the *d–d* channel impedance Z_{dd_c} could be further simplified to

$$Z_{dd\_c1} = sL + V_{\rm dc}k_{ip}e^{-T_{\rm del}s}. \tag{12}$$

The Bode plots of Z_{dd_c} and Z_{dd_c1} are compared in Fig. 7. It is verified that the impedance trough is hardly influenced by the integral operator. Hence, this simplification is reasonable if only the impedance trough is studied.

The frequency location of the impedance trough in Fig. 7 could be calculated by performing a derivative operation on the modulus of Z_{dd_c1}, which is defined as follows:

$$M = \sqrt{\left[V_{\rm dc}k_{ip}\cos(\omega T_{\rm del})\right]^2 + \left[\omega L - \sin(\omega T_{\rm del})\right]^2}. \tag{13}$$

By solving the following derivative equation:

$$\frac{dM}{d\omega} = 0 \tag{14}$$

the extreme point should have been obtained. However, due to the triangular functions in M, an analytic solution for (14) does not exist. To simplify, the first-order Padé approximation of delay $G_{\rm del}$ is applied

$$G_{\rm del} = \frac{1 - 0.5T_{\rm del}s}{1 + 0.5T_{\rm del}s}. \tag{15}$$

Then, Z_{dd_c1} is further simplified to

$$Z_{dd\_c2} = sL + V_{\rm dc}k_{ip}\frac{1 - 0.5T_{\rm del}s}{1 + 0.5T_{\rm del}s}. \tag{16}$$

By calculating the modulus of Z_{dd_c2}, and solving (14), the extreme point frequency of the trough ω_c is obtained as follows:

$$\omega_c = \left(\frac{(2k_{ip}LT_{\rm del}V_{\rm dc})^{\frac{1}{2}} - L}{4LT_{\rm del}^2}\right)^{\frac{1}{2}}. \tag{17}$$

In (17), it could be seen that ω_c increases as output inductor L, dc-link voltage $V_{\rm dc}$, or the current loop proportional gain k_{ip} increase, whereas it decreases as delay $T_{\rm del}$ increases. Among

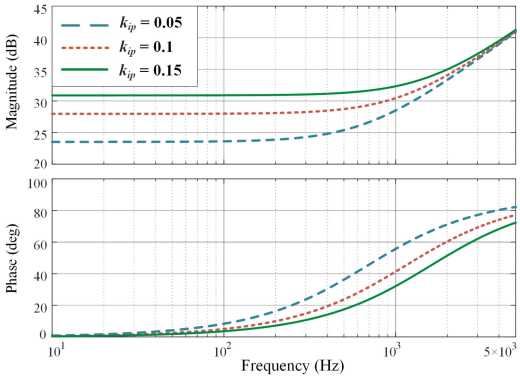


Fig. 8. Bode plots of Z_{dd_c1} without delay when $k_{ip} = 0.05$, 0.1, and 0.15.

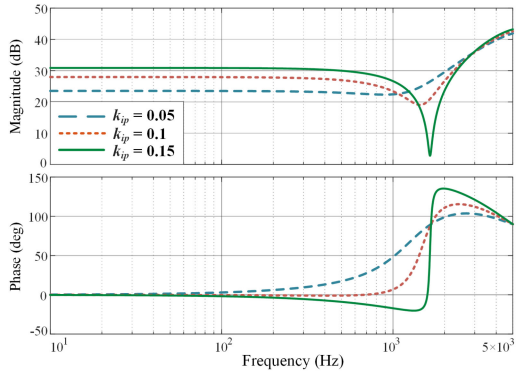


Fig. 9. Bode plots of Z_{dd_c1} with delay when $k_{ip} = 0.05$, 0.1, and 0.15.

them, L and $V_{\rm dc}$ are constant power-stage values, which will not be further analyzed here.

First, three sets of k_{ip} (i.e., 0.05, 0.1, and 0.15) are chosen. If delay is not considered, then the Bode plots of Z_{dd_c1} in (12) are shown in Fig. 8. Within the bandwidth of the current loop, Z_{dd_c1} behaves as a constant resistor characteristic. And as k_{ip} increases, the magnitude becomes larger, whereas the phase rises more smoothly. For all of these cases, the phase is limited to the 90° range.

Under the same k_{ip} conditions, if delay is considered and fixed at 150 μs, then the Bode plots of Z_{dd_c1} are redepicted in Fig. 9. Compared with Fig. 8, it could be seen that a disparate impedance trough appears when delay is considered.

As k_{ip} increases, the impedance trough gradually becomes deeper and sharper, and shifts to a higher frequency area, which is consistent with the analysis of ω_c in (17). Meanwhile, for all three cases, the phase at the trough rises steeply and exceeds 90°. Specifically, when $k_{ip} = 0.15$, the phase rises abruptly from –20° to 135°.

The severe impedance trough in Fig. 9 could be more directly explained via the complex plane representation in Fig. 10. Based on the compound principle in Fig. 5(d), as k_{ip} increases, the radius of the delay circle becomes larger. As a result, the curvature of the composite arch increases. In Fig. 10, on each curve, there exists one point closest to the origin point, labeled P_1, P_2, and P_3, respectively, and R_1, R_2, and R_3 represent the

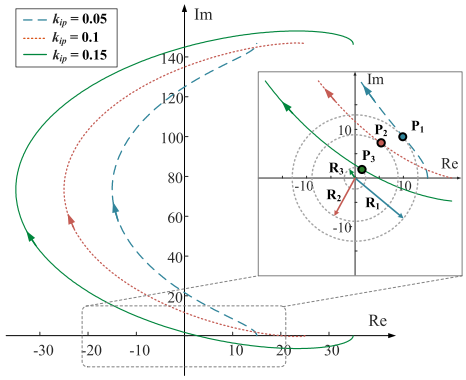


Fig. 10. Complex plane representations of Z_{dd_c1} with delay when $k_{ip} = 0.05$, 0.1, and 0.15.

minimum distances. Evidently, R_3 is much smaller than R_1 and R_2, thus resulting in a sharp magnitude drop in the Bode plot. Meanwhile, around point P_3, the phase changes rapidly from a negative degree to larger than 90°. Once the phase increases over 90°, the impedance will enter the second quadrant with a negative real part, behaving as a negative damping effect.

Correspondingly, it is worth observing the change of current loop gain $\mathbf{T_{cl}}$. In single current loop mode, the *d–d* channel loop gain is defined as T_{cl} and derived as

$$T_{cl} = \frac{sV_{\rm dc}\left(k_{ip} + \frac{k_{ii}}{s}\right)e^{-T_{\rm del}s}}{s^2L + \omega_0^2 L} \tag{18}$$

where $\omega_0 = 314$ rad/s. As shown in Fig. 11, as k_{ip} increases from 0.05 to 0.15, the bandwidth increases from 457 to 1365 Hz, whereas the PM gradually declines from 70° to about 25°.

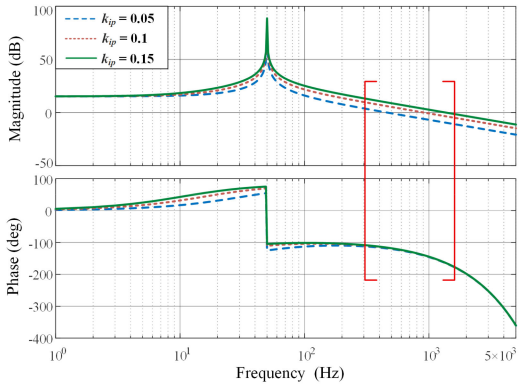
The second step is to analyze the effect of delay value. Fig. 12 presents the Bode plots of Z_{dd_c1} with three sets of $T_{\rm del}$ (i.e., 120, 150, and 180 μs), whereas k_{ip} is fixed at 0.1. As $T_{\rm del}$ augments, both the magnitude drop and the phase rise become more severe, which are similar to the case as k_{ip} increases. The difference is that the impedance trough gradually shifts to a low-frequency area.

Fig. 13 presents Z_{dd_c1} in the complex plane. As $T_{\rm del}$ increases, the rotating speed of the delay circle grows, making the minimum distance from the curve to the origin gradually decline and appear earlier at a lower frequency, which is in accordance with the trough change in Fig. 12.

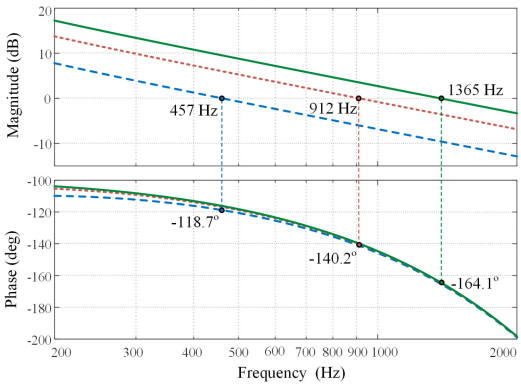
According to (18), the corresponding current loop gain T_{cl} with delay varied is depicted in Fig. 14. It is seen that no matter how $T_{\rm del}$ changes, the magnitude of T_{cl} does not change at all, whereas the phase gradually decreases due to the high-frequency phase-lag effect by delay. As $T_{\rm del}$ grows from 120 to 180 μs, the PM of the loop gain decreases by about 20°.

B. Dual-Loop Control Mode

In renewable energy plants, such as the PV plants, single-stage VSIs with a dc-link voltage control loop are widely applied. Hence, it is also necessary to analyze the effect of delay on the impedance of the VSI with dual-loop control. The *dq*-frame output impedance of the VSI in dual-loop control mode is



(a)



(b)

Fig. 11. Bode plots of T_{cl} when k_{ip} = 0.05, 0.1, and 0.15. (a) Full scale. (b) Zoom-in figure within the red border.

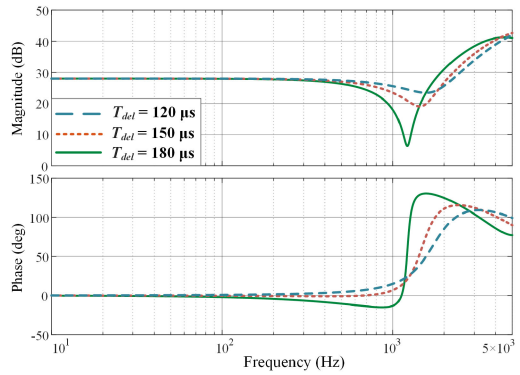


Fig. 12. Bode plots of Z_{dd_c1} when delay $T_{\rm del}$ = 120, 150, and 180 μs with k_{ip} fixed at 0.1.

deduced in (4). By neglecting the integral operator, expression of the *d–d* channel impedance could be obtained as

$$Z_{dd\_v} = \frac{D_d^2 + \beta k_{ip} e^{-T_{\rm del}s}}{sC + k_{vp}k_{ip}I_{Ld}e^{-T_{\rm del}s}} + sL \tag{19}$$

where $\beta = sCV_{\rm dc} + k_{vp}(D_dV_{\rm dc}) - D_dI_{Ld}$. In (19), both k_{ip} and k_{vp} have arithmetic operations with $G_{\rm del}$, indicating that both the current loop and the voltage loop interact with delay, shaping the impedance trough jointly.

In dual-loop control mode, the extreme point frequency is defined as ω_v, which could also be calculated by following the same steps as those outlined in Section IV-A

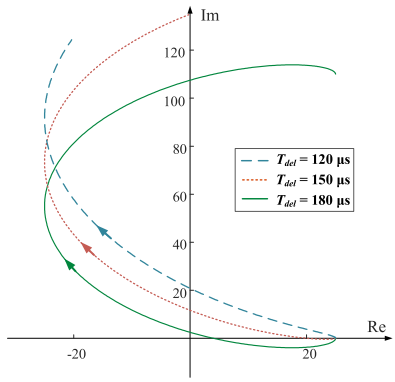
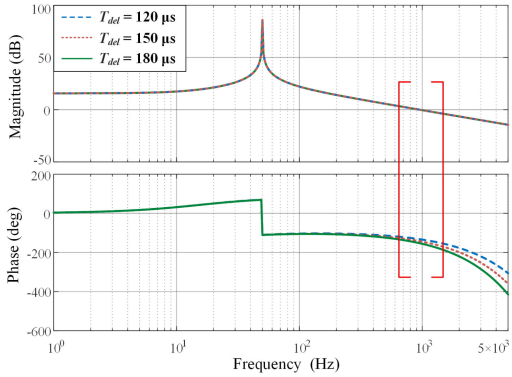
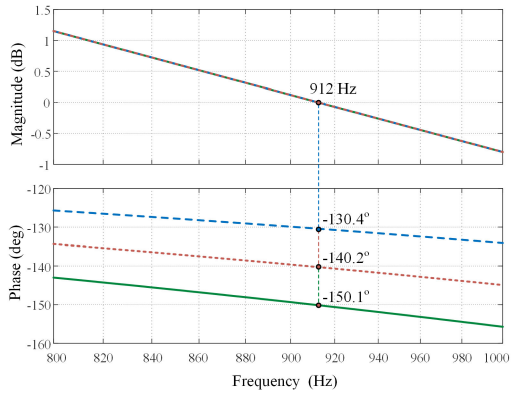


Fig. 13. Complex plane representations of Z_{dd_c1} when $T_{\rm del}$. = 120, 150, and 180 μs with k_{ip} fixed at 0.1.



(a)



(b)

Fig. 14. Bode plots of T_{cl} when $T_{\rm del}$ = 120, 150, and 180 μs. (a) Full scale. (b) Zoom-in figure within the red border.

$$\omega_v = \left(\frac{\left[2k_{ip}LT_{\rm del}\left(V_{\rm dc} + k_{vp}D_dI_{Ld}\sqrt[4]{L/C} \right) \right]^{\frac{1}{2}} - L}{4LT_{\rm del}^2} \right)^{\frac{1}{2}}. \tag{20}$$

From (20), the extreme point frequency increases as k_{ip} or k_{vp} increases, but decreases as $T_{\rm del}$ increases. Comparatively, the influence factor of k_{vp} is relatively low due to the existence of

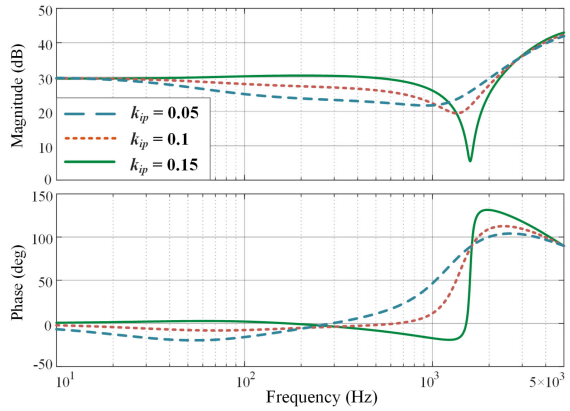


Fig. 15. Bode plots of Z_{dd_v} with three sets of gain $k_{ip} = 0.05$, 0.1, and 0.15.

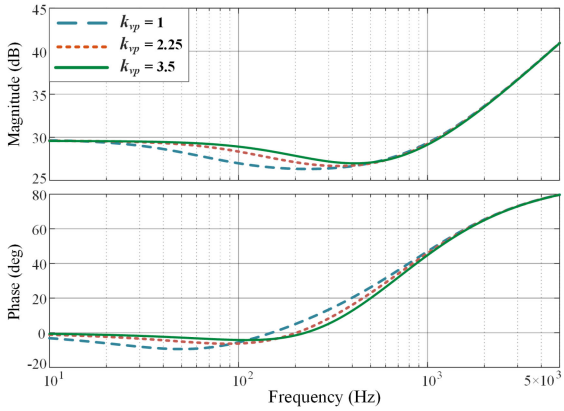


Fig. 17. Bode plots of Z_{dd_v} when $k_{vp} = 1$, 2.25, and 3.5 without delay.

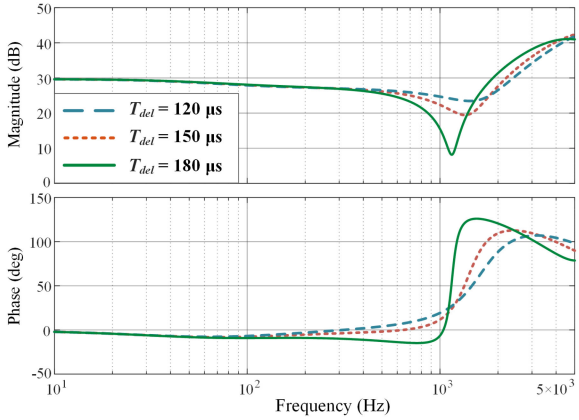


Fig. 16. Bode plots of Z_{dd_v} with delay $T_{\rm del} = 120$, 150, and 180 μs.

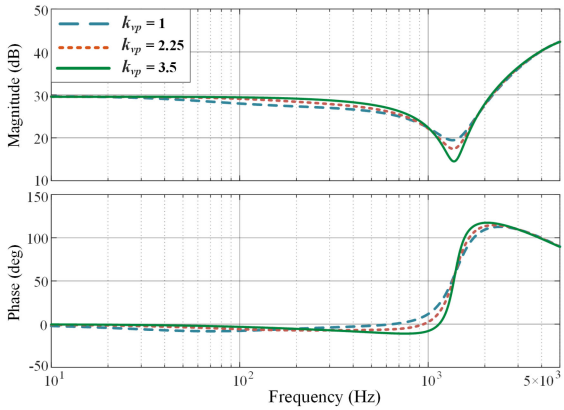


Fig. 18. Bode plots of Z_{dd_v} when $k_{vp} = 1$, 2.25, and 3.5 with delay considered.

$V_{\rm dc}$ in (20). In dual-loop control mode, the impedance trough is also influenced by current loop dynamics and delay. Therefore, the effects of k_{ip} and $T_{\rm del}$ need to be first compared with the case in the single current loop mode. Fig. 15 presents the Bode plots of Z_{dd_v} with the same sets of k_{ip} as in Fig. 9, where k_{vp} is 1 and $T_{\rm del}$ is 150 μs. Fig. 16 illustrates the Bode plots of Z_{dd_v} with varied delay values, where k_{vp} is 1 and k_{ip} is 0.1. By comparing Figs. 15 and 9, and Figs. 16 and 12, it could be manifested that the effects of current loop dynamics and delay value variations on the impedance trough are approximately identical under both control modes.

The second step is to analyze the effect of voltage loop dynamics on the impedance trough. If delay is not considered, then as k_{vp} increases from 1 to 3.5, the Bode plots of Z_{dd_v} are shown in Fig. 17, where k_{ip} is fixed at 0.1. It could be seen that within the voltage loop bandwidth, the inverter is controlled as a constant power source, behaving as a pure resistor. And, as the bandwidth increases, the range of the resistor characteristic extends. However, it is noteworthy that none of these three phases exceed 90°.

But when delay $T_{\rm del}$ is considered and fixed at 150 μs, then the bode plots of Z_{dd_v} are redrawn in Fig. 18. Compared with Fig. 17, it can be seen that when delay is considered, an evident impedance trough appears, and the phase rises over 90° within the range of 1–2 kHz. In addition to the deviation in the low-frequency area, as k_{vp} increases, the magnitude of the trough drops deeper and shifts slightly to the right, and its phase rises more. Although the changes are not as severe as the cases in Fig. 15 when k_{ip} changes, the slight deviation in phase rise is exactly the root cause of instability, as explained in the following section.

The corresponding complex plane representations of Z_{dd_v} are plotted in Fig. 19. As k_{vp} increases, the minimum distance from the curve to the origin points R_1–R_3 gradually shorten, explaining why the trough becomes deeper in Fig. 18. In general, due to the existence of the delay, the voltage loop dynamics will affect the high-frequency region in addition to the low-frequency region of the impedance.

One interesting finding from Figs. 10, 13, and 19 is that, due to the delay circle, the impedance is able to extend to the second quadrant in the complex plane, where the real part of the impedance becomes negative. Inevitably, a negative damping effect would be posed, and system stability would be threatened.

V. Stability Analysis With the Impedance Trough

The prerequisite for the stability of the grid-tied VSI system is that both the inverter and the grid are individually stable. Usually,

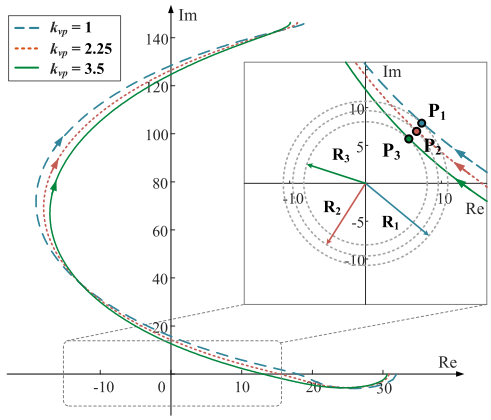


Fig. 19. Complex plane representations of Z_{dd_v} when $k_{vp} = 1$, 2.25, and 3.5.

the grid side is stable since the grid impedance is passive without right-half plane poles. Although the VSI is designed to be stable, its stability could not be guaranteed when considering changes in the control parameters and delay value. Consequently, it is necessary to first obtain the stability boundary of the standalone VSI. The stability boundary could be derived based on Routh's stability criterion by investigating the characteristic equation of the VSI.

For the stability of the grid-tied VSI system, the GNC or eigenvalue-based methods are the sufficient and necessary criteria [18], [19]. However, the root cause of the instability cannot be unveiled via these two approaches. Fortunately, for a high-power factor three-phase system, it has been verified that the stability at ac interfaces could be assessed directly from the impedance return ratios seen across the *d–d* and *q–q* interfaces [35], [36]. Then, the Nyquist criterion, or PM and gain margin (GM) theories in the dc system can be applied separately to the *d–d* and *q–q* subsystems. Via such methods, the root cause of the instability could be identified.

In this article, the VSI is controlled under the high-power factor condition. Meanwhile, in the single current loop control mode, the VSI is three-phase symmetrical. Hence, the *d–d* and *q–q* channel impedances are identical. In dual-loop control mode, although some deviations exist in the low-frequency portion due to voltage loop dynamics in the *d*-axis, the high-frequency parts are the same. Thus, if only the impacts of the impedance trough are discussed, the analysis could be further simplified based solely on the *d–d* channel impedances. Nevertheless, in order to ensure the seriousness of this analysis, the GNC-based method is adopted, either.

A. Single Current Loop Control Mode

In small-signal sense, the closed-loop information of the ac current-controlled VSI is characterized by the admittance, and its denominator is the system characteristic equation. Recall that the output impedance of the single current loop mode VSI $\mathbf{Z_{oc}}$ has already been obtained in (2). Thus, the inverse matrix of $\mathbf{Z_{oc}}$ is the output admittance, which is defined as follows:

$$\mathbf{Y_{oc}} = (\mathbf{I} + \mathbf{G_{id}}\mathbf{G_{del}}\mathbf{H_i})^{-1}\mathbf{G_{iv}}. \tag{21}$$

In $\mathbf{Y_{oc}}$, the denominators of the four elements are identical. Hence, only the *d–d* channel admittance is derived here, as

$$Y_{dd\_c} = \frac{sL + k_{ip}V_{\rm dc}e^{-T_{\rm del}s}}{\left(sL + k_{ip}V_{\rm dc}e^{-T_{\rm del}s}\right)^2 + \omega_0^2 L^2}. \tag{22}$$

When applying Routh's stability criterion, the characteristic equation should be written in the polynomial form. Substituting $e^{-T_{\rm del}s}$ with the first-order Padé approximation in (15), we obtain

$$Y_{dd\_c} = \frac{\left(1 + \frac{T_{\rm del}s}{2}\right)^2 sL + \left(1 - \left(\frac{T_{\rm del}s}{2}\right)^2\right) k_{ip}V_{\rm dc}}{a_1 s^4 + b_1 s^3 + c_1 s^2 + d_1 s + e_1}. \tag{23}$$

Here, the characteristic equation of Y_{dd_c} is defined as follows:

$$C_c = a_1 s^4 + b_1 s^3 + c_1 s^2 + d_1 s + e_1 = 0 \tag{24}$$

where the coefficients are

$$\begin{aligned} a_1 &= 0.5T_{\rm del}L, b_1 = T_{\rm del}L(L - 0.5T_{\rm del}k_{ip}V_{\rm dc}) \\ c_1 &= (0.5T_{\rm del}k_{ip}V_{\rm dc})^2 + L^2 + (0.5T_{\rm del}L\omega_0)^2 \\ d_1 &= T_{\rm del}(\omega_0^2 L^2 - k_{ip}^2 V_{\rm dc}^2) + 2k_{ip}V_{\rm dc}L \\ e_1 &= \omega_0^2 L^2 + k_{ip}^2 V_{\rm dc}^2. \end{aligned}$$

If T_s or $T_{\rm del}$ is fixed, then according to Routh's criterion, the stability boundary for k_{ip} is derived as follows:

$$k_{ip} < \frac{4L}{V_{\rm dc}T_{\rm del}} - \frac{2\omega_0 L}{V_{\rm dc}}. \tag{25}$$

Substituting the actual values of the variables listed in Table I into (22) yields $k_{ip} < 0.23$. More specifically, $T_{\rm del}$ is 150 μs.

If k_{ip} is constant and satisfying (22), then the stability boundary for $T_{\rm del}$ is derived as follows:

$$T_{\rm del} < \frac{4L}{k_{ip}V_{\rm dc} + 2\omega_0 L}. \tag{26}$$

Taking the actual value into (26) yields $T_{\rm del} < 225$ μs, when k_{ip} equals to 0.15.

The stability of the grid-tied system is first assessed based on the PM and GM theories by investigating the *d–d* channel impedance matching. Fig. 20(a) depicts the *d–d* channel grid impedance Z_{gdd} and the VSI output impedance Z_{dd_c} when k_{ip} equals to 0.05, 0.1, and 0.15, respectively. The part within the gray border where Z_{gdd} and Z_{dd_c} intersect is zoomed in Fig. 20(b). For the *L–C* type grid impedance, the phase of Z_{gdd} is around $-90°$ in the high-frequency area. Therefore, as long as the phase of Z_{dd_c} exceeds 90° at the intersection point, the stability of the system will be lost.

As illustrated in Fig. 20(b), when $k_{ip} = 0.05$, the phase of Z_{dd_c} at the intersection point is 75.1°. When $k_{ip} = 0.1$, Z_{gdd} intersects with Z_{dd_c} at 1.67 kHz with a phase of 89.6°, indicating a marginally stable system. As k_{ip} further increases to 0.15, the phase will reach 133.8° and the system will be unstable. However, if the digital control delay is not considered, then the phase of Z_{dd_c} would be limited to 90° and the system would always be stable no matter how k_{ip} changes.

The stability of the grid-tied VSI system could only be precisely assessed based on GNC by evaluating whether the eigenvalues of the system's return ratio encircle the (–1, *j*0)

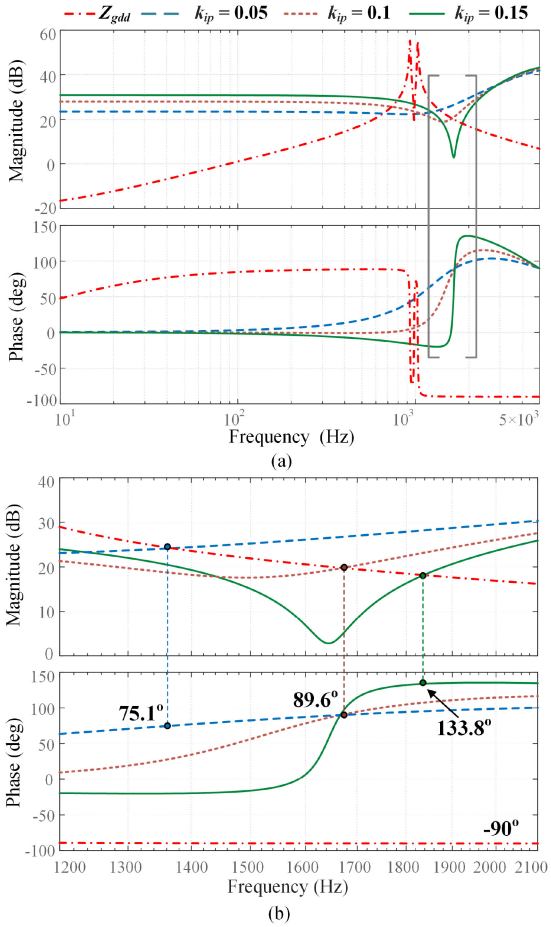


Fig. 20. *d–d* channel grid impedance Z_{gdd} and VSI output impedance Z_{dd_c} with three sets of k_{ip}. (a) Full scale. (b) Zoomed-in figure within the gray border.

point. For a single current control mode VSI, the return ratio of the grid-tied system is defined as follows:

$$\mathbf{L_c} = \mathbf{Y_{oc}Z_g}. \tag{27}$$

Fig. 21 presents the Nyquist diagram of the two eigenvalues. When k_{ip} is 0.05, the Nyquist contour does not encircle the (–1, *j*0) point, hence, the system is stable. When k_{ip} increases to 0.1, the contour just passes through the (–1, *j*0) point, indicating a marginally stable state. When k_{ip} increases further to 0.15, the contour encircles the critical point and the system will become unstable with divergent oscillation. The results based on GNC are consistent with that based on the GM and PM criteria in terms of *d–d* channel impedance.

Fig. 22 presents the grid impedance Z_{gdd} and VSI output impedance Z_{dd_c} under different delay value conditions. Specifically, k_{ip} here is fixed at 0.1. When $T_{\rm del}$ increases from 120 to 180 μs, the system gradually changes from the stable to the unstable state. It is worth noting that the frequency point where Z_{gdd} and Z_{dd_c} intersect when $T_{\rm del}$ = 180 μs is lower than the case when $T_{\rm del}$ = 150 μs, which is due to the deeper impedance trough located at a lower frequency in the former

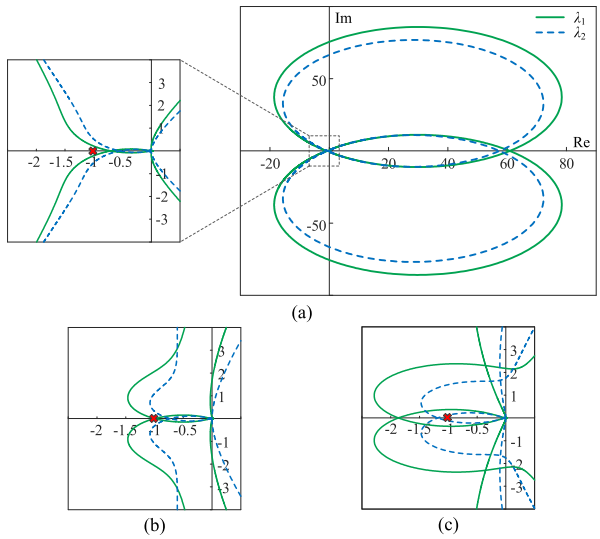


Fig. 21. Nyquist plot of eigenvalues of the return ratio $\mathbf{L_c}$ with three sets of k_{ip}: (a) k_{ip} = 0.05; (b) k_{ip} = 0.1 zoomed in; and (c) k_{ip} = 0.15 zoomed in.

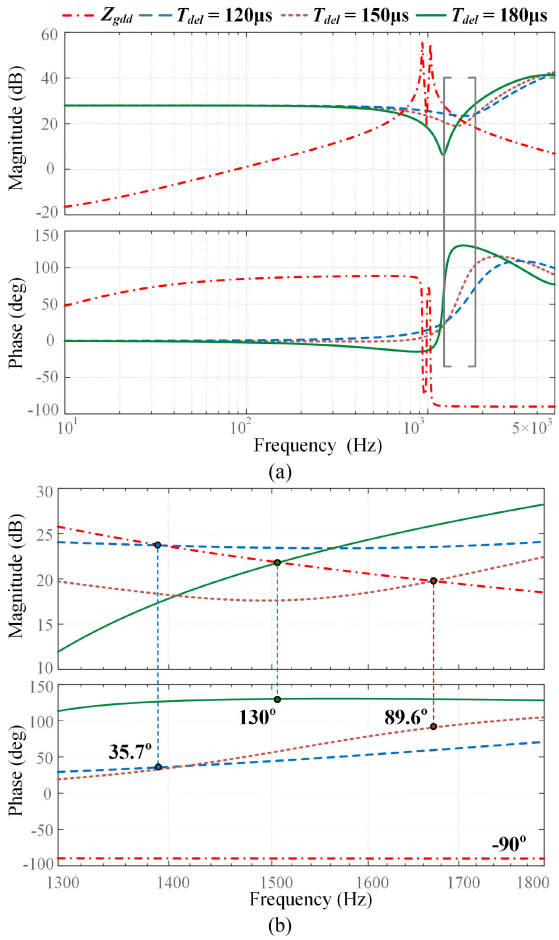


Fig. 22. *d–d* channel grid impedance Z_{gdd} and VSI output impedance Z_{dd_c} with three sets of $T_{\rm del}$. (a) Full scale. (b) Zoom-in figure within the gray border.

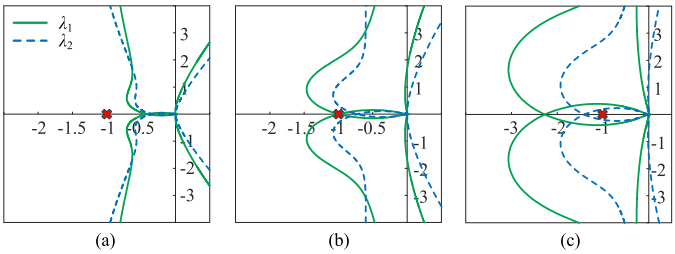


Fig. 23. Zoomed-in Nyquist plot of eigenvalues of the return ratio $\mathbf{L_c}$. (a) $T_{\rm del} = 120$ μs. (b) $T_{\rm del} = 150$ μs. (c) $T_{\rm del} = 180$ μs.

condition. The Nyquist diagrams of the system return ratio's eigenvalues in Fig. 23 also verify that as delay increases the stability of the system will gradually lose, which is consistent with the conclusions derived from Fig. 20.

B. Dual-Loop Control Mode

In dual-loop control mode, the output admittance of the VSI is defined as $\mathbf{Y_{ov}}$, which could be directly obtained from inversion of the impedance $\mathbf{Z_{ov}}$ in (4)

$$\mathbf{Y_{ov}} = (\mathbf{I} + \alpha \mathbf{G_{del}} \mathbf{H_i})^{-1} [\mathbf{G_{iv}} - \alpha \mathbf{G_{del}} \mathbf{H_i} \mathbf{H_v} \mathbf{G_{vv}}]. \quad (28)$$

In this mode, system characteristic equation is defined as follows:

$$C_v = a_2 s^5 + b_2 s^4 + c_2 s^3 + d_2 s^2 + e_2 s + f_2 = 0. \quad (29)$$

Due to the complexity of the fifth-order operation, only the numerical solution for C_v is given here. By keeping k_{vp} as the only unknown variable, and substituting the actual values of other parameters into (28), yields

$$a_2 = 1.03 \times 10^{-16},\ b_2 = 4.53 \times 10^{-13} - 6.72 \times 10^{-14} k_{vp}$$
$$c_2 = 3.12 \times 10^{-8} - 1.73 \times 10^{-10} k_{vp}$$
$$d_2 = 6.76 \times 10^{-5} - 1.62 \times 10^{-6} k_{vp}$$
$$e_2 = 2.29 + 6.43 \times 10^{-2} k_{vp},\ f_2 = 1143 k_{vp} - 6.53.$$

More specifically, k_{ip} is 0.1 and $T_{\rm del}$ is 150 μs. Then, the stability range for k_{vp} can be solved as $0.032 < k_{vp} < 6.85$. By following the same steps, the stability range of delay is obtained as $T_{\rm del} < 180$ μs, when k_{vp} is 1.

The *d–d* channel grid impedance Z_{gdd} and VSI output impedance Z_{dd_v} are shown in Fig. 24; it could be observed that when $k_{\rm vp}$ is 1, the phase of Z_{dd_v} at the intersection point is 82.1°, denoting a stable situation. When $k_{\rm vp}$ increases to 2.25, at the intersection point (i.e., around 1.51 kHz) the phase of Z_{dd_v} has already hit the 90° limit, indicating that the system is marginally stable. If k_{vp} further increases to 3.5, the system will fall into an unstable state with a negative PM.

For the dual-loop control mode VSI, the return ratio of the grid-tied system is defined as follows:

$$\mathbf{L_v} = \mathbf{Y_{ov}} \mathbf{Z_g}. \quad (30)$$

The Nyquist plots of the two eigenvalues of $\mathbf{L_v}$ are plotted in Fig. 25. When $k_{\rm vp} = 1$, the contour does not encircle the (–1, *j*0) point. When $k_{\rm vp} = 2.25$, the (–1, *j*0) point is just on the boundary

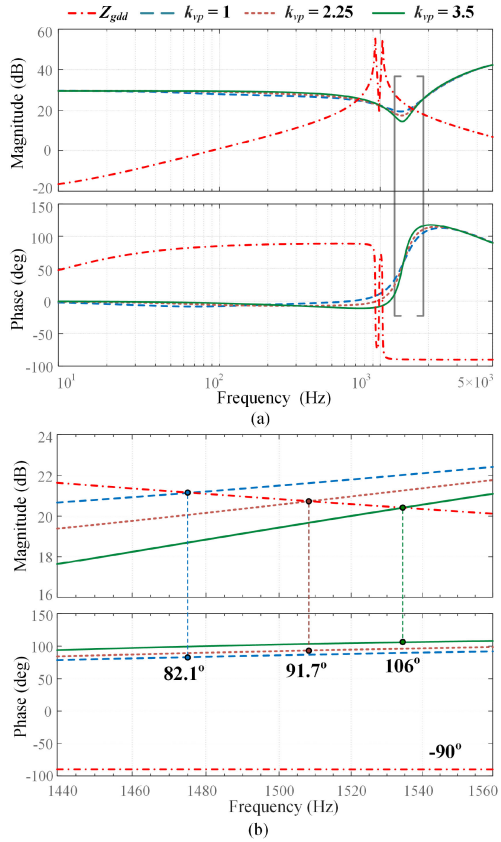


Fig. 24. *d–d* channel grid impedance Z_{gdd} and VSI output impedance Z_{dd_v} with three sets of k_{vp}. (a) Full scale. (b) Zoom-in figure within the gray border.

of the curve, indicating a critical stable state. When $k_{\rm vp} = 3.5$, the point is encircled and the system is unstable.

For the dual-loop control mode VSI, it can be interpreted from Fig. 24 that due to the delay effect, as control parameter $k_{\rm vp}$ changes, in the high-frequency area, the magnitude of the impedance varies only slightly, whereas the phase rises obviously, which is the root cause of system instability.

The impedance changes due to delay variations are similar in both control modes. Hence, only the results are provided: k_{ip} and k_{vp} is set to 0.1 and 2.25, when $T_{\rm del} = 150$ μs, the system is critically stable. If $T_{\rm del}$ declines by 30 μs, then the stability margin increases. On the contrary, if $T_{\rm del}$ increases by 30 μs, then the system would be unstable.

C. Impact of Grid Impedance Variations

Grid impedance is one of the crucial factors determining the stability of the grid-tied system. To analyze the impact of grid impedance, in single current loop control mode, three sets of grid-side inductors L_g (i.e., 3.5, 1.75, and 1 mH) are tested, whereas the capacitor remains unchanged at 15 μF. The *d–d* channel impedances of these three sets of grids are denoted by Z_{gdd1}, Z_{gdd2}, and Z_{gdd3}, respectively.

As plotted in Fig. 26, as L_g decreases, the two resonance peaks of Z_{gdd} gradually move to a higher frequency area. Z_{ddc} in Fig. 26 is the critical stable case with $k_{ip} = 0.1$. The phase of

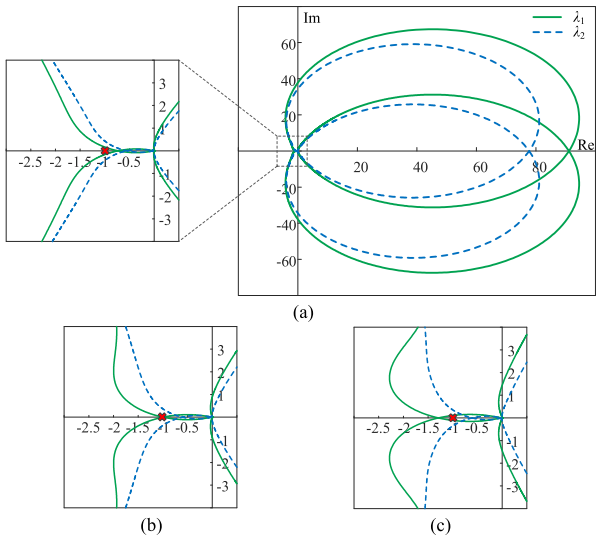


Fig. 25. Nyquist plot of eigenvalues of the return ratio $\mathbf{L_v}$ with three sets of k_{vp}: (a) $k_{vp} = 1$; (b) $k_{vp} = 2.25$ zoomed in; and (c) $k_{vp} = 3.5$ zoomed in.

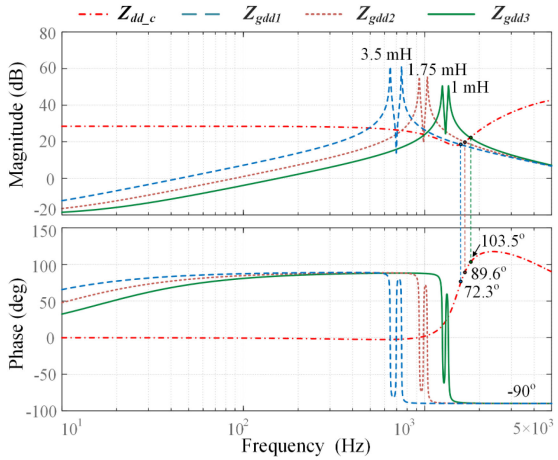


Fig. 26. *d–d* channel VSI output impedance Z_{dd_c} and three sets of grid impedances Z_{gdd1}, Z_{gdd2}, and Z_{gdd3}.

Z_{dd_c} at the intersection point between Z_{gdd2} is 89.6°, indicating a marginally stable state. When L_g decreases to 1 mH, the phase error increases to 193.5°, hence the stability will be lost. But when L_g increases to 3.5 mH, the system will be stable with a PM of 18°.

The corresponding Nyquist plots of the two eigenvalues of $\mathbf{L_c}$ under these three grid cases are shown in Fig. 27, in which the results are consistent with analysis in Fig. 26.

VI. Experimental Verifications

To verify the stability analysis above, an experimental setup of the three-phase grid-tied VSI system that has been studied above is built, as shown in Fig. 28. A Chroma grid simulator 61860 is employed to simulate the three-phase ac grid. A Myway inverter unit MWINV-9R144 embedded with a digital control system is applied as the three-phase VSI. The dc side of the inverter is

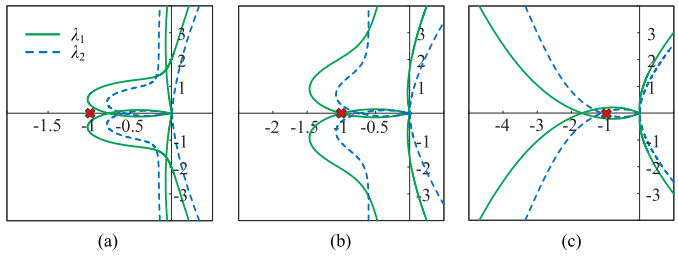


Fig. 27. Zoomed-in Nyquist plot of eigenvalues of the return ratio $\mathbf{L_c}$ under three different grid cases. (a) Z_{gdd1}. (b) Z_{gdd2}. (c) Z_{gdd3}.

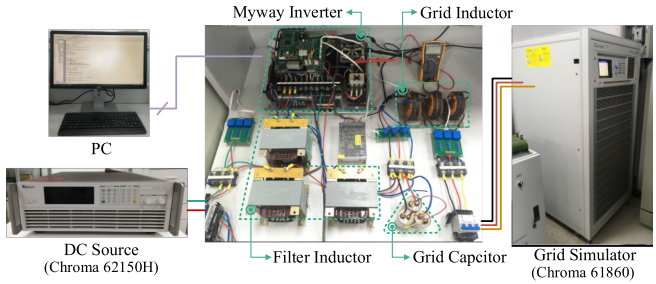


Fig. 28. Experimental setup of the studied three-phase grid-tied VSI system.

supplied by a Chroma dc source 62150H, which can operate in both the constant voltage (CV) and the constant current (CC) modes to test the two control modes analyzed in this article. The components and control parameters adopted in the test setup are the same as those in the model analysis, which are listed in Table I. The experimental verifications also include both the single current loop control and the dual-loop control modes. And in each case, three sets of control parameters k_{ip} or k_{vp}, delay values $T_{\rm del}$ and grid impedances Z_{gdd} are tested.

A. Single Current Loop Control Mode

In the single current loop control mode, the effects of k_{ip} and delay $T_{\rm del}$ on system stability are investigated. Throughout the tests, the *d*-axis inductor current reference $I_{\rm dref}$ is set to 6 A, and the *q*-axis inductor current reference is set to 0 A to ensure a high-power factor system. In addition, the grid voltage V_g is set to 110 V in the rms value.

First, the delay value $T_{\rm del}$ is fixed at 150 μs and three sets of k_{ip} (i.e., 0.05, 0.1, and 0.15) are tested in sequence. Fig. 29(a) presents the measured waveforms of phase-*A* point of common coupling (PCC) voltage $v_{\rm pcc\_A}$ and the inductor current i_{LA} when $k_{ip} = 0.05$, which are stable. When k_{ip} increases to 0.1, $v_{\rm pcc\_A}$ and i_{LA} are both slightly distorted with harmonic resonance around 1.7 kHz, which indicates that the system is in a marginally stable state. Simultaneously, the measured harmonic spectrum of the PCC voltage $v_{\rm pcc\_A}$ is shown in Fig. 30. It can be clearly seen that the high-frequency oscillations arise at 1650 and 1750 Hz, which agree well with the analysis based on *d–d* channel impedance matching in Fig. 20.

As k_{ip} increases to 0.15, divergent oscillations appear, and over a short period of time the VSI breaks down due to the protection. The waveforms of the imminent divergence are captured

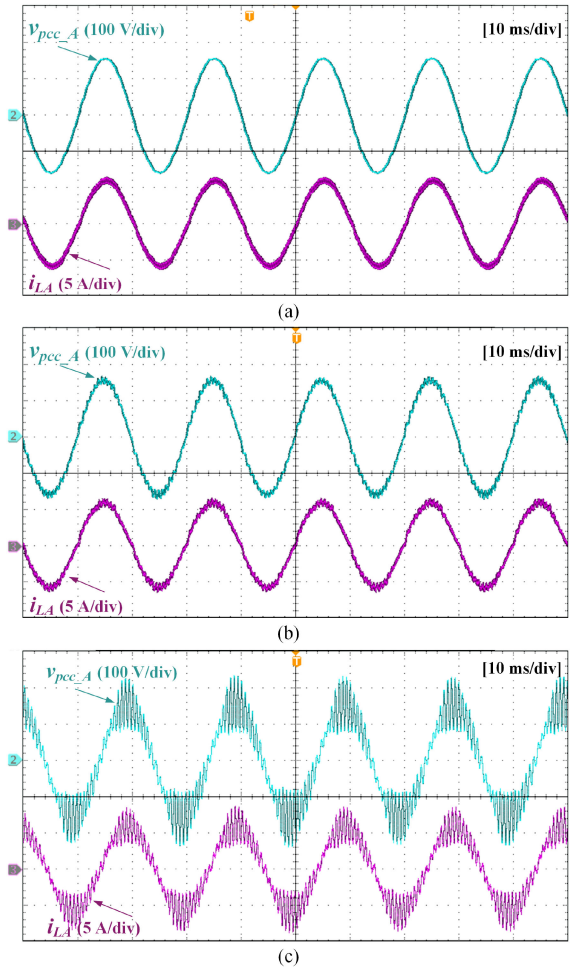


Fig. 29. Measured waveforms of the phase-*A* PCC voltage $v_{\mathrm{pcc\_}A}$ and grid current i_{LA}. (a) $k_{ip} = 0.05$. (b) $k_{ip} = 0.1$. (c) $k_{ip} = 0.15$.

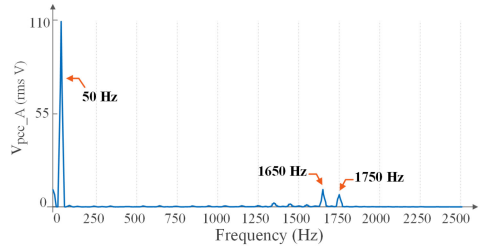


Fig. 30. Measured harmonic spectrum of PCC voltage $v_{\mathrm{pcc\_}A}$ when $k_{ip} = 0.1$.

in subplot Fig. 29(c). Generally, the tested results are consistent with the analysis based on GNC in Fig. 21.

The second step is to evaluate the effect of delay T_{del} on the stability of the system. From the previous step, the critical stable state with $k_{ip} = 0.1$ is adopted here, and three sets of T_{del} values (i.e., 120, 150, and 180 μs) are tested separately.

The middle case with $T_{\mathrm{del}} = 150$ μs has already been tested as marginally stable and been shown in Fig. 29(b). In the first case with $T_{\mathrm{del}} = 120$ μs, Fig. 31(a) shows that the system is not only stable but also has superior control performance than

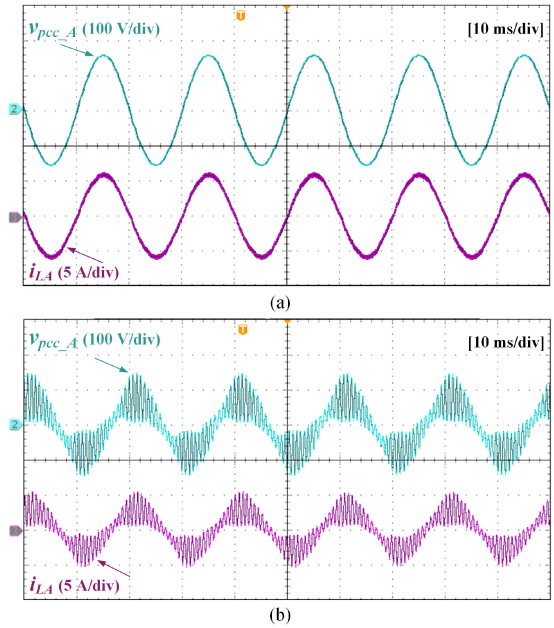


Fig. 31. Measured waveforms of phase-*A* PCC voltage $v_{\mathrm{pcc\_}A}$ and grid current i_{LA}. (a) $T_{\mathrm{del}} = 120$ μs. (b) $T_{\mathrm{del}} = 180$ μs.

the case when $k_{ip} = 0.05$, as presented in Fig. 29(a). However, as T_{del} increases to 180 μs, severe high-frequency oscillations appear in the waveforms, and the system becomes unstable, as shown in Fig. 31(b). It is noteworthy that the oscillation due to the 30-μs increment of delay is even more severe than the case of $k_{ip} = 0.15$ shown in Fig. 29(c).

B. Dual-Loop Control Mode

In the dual-loop control mode VSI system, the dc-link voltage v_{dc} is adjusted to 400 V and the grid voltage v_g is still set to 110 V in rms value. The dc-link input current is 5 A, and according to power balance the magnitude of the inductor current is 6 A, which is the same as in the previous tests. More specifically, the current controller gain k_{ip} here is fixed at 0.1. First, T_{del} is kept at 150 μs, and three sets of k_{vp} (i.e., 1, 2.25, and 3.5) are tested. In the first case, with $k_{vp} = 1$, the system is stable, and the measured waveforms of the dc-link voltage v_{dc}, phase-*A* PCC voltage $v_{\mathrm{pcc\_}A}$, and grid current i_{LA} are displayed in Fig. 32(a). In the second case, when k_{vp} increases to 2.25, small-amplitude high-frequency oscillations appear in the waveforms, and the system is under a critical stable state. Meanwhile, the measured harmonic spectrum of the PCC voltage $v_{\mathrm{pcc\_}A}$ is presented in Fig. 33. It can be seen that high-frequency oscillations arise at 1450 and 1550 Hz, which are close to the analysis based on *d–d* channel impedance in Fig. 20. If k_{vp} increases further to 3.5, then the system will become unstable, as shown in Fig. 32(c).

The tested results agree well with the GNC-based analysis in Fig. 25, which again demonstrate that the dynamics of the dc-link voltage loop could induce high-frequency oscillations.

The next step is to test the effect of delay T_{del} on system stability. Similarly, a critical stable case with $k_{vp} = 2.25$ in the previous step is chosen, and three sets of T_{del} (i.e., 120,

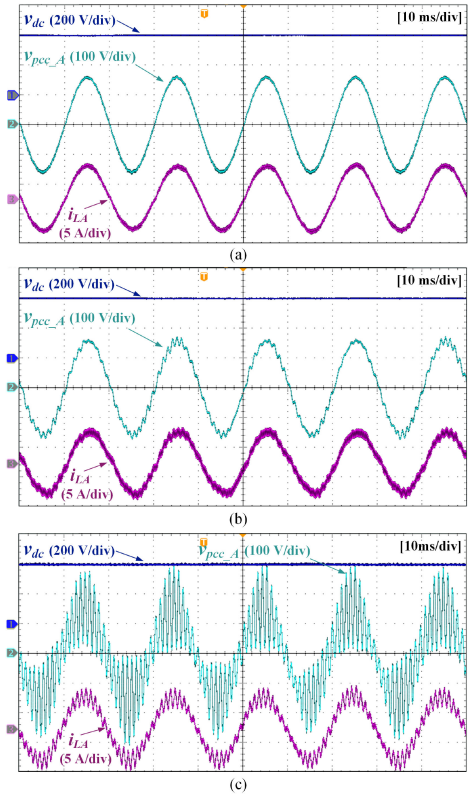


Fig. 32. Measured waveforms of dc-link voltage $v_{\rm dc}$, phase-A PCC voltage $v_{\rm pcc\_}A$, and grid current i_{LA}. (a) $k_{vp} = 1$. (b) $k_{vp} = 2.25$. (c) $k_{vp} = 3.5$.

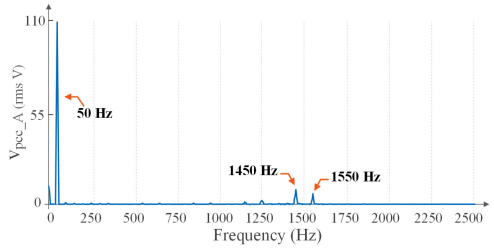


Fig. 33. Measured harmonic spectrum of PCC voltage $v_{\rm pcc\_}A$ when $k_{vp} = 2.25$.

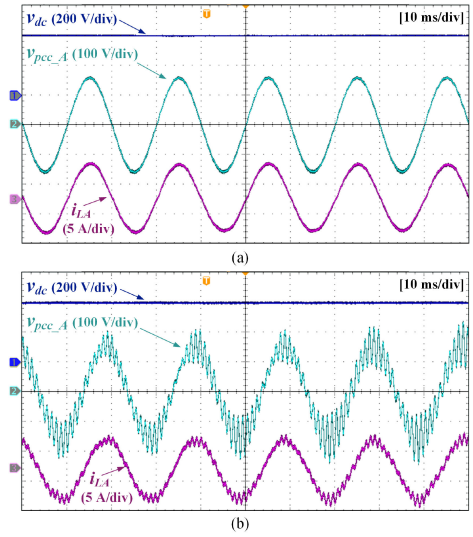


Fig. 34. Measured waveforms of dc-link voltage v_{dc}, phase-A PCC voltage $v_{\rm pcc\_}A$, and grid current i_{LA}. (a) $T_{\rm del} = 120$ μs. (b) $T_{\rm del} = 180$ μs.

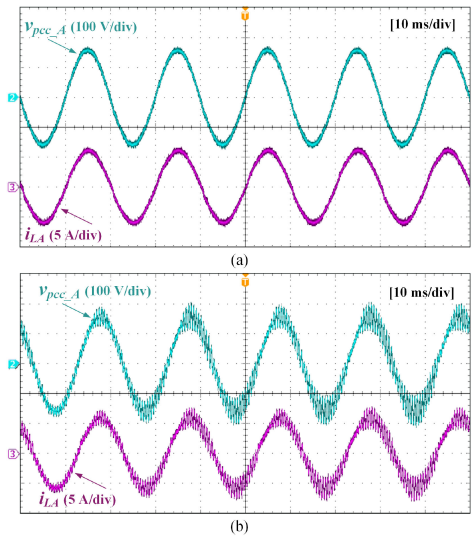


Fig. 35. Measured waveforms of phase-A PCC voltage $v_{\rm pcc\_}A$ and grid current i_{LA} under two different grid cases. (a) Z_{gdd1}. (b) Z_{gdd3}.

150, and 180 μs) are tested, separately. The critical stable case of $T_{\rm del} = 150$ μs has already been measured and displayed in Fig. 32(b). When $T_{\rm del}$ decreases by 30 μs, the system returns to the stable state, as shown in Fig. 34(a). But when T_d increases to 180 μs, the waveforms are distorted with serious high-frequency oscillations. The tested results are consistent with the upper stability analysis on the impacts of $T_{\rm del}$ variations.

C. Impact of Grid Impedance Variations

To verify the impact of grid impedance on system stability, the same three sets of grid impedances (i.e., Z_{gdd1}, Z_{gdd2}, and Z_{gdd3}) are tested. The middle case with $L_g = 1.75$ mH has already been displayed in Fig. 29(b), which is marginally stable. The other two cases are measured in in Fig. 35. When L_g equals 1 mH, the system is unstable, whereas when L_g increases to 3.5 mH, the system becomes stable. The measured results validate the correctness of the above theoretical analysis from Figs. 26 and 27.

In summary, from the measured waveforms in Figs. 31 and 34, it is verified that the stability of the system is sensitive to delay variations. Consequently, it could be inferred that in real power stations with high power level VSIs, the switching frequency is relatively low and the time delay is larger, making the influences of the delay even more serious.

VII. Conclusion

This article provides a deep insight into the impacts of digital control delay on VSI output impedance and the stability of the grid-tied inverter system working in both single current loop control and dual-loop control modes. Due to the frequency-dependent periodicity of delay, a phenomenon of impedance

trough is introduced into the VSI output impedance Z_{dd} and Z_{qq}. This impedance trough influences not only the phase, but also the magnitude of the impedance in the high-frequency area. The changing rules of the impedance trough to the control parameters and delay are summarized as follows.

1) The extreme point frequency of the trough increases as the controller gain k_{ip} or k_{vp} increases, whereas decreases as the delay value $T_{\rm del}$ increases.
2) For each of these three parameters, the larger the value, the more severe the impedance trough will be.
3) As k_{ip} or $T_{\rm del}$ increases, in both modes, a deep magnitude drop and a steep phase rise appear at the impedance trough. But in the dual-loop control mode, as k_{vp} increases, the impedance magnitude drops only slightly at the trough region, whereas the phase still rises distinctly.

In general, from the impedance-based perspective, the root cause of the delay-induced high-frequency oscillations in the grid-tied VSI system is the impedance mismatch between the grid and the VSI due to the existence of impedance trough.

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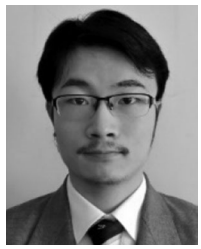

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