Evolutionary Design Automation of High Efficiency Series Resonant Converter for Photovoltaic Systems

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***Abstract*—Series resonant converter (SRC) is one of the main parts which has to be designed carefully to be compatible with the general requirements of photovoltaic (PV) grid-connected system. The extensive search space for design parameters of SRC such as resonant tank component values, transformer turn ratio, dead time and switching frequency requires an automated design framework. The proposed framework is developed using genetic algorithm (GA), differential evolution algorithm (DEA), and nondominated sorting genetic algorithm (NSGA-II) for the multi-objective optimization of SRC circuit while accomplishing zero voltage switching (ZVS). Regulating the output voltage while minimizing the losses of MOSFET, diode and transformer are the design objectives. FEM is applied to subdivide the single phase transformer into simpler and finite parts to calculate flux density value according to the optimized design parameters. Amongst these evolutionary algorithms, NSGA-II achieved the best optimization performance considering various operation modes and required specifications. Simulation results are also provided to validate the efficient and robust automated design of SRC to be used in photovoltaic systems.**

***Index Terms*—Nondominated sorting genetic algorithm, photovoltaic, series resonant converter, zero voltage switching.**

NOMENCLATURE

(C_1-C_9)	Coefficients for optimized transformer parameters.
(X_1-X_9)	Optimized parameters for single phase transformer.
B	Transformer flux density, (T).
C_O	SRC output filter capacitor, (F).
C_r	Resonant tank capacitor, (F).
D	Duty cycle.
f_r	Resonant frequency of SRC, (Hz).
f_S	Selected switching frequency, (Hz).
F_X	Switching frequency to resonant frequency ratio.
$I_{\rm av}$	MOSFET average current, (A).
$\rm I_{Lr}$	Resonant tank current, (A).
$I_{\rm Sec}$	Transformer secondary current, (A).
L_r	Resonant tank inductor, (H).
N	Single phase transformer turn ratio.
$R_{\rm ds}$	MOSFET drain-source resistance, (Ω).
$R_{\rm load}$	SRC load resistor, (Ω).
$R'_{\rm load}$	Apparent load resistor of SRC equivalent circuit, (Ω).
$r_{\rm eq}$	Apparent equivalent resistor of SRC equivalent circuit, (Ω)
$R_{\rm pv}$	Photovoltaic cable resistor, (Ω).
$T_{\rm dt}$	Dead time
$T_{\rm SW_{off}}$	Switching turn-OFF time, (s).
$T_{\rm SW_{on}}$	Switching turn-ON time, (s).
$V_{\rm ab}$	Switching stage voltage, (V).
$V_{\rm Cr}$	SRC capacitor voltage, (V).
$V_{\rm DS}$	MOSFET drain–source voltage, (V).
V_f	Diode forward voltage, (V).
V_O	SRC output voltage, (V).
$\rm V'_O$	Apparent output voltage of SRC equivalent circuit, (V)
$\rm V_{req}$	Apparent voltage of SRC equivalent resistor, (V).
$\rm V_{SW}$	MOSFET gate voltage, (V).
η	DC/DC converter efficiency.

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I. INTRODUCTION

DUE to shortage of fossil fuels and the fast growing in energy demand unlatch away to notice renewable energy sources which has been changing to be imperative. Among all types of renewable energy sources, solar photovoltaic (PV) supplies have privilege as a result of clean and emission free aspects. However, irradiation and shading area has a remarkable impact on the solar power. Wide range of output voltage and varying current conditions require an adjustable and efficient design of a solar PV grid system. Putting PV panels in array with a series connection has several limitations in keeping with weather and shading. Moreover, conjunct constant current may not be provided. In order to achieve high performance power generation various studies are carried out. In [1], a loss optimization method is suggested for zero voltage switching (ZVS) with two inductors as resonant parts. In [2], module integrated converter (MIC) and its cost balance effectiveness is pointed out. In [5], a control mechanism with series resonant harmonic compensator (SRHC) for minimizing voltage distortion is presented in [3]. PV grid connections are mainly implemented as series (where high output voltage is desired) or parallel (for special purposes of low output voltage requirement) as reviewed in [4]. A dc/dc converter design for PV system [5] achieved high accuracy for full load condition comparing to the traditional types. A different implementation [6] is used to retrieve losses due to weather conditions like shading and dust by using a resonant switched capacitor convertor for mismatching purposes. In [7], voltage stress of low input voltage and its effect

on reduction of power losses is studied. The resonant capacitor convertor is implemented for managing the variation of power generated from PV system as in [8]. Two types of solar array are utilized to show that the current-voltage (IV) characteristics of PV generators are mainly affected by dynamic resistance and it needs a calibration due to differences in current-voltage region [9]. A wide range dc/dc converter operation required for specific PV applications like power conditioning system are analyzed in [10], [11].

The main advantages for the implementation of series resonant converter (SRC) for grid connected solar PV systems are to achieve high power density, high effectiveness, reduced losses and low cost. A fine-tuned switching frequency with a fine-tuned duty cycle is theoretically implemented for full bridge switching of SRC in [12]. Working with higher switching frequencies as in [13], [14] decreases the circuit size and increases efficiency with more frugal costs. In addition, a high voltage transformer design with core and copper loss calculations showed that the switching frequency and flux density are the paramount parameters for the evaluation of losses. In [15], a multilayered printed circuit board is designed for high frequency SRC and core losses are studied due to its frequency dependency. A control circuit design has been carried out to amend the SRC performance by determining the delay time of switching circuit signal regardless transmuting of wide range of input voltage, while Petri-nets showed that the transition between modes is depending on resonant current, as in [16] and [17], respectively.

Mismatch of solar cells or even modules in series connection is an active research area for PV systems. The output power of a PV in general is determined by the solar cell/module having the lowest output power part amongst the rest of the solar cells/modules of the array. This occurs when cell/cells are shaded which in turn can cause a power dissipation and eventually the total resultant PV power is reduced. This type of dissipation might damage the total module, and a reliable and accurate converter design is required which can handle the change in PV output voltage (50–240 V) that is provided as an input to SRC. Output voltage of SRC is determined according to the demands. It is proposed that solar power systems can assemble adequate energy to macro base station at out range of a coverage area as in [18], [19]. Interference Cancellation System (ICS), radio frequency, frequency shift, fiber optic and digital repeaters are used as an essential parts of signal receiving and transmitting process to non or weak coverage area. It is shown that these devices can be preferred due to lower cost, lower complexity and reduced time instead of building a new Base Transceiver Station (BTS) to cover a wider distance area. Here, a minimum 96 V dc voltage is required from the output of solar power system. Therefore, considering a practical application area, the target output voltage is set as 100 V for this work. According to the voltage range of PV module, component values of the converter should be determined for various operation conditions and design requirements such as loss minimization and voltage regulation. Since the search space for optimal parameter values cannot be explored with conventional methods due to its complexity, an automated design methodology is required.

Parametric automation granted a pure identification of the popular base with the natural process between power electronics and automated circuit design. In addition, determining the boundary of the appropriate solution space for optimal circuit design considering design specifications and constraints turns out to be a rough issue with increasing number of design parameters. Besides, automated circuit design characterizes the upcoming needs and becomes a significant strategic method among power electronics community especially for multi object optimization and high frequency applications. Recently, employment of artificial intelligence for reliable measurements with parametric design is presented in [10], [20] and [21]. Two combined systems are proposed leaning on parametric model for power converter design of PV implementation to prompt the parameter identification with relevant conditions in [20]. In [21], an evolutionary algorithm (EA) is used for parametric design of z-source inverter. The importance of automated design in power electronics field especially in the combination of dispersed generation is discussed in [22]. The suggested model discovers more than one possible solution according to requirements. Automated design of SRC provides a proper evaluation for several design demands and explores the optimal solution in reasonable amount of time. This article proposes dc/dc converter design automation and optimization based on loss analysis model and output voltage regulation. SRC provides a smooth transition among different operation modes in addition to its ability of operating in a discontinuous conduction mode with an adjustable dead time value. An automated design algorithm for SRC converter is developed depending on time domain waveforms, as in [23], and [24]. Complexity of time domain calculations, increasing number of parameters, application dependent requirements and constraints are challenging issues and the proposed methods provides effective solutions. In SRC circuit design automation, all parameters are initially set to random values and in the following steps these values are updated according to a mathematical model. In [25], design parameters are set theoretically and it is shown that utilizing of a snubber *RC* circuit is subsidiary for reducing switching losses and to avert overloading voltage across switching circuit. Due to the effect of duty cycle on switching losses, a pulse engendered circuit is studied in [26].

After selection of the appropriate PV module [27] maximum power points of 6-PV module are being tracked. The tracking process is carried out according to tilt and azimuth angle within the environmental condition of the selected area and simulated by using Helioscope software and Design Builder software [27]. A wide range of output voltage values delivered from these modules are collected during tracking which in turn, requires an accurate implementation of SRC to regulate this variation. In this work, automated design of SRC topology is developed using three EAs: genetic algorithm (GA) [28], Differential Evolution Algorithm (DEA) [29] and Non-Dominated Sorting Genetic Algorithm (NSGA-II) [30] to optimize the design parameters of the converter for loss minimization and output voltage regulation for various loads. EAs were previously used for minimizing the loss of three phase transformer designed with five parameters

[31]. In this article, four additional parameters are included to enhance the efficiency of the single phase transformer by providing more precise calculation of no-load and load losses of transformer. The MOSFET switching loss, MOSFET & diode conduction losses, and transformer losses are defined by means of SRC design parameters. These loss expressions together with the output voltage variation expression are used as the cost function of evolutionary algorithms. In order to minimize the number of physical models and design parameters in the early stage of design process, Finite Element Method (FEM) is utilized [31]. In this article, FEM was applied to subdivide the single phase transformer into simpler and finite parts to calculate flux density value according to the optimized parameters. Following, these small parts are brought together to form single phase transformer parts which will be gathered into one model to calculate overall flux density with a sufficient knowledge of major affective elements on the design.

Reduction of overall losses of SRC, achieving ZVS condition with robust circuit performance and regulation of output voltage for various loads are the major challenges of this study. Multiobjective optimization of SRC design is carried out with EAs and FEM, where the evaluation performances of EAs are validated comprehensively. In addition, NLL and LL of single phase transformer are also optimized according to 9 parameter model to obtain lower loss values than that of 5-parameter model used in [31]. Other contributions of this study can be listed as the investigation of loss value dependency on particular SRC design parameters, selection of optimum operation mode for robust performance, and validation of optimization performances of EAs for different aspects and conditions.

Following introduction, the characteristics of selected PV module which has been optimized for shaded and nonshaded configuration are provided in Section II. In Section III, loss analysis model of SRC is provided according to the selected optimization technique and SRC equivalent circuit with additional design parameters is given. Moreover, output voltage regulation and SRC operation modes are specified according to the SRC design parameter values. Section IV presents simulation and optimization results comprehensively. Finally, concluding remarks and suggestions for future work is discussed in Section V.

II. PV Module

PV system configuration mainly consists of PV module(s), unidirectional dc/dc converter or bidirectional dc/dc converter when conducting a storage unit. In this paper, a unidirectional dc/dc converter is designed with Pulse Width Modulation (PWM) as a controlling scheme for PV array as given in Fig. 1. Maximum power point tracking (MPPT) is used to optimize annual voltage variation delivered from PV array, due to climate conditions, shaded and non-shaded areas and other different reasons. A wide range of input voltages under these conditions requires a reliable dc/dc converter to respond efficiently to PV voltage variations. The selected PV module and electrical characteristics are provided in [27].

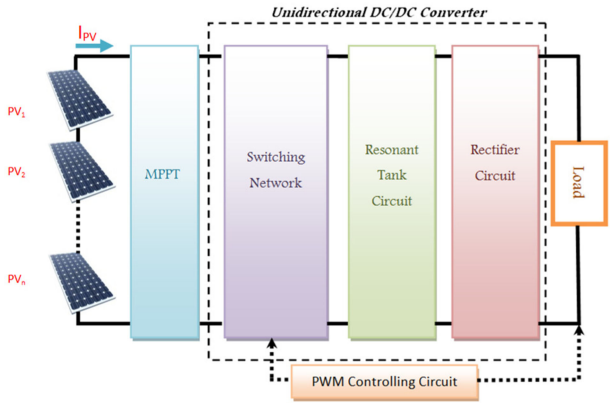

Fig. 1. PV system configuration.

III. Multi-Objective Optimization of Overall Loss and Output Voltage Variation

The loss calculations and output voltage variation of SRC circuit according to load variation are carried out by indicating values of switching frequency, resonant inductor, resonant and output filter capacitors, transformer turn ratio, dead time and apparent load resistor which are the design parameters of SRC. For this purpose, optimal values of these parameters are determined using (GA), (DEA), and (NSGA-II), and the optimization performances of those are evaluated comprehensively.

In GA [28], first generation consists of random individuals called chromosomes. Each of them has the actual value and gene code. The quality of these solutions is measured by a metric called cost function. Selection of next generations depends on solutions' quality which is acquired after cost function calculation. The selected solutions are used as parents to generate different off-springs better than previous parents using cross-over. Following, some chromosomes are randomly selected from the current generation using a scaling factor to control the variety of solutions during mutation. The procedures are terminated when next generation cannot provide better solutions than the previous one. Unlike GA, DEA [29] starts with mutation process to obtain a target vector and then crossover is applied to generate a trial vector. Following, a stochastic decision is carried out to determine the next generations and tournament process is used to specify which vectors should remain for the next iterations. DEA operates with continuous and noisy parameters in a large search space of solutions and results in reasonable amount of computation time. GA requires long execution time for multiobjective problems and provides fewer solutions compared to NSGA. NSGA-II [30] reduces the computational complexity with crowding distance procedure. It provides solutions with better spread and closest to the optimal Pareto front line. Each solution is compared with previous generations to check the dominated sets of Pareto lines. Cost function is normalized for each solution before crowding distance calculation. Then, each edge parameter is assigned to be infinite distance value referring to the lowest and highest cost function values of each Pareto front lines. Intermediate solutions will be measured according to crowding distance procedure and ranked with their lines.

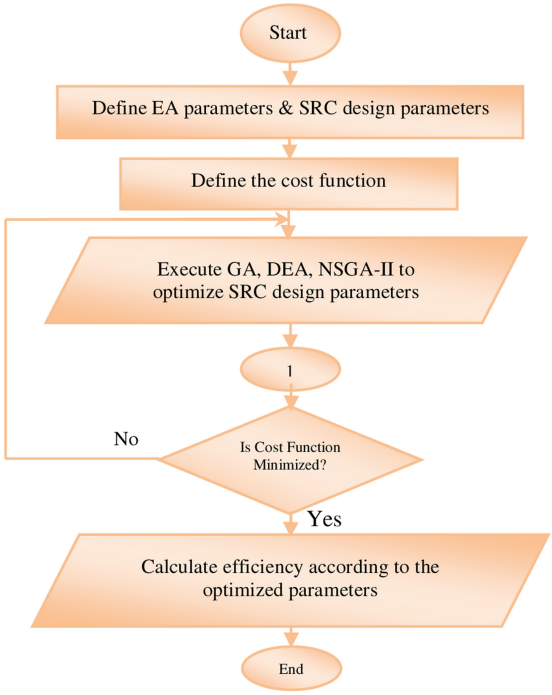

Fig. 2. Multi-objective optimization methodology for SRC design.

Selection, cross-over and mutation processes are also used in overall optimization process as in GA and DEA. NSGA-II differs from the mentioned EAs such that the first and the second generations are combined together and separated by ranking and crowding distance procedures [31].

Following, FEM performed for flux density calculation of the single phase transformer design. Valuable information of the most effective parameters like transformer turn ratio which influences transformer loss calculation on the overall SRC design is gathered through FEM. Multi-objective optimization methodology for high efficient SRC circuit is presented in Fig. 2. First of all, the own parameters of EAs and resonant tank component values, switching frequency, apparent load resistor and the input voltage of SRC which is provided from the PV panel are introduced to the algorithm. Meanwhile expressions for output voltage variation and overall loss (sum of conduction, switching and transformer losses) are defined as the cost function of EAs.

Setting the switching frequency value equal, higher or lower than the resonant frequency determines the region of operation, as shown in Fig. 3. Following, operating modes are analyzed through equivalent SRC circuit according to the input voltage range of SRC which is provided from the output of 6-PV module. Due to the different regions and modes of SRC, an automated design is required for the effective search of extensive possible solutions and accurate parameter value selection for loss minimization and output voltage regulation. For each operating mode of SRC equivalent circuit, loss values, actual output voltage and efficiency is calculated. FEM is used for validating the flux density change after NLL and LL evaluation to determine which design parameters are the most effective on transformer loss minimization.

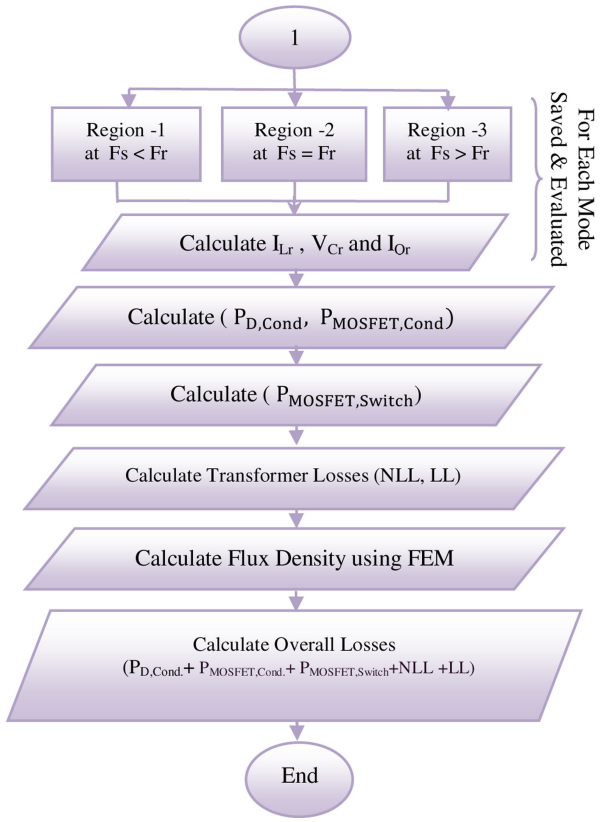

Fig. 3. SRC loss analysis model.

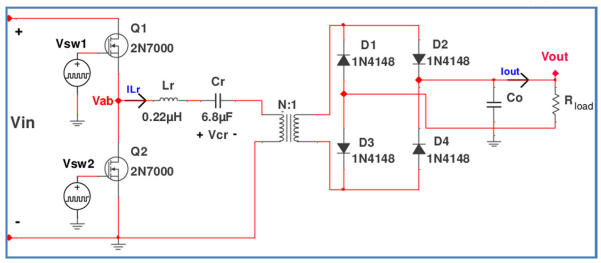

Fig. 4. Series resonant converter topology.

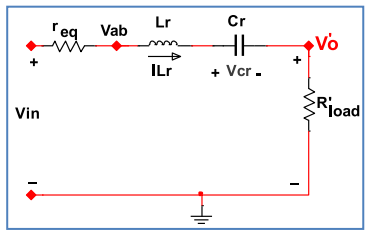

Fig. 5. Series resonant converter equivalent circuit.

A. *Equivalent SRC Circuit*

SRC topology as shown in Fig. 4 can be approximated to its fundamental equivalent circuit as given in Fig. 5. Load resistor (R_{load}) in Fig. 4 is affected by the charging process of the transformer primary side, therefore it is considered in the

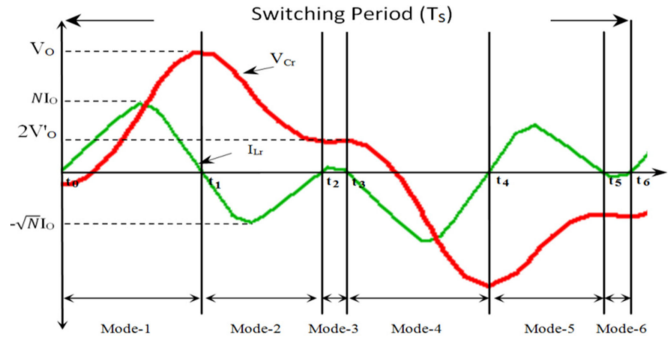

Fig. 6. Waveforms of resonant inductor current and capacitor voltage.

expression of apparent load resistance. In Fig. 5, $r_{\rm eq}$ is the series connection of MOSFET drain-source resistance $R_{\rm ds}$ (only one switch will be ON) and photovoltaic cable resistance $R_{\rm pv}$. The effect of diodes on primary side is neglected. Design equation for the apparent load resistance is given in

$$R'_{\rm load} = \frac{8\,N^2}{\pi^2} * R_{\rm load} * D. \tag{1}$$

As shown in Fig. 5, the load connected in series with the resonant tank components made SRC operate as a voltage divider circuit. In [14] and [32], operating modes were explained based on capacitor charging time and influence by the primary side due to transformer turning ratio. While in this article, resistance of PV cable and MOSFET drain-source resistance are added to the equivalent circuit for more realistic results. Some of PV modules has large value of cable resistance and it should be considered in the optimization of losses. These additional elements may cause extra power consumption losses if ignored during design process, especially for applications that deals with delivering high currents. Also, the voltage on the primary side may be reduced due to the effect of these resistances which makes voltage regulation on the secondary side more difficult.

B. Operating Modes

Resonant current and capacitor voltage waveforms for single switching period are plotted in Fig. 6 according to the parameters shown in Fig. 4 when $(f_s < 1/2f_r)$. The equations for modes 1, 2, and 3 are given as follows [33]

$$I_{Lr}(t) = \left[\left(V_{\rm in} - V_{r_{\rm eq}} - V_{Cr}(t_0) - V'_O \right) * \frac{C_r}{L_r} * \sin\left(\frac{t}{\sqrt{L_r C_r}} \right) \right] \tag{2}$$

$$V_{Cr} = \left[\left(V_{\rm in} - V_{r_{\rm eq}} - V'_O \right) - \left(V_{\rm in} - V_{r_{\rm eq}} + V'_O - V_{Cr}(t_0) \right) * \sqrt{\frac{C_r}{L_r}} * \cos\left(\frac{t}{\sqrt{L_r C_r}} \right) \right] \tag{3}$$

TABLE I
OPTIMAL OWN PARAMETER VALUES OF EA METHODS

Proposed Methods	Population Number	Crossover probability	Mutation probability
GA	100	0.3	0.1
DEA	150-200	0.5	0.15
NSGA-II	100	0.3	0.1

$$I_{Lr}(t) = \left[\left(-V_{\rm in} + V_{r_{\rm eq}} + V_{Cr}(t_1) + V'_O \right) * \frac{C_r}{L_r} * \sin\left(\frac{t}{\sqrt{L_r C_r}} \right) \right] \tag{4}$$

$$V_{Cr} = \left[\left(V_{\rm in} - V_{r_{\rm eq}} + V'_O \right) - \left(-V_{\rm in} - V_{r_{\rm eq}} + V'_O - V_{Cr}(t_1) \right) * \sqrt{\frac{C_r}{L_r}} * \cos\left(\frac{t}{\sqrt{L_r * C_r}} \right) \right] \tag{5}$$

$$V_{Cr} = 2V'_O. \tag{6}$$

C. Calculation of SRC Overall Losses

The parameters of loss expressions that mainly affect the efficiency are investigated. The transformer turn ratio is the most influencing element on both transformer losses and diode conduction loss. Conduction losses of MOSFET & diode are more dependent on dead time, resonant frequency and resonant tank parameters. After calculating overall losses [33] using (7), cost function is derived with the inclusion of output voltage variation

$$P_{\rm Overall\_Losses} = P_{D,\rm Cond.} + P_{\rm MOSFET,Cond.} + P_{\rm MOSFET,Switch.} + \rm NLL + LL \tag{7}$$

$$P_{D,\rm Cond.} = V_f * N * I_{Lr} * D \tag{8}$$

$$P_{\rm MOSFET,Cond.} = I^2_{\rm av} * R_{\rm ds} * D \tag{9}$$

$$P_{\rm MOSFET,Switch.} = \frac{1}{2}\left(T_{\rm SW_{on}} + T_{\rm SW_{off}}\right) * V_{\rm DS} * I_Q * f_s. \tag{10}$$

The transformer model in [31] utilizes five parameters, while in this article, bobbin's height (X_6), bobbin's depth (X_7), core area (X_8), and window's width (X_9) are also included for more accurate NLL & LL calculations.

D. Calculation of Output Voltage Variation

Another objective towards robust SRC design is the output voltage regulation. Minimization of voltage variation (11) under different load resistor, input voltage and region conditions is evaluated. The desired output voltage is 100 V, as explained in introduction

$$V_{\rm out\_var} = \left| V_{\rm out_{Desired}} - V_{\rm out_{Actual}} \right|. \tag{11}$$

TABLE II
OPTIMIZATION RESULTS FOR GA BASED METHOD

Condition	fs = fr (Region 2)								
Input Voltage	Vin = 240 V			Vin = 170 V			Vin = 100 V		
External Load*	FL	HL	NL	FL	HL	NL	FL	HL	NL
Vout (V)	98.1	97.4	92.9	98	97.7	82.7	74.7	74.4	61.6
$P_{D,Cond}$ (mW)	321	400	427.8	199.4	264.5	319.7	216	273.1	348.6
$P_{MOSFET,Cond.}$ (mW)	307.9	307.3	432.5	292.2	309.3	334.1	170	277.3	362.9
$P_{MOSFET,Switch}$ (W)	11.3	13.4	13.5	11	11.4	11.7	8.4	10.7	12.2
NLL + LL (W)	4.8	4.2	2.7	4.8	3.9	2.7	4.3	3.4	2.7
Overall Loss (W)	16.7	18.3	17.1	16.3	15.9	15.1	13.1	14.7	15.6
Efficiency (%)	87.9	85.8	85.0	88.2	87.7	75.8	69.2	67.9	54.5
Condition	fs > fr (Region 3)								
Input Voltage	Vin = 240 V			Vin = 170 V			Vin = 100 V		
External Load*	FL	HL	NL	FL	HL	NL	FL	HL	NL
Vout (V)	99.1	98.3	87.5	95.9	93.4	87.4	89.5	87.7	69.3
$P_{D,Cond}$ (mW)	245.5	306.9	461.5	344.9	414.3	425.3	195.1	244.2	321
$P_{MOSFET,Cond.}$ (mW)	168.9	238.2	292.4	168.9	191.8	280	166.8	168.5	282.8
$P_{MOSFET,Switch}$ (W)	8.3	9.9	11	8.4	8.8	10.7	8.3	8.9	10.8
NLL + LL (W)	6.4	5.6	3.5	5.2	4.3	3.5	4.7	3.8	3.5
Overall Loss (W)	15.1	16.0	15.3	14.1	13.7	14.9	13.5	13.2	14.9
Efficiency (%)	89.1	87.1	77.8	86.2	87.7	77.5	79.9	72.1	62.8
Condition	fs < fr (Region 1)								
Input Voltage	Vin = 240 V			Vin = 170 V			Vin = 100 V		
External Load*	FL	HL	NL	FL	HL	NL	FL	HL	NL
Vout (V)	96.5	91.8	89.7	89.8	87	88.4	68.7	67.8	66.3
$P_{D,Cond}$ (mW)	282.9	306.9	375	256.5	314.2	386.2	258.4	294.6	314.2
$P_{MOSFET,Cond.}$ (mW)	142.5	170	217.4	158.5	192.9	202.1	146.5	148.5	168.9
$P_{MOSFET,Switch}$ (W)	8.2	8.4	9.5	8.1	8.9	9.1	8.1	8.5	8.7
NLL + LL (W)	4.3	3.9	2.5	4.2	3.8	2.5	4.1	4.1	2.5
Overall Loss (W)	13.0	12.8	12.6	12.7	13.2	12.2	12.6	13.0	11.6
Efficiency (%)	86.8	83.9	69.1	80.5	79.4	74.0	63.4	62.3	61.1

∗FL: Full Load = 750 Ω, HL: Half Load = 300 Ω, NL: No Load = 25 Ω.

E. Cost Function and Efficiency

Cost function is derived by taking into consideration of overall loss ($P_{\mathrm{Overall-Losses}}$) and output voltage variation ($V_{\mathrm{out-var}}$). The objectives are the minimization of these functions and optimization performances of EA methods are validated comprehensively. Following, efficiency of SRC circuit is calculated using

$$\eta = \frac{P_{\mathrm{in}} - P_{\mathrm{Overall\ Losses}}}{P_{\mathrm{in}}}. \tag{12}$$

IV. SIMULATION AND OPTIMIZATION RESULTS

Table I shows the optimal own parameter values of each EA method which provides the minimum overall loss and output voltage regulation. The population number for GA and NSGA-II is equal and less than that of DEA. In order to achieve diversity in individuals' solutions for DEA, higher crossover probability value is applied. On the other hand, GA and NSGA-II provides more flexible solutions with crossover probability selected as "0.3." Mutation probability is set to be low so as to keep diversity without moving towards primitive random searching process.

Calculation of minimized overall losses, actual output voltage and efficiency after optimization process is shown in Tables II–IV considering a wide input voltage range with various conditions regarding switching frequency and load. Exact values of switching and resonant frequencies of three possible regions are calculated by EA methods. GA based optimization results are given in Table III and it is shown that working with high input voltage provides lower overall losses for all frequency conditions. Automated SRC design is proved to be more efficient on full load than other conditions regardless of input voltage values. In addition, operating in regions 2 and 3 where $f_s = f_r$ and $f_s > f_r$, respectively provided better performance due to fast switching operation than in region 1 where $f_s < f_r$. In region 1, hold-up time is increased which forces SRC circuit to keep regulating the output voltage. The best result of GA based optimization is obtained between 170–240 V input voltage range on full load condition for regions 2 and 3. Using GA, dead time is optimized as 1.27 μs which is considered to be a long hold-up period for SRC circuit to regulate output voltage.

Table IV presents DEA based optimization results which are improved compared to GA based results; e.g., 10.9% efficiency increase is gained at full load condition when $V_{\mathrm{in}} = 240$ V. Dead time is optimized as 0.31 μs using DEA which is a shorter period than that of GA. The highest efficiency obtained with DEA is 96% when $V_{\mathrm{in}} = 240$ V with full load condition.

NSGA-II based optimization results are provided in Table V. Dead time is optimized as 0.75 μs using NSGA-II which is a sufficient turning OFF and ON time for the overall process. A proper optimization of dead time as well as other SRC design parameters is crucial to prevent high current absorption which may damage switching components of SRC circuitry. According to Table V, output voltage is properly regulated to 100 V for an input range of 170–240 V when operating in region 2. Even when the input is decreased to 100 V, output voltage is 98.4 V at no load condition and 98.8 V at full load condition.

TABLE III
OPTIMIZATION RESULTS FOR DEA BASED METHOD

Condition	fs = fr (Region 2)								
Input Voltage	Vin = 240 V			Vin = 170 V			Vin = 100 V		
External Load*	FL	HL	NL	FL	HL	NL	FL	HL	NL
Vout (V)	99.9	99.8	96.3	95	91.1	89.5	90.3	89.6	88.2
$P_{D,Cond}$ (mW)	613.8	1103.7	415.1	564.6	619.1	993.2	389.4	604.8	844.8
$P_{MOSFET,Cond.}$ (mW)	87.3	89.2	78.6	77.8	77	73.7	80.3	80.7	70.4
$P_{MOSFET,Switch}$ (W)	5.3	4.9	5	5	4.9	4.8	5	5	4.7
NLL + LL (W)	3.8	3.4	1.5	3.6	3.4	1.5	3.5	3.1	1.5
Overall Loss (W)	9.8	9.5	7.0	9.2	9.0	7.4	9.0	8.8	7.1
Efficiency (%)	96.0	91.9	89.2	90.3	87.5	86.1	86.6	86.0	85.0
Condition	fs > fr (Region 3)								
Input Voltage	Vin = 240 V			Vin = 170 V			Vin = 100 V		
External Load*	FL	HL	NL	FL	HL	NL	FL	HL	NL
Vout (V)	99.9	95.5	79.7	91.1	90.7	84.6	76.7	74.7	66.3
$P_{D,Cond}$ (mW)	352.6	569.1	686.3	349.3	624.9	745.4	248.8	392.8	708.6
$P_{MOSFET,Cond.}$ (mW)	74.5	75.2	80.2	86.4	86.3	79.5	54	58.3	62.7
$P_{MOSFET,Switch}$ (W)	4.9	5	5.1	5.2	5.2	5	4.1	4.3	4.5
NLL + LL (W)	5.2	4.8	2.4	4.9	4.4	2.4	4.8	4.2	2.4
Overall Loss (W)	10.5	10.4	8.3	10.5	10.3	8.2	9.2	9.0	7.7
Efficiency (%)	96.0	90.5	76.1	87.1	86.6	78.2	73.3	71.3	63.1
Condition	fs < fr (Region 1)								
Input Voltage	Vin = 240 V			Vin = 170 V			Vin = 100 V		
External Load*	FL	HL	NL	FL	HL	NL	FL	HL	NL
Vout (V)	99.9	95.8	73.4	92.9	91	89.9	84.4	82.6	69.1
$P_{D,Cond}$ (mW)	520	583.7	697.5	659.5	815.7	997	362.7	579.2	943
$P_{MOSFET,Cond.}$ (mW)	82	121.1	141.7	87.3	122.1	223.2	38.6	65.7	82
$P_{MOSFET,Switch}$ (W)	5.1	6.2	6.7	5.3	6.2	8.4	3.5	4.6	5.1
NLL + LL (W)	3.7	3.6	1.5	3.5	3.4	1.5	3.3	3.1	1.5
Overall Loss (W)	9.4	10.5	9.0	9.5	10.5	11.1	7.2	8.3	7.6
Efficiency (%)	96.1	87.5	69.3	89.0	83.6	80.7	81.6	79.2	65.7

∗FL: Full Load = 750 Ω, HL: Half Load = 300 Ω, NL: No Load = 25 Ω.

TABLE IV
OPTIMIZATION RESULTS FOR NSGA-II BASED METHOD

Condition	fs = fr (Region 2)								
Input Voltage	Vin = 240 V			Vin = 170 V			Vin = 100 V		
External Load*	FL	HL	NL	FL	HL	NL	FL	HL	NL
Vout (V)	99.9	99.8	99.8	99.9	99.6	99.6	98.8	98.6	98.4
$P_{D,Cond}$ (mW)	159.9	277.7	659.6	396.8	21.7	157.4	556.7	601.4	353.4
$P_{MOSFET,Cond.}$ (mW)	412.2	654.3	566	394.2	415.8	390.7	66.9	310.4	387.2
$P_{MOSFET,Switch}$ (W)	10.9	13.7	12.8	10.6	10.9	10.6	8.4	9.4	10.5
NLL + LL (W)	2.1	2.0	1.3	2.0	1.9	1.3	2.0	1.8	1.3
Overall Loss (W)	13.6	16.6	15.3	13.4	13.2	12.4	11.0	12.1	12.5
Efficiency (%)	96	95.2	95	96	94.8	94.8	95.6	94.7	94.8
Condition	fs > fr (Region 3)								
Input Voltage	Vin = 240 V			Vin = 170 V			Vin = 100 V		
External Load*	FL	HL	NL	FL	HL	NL	FL	HL	NL
Vout (V)	99.9	77.6	64.8	99.9	82.5	61.5	98.9	77	58.2
$P_{D,Cond}$ (mW)	151.2	269	705.5	324.8	200.8	487.3	321.1	453.8	820.8
$P_{MOSFET,Cond.}$ (mW)	568.1	570.3	563.4	566	567.1	561.6	406.8	402.7	388.9
$P_{MOSFET,Switch}$ (W)	12.8	12.8	12.8	12.8	11.5	12	10.8	10.5	9.6
NLL + LL (W)	2.5	2.4	1.4	2.5	2.2	1.4	2.4	2.3	1.4
Overall Loss (W)	16.0	16.0	15.5	16.2	14.7	14.4	13.9	13.7	12.2
Efficiency (%)	92.5	70.2	57.4	92.5	75.7	54.7	92.5	67.8	52.5
Condition	fs < fr (Region 1)								
Input Voltage	Vin = 240 V			Vin = 170 V			Vin = 100 V		
External Load*	FL	HL	NL	FL	HL	NL	FL	HL	NL
Vout (V)	99.9	86	66.7	92.3	86	64.9	91.4	77.2	59.3
$P_{D,Cond}$ (mW)	869.2	789.8	653.4	746.4	786.1	789.8	750.2	908.9	1326
$P_{MOSFET,Cond.}$ (mW)	865.9	821.7	821.6	988.4	887.1	820.6	831.5	866	866.4
$P_{MOSFET,Switch}$ (W)	15.8	15.4	15.4	16.9	16	16.1	16.8	16.7	16.8
NLL + LL (W)	2.0	1.9	1.2	1.8	1.8	1.2	1.8	1.7	1.2
Overall Loss (W)	19.5	18.9	18.1	20.4	19.5	18.9	20.2	20.2	20.2
Efficiency (%)	90.6	77.1	58.0	82.6	76.7	55.8	81.8	67.5	49.6

∗ FL: Full Load = 750 Ω, HL: Half Load = 300 Ω, NL: No Load = 25 Ω.

TABLE V
TRANSFORMER NLL&LL AND FLUX DENSITY EVALUATION FOR 5P AND 9P MODELS

GA				
Condition	NLL+LL (W)		B (Wb/m2)	
	5P Model	9P Model	5P Model	9P Model
fs=fr	4.62	4.8	2.36	2.10
fs>fr	6.98	6.4	2.388	2.23
fs<fr	5.61	4.3	1.983	1.95
DEA				
Condition	NLL+LL (W)		B (Wb/m2)	
	5P Model	9P Model	5P Model	9P Model
fs=fr	4.137	3.8	1.94	1.8
fs>fr	5.35	5.2	2.217	1.88
fs<fr	4.08	3.7	2.05	1.71
NSGA-II				
Condition	NLL+LL (W)		B (Wb/m2)	
	5P Model	9P Model	5P Model	9P Model
fs=fr	3.272	2.1	1.712	1.20
fs>fr	3.86	2.5	1.758	1.65
fs<fr	2.54	2.0	1.624	1.20

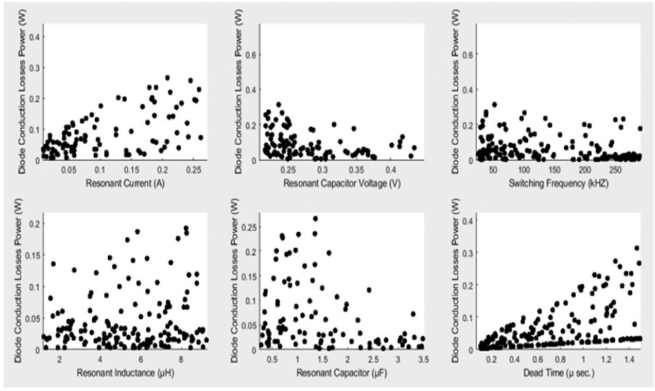

Fig. 7. Diode conduction loss variation according to SRC design parameter variation.

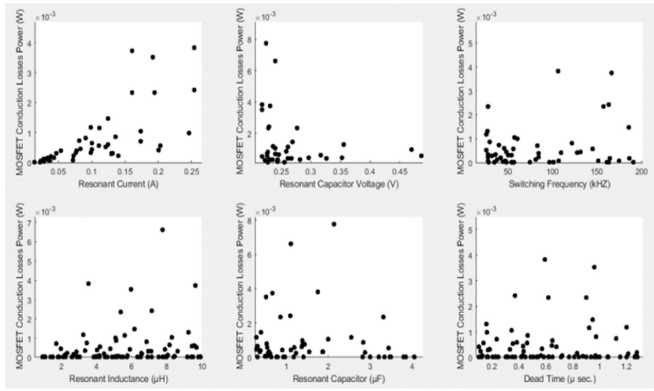

Fig. 8. MOSFET conduction loss variation according to SRC design parameter variation.

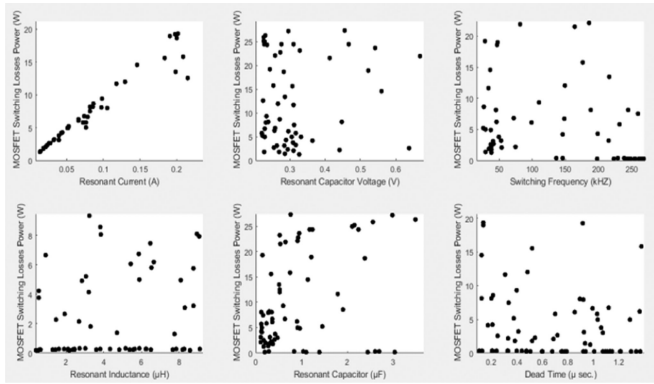

Fig. 9. MOSFET switching loss variation according to SRC design parameter variation.

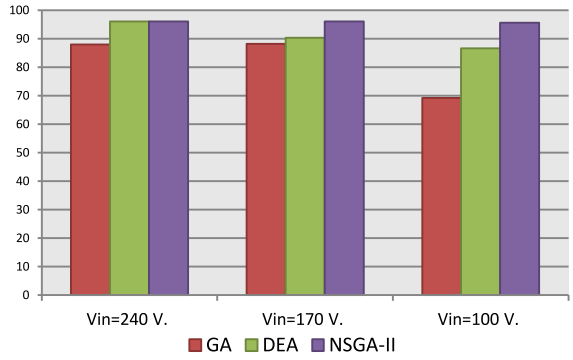

Fig. 10. Efficiency of EA based designs at varying input voltages.

However output regulation is not preserved when input voltage is decreased in region 2. Moreover, NSGA-II provides lower transformer losses compared to GA and DEA with about 56% and 44%, respectively. Amongst them, NSGA-II obtained the smallest error between the desired output voltage and actual output voltage in region 2 with minimum overall losses and the highest efficiency.

Variation of losses according to the optimized parameter values of SRC circuit are given in Figs. 7–9, respectively. It can be observed that higher switching frequency leads to decreased MOSFET switching loss. On the other hand, dead time is one of the main effective parameters on diode conduction loss. Moreover, resonant current that depends on resonant inductor and capacitor has a significant impact on the overall losses.

In this article, NLL & LL optimization and flux density calculation are carried out with nine parameters in order to increase accuracy. Table V provides a comprehensive insight for 5-parameters (5P) model and 9-parameters (9P) model considering single phase transformer design. As given in the table, GA results are not improved with 9P model due to premature convergence. DEA results are improved using 9P model. However, optimized results with 9P model are obtained with the usage of NSGA-II for both loss minimization and flux density calculation.

Fig. 10 shows the comparison of efficiency values of EA based designs at varying input voltages at full load condition. NSGA-II provides more stable efficiency values for the provided input voltage range when compared to other EAs. Moreover, overall performance of EAs is reduced when input voltage is decreased except for NSGA-II.

TABLE VI
OUTPUT VOLTAGE REGULATION USING EA TECHNIQUES FOR 25 RUNS

GA (fs=fr)			
Metric	Vin=240 V.	Vin=170 V.	Vin=100 V.
Min. Vout (V)	90.20	79.67	55.423
Max. Vout (V)	98.16	98.002	74.68
Median (V)	93.621	86.964	66.113
RMSE	0.06725	0.1291	0.360
DEA (fs=fr)			
Metric	Vin=240 V.	Vin=170 V.	Vin=100 V.
Min. Vout (V)	95.005	87.042	82.005
Max. Vout (V)	99.934	94.993	90.287
Median (V)	97.497	90.887	86.409
RMSE	0.0283	0.0932	0.1386
NSGA-II (fs=fr)			
Metric	Vin=240 V.	Vin=170 V.	Vin=100 V.
Min. Vout (V)	96.017	95.073	95.018
Max. Vout (V)	99.990	99.987	98.806
Median (V)	97.754	97.405	96.538
RMSE	0.0242	0.0287	0.0357

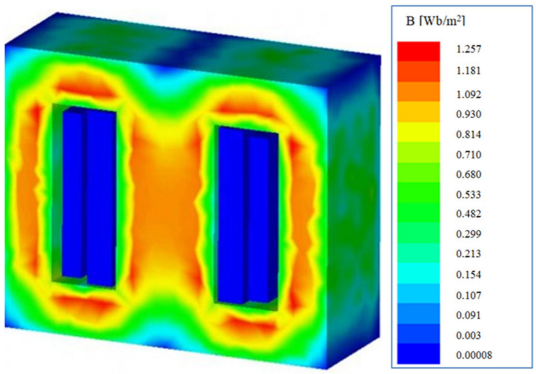

Fig. 11. Single phase transformer flux density calculation using FEM method.

Table VI presents a clear view of output voltage regulation using EA techniques considering varying input voltages. Algorithms were run for 25 times to provide the minimum output voltage, the maximum output voltage, the median and the root mean square error (RMSE) regarding each EA. As given in Table VI, GA delivered a large gap between minimum and maximum output voltages especially for lower input voltages. This is the prime reason of higher RMSE value of GA when compared to that of DEA and NSGA-II. The gap between maximum and minimum values of output voltages is still high for DEA for lower input voltages, but improved when compared with GA. The lowest RMSE and best output voltage regulation is obtained with NSGA-II after 25 runs.

Depending on the best optimization result of NSGA-II amongst the EA methods, SRC design parameters together with the transformer design parameters are selected with NSGA-II for loss minimization and output voltage regulation. Providing the input voltage range and output load variation, the highest efficiency of SRC is obtained when the design parameter values are set, as given in Table VII. Apparent load resistor is calculated for full load condition where $R_{\text{load}} = 750\ \Omega$.

Table VIII shows the impact of each transformer design parameter for calculation of NLL & LL and flux density considering 5P model and 9P model using NSGA-II. It is evident that

TABLE VII
SRC DESIGN PARAMETERS OPTIMIZED WITH NSGA-II

Transformer Design Parameters for NLL & LL			SRC Design Parameters for MOSFET & Diode Losses		
Definition	Unit	Values	Definition	Units	Values
X1	mm	6.12	fs	kHz	130.26
X2	-	55	fr	kHz	130.02
X3	-	320	Lr	µH	0.22
X4	mm^2	6.31	Cr	µF	6.81
X5	mm^2	14.70	N	-	6
X6	mm	7.28	T_{dt}	µs	0.75
X7	mm	4.92	R'_{load}	kΩ	1.12
X8	mm^2	53.67	Co	nF	9.67
X9	mm	5.78	-	-	-

TABLE VIII
COMPARISON OF SENSITIVITY TO TRANSFORMER DESIGN PARAMETERS BETWEEN 5P-MODEL AND 9P-MODEL USING NSGA-II

Parameters.	NLL + LL		B	
	5P Model	9P Model	5P Model	9P Model
X1	3%	10%	1.7%	10.8%
X2	18%	12%	10.5%	18.25%
X3	30.9%	26%	78%	26%
X4	18.3%	9.1%	0.9%	8.1%
X5	29.8%	14%	8.9%	5%
X6	-	13.6%	-	10.3%
X7	-	12.1%	-	13.9%
X8	-	1.5%	-	4.35%
X9	-	1.7%	-	3.3%

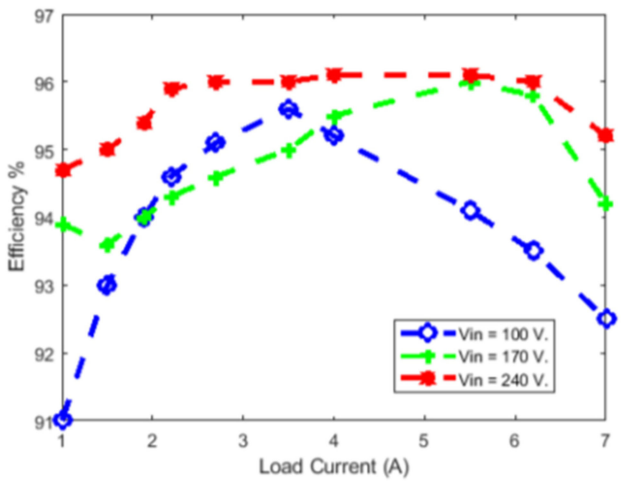

Fig. 12. Efficiency variation of SRC versus load current for input voltages of 100, 170 and 240 V.

in 9P model, the impact of parameters are more distributed than in 5P model, so the sensitivity to transformer design parameters value is decreased. Especially, the impact of X3 in 5P model is 78% while it is decreased to 26% in 9P model for the calculation of flux density. Hence, focusing on adjusting the impact of

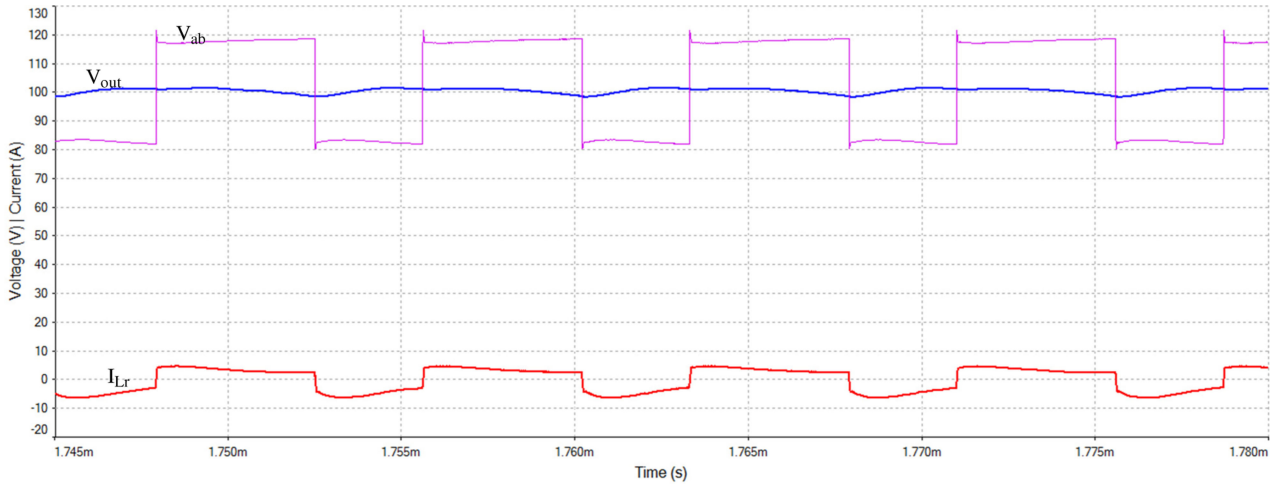

Fig. 13. V_{ab}, V_{out}, I_{Lr} @ $V_{\text{in}} = 240$ V for full load condition.

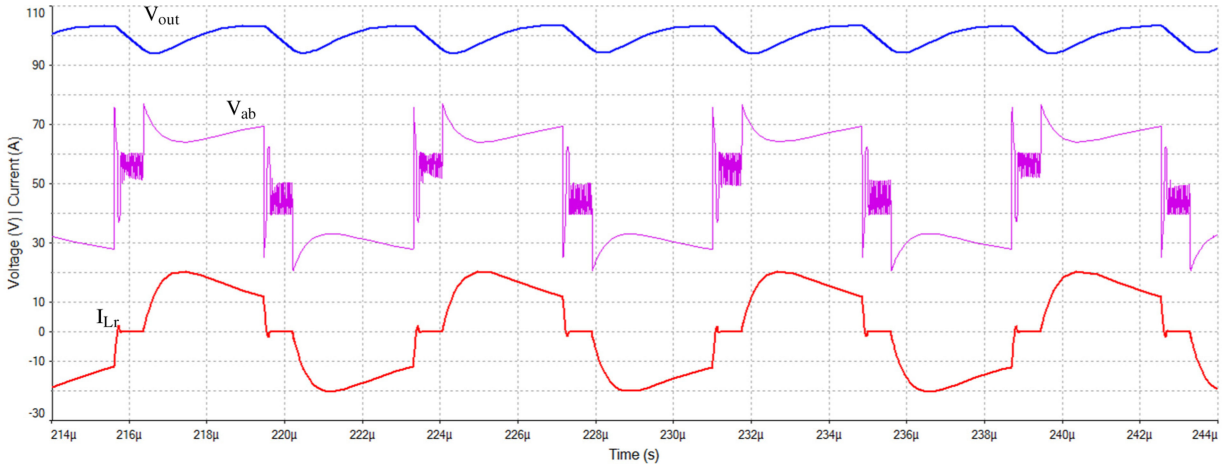

Fig. 14. V_{ab}, V_{out}, I_{Lr} @ $V_{\text{in}} = 100$ V for full load condition.

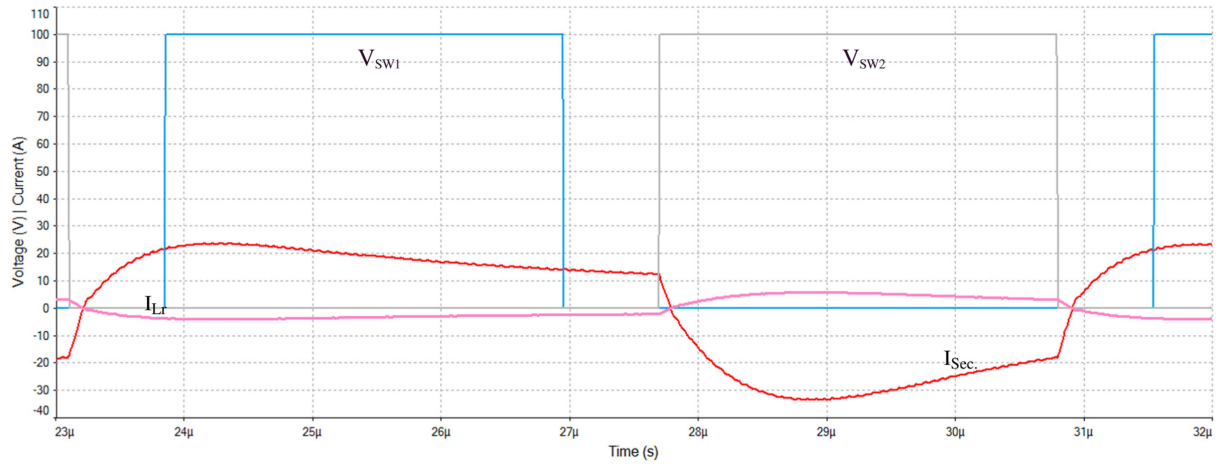

Fig. 15. ZVS condition for NSGA-II based SRC design @ $V_{\text{in}} = 240$ V, $V_{\text{out}} = 100$ V.

transformer design parameters leads to minimizing transformer losses as well as flux density. It is also shown that FEM provides accurate calculation according to optimization of single phase transformer losses and clarify the effectiveness of transformer design parameters.

According to Table VI, NSGA-II combined with a mathematical tool as FEM provided more suitable solutions than other EA techniques. Moreover, NSGA-II is able to search the closest optimal individuals to the desired Pareto-front line. Flux density calculation followed by NLL and LL optimization using NSGA-II and FEM is shown for each part of transformer in Fig. 11.

The efficiency variation of NSGA-II based SRC design versus load current is provided in Fig. 12 for input voltages of 100, 170 and 240 V. Operation in region 2 ($f_s = f_r$) is preferred because of the minimized losses when compared to that of regions 1 and 3. Higher input voltage improves circuit efficiency and output voltage is successfully regulated.

Output voltage and resonant current waveforms of NSGA-II based SRC design are given in Figs. 13 and 14 for full load condition with 240 and 100 V input voltages, respectively. The selection of region 2 depends on high efficiency and the achievement of regulated output voltage. According to the results in Table VI and Figs. 13 and 14, NSGA-II based design results meets ZVS requirements. Therefore, ZVS can be applied at all regions for input voltage range of 100–240 V, as shown in Fig. 15.

V. Conclusion

In this article, GA, DEA and NSGA-II are utilized to optimize SRC design parameters together with single phase transformer design parameters. In addition, operation modes of SRC are analyzed to determine the optimal operating conditions according to PV voltage and load variations. MOSFET & diode conduction losses, MOSFET switching losses, transformer NLL & LL and output voltage regulation are derived as the cost functions to be minimized. Flux density is calculated using FEM to demonstrate the effectiveness of the optimized parameters on transformer design. In this article, 8 parameters for MOSFET & diode losses and 9 parameters for single phase transformer losses are optimized. It is also proved that using 9P model for transformer design decreases sensitivity when compared to 5P model.

Considering optimization performances of EAs, GA sometimes diverges from optimal solutions. In early stages of iteration, GA may cause a premature convergence such that resonant frequency is determined far from the global solution as soon as lower switching losses is achieved regardless of output voltage regulation. DEA is very sensitive to population size, mutation and crossover probability. Increasing crossover probability leads to quicker convergence with a strong possibility of missing the optimal solutions. While smaller crossover probability is able to slow down the optimization process and thus DEA requires more iterations than GA and NSGA-II. A large population size ensures that solutions are adequate for mutation which is computationally long. NSGA-II selection process differs by means of ranking best solutions and crowding distance evaluation. Therefore solutions can be spread closer to the global minima value than that of GA and DEA as given in Tables IV–VI. Achieving better rank or higher crowding distance, individual solutions are to be proceeded further with a better chance to be reproduced.

The importance of artificial intelligence based automated design in power electronics is growing as the design parameter selection for complicated circuits requires enormous search space. Moreover, parametric automation of circuit design provides faster optimization than trial and error methods. This article proves that NSGA-II, as one of the state-of-art EA techniques, is very suitable for multi-objective optimization of SRC circuit having a large number of design parameters to be properly selected. It is also shown how to find the optimal balance between the robustness and loss minimization in SRC with respect to several design constraints and specifications.

As further work, the proposed methodology will be enhanced for more improvements in the challenging issues of power electronics circuit design.

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