Design of a GaN-Based Interleaved Nine-Level Flying Capacitor Multilevel Inverter for Electric Aircraft Applications

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***Abstract*—Multilevel inverters such as the flying capacitor multilevel inverter (FCML) hold large potential benefit in applications where the size and weight of the inverter is constrained. This article presents the design and implementation of an inverter module that incorporates two individual nine-level FCML single-phase inverters in an interleaved design. Each inverter utilizes GaN field-effect transistors (FETs) switching at 100 kHz for an effective inductor ripple frequency of 800 kHz. The implementation features an innovative dual-sided integrated switching cell layout, which decreases the commutation loop inductance of the inverter and allows fast switching with minimal ringing, while also enabling efficient double-sided cooling. The switching cell layout is particularly well suited for high-voltage applications, as creepage and clearance requirements can be easier met compared to single-sided solutions. The effectiveness of the approach is demonstrated in a hardware inverter prototype intended for driving low-inductance electric machines for future electric aircrafts. The 1000 $\mathrm{V_{dc}}$ to 380 $\mathrm{V_{ac,rms}}$, 6-kW prototype achieves a peak efficiency of 98.6% and a peak power density of 15 kW/kg.**

***Index Terms*—DC–AC power converters, electric flight, flying-capacitor multilevel, multilevel power converter.**

I. Introduction

CATALYZING the electrification of transportation is one avenue for increasing energy efficiency and reducing fuel burn emissions such as carbon dioxide and oxides of nitrogen (NOx). For subsonic aircraft in particular, an examination of the fuel usage by all classes of commercial aircraft highlighted that single-aisle aircraft carrying between 100 and 200 passengers consume approximately 55% of all aircraft fuel [1], [2]. The National Aeronautics and Space Administration's Aeronautics Advanced Air Transport Technology (AATT) project estimates that hybrid-electric aircraft could achieve reductions of 33% in fuel consumption, 55% in NOx emissions at cruise, and 60% in NOx emissions at landing and take-off [1], [2]. Yet, the adoption of a more-electric powertrain for aircraft to reduce this fuel burn during landing, take-off, and cruise has been hindered by improvements in conventional propulsion technology. Over past 60 years, the gas turbine engine for aircraft has been optimized to obtain a 350% increase in the thrust-to-weight ratio and a 45% improvement in efficiency [2]. Thus, for an electrified powertrain to compete against advancements in gas turbine engine technology, both the efficiency and the specific power density, i.e., the power-to-weight ratio (kW/kg), of the electric system—including the electric machines and power electronics—must dramatically increase compared to the current state-of-the-art [3]–[7].

A recent survey of high specific power density electric machines revealed that permanent magnet synchronous machines hold great promise as an enabling technology for a more-electric aircraft powertrain [8]. Since this design choice results in increasing the operational frequency and reducing the amount of iron in the machine, the corresponding low winding reactance indicates that a traditional two-level inverter would require large output inductors to filter switching frequency harmonics in the output current [5], [8], [9]. Moreover, it is desirable to achieve low total harmonic distortion (THD) of the currents in the machine to reduce losses for this subsystem.

Flying capacitor multilevel inverters with an increased number of levels have been demonstrated as a viable approach to provide sinusoidal currents with low distortion for loads with negligible inherent filtering, while simultaneously increasing inverter specific power density and efficiency [10], [11]. Multilevel topologies enable the reduction in the size and weight of inverter filter components because of the reduced harmonic content of the multilevel waveform. Hybrid inverters combining neutral point clamped and flying capacitor inverter elements that can achieve very high efficiency have also been reported [12]. The hybrid approach reduces the number of flying capacitors needed for a certain number of voltage levels, and also the number switches operating at high frequency. This comes at the cost of requiring a number of switches with higher blocking voltage and, more

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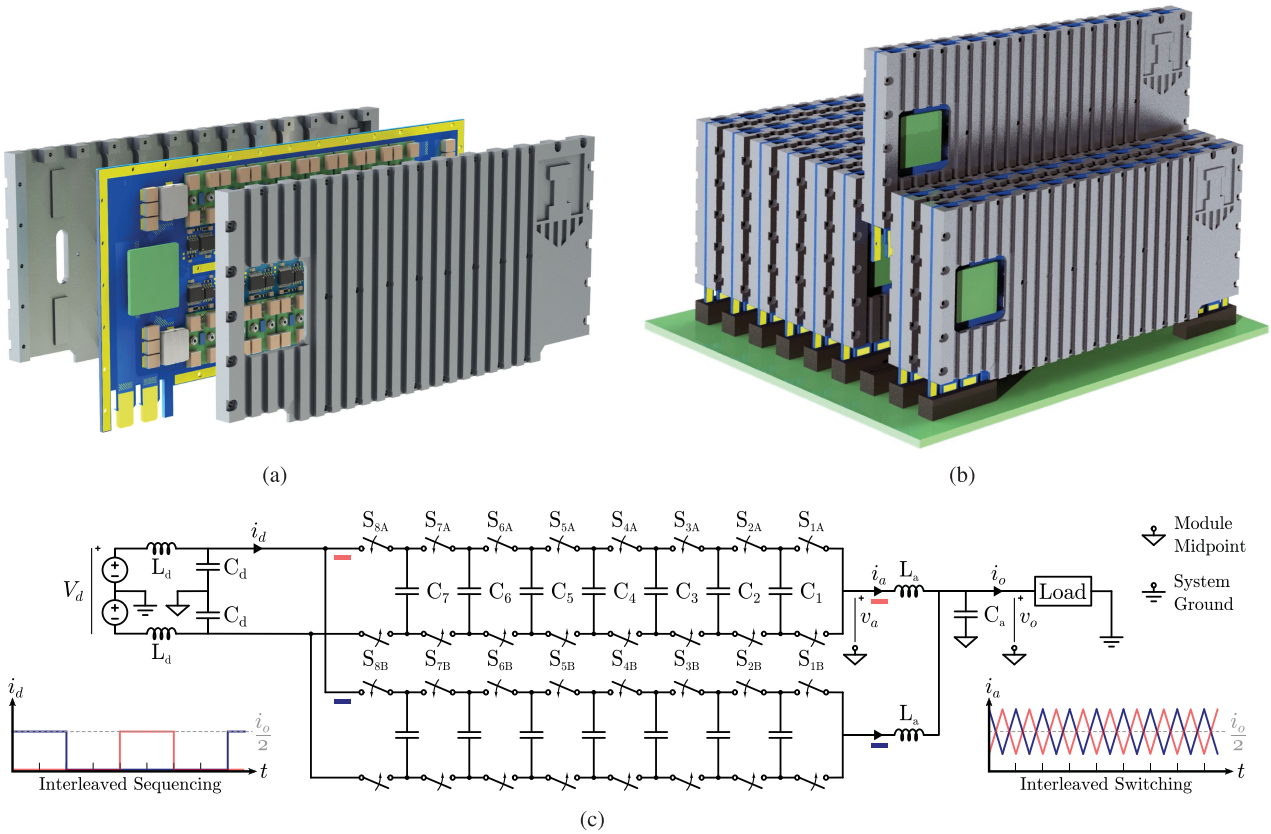

Fig. 1. Dual-interleaved, nine-level FCML inverter system for electric aircraft propulsion. (a) One 10–20 kW interleaved FCML inverter module. (b) Mainframe concept demonstrating paralleled modules. (c) Schematic of the interleaved FCML inverter module showing illustrative current waveforms.

TABLE I
TARGET INVERTER SPECIFICATIONS

DC input voltage	1000 V
AC RMS output voltage	353 V
Output power	10-20 kW
Output frequency	0-3 kHz
Efficiency	$\geq$ 98%
Specific power density	$\geq$ 12 kW/kg

importantly, concentrating the switching losses in fewer switch devices.

The advantages of the multilevel approach are the foundation for developing an inverter to meet the The National Aeronautics and Space Administration's (NASA) Aeronautics Advanced Air Transport Technology (AATT) targets for a more-electric powertrain outlined in [13]. In an aircraft application, several multilevel converters can be connected in parallel to provide higher power and redundancy. The key specifications for one module within such a converter are given in Table I, with the dual interleaved flying capacitor multilevel (FCML) inverter module presented in this article shown in Fig. 1. While operation principles of the FCML inverter can be found in [11], [14], and [15], this article outlines the design of a low inductance, interleaved, nine-level, GaN-based, FCML inverter and how double-sided layout enables both isolation and low inductance.

This article extends our previous conference publications on this topic [16], [17], with a more detailed loss model, additional experimental measurements, and added descriptions of the hardware. The remainder of this article is organized as follows: First, Section II details how models for the loss components of the FCML converter utilizing gallium-nitride (GaN) field-effect transistors (FETs) in dc–dc operation were developed, verified with experimental observations, and incorporated into a Monte Carlo optimization. Then, Section III explains how a design was selected from the Pareto-optimal front from this optimization, which revealed a clear tradeoff between the relative weight and relative losses of the randomized solutions. After reviewing the basic structure and operation of the interleaved FCML inverter, Section IV then introduces the inverter design of this article with specific consideration of the tradeoffs between a lateral (single-sided) and vertical (double-sided) layout on the commutation loop inductance and component isolation. Finally, Section V reports experimental results and analysis from the operation of a hardware prototype for different power and voltage levels.

II. LOSS MODELING

To facilitate the optimal design of high efficiency FCML inverters, we first seek to model the most pertinent losses. While

some are dependent on switching frequency, many converter losses also exhibit a nontrivial correlation to the output voltage and current. The losses considered in the efficiency calculation employed here were: transistor conduction, switching (overlap and output capacitance related), flying capacitor and input and output inductor losses. Each is computed at the instantaneous operating point over a discrete number (1000) of time-steps for one fundamental period, and the resulting efficiency is calculated from the averaged losses.

A. Switching Losses

The switching losses in hard-switched converters is generally dominated by so called overlap losses, i.e., losses due to nonzero current and voltage overlapping during the transitions between the transistor ON and OFF states, and lossy charging/discharging of parasitic capacitances. To compute the overlap losses the duration of the overlap is needed. It can be calculated using an equivalent gate charge, $Q_{\rm gsw}$, which describes how much charge is needed to make the transition between ON and OFF states. Different driving voltages and gate resistances can result in nonequal turn-ON and turn-OFF times

$$t_{\rm on} = R_{\rm gon} \cdot Q_{\rm gsw}/(V_{\rm drv} - V_{\rm th}) \tag{1}$$

$$t_{\rm off} = R_{\rm goff} \cdot Q_{\rm gsw}/V_{\rm th} \tag{2}$$

where $R_{\rm gon}$ and $R_{\rm goff}$ are the turn-ON and turn-OFF gate resistances, $Q_{\rm sw}$ is the equivalent gate charge at the given drain–source voltage and $V_{\rm drv}$ and $V_{\rm th}$ are the gate drive supply and GaN transistor plateau voltages, respectively.

To account for full and partial soft-switching at turn-ON, an effective drain–source voltage, $v_{\rm dse}$, is also calculated to account for the lossless discharge of the parasitic capacitances during the commutation deadtime. First consider the high-side switches switches $\rm S_{1A}$...$\rm S_{8A}$. For positive output currents ($i_a > 0$), the drain–source voltage is clamped by the diode-like conduction of the low-side switches and the deadtime does not reduce this voltage. For $i_a < 0$, the drain–source voltage of the high-side switch is reduced at a rate of $i_a/(2C_{\rm oss})$ during the deadtime. If the deadtime is sufficiently long, full discharge of the parasitic capacitances can be achieved and the voltage is clamped close to zero by the diode-like conduction of the high-side switch. Consequently, the effective drain–source voltage for a high-side switch at turn-ON is

$$v_{\rm dse} = \begin{cases} V_{\rm ds} & \text{if } 0 < i_a, \\ V_{\rm ds} - \frac{t_{\rm de}|i_a|}{2C_{\rm oss}} & \text{if } -\frac{2V_{\rm ds}C_{\rm oss}}{t_{\rm de}} < i_a < 0 \\ 0 & \text{if } i_a < -\frac{2V_{\rm ds}C_{\rm oss}}{t_{\rm de}} \end{cases}$$

where $t_{\rm de}$ is the effective deadtime, including both deadtime introduced by the control and deadtime produced by any nonequal delay in turn-ON and turn-OFF. $V_{\rm ds}$ is the nominal drain–source voltage calculated by

$$V_{\rm ds} = \frac{V_d}{N-1} \tag{3}$$

where V_d is the inverter input voltage and N is the number of voltage levels (e.g., $N = 9$ in the design of Fig. 1). The overlap turn-ON and turn-OFF losses can then be calculated by

$$P_{\rm ton} = \frac{1}{2} f_s t_{\rm on} v_{\rm dse} |i_a| \tag{4}$$

$$P_{\rm toff} = \frac{1}{2} f_s t_{\rm off} v_{\rm dse} |i_a|. \tag{5}$$

Expressions for the low-side drain–source voltages at turn-ON can be derived in an analogous fashion.

As a FET turns ON, it will discharge its parasitic output capacitance and simultaneously charge the parasitic output capacitance of the complementary FET in a lossy manner. Therefore both capacitances contribute to the losses in the FET, and this loss can be calculated by

$$P_{\rm coss} = \frac{1}{2}(2C_{\rm oss}) \cdot v_{\rm dse}^2 f_s. \tag{6}$$

B. Conduction Losses

The conduction losses are calculated as

$$P_{\rm cond} = D R_{\rm dson} i_a^2 \tag{7}$$

where D is the cycle duty. The ON-state resistance of the GaN switches used has a fairly strong temperature dependence, so an effective resistance adjusted for an expected temperature rise based on the expected performance of the heatsink and thermal interface material is employed in this article. Furthermore, many GaN HEMT devices have been plagued by so called dynamic ON-state resistance phenomena, where the ON-state resistance dramatically increases dependending on the voltage applied in the OFF-state. While the dynamic ON-state resistance has been improved in newer GaN devices, high OFF-state voltage can significantly increase the conduction losses. Given enough time the ON-state resistance decays back to lower value, so in theory a loss model should take into account both voltage and time dependency. However, based on the long decay time constants reported in [18], in most practical applications the dynamic contribution to the ON-state resistance can be accurately modeled by a fixed coefficient calculated from the maximum voltage applied in the OFF-state.

Another effect that can increase the GaN conduction losses is the diode-like conduction mode used during deadtime, but for the deadtimes and switching frequencies considered these losses are negligible. The losses associated with charging and discharging of the gate capacitance are also sufficiently small in this application to be negligible. Capacitor losses were calculated using a fixed, equivalent series resistance and the inductor losses using conduction and core losses approximating manufacturer-provided data. We note that early experimental work evaluating ceramic capacitors has indicated an increase in effective equivalent series resistance (ESR) with dc bias [19]. This effect is not modeled here, but could be explored in future work.

C. Experimental Verification

To verify the model, the loss components calculated for a three-level FCML converter in dc–dc operation for different output currents were compared to measurements on a lab prototype.

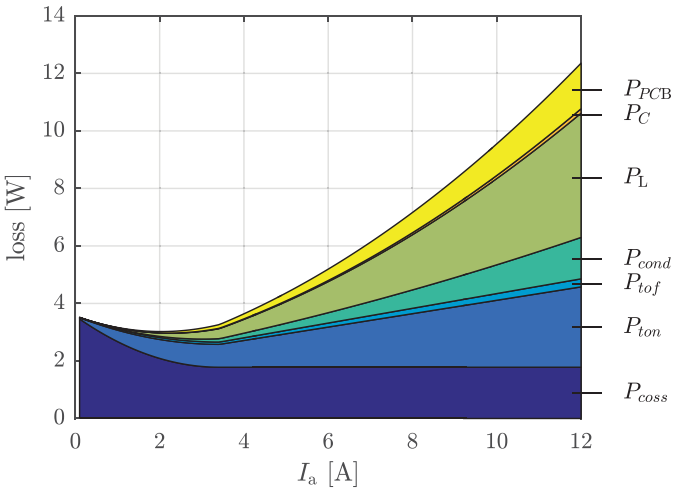

Fig. 2. Calculated loss components for a three-level FCML in dc–dc operation. Switching frequency $f_s = 180$ kHz.

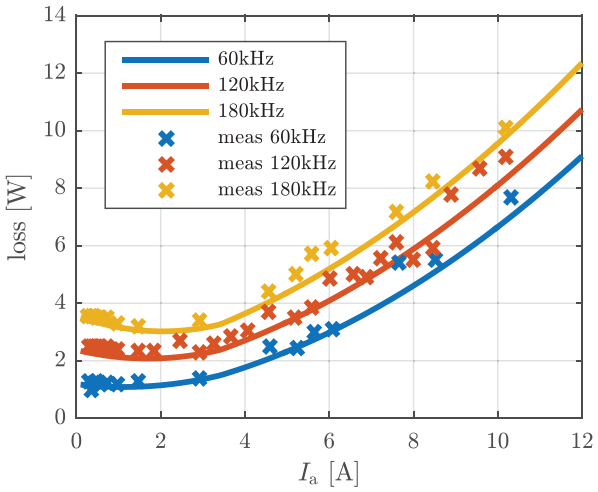

Fig. 3. Comparison of calculated (solid lines) and measured losses for a three-level FCML converter in dc–dc operation.

To allow a direct comparison, the model includes conduction losses in the printed circuit board (PCB) using a measured resistance for the prototype used. A breakdown of the calculated losses for one operating point is shown in Fig. 2, while total calculated losses at three different switching frequencies are compared to measurements in Fig. 3. The loss model shows the increase in switching losses (P_{coss}) at low output currents as less soft-switching is achieved, i.e., the parasitic capacitances are not fully recharged during the deadtime.

III. Monte Carlo Optimization

The FCML topology offers a wide design optimization space. To address this challenge, a Monte Carlo approach was adopted. First, a small number of prospective capacitors and inductors, where selected based on prior work [10], [11]. This article was also the basis for selecting a limited range of voltage levels (9 and 10), rated output currents (10–50 A in 1 A increments) and switching frequencies (10–500 kHz in 1 kHz increments) for the Monte Carlo study). From this a large number (50 000) of randomly selected designs were then generated, with the constraints and randomized input variables used listed in Table II.

TABLE II
Monte Carlo Variables and Constraints

Randomized Input Variables
Type and number of flying capacitors
Type and number of filter inductors
Number of voltage levels
Switching frequency
Gate resistance (switch transition speed)
Current loading
Design Constraints
Maximum transistor drain-source voltage
Converter output current ripple
Inductor peak current, i.e. saturation
Capacitor peak current, limited by losses

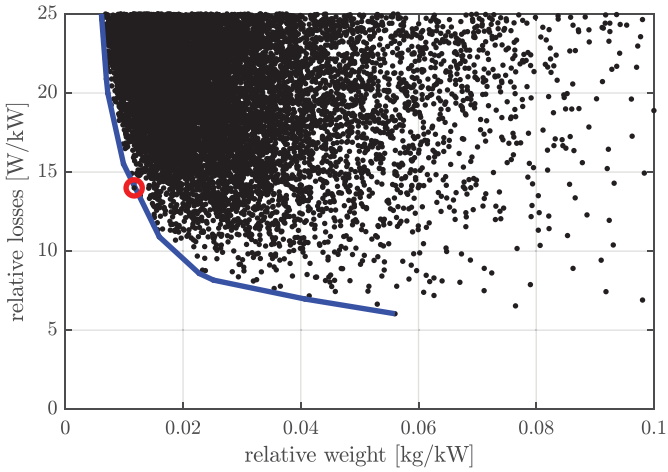

Fig. 4. Calculated performance of randomized designs. Each dot represents a separate inverter design and the Pareto-optimal front is marked in blue.

Designs not satisfying the constraints were removed from the set, while those that remained were evaluated based on calculated efficiency and weight. The weight estimates were based on the known weight of the passive components for a given design and an estimated weight of PCB and heatsink based on the board area needed for the design.

All randomized designs satisfying the constraints are shown in Fig. 4, where each dot represents a separate design plotted against the key performance metrics. Also shown is the Pareto-optimal front, which directly highlights tradeoff between efficiency and power density for this particular type of converter. The design chosen for the hardware prototype is marked by a red circle, with the component selection detailed in Table III.

IV. Inverter Design

The high effective switching frequency offered by FCML inverters allows the size of the filters to be made very small.

TABLE III
COMPONENT LIST FOR DESIGN CANDIDATE

Component	Part Number	Parameters
GaN switches	EPC - EPC2034	200 V, 7 mΩ
GaN gate driver	TI - LM5114	GaN driver
GaN gate resistors		30 Ω
Flying capacitors	TDK - C5750X6S	2.2 μF
Input inductors	Vishay - IHLP5050CE	10 μH
Output inductors	Vishay - IHLP5050CE	10 μH
Digital isolators	Silicon Labs - Si8423BB	
Power isolators	Analog Devices - ADUM5210	

This reduces or eliminates potential problems that can arise with unfiltered converter outputs, most importantly it reduces cable-coupled radiated electromagnetic interference (EMI), reduces capacitive currents, and avoids high dv/dt voltage stress of motor windings. The design described herein incorporates two converters in parallel to allow for further reductions in filter size through interleaving and ripple cancellation. Interleaving of three-level FCML converters has been proposed for both isolated [20] and nonisolated dc–dc converters [21], [22] to reduce the size of magnetic components.

As illustrated in Fig. 1(c), operating the two FCML converters with their respective switching phase-shifted by 180°, largely cancels the output current ripple of the two converters due to the triangular shape of the waveforms. This allows the use of large inductor current ripple in each interleaved phase and less output filter capacitance, thereby reducing output filter losses and mass while providing high bandwidth control of the output waveform. At the input side, the current ripple waveforms of the two converters have rectangular shapes. By interleaving the switch sequencing between the two phases the ripple frequency can be effectively doubled, thereby reducing the requirements on the input filter.

Fig. 1(c) also illustrates the use of a split dc bus. Combined with the vertical design introduced in the next section, this limits the maximum ground-referenced voltage on the converter to half of the total dc voltage—easing component and insulation requirements. The schematic also defines a separation between the module midpoint and the system ground. Though these nodes are virtually equivalent, they need not be explicitly connected, or may be connected through a high-frequency choke. Accordingly, the high-frequency switching currents filtered through C_a are returned through the dedicated module midpoint. As such, the input filter components, C_d and L_d, are sized to provide a low-impedance return path on-module and prevent the conduction of switching currents to the system supplies, while not adding unnecessary losses or mass. The design of the input filter depends on external requirements, but in general a filter corner frequency well below the ripple frequency is desired in order to suppress switching noise, both fundamental and harmonics. As the converter module is intended to be run in parallel with other converter modules, where a common filter on the dc bus can provide additional filtering, a relatively high corner frequency of half the switching frequency is used for this design study. It should be noted that compared to the flying capacitors the input filter capacitors carry a much larger rms current. Therefore, in a design optimized for efficiency and mass the input filter capacitance will be much larger than the flying capacitors, assuming that the same capacitor technology is used for both.

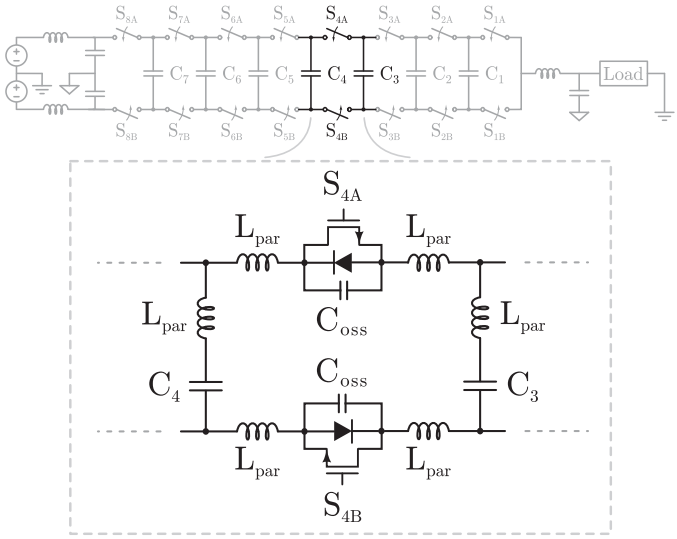

Fig. 5. Commutation loop between a given pair of complementary switches in a single nine-level FCML inverter.

A. Dual-Sided Converter Layout

The GaN switches in Table III enable designs that are simultaneously low loss and low weight. However, leveraging these devices in FCML converters requires mitigation of the parasitic inductance in the commutation loops. Fig. 5 illustrates this inductance, $L_{\rm par}$, arising between a given set of complementary switches in a nine-level FCML inverter. Here, the commutation loop is formed by the two switches, $S_{4\rm A}$ and $S_{4\rm B}$, and the neighboring flying capacitors, C_3 and C_4. At each switch transition a resonant circuit formed by the parasitic inductances and the parasitic output capacitance, $C_{\rm oss}$, of the GaN FETs is excited. This resonance can give rise to large voltage oscillations across the FETs when they are switched quickly with low gate resistance, potentially stressing the switches beyond their rating and causing EMI issues.

In many ways this is similar to the commutation loop in conventional two-level converters, but the addition of the two flying capacitors together with a high-voltage stand-off requirement makes the minimization of the loop inductance difficult. As the single loop inductance of Fig. 5 is connected to a series of other adjacent switches and flying capacitors, the overall converter current flow must also be considered during layout. While ringing can be reduced by slowing down the switch transition, e.g., by increasing the gate resistance, this increases switching losses and limits the maximum switching frequency which may be used. Thus, the incentive to minimize the loop inductance is threefold: a faster slew rate will decrease overlap losses, reduced overshoot will lessen device stress, and damped ringing will mitigate EMI.

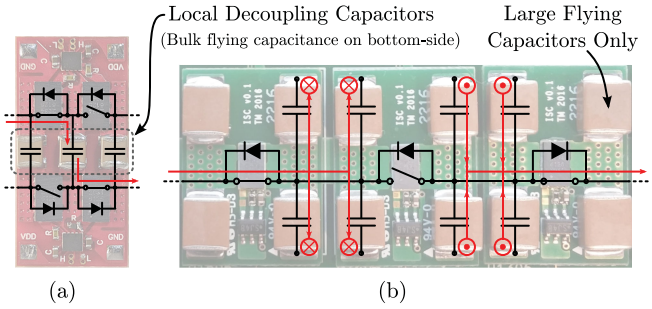

Fig. 6. Side-by-side comparison of lateral and vertical layouts. (a) Lateral. (b) Vertical.

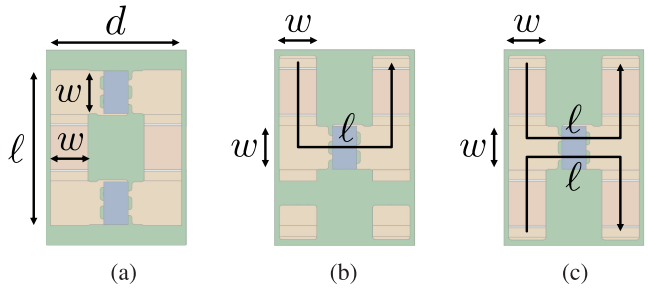

Fig. 7. Dimensions used in the commutation loop inductance calculations (8) and (10) for the lateral and vertical layouts. (a) Lateral. (b) One-branch. (c) Two-branch.

In a lateral switching cell layout illustrated by the hardware in Fig. 6, the flying capacitors are located on the back-side of the PCB and small decoupling capacitors are next to the switches to reduce the effective parasitic inductance. Therefore, the principal commutation loop is formed in the plane of the PCB, and its dimensions are dictated by the creepage requirements. Modeling the commutation loop as a flat rectangle of width d, length ℓ, and trace thickness w, as indicated in Fig. 7(a), the inductance can be shown from [23] to be approximately

$$L_{\text{lateral}} = \frac{\mu_0}{\pi}\left(\ell \cdot \ln\left[\frac{2d-w}{w}\right] + d \cdot \ln\left[\frac{2\ell - w}{w}\right]\right). \quad (8)$$

Thus, there is a direct tradeoff between creepage distance (which drives the length ℓ) and commutation loop inductance in lateral layouts of FCML converters; as the required creepage distances increase so does the parasitic loop inductance. While [10] has shown that local bypass capacitors can be used to reduce the effective commutation loop inductance, maintaining adequate creepage and clearance at voltages near the 1 kV design target is challenging using this approach.

Fortunately, a two-sided layout can be implemented to utilize the dielectric properties of the PCB core material (typically FR-4 glass-fiber-epoxy) to provide a much more advantageous tradeoff between voltage isolation capability and commutation inductance. The voltage stress is then mainly across the PCB thickness, t_{PCB}, which has a much better insulation characteristics than air. This two-sided layout allows the complementary switch devices to be placed in close proximity vertically, separated by a thin layer of PCB material. Even for converters in the multiple-kilovolt range, the PCB thickness is likely to be limited by mechanical concerns rather than electrical requirements.

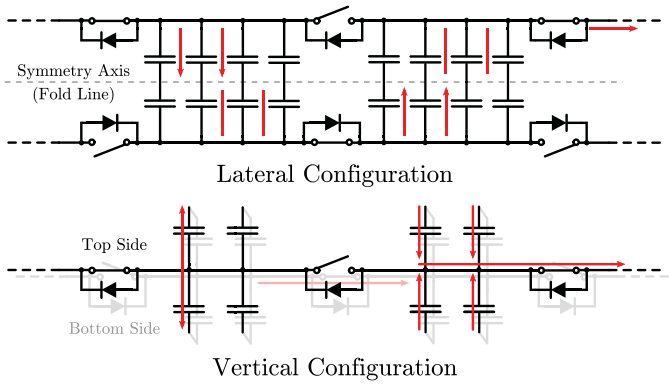

Fig. 8. Schematic demonstrating that a folded lateral layout yeilds the lower inductance, dual-sided, vertical configuration.

This vertical layout can intuitively be visualized as a folding of the lateral layout along the horizontal symmetry axis, as shown in Fig. 8. The magnetic flux of the commutation loop is then forced to pass between the traces (or capacitors) through the thin, cross-sectional area of the PCB over a distance equivalent to the PCB trace (or capacitor) width, w. These dimensions, along with PCB trace (or capacitor) length, ℓ, are shown in Fig. 7(b). For the geometries considered, i.e., wide and closely spaced traces, the reluctance of the flux path between the traces is much larger than the reluctance of the return path on the outside. Furthermore, for such geometries the flux density between the traces is more or less constant over the cross section. Therefore, the commutation loop reluctance can be approximated, with little loss of accuracy, as

$$\mathcal{R} \approx \frac{w}{\mu_0 \cdot A_{\text{PCB}}} \quad (9)$$

and the inductance as

$$L_{\text{vertical}} = \frac{1}{\mathcal{R}} \approx \frac{\mu_0 \cdot \ell \cdot t_{\text{PCB}}}{w} \quad (10)$$

where t_{PCB} is the PCB thickness. A symmetric commutation path may be implemented in parallel on the opposite side of the switch, effectively halving this inductance for the "two-branch" case of Fig. 7(c). The capacitors of adjacent switching cells also provide parallel paths (branches) that further serve to reduce the inductance, as shown in Fig. 9.

One noticeable element of the vertical layout in Figs. 8 and 9 is the use of series connected capacitors. Specifically, there are four parallel sets of two series-connected capacitors situated between each of the GaN switches in the inverter. This approach is followed in order to accommodate the ceramic capacitors specified in Table III. These capacitors were found to have the highest energy density available on the market at the time of writing [24]; However, their voltage rating dictates that two capacitors must be used in series to meet the converter specifications, while the available capacitance required paralleling for this design. Nonetheless, this solution uses only the large flying capacitors (no local bypass capacitors), thereby achieving creepage requirements through appropriate component selection—and the

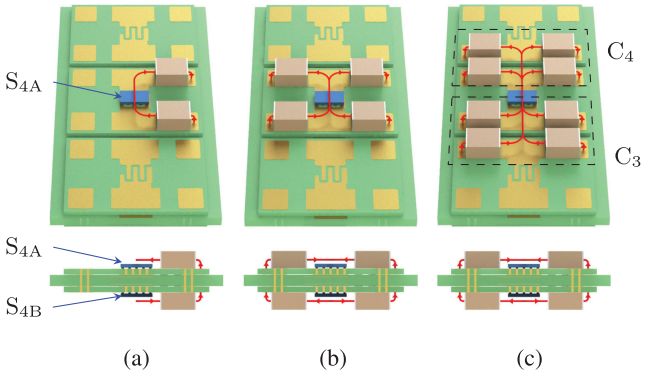

Fig. 9. Illustration of the vertical layout commutation loops. (a) One branch. (b) Two branches. C4 C3. (c) Four branches.

TABLE IV
SIMULATED AND MEASURED COMMUTATION LOOP INDUCTANCE

	Inductance @ 100 MHz	
Branches	Simulated	Measured
1	10.3 nH	11.1 ± 0.34 nH
2	7.17 nH	7.26 ± 0.28 nH
4	6.17 nH	6.68 ± 0.26 nH
Electrically Thin Design		
1	3.58 nH	3.08 ± 0.22 nH
2	2.42 nH	2.61 ± 0.20 nH
4	2.32 nH	2.50 ± 0.20 nH

current loop area is thus restricted only by the necessary PCB thickness. An experimental comparison to the design of [10] is not directly applicable due to the mismatch in clearance requirements. However, examination of the differences between layouts of compatible specification—and the broader applicability of the electrically thin approach, introduced in the next section, on lateral designs—is an area of active research.

Finite element analysis with Ansys Maxwell was used in [16] to estimate the commutation loop for each of the configurations in Fig. 9. In this article, these inductance values were recalculated for the fabricated designs with Ansys Q3D, and are listed as the first three entries in Table IV. To isolate contributions to the loop inductance from the PCB layout, the flying capacitor pads were shorted with copper strips in the simulation. Measurements performed using a high frequency impedance analyzer[1] are also reported in Table IV and include error calculated as specified in the equipment datasheet. The test frequency of 100 MHz was chosen to both assist in measuring the very small inductances, as well as match the order of magnitude at which hard-switched ringing is commonly observed. The inductance measurement setup is shown in Fig. 10, where the inset photo also features the use of physical copper strips to short the flying capacitor terminals so as to measure only the inductance contributed by the PCB.

[1]Keysight E4990A with 42941A impedance probe.

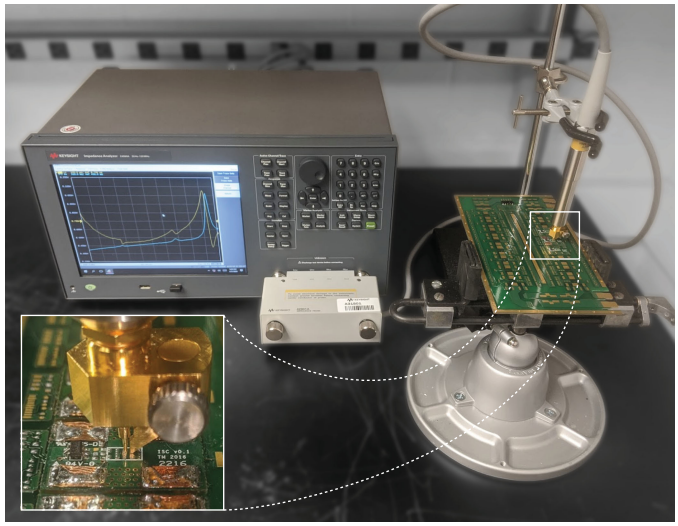

Fig. 10. Impedance analyzer and probe used to measure the commutation loop inductance. After calibration is carried out to the adaptor tip endpoint (inset), the loop impedance between the drain to source pads can be measured with high accuracy.

TABLE V
MEASURED LOOP INDUCTANCE AND OVERSHOOT WITH CAPACITORS POPULATED FOR THE GIVEN NUMBER OF PARALLEL BRANCHES

Branches	Inductance @ 100 MHz	Overshoot
1	12.2 ± 0.35 nH	44.2 %
2	7.44 ± 0.28 nH	24.4 %
4	6.75 ± 0.27 nH	21.3 %
Electrically Thin Design		
1	4.49 ± 0.24 nH	21.3 %
2	3.60 ± 0.22 nH	18.5 %
4	3.22 ± 0.22 nH	15.7 %

With the flying capacitors populated, the inductance for each configuration was again measured and is reported in Table V. Due to the package inductance associated with the X6S capacitors used, the overall loop inductance can be seen to increase with the populated board. However, the impedance is still clearly dominated by the PCB routing. Additionally, the hard-switched overshoot, arising from the loop inductance oscillating with the capacitance of the EPC2034 GaN FET of this design, was obtained using the circuit shown in Fig. 11. Resistors R_1 and R_2, both 470 Ω, isolate the commutation cell from the parasitic capacitance of the voltage source, while R_3 (33 kΩ) provides a path for a low but nonzero current (∼4 mA) to bias the complementary switch (S_{4A}) in the ON-state prior to the turn-ON of S_{4B}. An ultraminiature coaxial connector was affixed in tight proximity to the drain and source terminals of S_{4A} and, when used with a high-bandwidth passive probe[2] and associated coaxial accessories, provided a high-fidelity measurement of v_{ds}.

[2]Keysight N2894A 700 MHz passive probe.

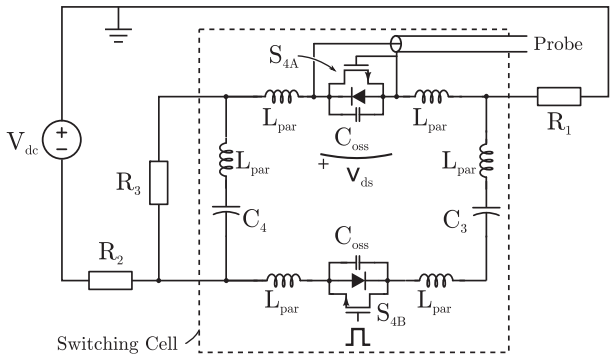

Fig. 11. Test circuit used for measuring commutation overshoot during hard switching. The ground referenced source of S_{4A} allows for a high-fidelity, single-ended measurement.

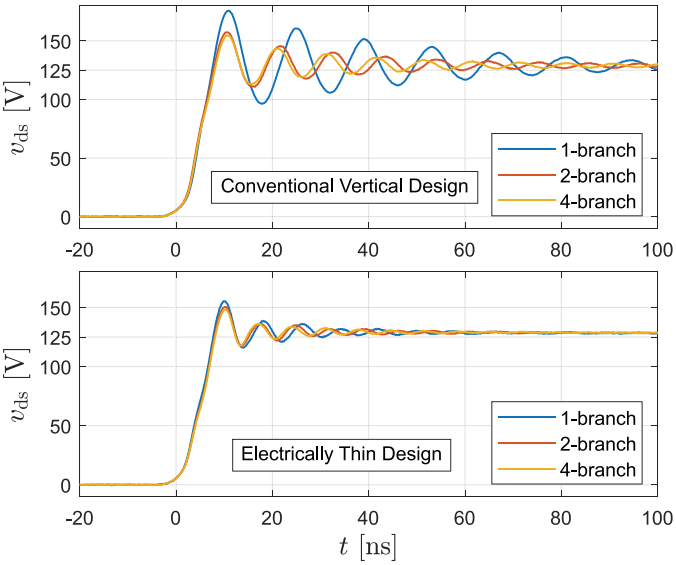

Fig. 12. Experimentally measured hard-switched overshoot for different number of parallel capacitor branches mounted.

Careful measurements of the specified EPC2034 GaN FETs and a 10 Ω gate resistance produced the hard-switched $v_{\rm ds}$ waveforms in Fig. 12, shown at the nominal operating point of 125 V for a nine-level design with a 1 kV dc bus. Combining the 6.75 nH of the four-branch configuration used in this design in series with the typical ∼0.5 nF drain–source capacitance of the EPC2034 GaN devices, yields a ringing frequency of 84 MHz—in agreement with the observed ringing. From both the simulated and experimental results, it can be noted that the addition of a second branch reduces the inductance and overshoot significantly. However, further parallel paths from adjacent switching cells have a diminishing effect.

B. Electrically Thin Switching Cells

In Fig. 9, the commutation loop is shown to span across three PCBs: the converter motherboard with two complementary integrated switching cell PCB modules, each containing a switch and half of the series flying capacitance, mounted to the top and bottom. Designers have previously discounted dual-sided

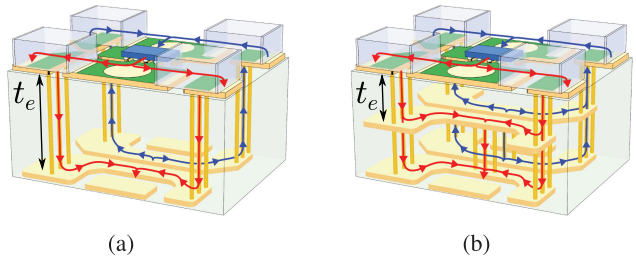

Fig. 13. Inner routing and 3-D commutation paths for ISC modules in FCML converters with vertical layouts. (a) Traditional two-layer design. (b) Electrically thin design.

designs due to the relatively large cross-sectional area realized from vias connecting complementary transistors on the top and bottom layers of a PCB [25], [26]. However, as the loop area in the vertical layout is primarily driven by the thickness between electrical layers, a physically thinner substrate could be used to reduce the inductance. Standard two-layer FR4 stack-ups can be found down to 0.25 mm thickness while designs on polyimide cores around 0.025 mm thick are possible. Yet physically thin circuit assemblies pose manufacturing and reliability concerns—especially with chip-scale packages common in GaN devices.

A more robust option leverages the use of inner layers and blind or buried vias to make the ISC "electrically thin" [27]. This concept is demonstrated in Fig. 13: the two-layer ISC concept in Fig. 13(a) can be migrated to a four-layer FR4 stack-up of comparable thickness in Fig. 13(b) (inner layers shown collapsed for simplicity). Here, the loop area is confined to the substrate between the uppermost inner layer and the top layer and scales with substrate thickness, t_e. In practical implementations, t_e can be as low as 0.11 mm for standard 0.8 mm thick four-layer stack-ups. Thus, $t_{\rm PCB}$ from (8) for the ISC would appear 1/8 as thick electrically. This design is further improved by tightening the ISC module footprint, drawing the current path toward the center of the module. Then, instead of tracing a rectangle as in Fig. 7(c), the commutation current flows along the diagonal—thus reducing the trace length ℓ by approximately $\frac{\sqrt{2}}{2}$. It follows that the four-branch configuration would be similarly improved.

To verify the expected improvements, the electrically thin designs were again studied with FEA and impedance measurements. These results are reported in Tables IV and V, and demonstrate a more than twofold reduction in loop inductance. While some deviation between simulation and measurement is expected, especially due to manufacturer variation in PCB stackup, it is worth noting that the discrepancies in Table IV are largely due to simplifications made to the 3-D model of the switching cells. For instance, by substituting small or thin features, such as vias and internal shielding planes, with solid copper, meshing, and computation is drastically simplified and produces the reasonably accurate results above. Fully modeling each thin, internal plane and the individual vias can be shown to produce simulated values much closer to the measurements; however, these simulations can take an order of magnitude longer to compute.

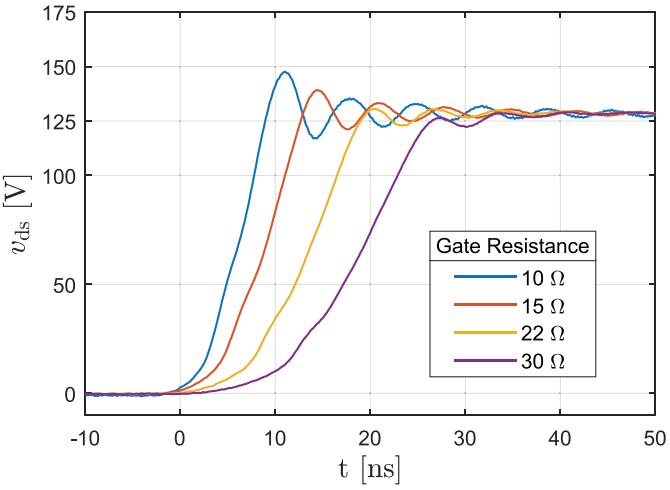

Fig. 14. Measurement of hard-switched commutation overshoot on an electrically thin ISC for different gate resistances.

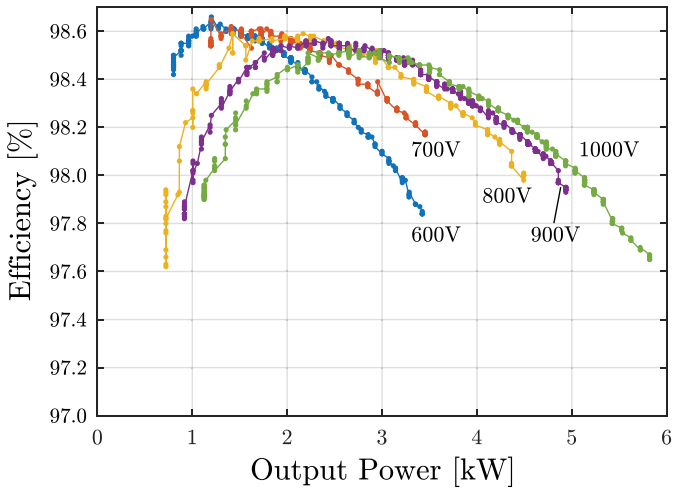

Fig. 15. Efficiency of single nine-level FCML converter leg for different input voltages and resistive loads. Switching frequency $f_s = 110$ kHz and modulation index $M = 0.96$.

Circuit simulation of hard-switched commutation demonstrated further reduced overshoot—similarly verified through experimental testing, as shown in Fig. 12—before a full converter was built using this design [27]. These tests indicated that a faster rise time, i.e., lower gate resistance than that prescribed by Table III, might indeed be used to reduce overlap losses without risking transient over voltage of the FETs. Consequently, experimental evaluation demonstrated in Fig. 14 showed that a modest change in gate resistance from 30 to 22 Ω could reduce overlap losses by up to 20% with the electrically thin implementation.

V. Converter Hardware and Experimental Results

Hardware testing consisted of two converter iterations, both informed by the discussion above. The control and modulation for both FCML inverter prototypes was implemented using an Altera MAX10M08 FPGA. In this article, phase-shifted pulsewidth modulation was used [14]. With this approach, acceptable capacitor voltage balancing is accomplished passively [28], given that key constraints on switching timing and input capacitance are met, as detailed in [29].

A. Initial Design Evaluation

Based on the Monte-Carlo optimization, an initial inverter prototype was built and characterized—though only one of the nine-level FCML converter legs (i.e., noninterleaved operation) was tested. Thermal management was accomplished through dual-sided cooling using solid aluminum heat sinks/spreaders mounted to the top and bottom sides of the converter. A 1 mm thick thermal interface material[3] was used between the GaN chips, capacitors, and inductors and the aluminum heat sinks. Results from testing of this prototype across various dc bus voltages and resistive loads are plotted in Fig. 15, with key measured performance figures summarized in VII. For this testing, a Yokogawa WT3000E power meter was used, and an output frequency just below 1 kHz was used in order to utilize one of the higher accuracy frequency ranges of the instrument.

The peak efficiency of 98.6% is achieved at lower voltage levels, where the dynamic ON-state resistance effect is less pronounced. At higher input voltage the efficiency drops mainly due to that effect. Other voltage-dependent loss components, i.e., the charging and discharging of the transistor output capacitances, have much less impact. Overall, the efficiency of the single-leg inverter was in line with what was predicted by the loss calculations described in the previous section. Additionally, it is evident that power density can be traded against efficiency by adjusting the current rating of the inverter. Yet, this iteration did not leverage the electrically thin approach, and measurements of device temperatures at peak power indicated thermal management could also be improved through a subsequent design.

B. Improved Design Iteration

An improved design, as enumerated in Table VI, maintained much of the components originally specified by the optimization. Major changes included a tighter PCB layout, higher thermal conductivity gap pad and aluminum heat sink, and the implementation of electrically thin switching cells [17]. The latter allowed for a lower, 22 Ω turn-ON resistance and the higher switching frequency listed in Table VII. A fully annotated photo of the converter is shown in Fig. 16, while a complete mass breakdown can be found in [17].

Waveforms from experimental testing of the hardware are plotted in Fig. 17, illustrating the successful demonstration of balanced interleaving of two FCML inverter phases. The magnified region serves to illustrate the phase-shifted voltage waveforms of each phase. Though the unfiltered output voltage of an ideal, balanced FCML inverter would present as square pulses of equal amplitude, experimental waveforms can vary for several reasons. First, while the electrically thin approach significantly reduces parasitics, inductances in high current paths are nonetheless still present and can resonate during certain switch

[3]Henkel Bergquist Gap Pad 5000S35.

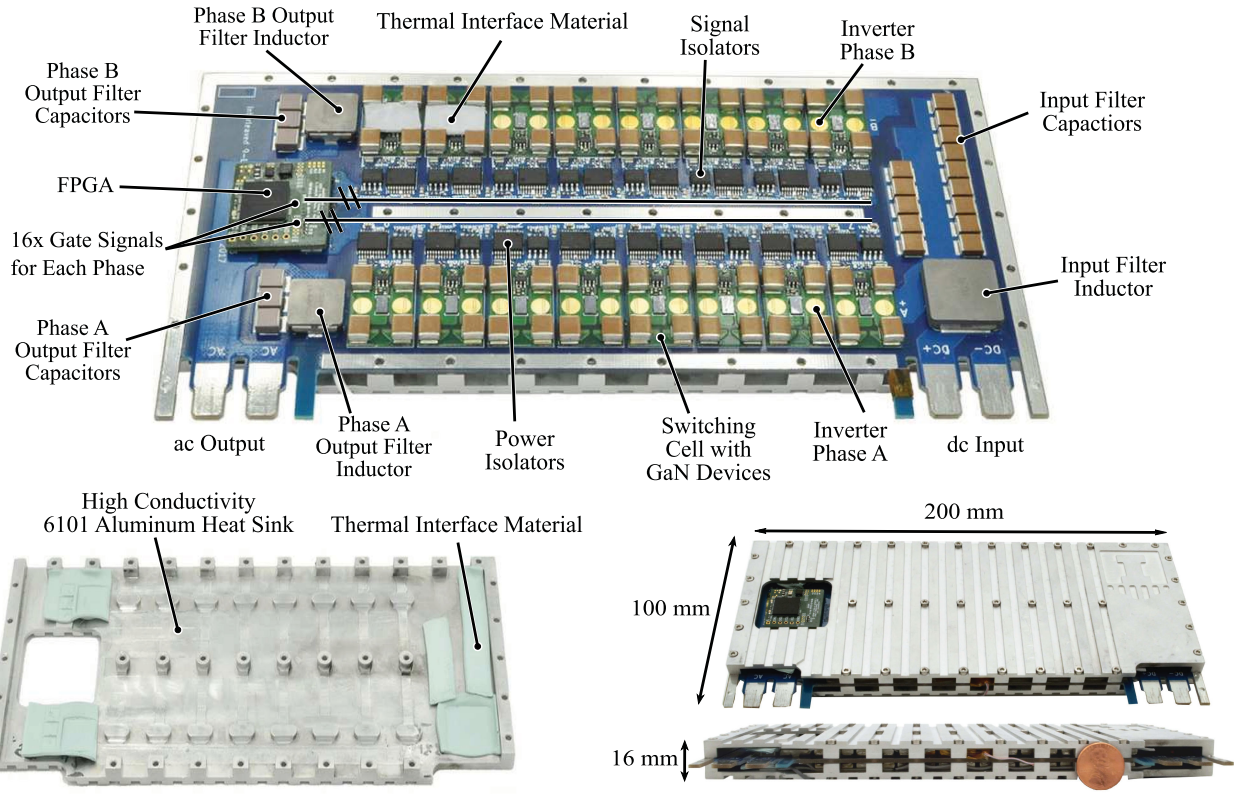

Fig. 16. Annotated view of the nine-level dual-interleaved FCML inverter hardware.

TABLE VI
IMPROVED CONVERTER BILL OF MATERIALS

Component	Part Number	Parameters
Gate driver	TI - LM5114	GaN
Gate resistors		22 Ω
GaN transistors	EPC - EPC2034	200V, 7 mΩ
Output inductors	Vishay - IHLP5050CE	10 μF
Digital isolators	Silicon Labs - Si8423BB	
Power isolators	Analog Devices - ADUM5210	
Flying capacitors	TDK - C5750X6S	2.2 μF
	4 parallel sets of 2 in series	
Input capacitors	TDK - C5750X6S	2.2 μF
	14 parallel sets of 2 in series	
Input inductor	Vishay - IHLP6767DZ	3.3 μH
	2 in series, one at each dc terminal	
Output capacitors	TDK - C5750C0G	0.1 μF
	6 in parallel per phase	
Output inductors	IHLP5050CE	10 μF
	2 in parallel per phase	

TABLE VII
KEY INVERTER PERFORMANCE FIGURES

	Design Iteration	
Parameter	Initial	Improved
Switching frequency	100 kHz	120 kHz
Effective frequency	800 kHz	960 kHz
Peak efficiency	98.6 %	98.6 %
Output power	5.8 kW	9.7 kW
Weight	0.5 kg	0.56 kg
Power density	12 kW/kg	17 kW/kg
THD	$\leq$ 3 %	$\leq$ 2 %
Input voltage, DC	1000 V	
Output voltage, AC	340 V RMS	
Modulation frequency	0 – 3 kHz	

transitions. Additionally, the capacitance of the X6S flying capacitors derates with applied dc bias. However, to simplify the design of this converter, a common switching cell block was used for for each level; as such, the capacitance variation was left uncompensated. Thus, a constant and expected deviation from the nominal flying capacitor voltages exists, and presents in the output voltage waveform as periodically varying pulse heights. Finally, the slope that appears on the nominally square pulses is due to the finite flying capacitances discharging and charging each cycle according to the output current. The amount of discharge, and thus voltage ripple, was factored into the Monte Carlo process—each device remains within acceptable voltage ranges at peak power.

In general, excellent current sharing was observed and the relatively constant heights of the switching nodes demonstrate good capacitor voltage sharing. Here, the successful balancing of the flying capacitors in each converter verifies the strength of the passive balancing mechanism leveraged in this design. In this article, care was taken to consider the effects of propagation delay mismatch and adequate input capacitance, both identified as key contributors to potential capacitor voltage mismatch [29].

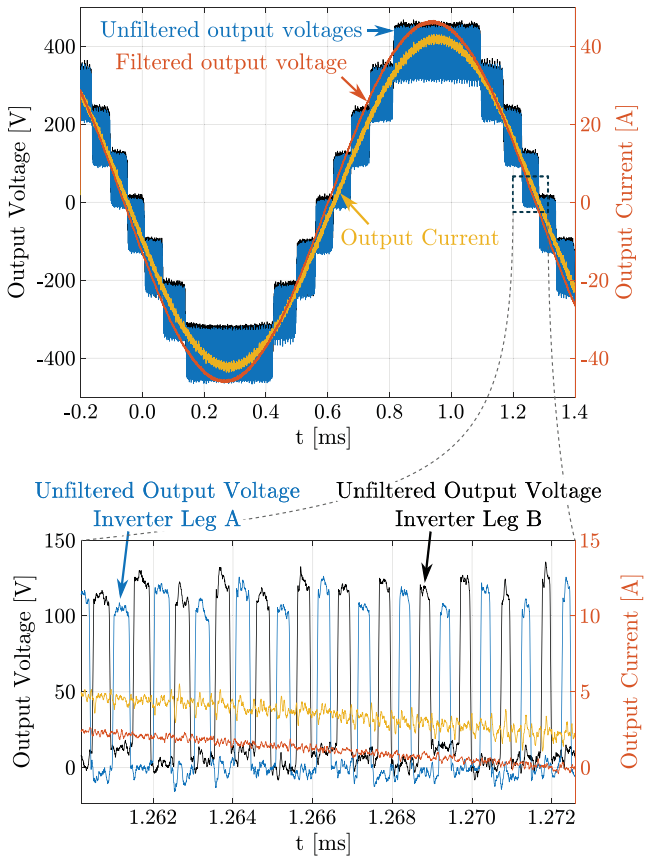

Fig. 17. Measured waveforms for interleaved operation at peak power. The zoomed view shows interleaving of the two phases, passive voltage balancing, and the effect of the output filters.

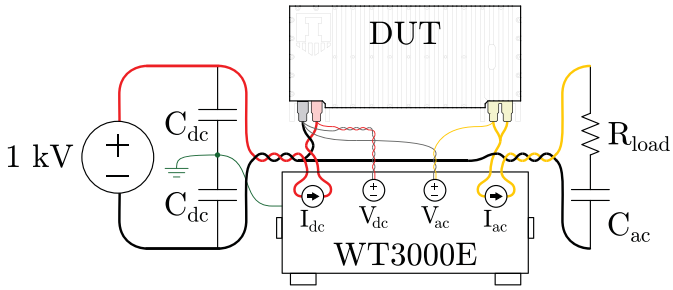

Fig. 18. Diagram of the experimental setup used for measuring high efficiency at high voltage and high power.

Since interleaving enables both the construction of higher power converters by the paralleling of many quasi-independent converters and the capability for further reduction in output filter size due to increased ripple frequency [30], this hardware demonstration supports a system level goal of paralleling many of these dual-interleaved converter modules, as illustrated in Fig. 1(c), to supply power to a single phase of a megawatt scale electric machine [8]. Fig. 17 also qualitatively illustrates very low THD in the output voltage and current, measured at ≤ 2 %.

The experimental setup used to measure the converter performance is illustrated in Fig. 18. Here, a Magna Power TS 20 kW supply provided the 1 kV dc bus voltage, split and ground referenced as shown. Additionally, an ac coupling capacitor, C_{ac}, was used to return output current directly to the negative rail of

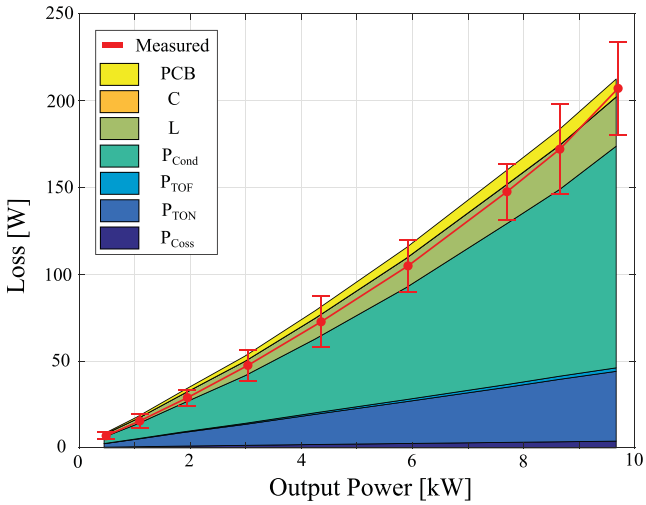

Fig. 19. Comparison of modeled performance to actual performance.

the dc supply, and both the ac and dc capacitors were chosen to be sufficiently large, low-loss film capacitors. Finally, efficiency measurements were recorded using a Yokogawa WT3000E fitted with 30 A, 1000 V elements. Sampling of both elements was synchronized to the ac output current, and voltages were measured with Kelvin connections as close to the converter terminals as possible.

These measurements are reported in Fig. 19, which plots the output power against the overall losses. This revision was able to achieve higher output power than the initial prototype, and it became evident that the voltage dependent dynamic r_{dson} effects—omitted in the initial loss modeling—played a much more significant role than initially expected. As such, the conduction losses were reworked to account for dynamic r_{dson} using the methodology in [18] and were factored into the updated loss breakdown estimates also included in Fig. 19. The difference between the measured and calculated losses are most likely due to mismatch in the modeling of the dynamic r_{dson} effect.

VI. Conclusion

This article has reviewed the major aspects of the design and optimization of a dual, interleaved nine-level FCML inverter module. A double-sided mounting scheme allows for reduction of the commutation loop inductance, which leads to gains in efficiency and power density—especially when coupled with an electrically thin design approach. The design optimization and light load experimental results indicate that interleaved FCML converters can provide both very high efficiency and very high specific power density. Finally, this article illustrates that overcoming the increased losses from the r_{dson} will be a key challenge toward further pushing the power density of this design, as will the development of improved thermal routing from chip-scale GaN devices.

Acknowledgment

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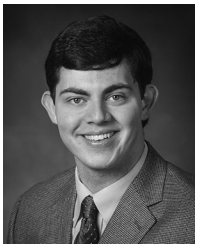

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