Design and Experimental Verification of an Efficient SSCB Based on CS-MCT

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***Abstract*—A novel solid state circuit breaker (SSCB), which uses the cathode-short MOS-controlled thyristor (CS-MCT) as the main switch to achieve high power efficiency, is proposed for direct current (dc) microgrid protection. The proposed SSCB features the commutating circuit with a one-shot triggering characteristic and a compact size, which makes the SSCB realize a simple tripping process and easy integration. Furthermore, the SSCB charges the commutating capacitor and offers the interruption capability before the main switch is turned ON. This avoids the possible failure of the breaker under the fault that occurs at the initial stage of the turn-ON of the main switch, thus providing highly reliable and robust interruption capability for the SSCB. Circuit analysis and design guidelines are discussed in detail through the mathematical modeling. Moreover, the practical value and the feasibility of the SSCB are validated by 600-V/15-kW prototype experiments and further verified in dc microgrids through simulations.**

***Index Terms*—Circuit breakers, CS-MCT, microgrids, power efficiency, power system protection.**

I. Introduction

IN RECENT years, increasing attention has been drawn to direct current (dc) microgrids and power distribution systems, as they can reduce the system redundancy, increase the power transfer capability, as well as provide higher power efficiency and reliability in comparison with alternating current (ac) systems [1]–[3]. These features have promoted dc applications in shipboards, airplanes, telecommunication systems, buildings, electric vehicle charge stations, and data centers [4]–[7].

However, dc microgrids face a more serious fault protection problem than ac systems due to the lack of a natural current zero-crossing point [8], [9]. Unlike ac systems, adopting mechanical circuit breakers (MCBs) to protect dc microgrids under the fault condition will cause arc erosion, leading to a higher maintenance cost and complexity [5]–[9]. Moreover, MCBs based on thermal and electromagnetic principle have a long response time (tens of milliseconds) [10]. Such long response time cannot meet the high speed protection requirement in dc microgrids because the small dc circuit impedance in dc line usually brings a fast rising fault current [11]. Hence, an arcless breaker with fast tripping response and low power losses is essential for the dc microgrid protection.

Solid-state dc circuit breakers, which use semiconductor devices with fast response time, can achieve a rapid interruption without arc erosion. Si-IGBT-based breakers have been proposed to interrupt fault current almost at the instant of receiving an interruption command [12], [13]. However, IGBT-based breakers feature relatively high power losses due to the finite conductivity modulation effect of the IGBT [14]. Besides, the maximum current interruption ability of these breakers are also limited by the saturation current of the IGBT. The interruption ability of IGBT-based breakers can be improved utilizing the parallel technology. Nevertheless, this will introduce challenges in terms of the current balance and construction cost [15].

Thyristors can be also used in circuit breakers [7], [19]–[27]. Compared with full-controlled devices (e.g., IGBT and MOSFET), thyristor-based circuit breakers (TBCBs) maintain higher power efficiency and stronger tolerance to current and voltage surges [16], but need additional commutating circuits. Moreover, compared with voltage-controlled devices (e.g., IGBT, MOSFET and MCT), the thyristor requires a larger gate driving current for turn-ON, which demands mass passive elements, and thus increases the difficulty of the system compact integration [17], [18]. In terms of the circuit topology, TBCBs proposed in [19], [20] can commutate the fault current from the main conducting path to the commutating circuit through the discharge of the capacitor. However, these TBCBs need additional power supplies and charging strategies to pre-charge their capacitors, thus increasing control complexity and system costs. Z-source breakers proposed in [7], [21], and [22] can autonomously isolate dc faults. However, fault impedance variations may cause the malfunction. In [23] and [24], two-stage dc circuit breakers use the dc system voltage to charge the capacitor and isolate faults with a decreased voltage overshoot. However, the transformation between the two stages requires additional detection, resulting in a complex control unit. Besides, these breakers can just interrupt unidirectional fault current, which also limits their applications. Other bidirectional TBCBs also isolate the fault following the

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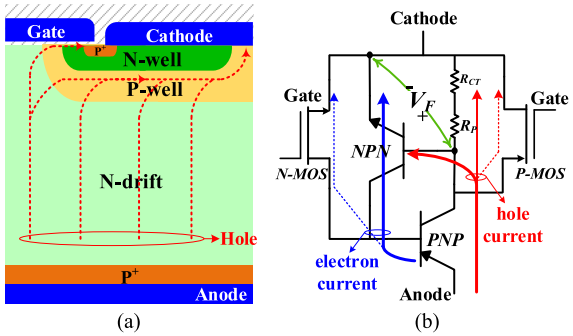

Fig. 1. (a) The cross section and (b) the equivalent circuit of the CS-MCT. Dashed lines of (a) represent the hole current paths during the OFF state or turn-OFF process.

commutation-forced turn-OFF principle using commutating capacitors [25]–[27]. However, for these TBCBs, the capacitors will not be charged until the main switch in the main conducting path is turned ON. If the fault still exists or a new fault occurs after the reclosing of the main switch, the breakers may fail to isolate the fault again because the capacitors have not been fully charged yet. In addition, due to the small turn-ON *di/dt* capability and the large reverse recovery time of the thyristor [28], TBCBs need specially designed commutating inductors to limit the rising rate of the commutating current and oversized commutating capacitors to increase the reverse-bias time interval of the thyristor during the fault protection process [25]–[27]. Otherwise, TBCBs may malfunction. These will increase the design complexity and the size of the breakers.

Recently, circuit breakers based on wide-bandgap (WBG) semiconductor devices, such as SiC JFET [5], [29], SiC SIT [30], and GaN HEMT [31], have been proposed. However, their proliferation into the mainstream market is impeded by high device costs and reliability concerns. The main reason is that the WBG technology is still immature nowadays [32], [33].

In our previous work, a novel device named cathode-short MOS-controlled thyristor (CS-MCT) has been fabricated using a modified DMOS process [34], [35]. The cross section and the equivalent circuit of the CS-MCT are shown in Fig. 1. Differing from the standard thyristor with large line width (hundreds of microns) and deep junctions (tens of microns) [36], the CS-MCT uses modern DMOS process to achieve smaller line width (e.g., 0.5 μm) and shallower junction depth (several microns) [37]. Therefore, the CS-MCT obtains a fine pattern thyristor and a shorted cathode structure inside. In the conducting state, the CS-MCT works in thyristor conducting mode, resulting in a relatively low ON-state resistance, as well as a high *di/dt* capability (over 100 kA/μs [35]). Besides, its voltage-controlled operation and normally-off characteristic enable a more simplified gate drive circuit in comparison with the thyristor and the conventional MCT [38], [39]. Furthermore, a 400-V SSCB based on the CS-MCT had been developed in our previous work [39], which shows that the CS-MCT is a competitive device used in dc fault protection. However, this kind of SSCB can just interrupt unidirectional fault current and need additional dc source to pre-charge the commutating capacitor, thus increasing the circuit complexity and limiting its applications.

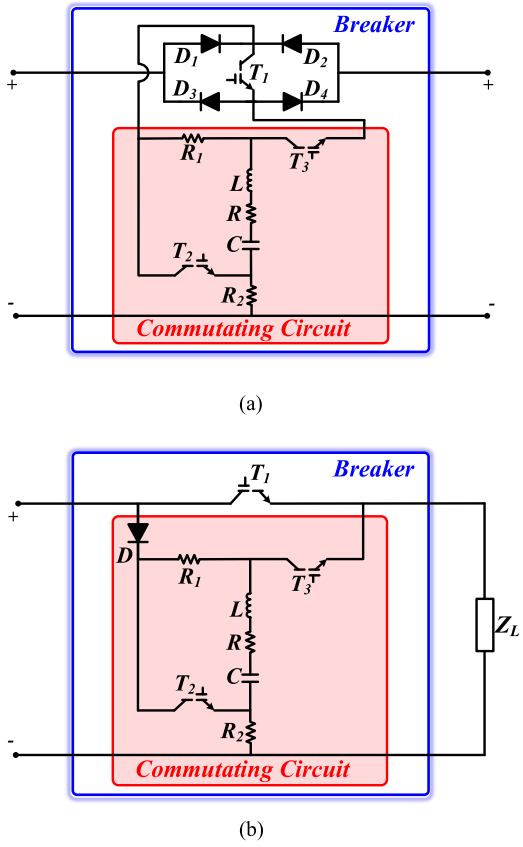

Fig. 2. Proposed SSCB: (a) bidirectional and (b) unidirectional topologies.

In this article, a novel solid state circuit breaker (SSCB), which uses the CS-MCT as the main switch to achieve high power efficiency, is proposed for dc microgrid protection. Both bidirectional and unidirectional topologies are shown in Fig. 2(a) and (b), respectively. T_1, T_2, and T_3 are all CS-MCTs. It can be seen that the proposed SSCB features a one-shot triggering commutating circuit (CC) using only one commutating capacitor. Moreover, the commutating capacitor can be charged by the dc source automatically, which omits the additional power supply to charge the capacitor. Consequently, the proposed SSCB can provide a more compact size and simpler fault protecting strategy than the existing TBCBs [7], [19]–[27]. Furthermore, the proposed SSCB charges the commutating capacitor before the turn-ON of the main switch (T_1). This can avoid the possible failure of the SSCB under the fault that occurs in the initial stage of the turn-ON of T_1, thus offering reliable and robust interruption capability for the SSCB. The only difference between the bidirectional topology and the unidirectional topology is that the bidirectional topology uses a bidirectional switch to conduct bidirectional currents. As a result, both topologies in Fig. 2 are based on the same operating principle and the unidirectional topology is taken as an example for presentation in the following discussions. Discussion of the fault protection process is carried out in Section II. Section III presents the circuit design guidelines based on detailed mathematical modeling. Following the design guidelines, a prototype of 600-V/15-kW SSCB is developed in Section IV, which validates the accuracy of the modeling and

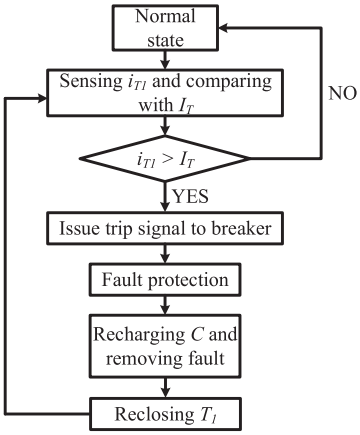

Fig. 3. Flowchart of the proposed SSCB protection scheme.

the operational performance of the SSCB. Section V compares the proposed SSCB with other breakers and verifies the practical value and feasibility of the proposed SSCB in LVdc microgrids. Finally, the conclusion is presented in Section VI.

II. Operation of The Proposed SSCB

The protection process of the SSCB is shown using a flowchart in Fig. 3. The operating process of the SSCB will be described in the following.

A. Normal Condition

During the normal condition shown in Fig. 4(a), T_1 is turned ON to conduct current flowing through the main conducting path (MC). Note that, at this time, the commutating capacitor (C) had been fully charged by the dc source. Consequently, both T_2 and T_3 work in the forward blocking state with a voltage of the dc source.

B. Current Commutation

With the monitoring unit, the current of T_1 (i_{T1}) is continuously sensed and compared with the preset threshold (I_T). In Fig. 4(b), the dc source is assumed to be a constant dc voltage ($V_{\rm dc}$) and the internal impedance of the dc source are L_s and R_s. When a fault occurs, i_{T1} will increase and exceed I_T set by the monitoring unit. Then, the monitoring unit will send a triggering signal to turn ON T_2 and T_3 simultaneously. After that, the commutating loop (C-R-L-T_3-T_1-D-T_2) will be turned ON. Because this loop has much smaller impedance than the other loops, a large transient discharge current with high *di/dt*, which is produced from C, mostly flows through T_1 in the reverse direction, thus countering the fault. This commutates the fault current from MC to CC, thereby forcing i_{T1} to cross zero. Consequently, T_1 can be turned OFF to isolate the fault. Note that the snubberless SSCB topology is suitable for the dc microgrids with small distributing inductive reactance. If the SSCB is applied in dc systems with large inductive reactance on the transmission and/or distribution line, the fault current limiter (FCL) and the snubber circuit (e.g., metal oxide varistor (MOV)) are suggested to be added. The former is connected in series with the SSCB to limit the dc fault current and its rising rate, thus reducing the surplus energy on the transmission and/or distribution line [40]. The latter is connected in parallel with the SSCB to limit the overvoltage and absorb the surplus energy [41]. As a result, dc microgrids continuous operation and healthy network ride-through can be guaranteed.

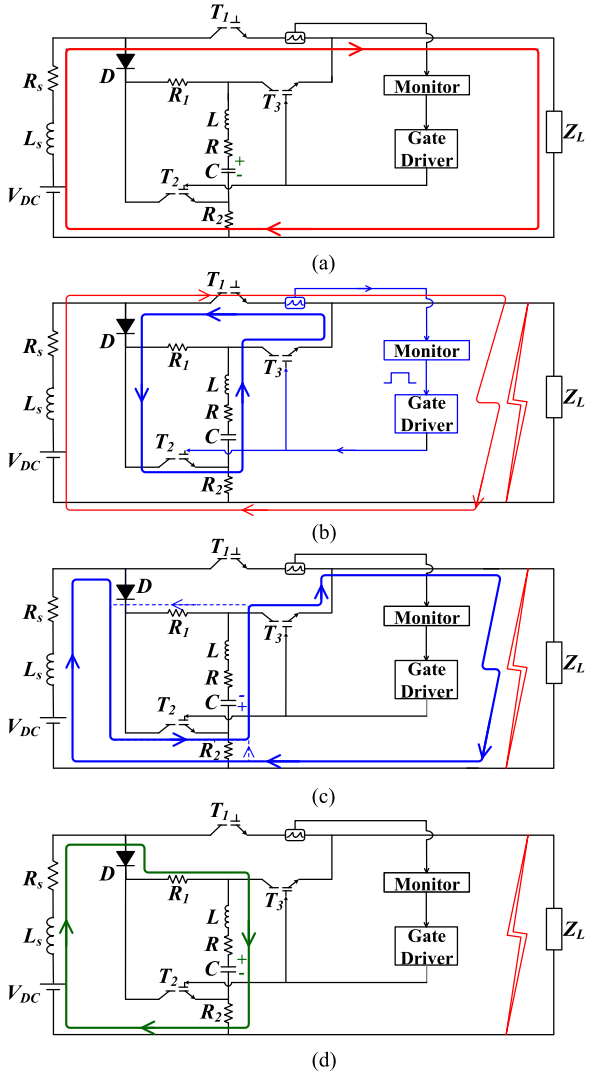

Fig. 4. Current paths in the SSCB during the fault current interruption process. (a) Normal operation. (b) Short circuit and current commutation process. (c) *RLC* series resonant process. (d) Recharge of the commutating capacitor.

C. RLC Series Resonance

In Fig. 4(c), when the proposed SSCB finishes the current commutation, T_1 will be turned OFF. As a result, C will discharge through three loops (C-R-L-T_3-R_2, C-R-L-R_1-T_2 , and C-R-L-T_3-V_{dc}-L_s-R_s-D-T_2), the currents of which depend on the circuit impedance of the loops. During the initial stage of the discharge process of C, T_1 undertakes a reverse blocking voltage and operates in the reverse recovery state, which extracts excess carriers stored in the device. If the reverse-bias time interval is longer than the reverse recovery time of T_1, T_1 will retain OFF

state and the fault isolation will be successful. Otherwise, T_1 will be triggered again (*i.e.*, mistriggered), leading to a failure for the current interruption. After the accomplishment of the discharge, *C* will be charged by the dc source. Note that, compared with the polarity in the normal condition [see Fig. 4(a)], *C* will be reverse-charged at the end of this period.

D. Recharge of Capacitor

After completing the *RLC* series resonance, the current of the *RLC* series branch is reduced to zero. However, there still exist currents in T_2 and T_3, the values of which depend on $V_{\rm dc}$, R_1 and R_2. If these currents are within the scope of the turn-OFF capabilities of T_2 and T_3, the devices will be turned OFF successfully. After that, *C* will be charged again through the V_{dc}-L_s-R_s-*D*-R_1-*L*-*R*-*C*-R_2 loop, as shown in Fig. 4(d). Otherwise, T_2 and T_3 will suffer from turn-OFF failure and *C* will not be recharged, leading to another failure of the SSCB.

E. Reclosing of T_1

After a successful fault current interruption, the proposed SSCB can charge *C* by the dc source automatically. Therefore, a short time after the accomplishment of the fault isolation, *C* will be charged again, and hence T_1 will be ready to reclose. If the system fault disappears, the proposed SSCB will operate in normal state. Otherwise, the proposed SSCB will repeat the fault protection discussed above again. Note that it is important for the breakers based on the commutation-forced turn-OFF principle to charge *C* before the reclosing of T_1 because the breakers may be needed to isolate the fault again if the fault still exists or a new fault happens after the reclosing of T_1.

III. Circuit Analysis and Design

A proper parameter design is essential for the proposed SSCB to isolate the fault successfully. In this section, a mathematical model is established to analyze fault isolation of the breaker and offer design guidelines for components sizing.

The most serious dc fault is the short-circuit fault due to the highest current rising rate. The fault current must be interrupted rapidly before it damages dc systems and loads. For the sake of security, the SSCB must be able to isolate the fault in this extreme case. Consequently, the circuit occurring a short-circuit fault at the output port is used in this section, as shown in Fig. 5(a). In order to simplify the analysis, the ON-state resistances of the CS-MCTs and the diode (*D*) are neglected. R_1 and R_2 are selected with the same resistance. Besides, the preset threshold (I_T) of the monitoring unit can be determined according to the requirements of practical applications. All variables are defined with polarities, as illustrated in Fig. 5(a). Furthermore, according to the operation waveforms of the proposed SSCB, as shown in Fig. 5(b), the fault protection of the proposed SSCB can be analyzed in the range: 1) $t_0 < t \le t_1$; 2) $t_1 < t \le t_2$; 3) $t_2 < t < t_3$; and 4) $t \ge t_3$.

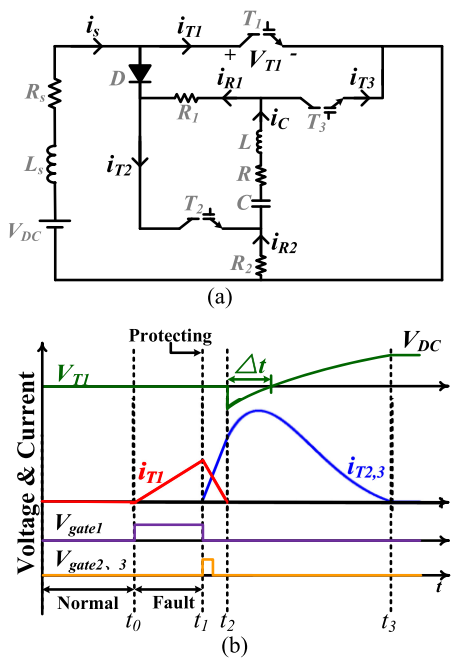

Fig. 5. (a) Fault protection modeling under short-circuit condition. (b) Corresponding current and voltage waveforms during the fault interruption of the proposed SSCB.

A. Period 1: Fault Occurrence ($t_0 < t \le t_1$)

The equation of the fault current over this period can be expressed as

$$i_s = i_{T1} = \frac{V_{\rm dc}}{R_s}(1 - e^{-\frac{R_s}{L_s}t}). \tag{1}$$

So, i_s keeps rising and reaches the preset threshold (I_T). After a short-time delay (t_d) of the monitoring unit, T_2 and T_3 are turned ON simultaneously due to the triggering signal sent by the monitoring unit. As a result, t_1 can be given by

$$t_1 = \frac{L_s}{R_s}\ln\frac{1}{1 - \frac{I_T R_s}{V_{\rm dc}}} + t_d. \tag{2}$$

B. Period 2: Current Commutation ($t_1 < t \le t_2$)

After t_1, T_2 and T_3 are triggered simultaneously, and the current is commutated from MC to CC. As shown in Fig. 6(a), i_{T2} can be obtained by applying Kirchhoff's voltage law (*KVL*) to the T_2-*C*-*R*-*L*-T_3-T_1 loop

$$i_{T2} = \frac{CV_{dc}S_1S_2}{S_2 - S_1}[e^{S_2(t-t_1)} - e^{S_1(t-t_1)}] \tag{3}$$

where

$$S_{1,2} = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}. \tag{4}$$

Then, i_{T1} can be calculated by applying Kirchhoff's current law (*KCL*)

$$i_{T1} = i_s - i_{T2}. \tag{5}$$

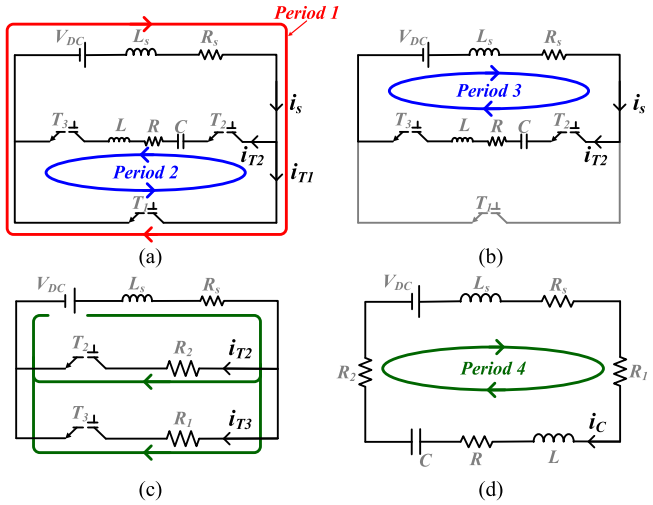

Fig. 6. Equivalent circuit diagram at (a) the periods 1 and 2, (b) the period 3, (c) $t = t_3$, and (d) the period 4.

Hence, t_2 can be calculated by solving

$$t_2 = t|_{i_{T1}=0}. \tag{6}$$

Further, $i_s(t_2)$, $i_{T2}(t_2)$ and $V_C(t_2)$ can be obtained as

$$i_s\left(t_2\right) = i_{T2}\left(t_2\right) = A \tag{7}$$

$$V_C\left(t_2\right) = -V_{dc} + \frac{1}{C}\int_{t_1}^{t_2} i_{T2}dt = B. \tag{8}$$

Because t_2 is usually short, (5) can be simplified according to Taylor formula

$$i_{T1} = \frac{V_{\rm dc}}{L_s}t - \frac{V_{\rm dc}R_s}{2{L_s}^2}t^2 - \frac{V_{\rm dc}}{L}\left(t - t_1\right) + \frac{V_{\rm dc}R}{2L^2}\left(t - t_1\right)^2. \tag{9}$$

Thus, a reliable current commutation can be guaranteed if (9) has at least one zero point ($t > t_1$). Consequently, L and R can be determined according to Vieta theorem

$$L < L_s/2 \tag{10}$$

$$R \le \frac{L^2 - 2\left(L_s - R_s t_1\right)L + {L_s}^2}{t_1\left(2L_s - R_s t_1\right)}. \tag{11}$$

In addition to guiding the choice of L, (10) also reveals that if there are no special requirements, a more practical SSCB design should focus on low L_s condition to meet most dc system requirements.

C. *Period 3:* RLC *Series Resonance* ($t_2 < t < t_3$)

After t_2, i_{T1} drops to zero, and thus T_1 is turned OFF naturally. Because R_1 and R_2 are chosen with a much larger resistance than R, i_{R1} and i_{R2} can be neglected when compared with i_c. As a result, the equivalent circuit at this period is shown in Fig. 6(b). According to *KCL*

$$i_s \approx i_{T3} \approx i_C. \tag{12}$$

Then, taking (7), (8) as the initial conditions, i_{T2} and V_C can be obtained by *KVL*

$$V_C = K_1 e^{\beta_1(t-t_2)} + K_2 e^{\beta_2(t-t_2)} + V_{\rm dc} \tag{13}$$

$$i_{T2} = C\left(K_1\beta_1 e^{\beta_1(t-t_2)} + K_2\beta_2 e^{\beta_2(t-t_2)}\right) \tag{14}$$

where

$$\beta_{1,2} = -\frac{R + R_s}{2\left(L_s + L\right)} \pm \sqrt{\left(\frac{R + R_s}{2\left(L_s + L\right)}\right)^2 - \frac{1}{\left(L_s + L\right)C}} \tag{15}$$

$$K_1 = -\frac{A - C\beta_2 B + C\beta_2 V_{\rm dc}}{C\left(\beta_2 - \beta_1\right)} \tag{16}$$

$$K_2 = \frac{A - C\beta_1 B + C\beta_1 V_{\rm dc}}{C\left(\beta_2 - \beta_1\right)}. \tag{17}$$

Thus, the voltage drop across T_1 (V_{T1}) can be calculated

$$V_{T_1} = V_C + i_{T2}R + L\frac{di_{T2}}{dt}. \tag{18}$$

Further, in Fig. 5(b), Δt is defined as the reverse-bias time interval that V_{T1} retains negative value. Therefore, Δt can be obtained by solving

$$\Delta t = t|_{V_{T1}=0} - t_2. \tag{19}$$

During Δt, T_1 operates in reverse recovery state. To turn OFF T_1 successfully, V_{T1} must retain negative until T_1 finishes its reverse recovery. Otherwise, T_1 will be mistriggered by excess carriers stored in the device. Hence, a proper C should be chosen to guarantee the reliable turn-OFF of T_1, which meets

$$\Delta t > t_q \tag{20}$$

where t_q is the reverse recovery time of the CS-MCT. According to (19), the relationships between Δt and R, L, C can be calculated, as shown in Fig. 7. It is illustrated that the increase of C can lead to a larger Δt, thus suppressing the mistriggering of the CS-MCT, according to (20). Since the typical reverse recovery time of the CS-MCT that operates at hundreds of amperes is usually tens of microseconds, Fig. 7 can guide the choice of C in practical SSCB design.

D. *Period 4: Recharging of* C ($t \ge t_3$)

The *RLC* series resonance is completed at t_3, and thus i_C reduces to zero. Therefore, the equivalent circuit of Fig. 5(a) can be simplified into Fig. 6(c). Since the resistance of R_1 and R_2 are much larger than R_s, i_{T2} and i_{T3} can be expressed as

$$i_{T2} = i_{T3} \approx \frac{V_{\rm dc}}{R_1}. \tag{21}$$

If i_{T2} and i_{T3} are within the current turn-OFF capability of the CS-MCT, T_2 and T_3 will be turned OFF, and C can be charged by the dc source through V_{dc}-L_s-R_s-R_1-L-R-C-R_2 loop again. Otherwise, T_2 and T_3 will suffer from switching failure, and the proposed SSCB will not isolate the fault successfully. Consequently, R_1 and R_2 should be selected as

$$R_1 = R_2 \ge \frac{V_{\rm dc}}{i_{\rm off}} \tag{22}$$

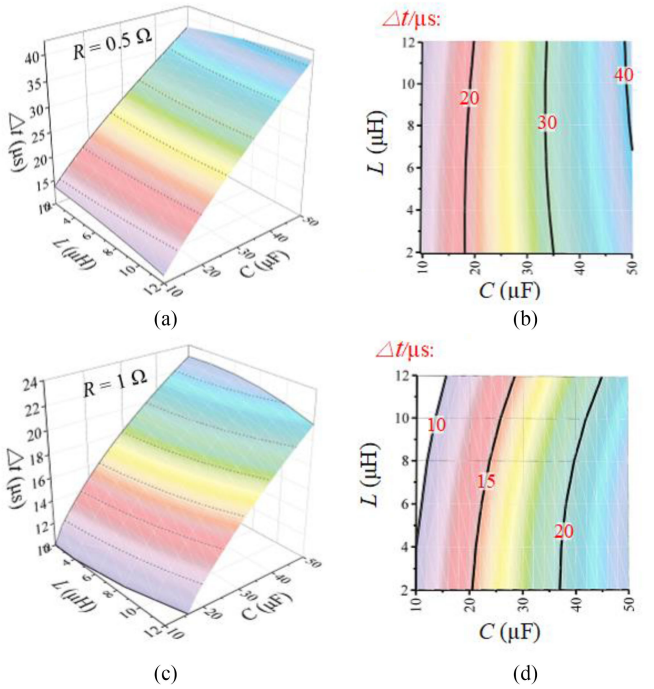

Fig. 7. Dependencies of Δt on capacitance C and inductance L at (a) and (b) resistance R of 0.5 Ω, (c) and (d) resistance R of 1 Ω. In this case, L_s and R_s are 27 μH and 1.2 Ω, respectively.

where i_{off} is the turn-OFF ability of CS-MCT.

Once T_1 and T_2 are turned OFF successfully, the equivalent circuit can be simplified into Fig. 6(d). It illustrates that C will be charged by the dc source through V_{dc}-L_s-R_s-R_1-L-R -C-R_2 loop with initial current: $i_C(t_3) = 0$, and initial voltage $V_C(t_3) = -V_{\text{dc}}$. Besides, R_s can be neglected when compared with R_1. Hence, V_C can be given according to *KVL*

$$V_C = \frac{2V_{\text{dc}}}{\alpha_2 - \alpha_1}\left[\alpha_1 e^{\alpha_2(t-t_3)} - \alpha_2 e^{\alpha_1\alpha_2(t-t_3)}\right] + V_{\text{dc}} \quad (23)$$

where

$$\alpha_{1,2} = -\frac{R_1}{L_s + L} \pm \sqrt{\left(\frac{R_1}{L_s + L}\right)^2 - \frac{1}{C\,(L_s + L)}}. \quad (24)$$

In summary, the proposed breaker can be designed with the following guidelines:

1) select CS-MCTs according to the power rating of the dc system (e.g., the dc voltage and the rated current) and efficiency requirement;
2) determine the preset threshold (I_T) of the monitoring unit according to the requirements of practical applications;
3) determine R and L referring to (10) and (11). Besides, the CS-MCT with high di/dt capability is suggested for T_2 and T_3 to accelerate the commutating process especially for high power applications;
4) choose C according to (20). The CS-MCT with low t_q is recommended for T_1 to reduce the requirement for the capacitance of C;
5) select R_1 and R_2 according to (22).

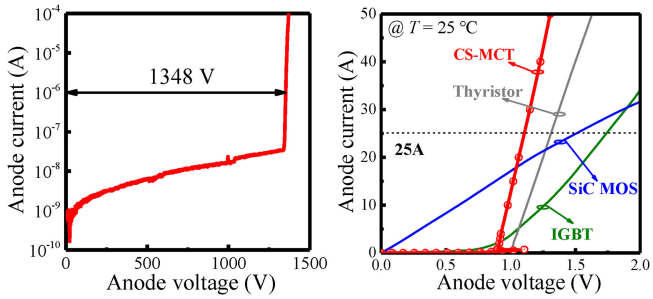

Fig. 8. Measured (a) forward blocking capability of the CS-MCT, and (b) *I–V* characteristics of the CS-MCT, the SiC MOSFET, SCR, and IGBT.

TABLE I
CHARACTERISTICS FOR DIFFERENT SWITCHES

Switch Type	SiC *MOSFET IMW120R0 60M1H*	IGBT *IKW25N12 0T2*	SCR *TN4050-12 PI*	**CS-MCT**
Rated current	26 A @100 °C	25 A @110 °C	25 A @82.5 °C	**25 A @110 °C**
BV	1200 V	1200 V	1200 V	**1348 V**
V_{on} (25 A/25 °C)	1.5 V	1.7 V	1.3 V	**1.1V**
Conduction loss	37.5 W	42.5 W	32.5 W	**27.5 W**
Maximum di/dt (A/μs)	-	-	Hundreds	**Tens of thousands**
Control-type	Voltage	Voltage	Current	**Voltage**
Driver	Simple	Simple	Complex	**Simple**
Technology	Immature	Mature	Mature	**Mature**

IV. EXPERIMENTAL VERIFICATION

A. Characterization of CS-MCT

In this article, the CS-MCT is fabricated using a modified DMOS process, thus featuring a fine pattern thyristor structure inside to obtain low ON-state voltage drop (V_{on}) and high *di/dt* capability [34], [35]. In Fig. 8(a), the CS-MCT provides a forward breakdown voltage (*BV*) of 1348 V, which can be used in 600 V applications. Fig. 8(b) shows the measured I-V curve of a 25 A CS-MCT with a chip area of 28 mm^2 at temperature of 25 °C. Furthermore, as shown in Fig. 8(b) and Table I, several mainstream devices, which have similar power capability to the CS-MCT, are list for comparison. The IGBT (*IKW25N120T2*) is represented the pinnacle of available full-controlled semiconductor switches. However, its limited conductivity modulation effect results in high ON-state voltage drop (V_{on}) of 1.7 V, which increases 55% compared with that of the CS-MCT. The SiC MOSFET (*IMW-120R060M1H*) is regarded as one of the most promising wide-bandgap semiconductor devices. Nevertheless, SiC MOSFET still features a relatively high V_{on} of 1.5 V (36% higher than that of the CS-MCT) due to its unipolar conduction mechanism. The thyristor (*TN4050-12PI*) can work in the current regenerative mode with an enhanced conductivity modulation effect. However, because of the large line width (hundreds of microns) and deep junctions (tens of

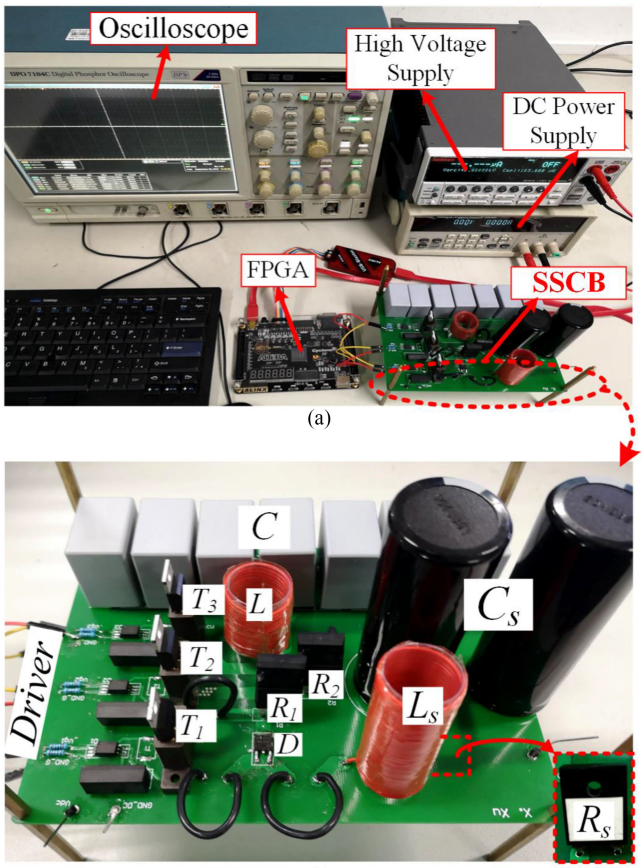

Fig. 9. (a) Test bench and (b) the laboratory prototype of the proposed SSCB.

microns) [37], the thyristor still provides 18% higher $V_{\rm on}$ than the CS-MCT. Besides, the thyristor also suffers from small *di/dt* capability. If the turn-ON *di/dt* of thyristors in the commutating circuit has not been properly limited, it may cause hot spots and result in thyristor failure under the fault isolation condition [29]. As for the CS-MCT, the decrease of $V_{\rm on}$ is significant for the proposed SSCB to achieve a high-efficiency since T_1 in the SSCB usually works in the conduction state and occupies the most of power losses. As a result, the proposed SSCB can achieve higher power efficiency than that of the breakers based on the IGBT, the SiC MOSFET and the thyristor. Besides, high *di/dt* capability of the CS-MCT also ensures a reliable fault interruption of the proposed SSCB.

B. Fault Isolation of Proposed SSCB

Fig. 9 shows the experimental prototype and the test bench of the proposed SSCB, which is design as 600-V/15-kW and can be used in LVdc microgrids. The capacitor Cs is precharged to 600 V, which acts as a dc voltage source. L_s and R_s represent the internal impedance of the dc source. I_T of the monitoring unit is set to 100 A (4 × of the nominal current) to avoid the mis-triggering of the SSCB under the inrush current conditions [42]. According to our previous work [39], a FPGA is adopted as a simplified monitoring unit with the delay time (t_d) of

TABLE II
PARAMETERS OF THE 600-V/15-kW SSCB

L_s	R_s	$R_1(R_2)$	R	L	C	t_q	i_{off}
27 μH	1.2 Ω	185 Ω	1 Ω	12 μH	37 μF	15.5 μs	4 A

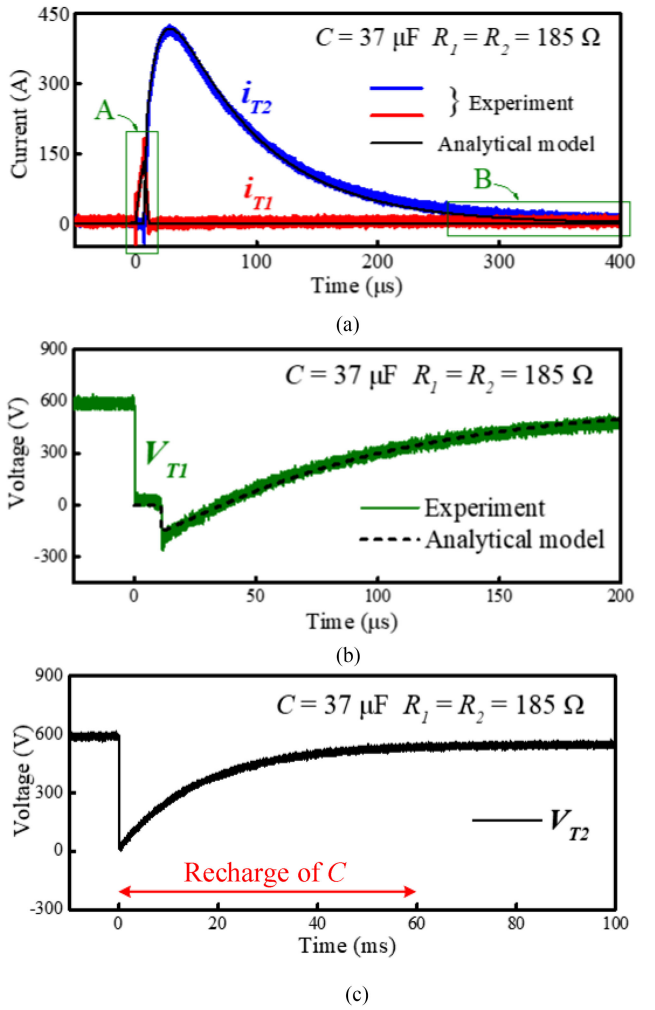

Fig. 10. Experimental waveforms of the designed breaker. The analytical model results are calculated by MATLAB.

1.2 μs. Unless otherwise specified, the detailed parameters of the SSCB are list in Table II. L of 12 μH is chosen, which meets the requirement of (10). According to (11), R should be less than 1.396 Ω and is chosen as 1 Ω. Calculated from (19), C of 37 μF can offer Δt of 17.7 μs, which can guarantee a reliable turn-OFF of T_1 according to (20). R_1 and R_2 are set to 185 Ω to meet the requirement of (22). In the following experiments, the short-circuit fault is assumed by directly replacing the load with a wire and occurs when a gate pulse is applied on T_1.

The experimental waveforms are shown in Fig. 10. It can be seen that both V_{T1} and V_{T2} are 600 V before $t = 0$, which means that C had been fully charged by the dc source, and hence the SSCB is ready to perform the fault isolation. At the moment of the short-circuit fault occurred ($t = 0$), the current through T_1 (i_{T1}) starts to increase. When i_{T1} exceeds I_T, T_2 and T_3

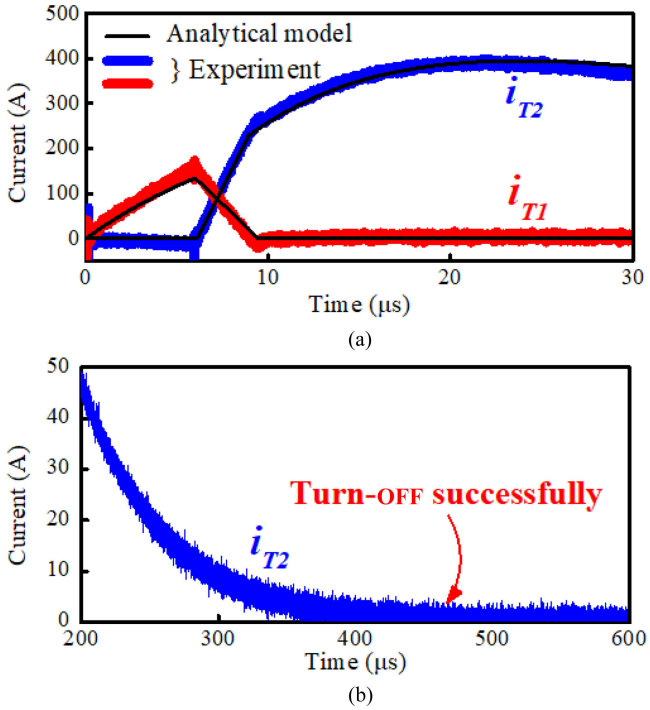

Fig. 11. Zoomed in detail of (a) the box A and (b) the box B in Fig. 10(a).

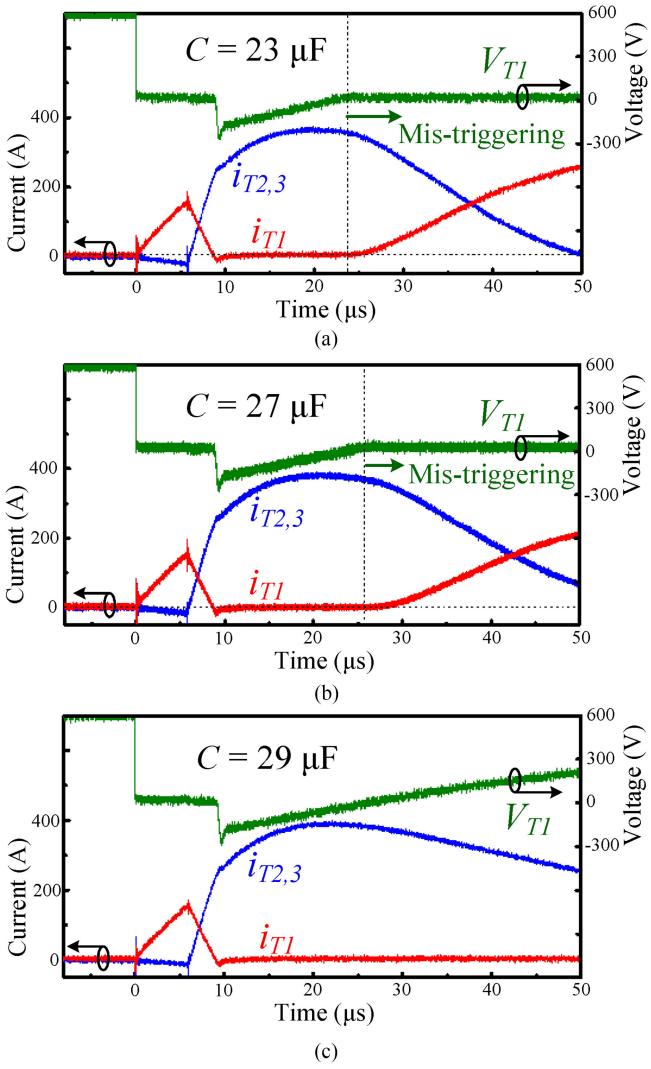

Fig. 12. Fault isolation at (a) $C = 23$ μF, (b) $C = 27$ μF, and (c) $C = 29$ μF.

are triggered simultaneously to commutate fault current from MC to CC accompanied by the discharge of C. Consequently, the fault current can be successfully interrupted, which protects the system from being damaged. After the accomplishment of fault isolation, T_1, T_2 and T_3 are all turned OFF. Then, C will be charged by the dc source again, and thus preparing for next fault isolation. The operations can be proved by waveforms of V_{T1} and V_{T2} because both V_{T1} and V_{T2} rise to the source voltage again, as shown in Fig. 10(b) and (c). Note that the fault protecting operation is in good agreement with the analysis discussed in Section II.

It can be seen in Fig. 11 that T_1 can be quickly turned OFF (2∼3 μs), which validates the rapid interruption capability for the proposed SSCB. It is also illustrated that, with the proper choice of circuit components utilizing the design guides, both the mis-triggering of T_1 and the turn-OFF failure of T_2 and T_3 have been avoided during the fault isolation of the proposed SSCB. On the other hand, in both Figs. 10 and 11, a good matching between experimental results and analytical results also demonstrates the validity of proposed breaker and the accuracy of the design guidelines presented in Section III.

C. Mistriggering of T_1

If the design of the proposed SSCB cannot meet the requirement of (20), T_1 will be triggered again after V_{T1} rises to voltage zero-crossing point, thus leading to isolation failure for the proposed SSCB. In Fig. 12, three different types of the SSCB with $C = 23$ μF, $C = 27$ μF, and $C = 29$ μF are discussed, Δt of which are 13.6, 15.2, and 15.7 μs, respectively. It can be seen that i_{T1} is quickly eliminated within the current commutation process firstly. However, for $C = 23$ μF and $C = 27$ μF, i_{T1} rises again near the voltage zero-crossing point of V_{T1}, leading to the isolation failure. According to the design guidelines, when C is increased to 29 μF, the proposed SSCB can successfully interrupt the fault current. Moreover, it can be inferred from (20) that t_q of the CS-MCT is about 15.5 μs. Such short t_q ensures high robust turn-OFF capability for the SSCB.

D. Turn-OFF Failure of T_2 and T_3

The CS-MCT provides low ON-state resistance due to the triggering of the parasitic fine-pattern thyristor. Even through its cathode-short structure can extract holes when the device is turned OFF, the turn-OFF capability of the CS-MCT is still limited to several amps. Therefore, according to the design guidelines, R_1 and R_2 are set to 185 Ω to meet the requirement of (22). In this part, R_1 and R_2 are reduced to 60 Ω to show the turn-OFF failure of T_2 and T_3. The measured results are shown in Fig. 13. It can be found that, during the fault isolation, T_1 is turned OFF successfully because V_{T1} can rise to the source voltage.

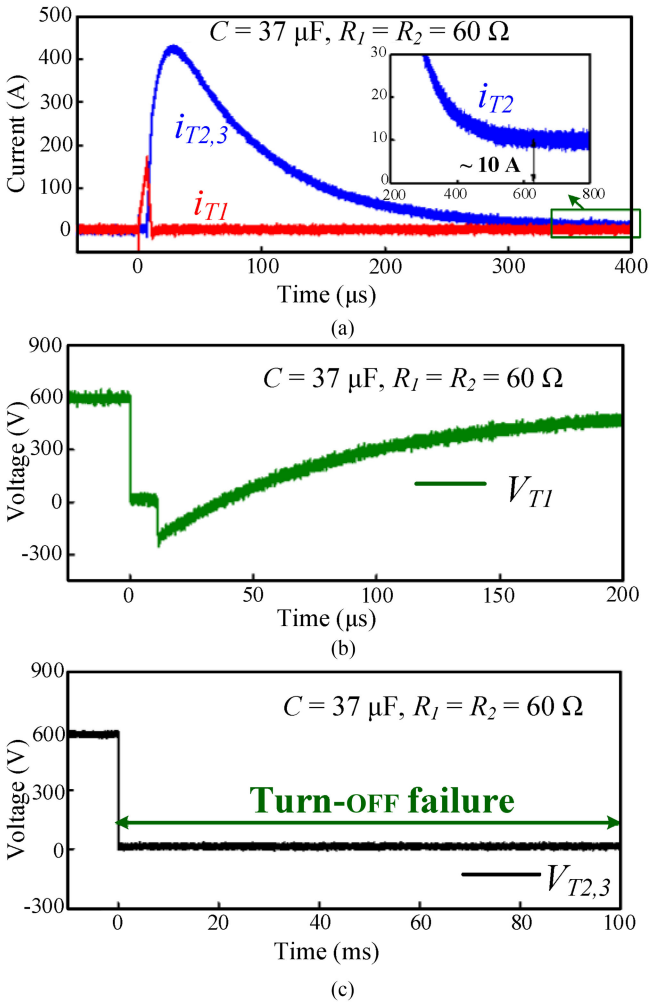

Fig. 13. Turn-OFF failure of T_2 and T_3 during the fault isolation. (a) i_{T1}, $i_{T2,3}$, (b) V_{T1}, and (c) $V_{T2,3}$ waveforms.

However, T_2 and T_3 suffer from turn-OFF failure since V_{T2} and V_{T3} retain their ON-state voltage drop during the entire fault isolation process. This can be physical interpreted that, after the accomplishment of *RLC* series resonance, i_{T2} and i_{T3} are still about 10 A, which are out of the turn-OFF capability of T_2 and T_3. Hence, T_2 and T_3 cannot be turned OFF, and thus *C* cannot be charged again, leading to the failure of the SSCB.

V. Practical Considerations

This section compares the proposed SSCB with TBCBs reported recently, and verifies the practical value and feasibility of the proposed SSCB in LVdc microgrids.

A. Comparison of Different Breakers

The power losses are important for breakers, especially for high-power designs. If breakers can provide lower power losses, a simplified cooling system and higher power efficiency can be achieved. As shown in Table I, the CS-MCT provides lower condition loss than that of the IGBT, the SiC MOSFET and the thyristor. This means that adopting the CS-MCT as the main switch in MC of the breaker (T_1) can enhance the power efficiency for the SSCB, since T_1 usually works in the conduction state and occupies the most of power losses.

Compared with the IGBT or the SiC MOSFET, the CS-MCT and the thyristor can offer lower conduction loss and stronger tolerance to current and voltage surges, but need additional forced commutation technology. As a result, the breakers based on the thyristor or the CS-MCT is attractive in terms of higher power efficiency and more robust fault isolation. Table III list several breaker topologies published recently, which are based on the commutation-forced turn-OFF principle using commutating capacitors (*C*) [22], [25], [27]. It can be seen that t_q of the CS-MCT is smaller than that of the thyristors because some electrons of the CS-MCT can be directly extracted through the cathode-short structure without flowing through the N-well region during the reverse recovery state. As analysed in Section III, the breakers should choose proper *C* to meet (20), thus avoiding the mis-triggering of T_1. Besides, for these breakers, larger t_q and interruption capabilities will result in higher requirement for the capacitance of *C*. Thus, the proposed SSCB adopting the CS-MCT with smaller t_q can choose smaller *C* to interrupt larger fault current in comparison with the other breakers list in Table III. In practice, the volume of C often takes a considerable part of the total breaker size, which indicates that the proposed SSCB can achieve a more compact size and easier integration than the TBCBs in [22], [25], [27].

The proposed SSCB and the TBCBs in [22], [25], and [27] interrupt fault current utilizing the discharge of *C*. Hence, the charging state of *C* plays a decisive role in the interruption capability of the breakers. However, for the breakers in [22], [25], [27], *C* cannot be charged until T_1 is turned ON. If a new fault happens during the charging process of *C* or the fault still exists after the reclosing of T_1, these breakers may fail to isolate the fault. The proposed SSCB can finish the charging process of *C* before T_1 is turned ON, which avoids the possible failure of the breaker under the above situations, and thus features highly reliable and robust interruption capability. Besides, the breaker proposed in proposed [22] can only permit unidirectional power flow, thus limiting the application of the breaker [43].

B. Evaluation of Proposed SSCB in Microgrids

To further verify the practical value and feasibility of the proposed SSCB, the operational performance of the SSCB is evaluated in LVdc microgrids [44]. A four-terminal symmetrical bipolar LVdc microgrid with a rated voltage of ±600 V is established in MATLAB/Simulink, as shown in Fig. 14. The microgrid studied includes five lines with a length of 1 km where the cable resistance and inductance are 17 mΩ/km and 3.3 mH/km, respectively. Each station is composed of an ac–dc three-level PWM converter. According to the experiment result shown in Fig. 12, a successful fault interruption of the SSCB can be guaranteed by selecting *L* of 12 μH, *R* of 1 Ω, *C* of 29 μF, and R_1 (R_2) of 185 Ω. As a result, this SSCB is applied in the dc microgrid.

To verify the performance of the SSCB, a positive pole-to-ground fault without any fault impedance (short circuit fault)

TABLE III
COMPARISON OF DIFFERENT BREAKERS

Breaker	Switch	t_q/μs	Fault current/A	C/μF	Power flow	Charging of C	Offering interruption ability before turn-on of T_1
In [23]	Thyristor	25	100	100	Unidirectional	After turn-on of T_1	No
In [26]	Thyristor	50	10	400	Bidirectional	After turn-on of T_1	No
In [28]	Thyristor	20	12	80	Bidirectional	After turn-on of T_1	No
Proposed	**CS-MCT**	**15.5**	**120**	**29**	**Bidirectional**	**Before turn-on of T_1**	**Yes**

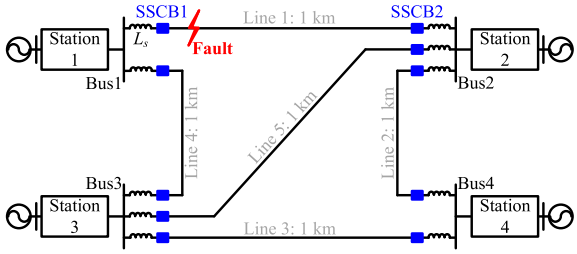

Fig. 14. Topology of the four-terminal bipolar microgrid.

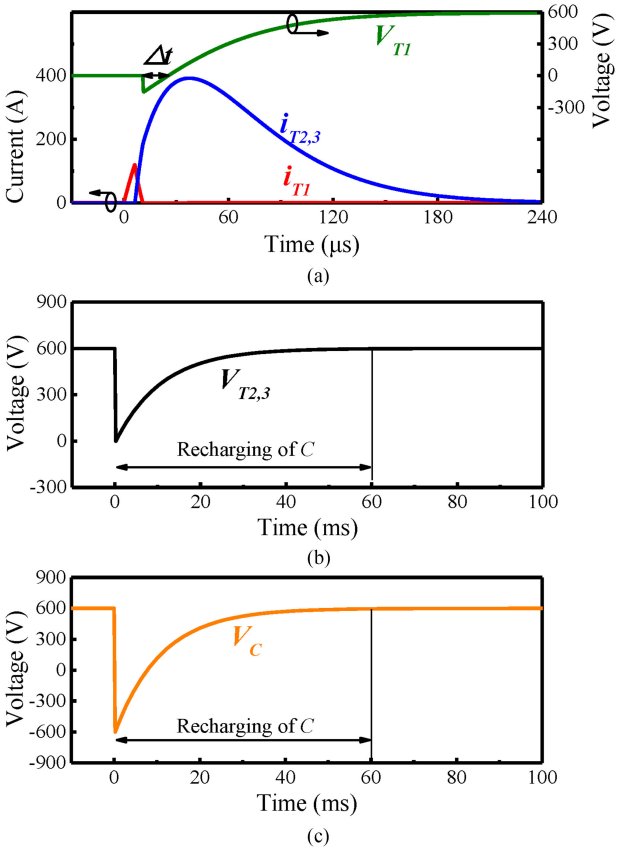

Fig. 15. Transient waveforms during interruption of the SSCB1. (a) i_{T1}, $i_{T2,3}$, V_{T1} and (b) $V_{T2,3}$ and (c) $V_c$waveforms.

is set on the side of the line1 near to the SSCB1 at t = 0. The fault location is shown in Fig. 14. In this case, the current on the line1 increases rapidly. To protect the dc microgrid from being damaged, both the SSCB1 and the SSCB2 should be triggered to isolate the fault.

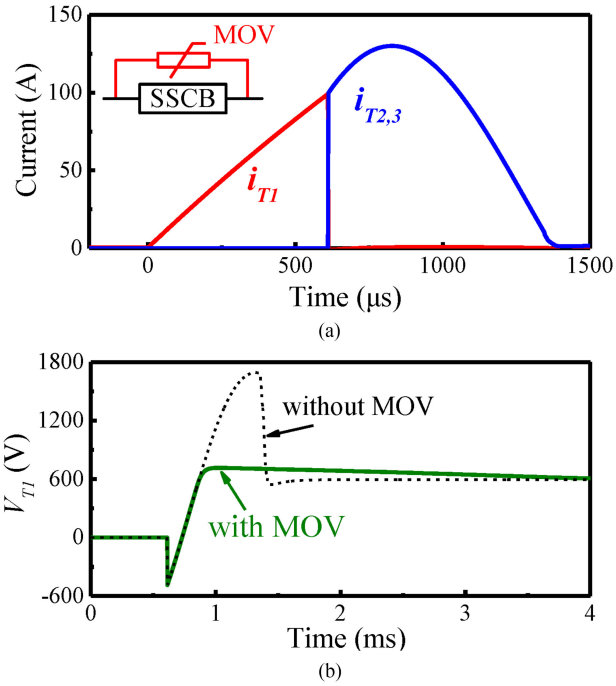

Fig. 16. Transient waveforms during interruption of the SSCB2. (a) i_{T1}, $i_{T2,3}$, and (b) V_{T1} waveforms.

The simulation results of the SSCB1 are shown in Fig. 15. It can be seen that, after the short circuit fault occurs, the line current increases rapidly. Once the fault is detected, the SSCB1 turns ON T_2 and T_3 simultaneously. Then, i_{T1} starts to commutate into $i_{T2,3}$. When i_{T1} drops to zero, T_1 is turned OFF naturally and the fault is isolated. Fig. 15(b) and (c) show that, after the interruption, the capacitor can be charged to the source voltage automatically. Thus, the SSCB can restore the interruption ability before the reclosing of T_1. It is also indicated that the simulation results agree well with the experimental result shown in Fig. 12(c). Differing from the SSCB1, the SSCB2 features large distributing inductive reactance on the transmission line. As the analysis in Section II, there still exists surplus energy on the transmission line after the turn-OFF of T_1, the release of which may cause the voltage overshoot or even damage the dc microgrid. Therefore, the metal oxide varistor (MOV) should be added, which connects in parallel with the SSCB to absorb the surplus energy. As shown in Fig. 16, compared with no suppression situation, the voltage overshoot is considerably reduced by using the MOV.

Fig. 17 shows transient waveforms of the Buses 1 and 2 voltage. It can be seen that the Bus1 voltage and Bus2 voltage

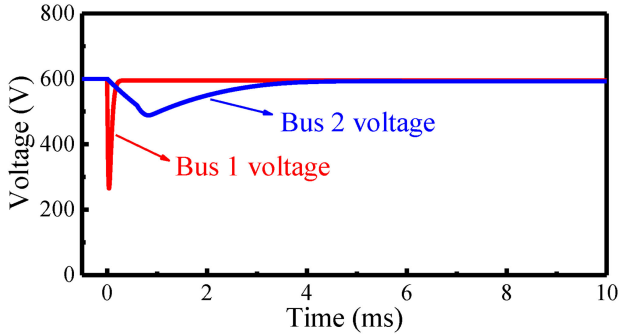

Fig. 17. Waveforms of the Bus1 voltage and the Bus2 voltage.

quickly decrease after the fault occurs. However, the bus voltages can recover after the fault is isolated by the SSCB1 and the SSCB2. As a result, the permanent voltage collapse can be avoided under the fault condition due to the operation of the SSCBs. The results verify the practical value and the feasibility of the proposed SSCB.

VI. Conclusion

A novel solid state circuit breaker (SSCB), which uses the CS-MCT as the main switch to achieve high power efficiency, is proposed for dc microgrid protection. The one-shot triggering characteristic of CC leads to a simple and fast protection process of the SSCB. Because C can be charged by the dc source automatically without additional power supply, CC maintains a compact size and can be easily integrated into dc microgrids. Besides, small t_q of the CS-MCT can reduce the requirement for the capacitance of C, thus further reducing the size of CC. Moreover, the SSCB offers interruption capability before the main switch is turned on. This can avoid the possible failure of the SSCB under the fault that occurs at the initial stage of the turn-ON of the main switch, thus featuring highly robust and reliable interruption capability. To ensure the successful fault isolation of the SSCB, design guidelines are presented through detailed mathematical modeling. Furthermore, the practical value and the feasibility of the SSCB are validated by a 600-V/15-kW laboratory prototype and further verified in LVdc microgrids by simulations. This breaker topology can offer an alternative method for dc microgrid protection that requires high supply reliability and high power efficiency.

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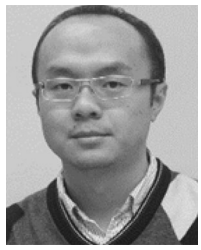

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