Design, Operation, and Loss Characterization of a 1-kW GaN-Based Three-Level Converter at Cryogenic Temperatures

Christopher B. Barth, *Member, IEEE*, Thomas Foulkes, *Member, IEEE*, Oscar Azofeifa, Juan Colmenares, *Member, IEEE*, Keith Coulson, Nenad Miljkovic, *Member, IEEE*, and Robert C. N. Pilawa-Podgurski, *Member, IEEE*

***Abstract*—This article investigates the potential for high power density, high-efficiency power conversion using GaN-based flying capacitor multilevel power converters at low temperature. Specific focus is given to the application of hybrid aircraft powered by liquefied natural gas. Building off of prior characterization of GaN switches over temperature, this article outlines the impact of near-cryogenic operation on the losses of a complete 1-kW inverter. Specific focus has been given to the characterization of the losses in ceramic capacitors and inductors at near-cryogenic operation. A 1-kW GaN-based three-level power converter was designed and successfully tested from room temperature down to −140 °C. Along with the first demonstration of a flying capacitor multilevel converter and associated components at such low temperature, a breakdown of losses over temperature is included to facilitate a better understanding of the opportunities and challenges introduced by this article.**

***Index Terms*—Capacitor, cryogenic, dynamic rdson, electrified aircraft, FCML, flying capacitor multilevel converter, gallium nitride (GaN), hybrid, inverter, liquefied natural gas (LNG), MLCC.**

I. Introduction

LIQUEFIED natural gas (LNG) has been proposed as a possible fuel for next-generation aircraft, such as drones and quadcopters, to reduce cost and minimize environmental impact [3]–[6]. Per unit of energy, natural gas has 23% lower CO_2 combustion emissions than conventional jet fuel in addition to reduced emissions of particulate matter and SO_2 [3]. LNG has the disadvantage of requiring more volume per unit of energy than jet fuel due to its lower mass density. However, per unit of energy, LNG is currently less than 50% of the cost of Jet A fuel and therefore could potentially offer aircraft operators a significant financial savings [7], [8].

Before combustion, LNG must be warmed from a storage temperature of −161 °C to operating temperature. This requirement opens the possibility for new system-level efficiency gains through using the thermal capacity of the LNG for cooling the power electronics required in hybrid fuel/electric systems as well as potentially high-temperature superconductors. The use of LNG for cooling could reduce or eliminate the need for auxiliary heat exchangers, which are normally used to increase the temperature of the LNG for combustion and potentially open the door for high-density, high-efficiency near-cryogenic power electronics.

It is important to note that the apparent power density benefits of LNG are complicated by system-level considerations. Cryogenic cooling offers the opportunity to realize improvements in the efficiency and size of the power conversion electrical system, through the elimination of cooling radiators and other air flow channels, which would otherwise be required. Conversely, LNG has lower energy density than other hydrocarbon fuels and requires cryogenic storage and fuel system insulation. Nevertheless, system-level studies of urban air mobility hybrid aircraft have found that by taking advantage of the low-temperature fuel to cool the power electronics and genset generator, the maximum system aircraft range could be extended by 20% [9].

In addition to aviation applications, LNG is seeing increasing use in utility power generation systems. Recent advancements in gas extraction have lowered the cost of natural gas and made it very competitive for electricity generation. After overseas shipping in liquid form to minimize shipping cost, evaporation of LNG is often accomplished using thermal energy from seawater or ambient air before the fuel is burned. The cooling of the generation system and supporting power electronics is another option for utilizing this low-temperature potential energy [10].

Historically, much of the work in the field of low-temperature power electronics has been focused on the survival of the power

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Christopher B. Barth, Thomas Foulkes, and Oscar Azofeifa are with the Electrical and Computer Engineering Department, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA (e-mail: cbarth2@illinois.edu; foulkes2@illinois.edu; ora2@illinois.edu).

Juan Colmenares is with the Infineon Technologies, 10044 Stockholm, Sweden (e-mail: juanco@kth.se).

Keith Coulson and Nenad Miljkovic are with the Mechanical Science and Engineering Department, University of Illinois at Urbana–Champaign, Urbana, IL 61801 USA (e-mail: kcoulso2@illinois.edu; nmiljkov@illinois.edu).

Robert C. N. Pilawa-Podgurski is with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA (e-mail: pilawa@berkeley.edu).

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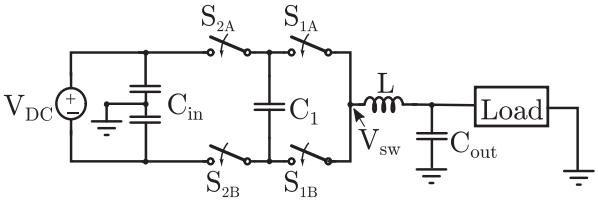

Fig. 1. Schematic drawing of the three-level GaN FCML inverter.

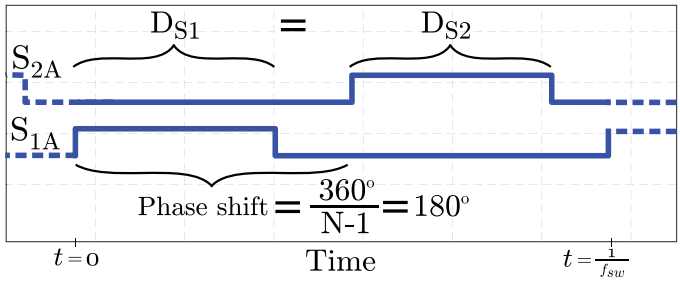

Fig. 2. High-side gate signals for three-level FCML driven with PSPWM.

electronic system at low temperature instead of on increased efficiency. In particular, significant work and numerous publications have been completed by NASA with a focus on deep space probes and satellites [11]–[15]. In these applications, converters are often packaged next to sources of heat, such as auxiliary heating units or radioisotope thermoelectric generators, specifically to ensure their survival at low temperatures. The ability to operate the converters without this heat simplifies spacecraft design and improves reliability. This earlier work tested silicon-based converters in the range of 5 W to 1 kW with switching frequencies in the range of 50 to 200 kHz. The hardware tested spanned both custom designed power converters as well as commercial, off-the-shelf power modules. Generally speaking, the converters performed fairly well down to $-190\,^{\circ}$C. Differences in control hardware led to variations in the regulation capability of the converters at low temperature and all converters resumed operation when warmed. Most changes in the total converter efficiency which were reported were minor, and both gains and losses in efficiency were reported.

A number of excellent survey papers have been published summarizing the work done in low-temperature power conversion [16]–[18]. The vast majority of the work on cryogenic power electronics performed to date has focused on silicon devices. As will be discussed further, silicon field effect transistor (FET) devices generally exhibit improved performance at low temperature in contrast to silicon bipolar devices, which degrade significantly. In contrast to the work that has been accomplished on silicon-based converters, relatively little work has been done to evaluate wide-bandgap (WBG) power transistors at ultralow temperatures. Even less attention has been paid to the benefits for a complete converter incorporating WBG devices at ultralow temperatures. To date, GaN devices have been found to operate far more effectively than SiC devices at reduced temperatures and appear to hold potential for both functionality and improved performance at cryogenic temperatures [19], [20].

This article seeks to build upon prior device characterization and demonstrate the implementation of a complete 1 kW, single-phase, three-level inverter, using GaN power FETs. The goal of the investigation is to verify system functionality, as well as quantify the efficiency improvements possible through low-temperature operation. A three-level flying capacitor multilevel (FCML) topology was chosen, as recent work has demonstrated its potential for very high power density and efficiency, which is critical in aerospace applications [21]–[24]. This article also demonstrates the use of an LN2 cooled heat sink in a simple enclosure as the mechanism for cooling the power converter without the need for a special temperature-controlled chamber. This technique is uncommon in the literature as most work on cryogenically cooled power converters has depended on temperature chambers or direct submersion into LN2.

The rest of this article is organized as follows. Section II of this article discusses the consideration given to the effects of low-temperature operation on each component in the design. In addition to the GaN FETs, the impact of temperature on the capacitors and inductors required to build the FCML converter is also key to the overall converter efficiency at low temperature. In Section III, the design of the converter hardware and thermal management as well as the construction of the test environment is discussed. The experimental results obtained for a full converter operation are presented in Section IV followed by a discussion of the elements of converter losses over the temperature range tested in Section V. Finally, a review and summary are given in Section VI. This article is an extension of earlier conference papers [1], [2], and includes significantly expanded analysis on the impact of temperature on the losses of each component in the converter as well as an improved model of the overall converter losses, which accounts for the trend in measured losses.

II. Design of Converter

The schematic diagram of the single-phase, three-level FCML converter is shown in Fig. 1. Since the introduction of the FCML [25], there has been increasing interest in the power density, efficiency, and electromagnetic interference advantages of this topology [21], [26]. The power density benefits of the FCML topology stem primarily from the higher energy storage density of capacitors than inductors. In practice, it is found that the energy storage of available capacitor technology is up to two orders of magnitude higher than that of inductive energy storage [27]. This suggests that, at present, topologies based primarily on capacitive energy transfer and filtering have the potential to achieve higher power density than those based on inductive energy transfer.

In this article, the three-level FCML is driven using phase-shifted pulsewidth modulation (PSPWM) [25], [28] in which each gate signal is controlled at equal duty ratio and phase shifted from adjacent signals by an angle of $\frac{360^{\circ}}{N-1}$ where N denotes the number of converter levels. The opposing switches are complementary with dead time added to prevent shoot-through. In this three-level converter, PSPWM control dictates that switch set S_1 in Fig. 1 is shifted 180° from switch set S_2, and switches A and B are complementary. Fig. 2 shows the PSPWM gate signals for

the high-side switches S_{1A} and S_{2A}. Each switch operates at the frequency f_{sw}. However, due to the relative phase shift between switch sets, the effective frequency seen by the filter inductor is $(N-1) \times f_{sw}$. Combined with the fact that the inductor voltage amplitude is reduced to $\frac{V_{bus}}{N-1}$, the required filter inductance is reduced by a factor of $(N-1)^2$ as compared to a two-level inverter operating off of V_{bus}.

Recent prototype demonstrations of high-level count FCML inverters [21], [23], [24], [26], [29] have generated renewed interest in the potential benefits of this multilevel topology for multi-kilowatt applications. The objective of this article is to extend the demonstrated benefits of the FCML topology to cryogenic applications. As cryogenic temperatures are well outside the range of performance specified in most component manufacturer data sheets, there is little information on the functionality of individual devices at low temperature. The remainder of Section II will discuss the impact of each component on the performance of the overall converter prototype.

A. FET Operation at Low Temperatures

Driven by the frigid hazards of space exploration [11], [12] and the opportunity to increase system-level efficiency through superconducting machines and power electronics [30]–[32], silicon FET performance at cryogenic temperatures has been studied extensively [33]. Reductions in ON-state resistance of 5–10 times have been demonstrated for some devices [34], as well as reduced diode reverse recovery and faster switching times yielding on the order of 25% reduction in total switching loss [35]. Additionally, silicon FET threshold voltages tend to rise slightly ensuring robust operation [34].

In the face of these benefits, there are also some challenges with the cryogenic operation of silicon devices. Although ON-state resistance decreases as the temperature is lowered from ambient, below 77 K (−196 °C) this trend reverses and conduction is limited by carrier freeze-out. The blocking voltage of Si devices has also been shown to decrease by 20%−30% at liquid nitrogen (LN2) temperatures [33], [35].

Wide bandgap GaN and SiC devices have been gaining traction in research and some industrial applications with the majority of focus being placed on the high-temperature capabilities of the devices. However, the improved figures of merit of wide-bandgap devices, minimal or no reverse recovery current (for SiC and GaN, respectively), as well as high conductivity have prompted investigation into the cryogenic operation of these devices. Additionally, the inherent radiation hardness of the wide-bandgap structure makes these devices potentially useful in space applications.

With their higher voltage ratings, SiC devices are appealing for many high-power applications, such as cryogenic machines. It has been shown that the breakdown voltage of SiC devices holds roughly constant under cryogenic conditions as does the threshold voltage. Thus, the devices are stable and functional at low temperature [38], [39]. However, although the devices are stable at cryogenic temperatures, their conduction and switching losses increase significantly. SiC ON-state resistance increases much more quickly than Si due to carrier freeze-out and electron trapping, with a significant increase in resistance at temperatures below 200 K (−73 °C). Additionally, SiC FET switching tends to slow down, which increases switching losses, and the body diode exhibits a higher voltage drop [19], [40]. Thus, while SiC devices are potentially functional at low temperatures, there appears to be no efficiency benefit to be gained.

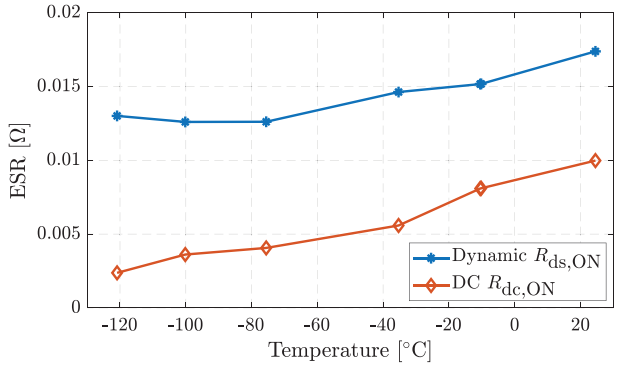

Fig. 3. Measured dc and dynamic $R_{ds,ON}$ of EPC2034 over temperature. While dc measurements suggest a ≈76% reduction, the dynamic ON-state resistance only decreases by ≈27%, and shows a slight increase below −80 °C [36], [37].

Gallium nitride devices have also been tested for operation under cryogenic temperatures. GaN devices do not suffer from carrier freeze-out at low temperature and exhibit significant reduction in dc conduction resistance. Additionally, GaN switching losses have been shown to decrease as the temperature is lowered and the blocking voltage exhibits minimal change [19], [41], [42].

In [36], Colmenares *et al.* documented the performance of the EPC2034, a high electron mobility transistor from Efficient Power Conversion Corporation (EPC) from ambient down to −195 °C. The dc ON-state resistance for the device decreased to 20% of its nominal value without any sign of carrier freeze-out, as shown in Fig. 3. The device operation also remained stable as the threshold voltage was relatively unchanged over the range tested. It should be noted that recent evaluation of higher voltage (i.e., 650 V) GaN devices [42] has shown a significant reduction in threshold voltage at low temperature, suggesting threshold tolerance at low temperatures differs among various GaN devices and voltages. Interestingly, the work in [36] also showed that although the response rate of Si gate drivers increased at low temperature, the switching speed of the EPC2034 itself did not change significantly with temperature.

Historically, one drawback of GaN has been the phenomenon of dynamic ON-state resistance, or dynamic $R_{ds,ON}$, which is a decaying $R_{ds,ON}$ exhibited when the device transitions from blocking voltage to conducting [43]. Dynamic $R_{ds,ON}$ is the result of electron trapping during the OFF-state of the device and is accentuated by higher blocking voltage stress and device temperature. The elevated conduction resistance of dynamic $R_{ds,ON}$, which decays on the order of milliseconds, dictates that the functional $R_{ds,ON}$ of the device in a switching power converter may be as high as twice the dc value provided in manufacturer data sheets. A detailed method of characterizing device $R_{ds,ON}$ as a function of blocking voltage and temperature is presented

in [37]. Using this approach, additional measurements of the EPC2034 dynamic $R_{ds,ON}$ were taken down to $-120\,^{\circ}C$ as shown in Fig. 3.

The measurements in Fig. 3 show that although the EPC GaN device does not exhibit carrier freeze-out like SiC, the dynamic $R_{ds,ON}$ of the EPC2034 does become more pronounced as the device is cooled, as suggested by the divergence of the dynamic and dc values at lower temperature. The dynamic $R_{ds,ON}$ at $-120\,^{\circ}C$ is indeed lower than at ambient temperature; however, the dynamic $R_{ds,ON}$ decreases less linearly than the dc $R_{ds,ON}$. It can be seen that the dynamic $R_{ds,ON}$ decreases down to $-80\,^{\circ}C$ and then increases slightly as the temperature is reduced further. This trend of increased impact from dynamic $R_{ds,ON}$ at low temperature is alluded to in [44], which reports that the drain-to-source current under the pulsed transient analysis was significantly more distorted at 100 K than at 300 K. It is believed that extra time is required for the trapped carriers to gain kinetic energy at cryogenic temperatures. This trend in the effective ON-state resistance will also become evident in the measurement of overall converter losses discussed in Section V.

Successive generations of GaN devices have exhibited reduced dynamic $R_{ds,ON}$ at ambient and elevated temperatures, as manufacturers work to resolve this nonideality. Dynamic $R_{ds,ON}$ data are not provided by manufacturers, but one example of this trend can be seen in the 27% reduction in dynamic $R_{ds,ON}$ at ambient temperature between successive generations of 200 V, nominally 10 mΩ devices shown in [37] and in the discussion on dynamic $R_{ds,ON}$ at high temperature in [45]. As the dynamic $R_{ds,ON}$ of these devices at ambient temperatures is improved, it can be expected that their performance at cryogenic temperatures will improve as well.

B. Gate Driver and Isolator Characterization

In [46], Colmenares *et al.* demonstrated that the LM5113 half-bridge gate driver functioned well down to $-195\,^{\circ}C$. The only change in behavior was a decrease in both the turn-ON and turn-OFF times of the gate driver. The equal decrease in both functions is attributed to the higher electron mobility of silicon at low temperature and means that the operation of the GaN switch would be unchanged and an equal duty ratio and dead time can be used.

In addition to gate drive ICs, the FCML topology requires gate driver isolation due to the multiple flying switching nodes. The ADUM5210 and SI8423BB-D-IS devices were used for power and signal isolation, respectively. During testing, it was found that ADUM5210 provided a stable isolated voltage over the temperature range of interest. As for LM5113, the signal propagation rate of SI8423BB-D-IS increased slightly due to the change in electron mobility of silicon. The change in signal propagation time was slightly less than the change in the LM5113 response rate due to the lower current required for signal driving as compared to the current required to charge the gate of EPC2034 FET.

C. Capacitor Characterization

Because capacitors play a critical role in the FCML converter operation, it is important to understand their loss characteristics over temperature. Multilayer ceramic capacitors (MLCCs) exhibit some of the highest energy storage density among dry electrolytic devices. MLC capacitors are grouped into three main classifications by IEC/EN 60384-1, of which two are most commonly used in power electronics applications. Class I capacitor dielectrics are paraelectrics with good capacitance stability over temperature and bias voltage, but relatively low energy storage density. Class II capacitor dielectrics are ferroelectrics with higher energy density, but these devices also exhibit higher variability over temperature and a decrease in capacitance with applied voltage bias. Within these classifications, devices are tailored for a range of operating temperatures, each designated by a three character code.

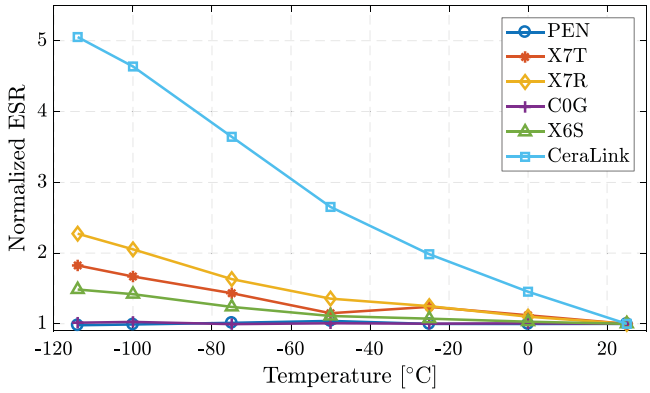

Fig. 4. Measured large signal equivalent series resistance (ESR) over temperature normalized to ambient value for several different capacitor dielectrics. Measurements are taken using the large signal test outlined in [47].

In order to understand the impact of cryogenic operation on MLCCs, six different devices were tested using the large-signal, low-frequency technique outlined in [47] over the temperature range of interest. In this test, the capacitor voltage was cycled from zero to rated voltage at 60 Hz, and energy flowing into and out of the capacitor was measured using Yokogawa WT310 power meters. Based on the capacitor round-trip energy efficiency, the capacitor losses and equivalent ESR can be calculated. Fig. 4 shows the relative change in ESR for each device over the temperature range tested.

It can be observed that the devices comprised of ferroelectric dielectric materials (X7T, X7R, and X6S) exhibit a measurable increase in ESR as their temperature decreases. The same holds for the CeraLink capacitor, which uses an antiferroelectric dielectric designed to exhibit maximum capacitance at rated bias [48]. The increase in ESR at low temperature is especially pronounced in the CeraLink device as a consequence of the fact that the device composition is tailored for the high-efficiency operation at temperatures of up to $150\,^{\circ}C$ to facilitate high-temperature power conversion. These findings for Class II devices are substantiated by prior literature [49], and similar results have been shown for solid tantalum capacitors [50], [51]. It is suspected that the higher dielectric loss in ferroelectric dielectrics at low temperature is the result of an increase in ferroelectric coercive field at low temperature [49].

In contrast to the high permittivity Class II materials, the Class I ceramic and film-based polyethylene naphtalate (PEN) capacitors exhibit negligible change in ESR over temperature,

corroborating the trend noted in [52]. This is because Class I capacitors, such as C0G, are made of a paraelectric, low permittivity, material and are very stable over temperature and voltage bias. This characteristic suggests that Class I dielectrics and film-based capacitors may be preferable in cryogenic applications provided they are able to meet energy density requirements. A significant drawback of C0G and film-based dielectrics is their lower permittivity as compared to Class 2 ceramics. This low permittivity results in a low energy storage density and a requirement for larger devices in power conversion applications. For applications requiring higher permittivity and higher density energy storage, fully functional capacitors using dielectrics optimized for operation near 77 K have been tested and may play a role in the design of future LNG or otherwise cryogenically cooled systems [52], [53]. In addition to having optimal permittivity at low temperature, these dielectrics also exhibit higher dielectric breakdown strength and higher thermal conductivity at cryogenic temperatures.

In this article, an X6S dielectric device was selected due to its high energy density [47] despite the X6S devices having somewhat higher ESR at low temperatures than the C0G devices. In specific applications, designers may be more likely to select a lower energy density technology with potentially lower ESR at cryogenic temperatures. The impact of temperature on the reliability of the capacitors would also be a significant consideration in the development of a cryogenically cooled converter for commercial applications. The coefficient of thermal expansion (CTE) for FR-4/G-10 boards has been reported to be in the neighborhood of $\approx$18 ppm/°C [54], whereas the CTE of barium titanate capacitors falls in the range of $\approx$8 to $\approx$13 ppm/°C [55]. Despite this mismatch, the ceramics have proven to be relatively robust to thermal cycling between the temperatures of -40 and $+85$ °C. This robust performance is likely due to the compressive stress exerted on the capacitors by the CTE mismatch between the ceramic in the capacitor and solder (both the capacitor end-plating and the printed circuit board (PCB) attachment). This compressive stress persists even at the temperature extremes tested and has reduced impact on the devices because the compressive strength of ceramic materials has been reported to exceed tensile strength by 5–10 times [55]. Additionally, the larger CTE of FR4 materials results in compressive stress on the capacitors as the assembly cools after soldering, and increases as the devices are cooled to cryogenic temperatures.

D. Inductor Characterization

Like capacitors, the dependence of inductor magnetic properties on temperature is well recognized. Nearly all magnetic materials have been found to exhibit some increase in hysteretic losses with a decreased temperature. Ferrites are some of the worst offenders with losses increasing as much as $10\times$ between ambient temperature and -196 °C. Different ferrite compositions can also exhibit significantly different responses depending on the temperature at which they are tailored to operate. Aside from ferrites, losses in powdered permalloys were found to increase in the neighborhood of 40% and iron composites also exhibit slightly increased losses at cryogenic temperatures [56]. These changes arise from an increased resistance to domain wall motion and rotation as well as changes in the coercive force that arise at low temperature [57]–[59]. In addition to increased losses, ferrite cores have also been shown to exhibit a decrease in permeability with decreasing temperature, which could be very detrimental depending on operating conditions and control strategy [18].

Prior studies of power inductors at cryogenic temperatures have suggested that powdered metal cores are less sensitive to low temperature variation in both their losses and inductance [56], [60], [61]. In [62], Jankowski *et al.* focused specifically on the behavior of iron-based powdered metals under cryogenic conditions to understand what role these materials could play, not only in the development of cryogenic inductors, but also in cryogenic machines and other magnetic systems. A careful characterization of two different materials was performed, which found that loss density increased between 37% and 200% depending on the material as the temperature was cooled from room temperature to -196 °C [62]. Additionally, the permeability of pure powdered iron was reported to remain nearly constant between room temperature and 4.2 K [63].

Inductors from the IHLP series by Vishay were used in this article. The final device used was the IHLP-6767-GZER220M-01 inductor. This device has a nominal inductance of 22 μH. Manufacturers do not fully disclose the materials their devices are made of; however, Vishay indicates that the "01" material is a compressed pure powdered iron with a particle size of $\approx$ 4 μm [64]. This small particle size minimizes the volume in which eddy currents are able to circulate and reduces losses. Additionally, the IHLP series of devices are offered with a wide selection of values and low form factor, which allows them to integrate well with the cold plate-based cooling.

Due to the powdered iron composition of the IHLP inductors, the losses and permeability are likely to be comparatively stable as the inductor is cooled. However, in an effort to better understand the loss mechanisms in the three-level FCML converter, direct measurements of losses over temperature were performed using a multistep measurement process combining electrical and calorimetric methods. The combined strategies were used for validation of electrical measurements because calorimetric methods are challenging at cryogenic temperatures.

Calorimetric loss measurements rely on a thermal mass with a known volume, density, and specific heat to capture losses generated from the device under test (DUT). The thermal mass is located in an isolated chamber with high thermal impedance to ambient, and any energy dissipated by the DUT into the thermal mass is exhibited as an increase in mass temperature. The thermal impedance from the mass to ambient and, indeed, the exact specific heat of the thermal mass can be calibrated based on a known power dissipation.

In this article, the system was calibrated using the DUT inductor with a dc current of 10 A_{dc}. The exact dissipation in the inductor during the calibration run was known based on the dc current passing through the inductor and the voltage across the terminal. The rise in thermal mass temperature over time was measured using thermocouples and the Fluke Hydra DAQ controlled by a LabView VI. In order to maintain a constant

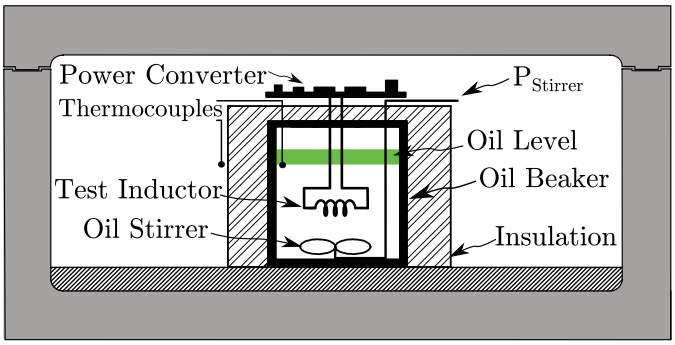

Fig. 5. Cooler-housed calorimetric measurement system cutaway. Power converter replaced with a dc source for calibration.

temperature throughout the oil, a stirring motor was submerged in the oil. Because the string mechanism was completely submerged, both the losses and stirring motion contributed to oil heating. The power applied to the stirrer (P_{stirrer}) was therefore added to the power dissipated in the inductor (P_{loss}) to determine overall dissipation in the oil (P_{cal}) such that

$$P_{\text{cal}} = P_{\text{loss}} + P_{\text{stirrer}}. \tag{1}$$

The relationship between the change in oil temperature over time and the power dissipated in the oil is then characterized as

$$P_{\text{cal}} = (m_{\text{oil}}\, C_{\text{oil}} + k)\left(\frac{\Delta\text{Temp}}{\Delta t}\right) \tag{2}$$

where the parameters m_{oil}, C_{oil}, and Δt are the total mass of oil, the heat capacity of the oil, and the time required to change the temperature of the oil by Δ Temp respectively. The factor k is the calibration factor for the test system and was calculated based on the known power dissipation during the dc calibration test and the measured rise in the temperature of the oil. This factor accounts for the thermal mass of the glass beaker and the heat loss from the system. It was assumed that the thermal impedance to ambient remained constant over the 25–40 °C temperature swing used for testing. The overall layout of the test chamber is shown in Fig. 5.

With the calibration factor known, the calorimetric test system was used to measure the loss in the inductor of the FCML converter while operating in dc–dc mode at a constant duty ratio. In an effort to increase the proportion of core losses in the measurement, two inductors were used in parallel and a length of wire was added between the inverter and the IHLP-676GZ-01 inductors, thus allowing them to be submerged in the beaker of oil while the converter was positioned above the beaker. The converter duty ratio was set at 75% in order to maximize the current ripple in the inductor and accentuate potential losses in the core material [65]. The converter was then run at a power level of 1.2 kW between source at 100 V and a load at 75 V. Solving (1) and (2) for P_{loss}, the power dissipated in the inductor during converter operation was found to be 6.0 W. This value is also in reasonable agreement with manufacturer-supplied loss estimates for this operating condition [66].

The final measurement of inductor losses was conducted electrically using the hardware in Table I. After experimentation and multiple iterations, the DA1855A differential amplifier

TABLE I
HARDWARE USED FOR ELECTRICAL LOSS MEASUREMENTS

Device	Model	Error
Differential voltage probe	DXC100A	$\pm 1\%$
Differential amplifier	DA1855A	$\pm 1\%$
Current Probe	CP030A	$\pm 1\%$
Oscilloscope	HDO6104A	$\pm 0.5\%$
	Error propagation	$\pm 1.5\%$

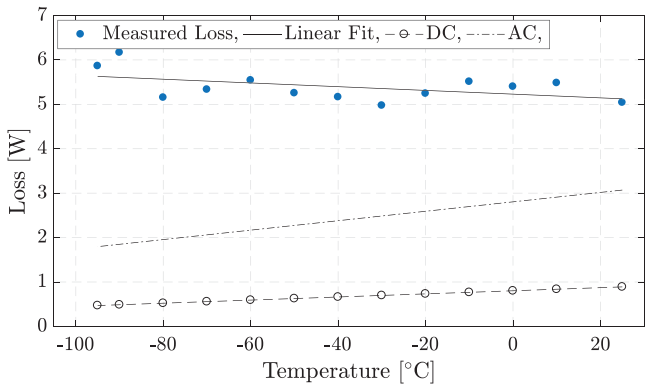

Fig. 6. Electrically measured losses for two parallel inductors in dc–dc test. $V_{\text{in}} = 100$ V, $D = 0.75$, $I_{\text{load}} = 7.4$ A, $F_{\text{sw}} = 70$ kHz, and $F_{\text{effective}} = 140$ kHz. It is observed that the overall losses remain relatively stable. The dc and ac losses plotted are estimated based on inductor temperature.

from Teledyne LeCroy with a DXC100A passive probe was selected for voltage measurements. This instrument has a signal conditioning preamplifier with a high common-mode rejection ratio of 94 dB at 100 kHz. A high common-mode rejection ratio proved essential for accurately measuring the average voltage across the inductor in the range of millivolts in the presence of an instantaneous voltage that fluctuated several tens of volts. In addition to the DA1855A/DXC100A combination used for measuring inductor voltage, the CP030A current probe was used to measure current flowing through the inductor and data were sampled at 10 GS/s using the HDO6104A oscilloscope. Average power lost in the inductor was calculated based on a running integral of the instantaneous power over 400 ns or 24 effective switching cycles at the converter switching node. After proper configuration of the measurement equipment, the electrically measured loss fell within 5% of the calorimetric measurements, thus giving validation that an effective system for electrically measuring loss and, in particular, change in loss over temperature had been obtained.

After validation of the electrical measurement configuration, measurements of inductor loss were taken at inductor core temperatures from 25 °C down to −95 °C. Fig. 6 plots electrically measured inductor losses over temperature for a single test condition. Due to the sensitivity of the measurement, there is a notable variation between data points; however, the trend in the data gives an understanding of the core material performance at low temperature. It can be seen that the overall inductor loss remained relatively constant over the temperature range tested. It is understood that this is due to the conflicting trends of the reduction in copper resistivity and the increasing losses in the

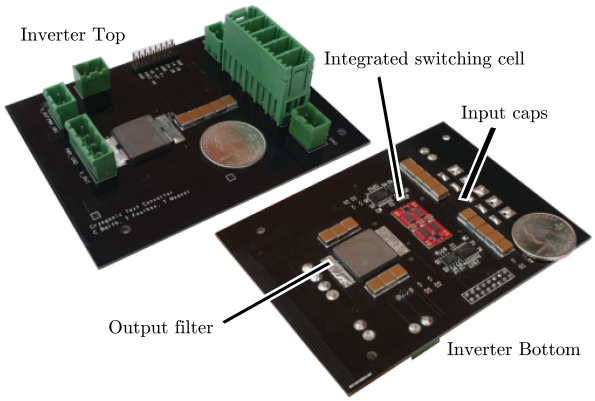

Fig. 7. Top and bottom views of a three-level inverter.

TABLE II
INVERTER COMPONENTS LIST

Component	Part Number	Parameters
GaN switches	EPC 2034	200 V, 7 mΩ
GaN gate driver	Texas Instrument LM5113	5 V, half bridge
$R_{\text{gate,on}}$		22.5 Ω
$R_{\text{gate,off}}$		0.5 Ω
Flying Cap., C_1	TDK C5750X6S2W225K250KA x5	2.2 μF, 4.3 mΩ
Filter Cap., C_{out}	TDK CGA9Q1C0G2J104J280KC x6	0.1 μF, 0.5 mΩ
Inductor, L	Vishay IHLP6767GZER220M01	22 μH, 25 mΩ
Signal isolators	Silicon Labs Si8423BB-D-IS	
Signal Filters	R = 229 Ω , C = 47 pF	
Isolated power	Analog Devices ADUM5210	
PWM Generator	TI TMS320F28069	

ferrite core. Based on the inductor current ripple, the dc and ac losses can be estimated using the modified Steinmetz equation incorporating the change in the resistivity of copper [66], [67]. The coefficient of resistivity for copper is 0.393% per °C. As a result, the inductor ohmic resistance decreased by 49% between 25 and −100 °C, leading to a 49% reduction in both the ac and dc winding losses.

III. HARDWARE DEVELOPMENT

A. Final Converter With Thermal Management

An annotated photograph of the full three-level FCML converter hardware prototype is shown in Fig. 7. In order to provide sufficient flying capacitance and minimize trace lengths and parasitic switching loop inductance, the flying capacitance is divided into two sections. The bulk of the capacitance is located immediately adjacent to the switches on the opposite side of the PCB. The parasitic inductance of the commutation loop is also further reduced through the use of local decoupling capacitors immediately adjacent to the EPC2034 GaN transistors [21]. The gate resistance and switch transition time were adjusted to be as small as possible without causing excessive ringing. A 22.5 Ω resistor in combination with the 4 A LM5113 gate driver was determined to be satisfactory. To ensure that all devices are cooled to a similar temperature, the supporting electronics, such as signal isolators, gate drivers, input bus capacitors, and the output filter capacitors are located with the GaN devices on the bottom of the inverter PCB. A complete component listing is given in Table II.

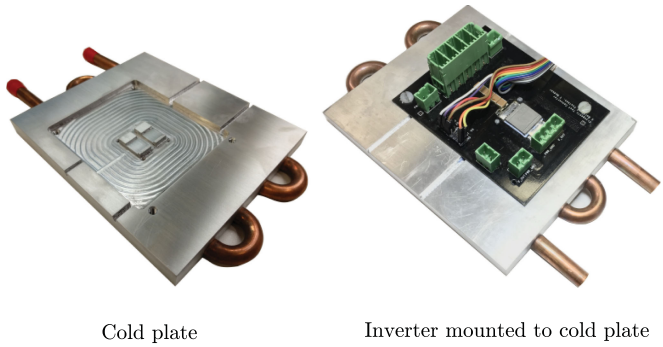

Fig. 8. Milled cold plate and cold plate with the FCML inverter.

The converter is cooled using a cold plate machined to the negative height of the primary converter components as depicted in Fig. 8. The entire cavity of the cold plate was covered with Bergquist gap filler 4000 in order to provide a good thermal interface and even cooling of the components on the lower side of the inverter. The space between the GaN devices and the heat sink must be large enough to provide electrical isolation between the uninsulated sides of the devices and the heat sink while simultaneously minimizing thermal impedance through the gap filler. In order to accomplish this, the clearance between the cold plate surface and the GaN devices was set at 0.02″. The cold plate adjacent to the remainder of the components was milled with 0.04″ clearance in order to minimize assembly challenges for the inductor and filter capacitors, and because the heat energy dissipated in these components is far less than the GaN devices. A hole for the output filter inductor was milled through the PCB so that the inductor is recessed through the PCB and located at the same height as the filter capacitors, thus minimizing the overall height of the PCB and cold plate.

The assembly strategy discussed here is sufficient for evaluating the electrical performance of the converter. The development of a flight-rated design would require a detailed analysis of the thermal expansion coefficient of each component in order to ensure long-term reliability. The EPC 2034 GaN FETs used in this article are fabricated on a passivated die with solder bumps. This configuration is important for minimizing commutation loop inductance and switching losses, but it also makes the device susceptible to mechanical stress [68] due to disparity between coefficients of thermal expansion in the FET and PCB. For this reason, a leaded package that provides for dissimilar expansion between the silicon and PCB may be preferable.

B. Design of Cryogenic Test System

Cryogenic cooling in ambient moisture levels will lead to water vapor condensation and icing on the power converter. Industrial cryogenically cooled systems depend on extensive insulation to limit heat intake from the ambient environment and prevent icing. In a research setting, this insulation would be time consuming to apply and remove between tests. To prevent icing on the converter in this article, the converter and cold plate were placed inside a Lesker chamber and purged with dry nitrogen gas. The chamber and cold plate test configuration are shown

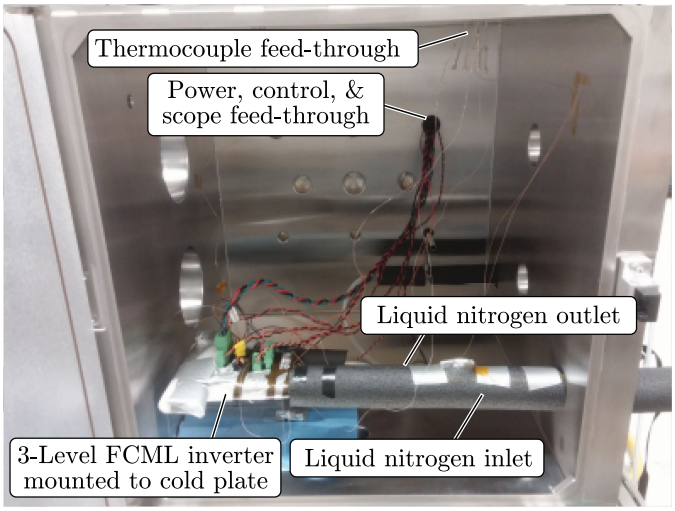

Fig. 9. Vacuum chamber with converter configured for testing. Thermocouples, power, and LN2 were passed through feedthroughs to the converter.

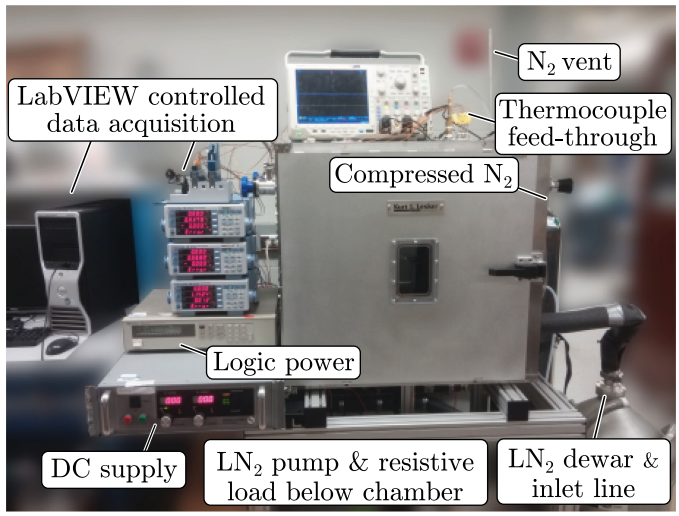

Fig. 10. Complete cryogenic experimental setup with NI LabVIEW data acquisition.

in Figs. 9 and 10. After the initial purge, a low-volume flow of gaseous nitrogen into the chamber was used to maintain a small positive pressure and minimize water vapor entering the unsealed wire feed-throughs. It should be emphasized that the Lesker chamber was simply a convenient volume in which to conduct tests. In [2], similar work was accomplished using an insulated picnic cooler. The converter was cooled by LN2 drawn through the cold plate using an Instec model LN2-P8AD10 eight-stage pump. The flow rate of the LN2, and consequently the temperature of the cold plate, was set by manually controlling the speed of the pump.

In order to minimize the heat absorbed by the LN2 as it was pumped up from the dewar into the cold plate, the LN2 feed line and cold plate were heavily insulated. Type K thermocouples were attached directly onto the integrated switching cell, the cold plate surface, the LN2 input line, the LN2 output line, and on the inductor. These temperatures were tracked and logged along with electrical measurements of voltage, current, and power at the input and output of the converter taken using Yokogawa WT310 digital power meters and a National Instruments LabVIEW automated data collection virtual instrument as shown in Fig. 10.

Although this system used a simple blanket of nitrogen for testing, the insulation required to implement cryogenic power electronics in a system such as a hybrid aircraft is an important aspect of the design. The use of cryogenic fuel for cooling the electric power conversion hardware could potentially eliminate much of the radiators and ducting otherwise required for cooling. In larger VTOL-type systems, this cooling strategy is estimated to increase the power conversion density by 50%–70% [69]. Despite this increase in the effective density of the power conversion components, the overall volume for hybrid electric VTOL powertrains is estimated to increase by 10% due to the required cryogenic support system [9]. This emphasizes the importance of careful design of the overall powertrain and thermal management system if the full benefits of cryogenic cooling are to be gained.

TABLE III
THREE-LEVEL FCML TESTING CONDITIONS

Parameter	Value
Input voltage	150 Vdc
Load Voltage	45 Vrms
Load Frequency	60 Hz
Load Type	Resistive
Load Value	4.7, 10.8, 16.8, 23.5 A
Power Factor	Unity

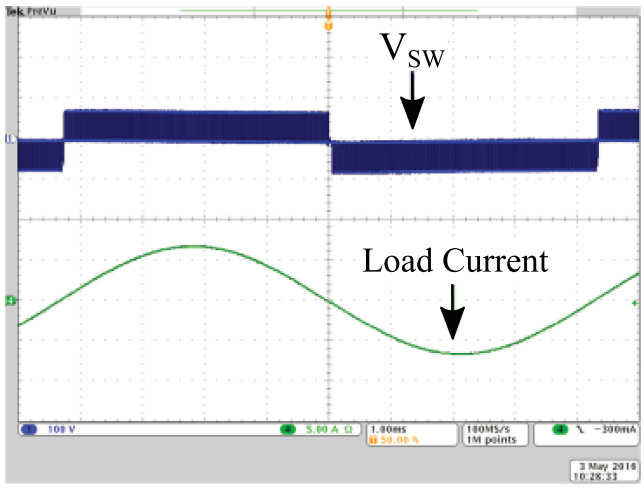

Fig. 11. Waveforms showing the output current and the switching node voltage (V_{SW}) of the three-level GaN converter.

IV. EXPERIMENTAL RESULTS

The testing conditions for the three-level FCML converter are captured in Table III. In this test, the converter is operating as an inverter at a low frequency of 60 Hz; however, the FCML topology is capable of operating as a dc–dc converter and passive balancing of the flying capacitor voltage has been demonstrated as high as 800 Hz [29] and 2.7 kHz [70]. Fig. 11 shows the

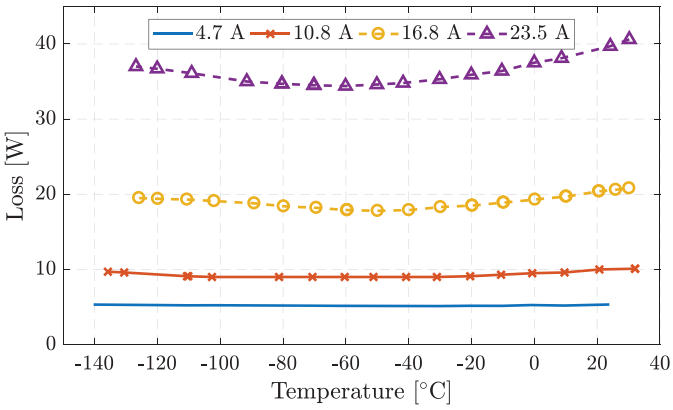

Fig. 12. Converter losses at four different loads. At higher load, conduction losses dominate and there is a measurable decrease in losses down to −60 °C.

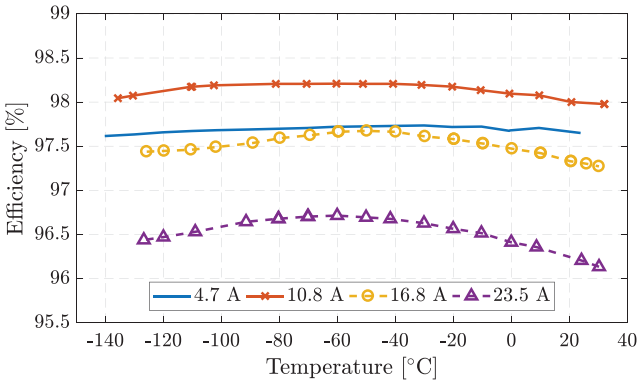

Fig. 13. Measured efficiency versus temperature for four different load levels. At light load, the converter losses are denominated by switching and therefore efficiency changes little with temperature.

three-level switching node voltage and output current for normal operation of the three-level converter.

Operating between 150 V_{dc} and 45 V_{RMS}, the converter was tested at four different load currents from light to rated load and operated successfully with a cold plate heat sink temperature between ambient and −140 °C. The finite cooling capability of the cold plate and Instec LN2 pump limited the lowest temperature achievable as the converter load and losses increased. For this reason, the light-load temperature sweep with 5 W of loss is cooled ≈10 °C further than the full load case with 40 W of loss as shown in the plot of total converter loss in Fig. 12 and overall efficiency in Fig. 13.

The data in Figs. 12 and 13 were taken for a fixed load over a temperature sweep. Taking data over a temperature sweep ensured that the system was in thermal equilibrium throughout the test and minimized thermal stress which would be accentuated during a step in converter output power due to the FET temperature quickly increasing without coming to thermal equilibrium with the PCB.

V. Power-Loss Analysis

The overall electrical losses in Fig. 12 were measured using a pair of Yokogawa WT310 meters. These losses correspond directly to the converter efficiency plotted in Fig. 13 and are plotted as a function of temperature for each load current tested. At the low power level of 4.7 A, the loss of the converter is largely consistent over the temperature range tested. At this low current, the temperature-dependent ohmic losses are minimal. Instead, the losses are dominated by energy dissipated from the FET drain–source parasitic capacitance each switching cycle, and remain largely constant with temperature. As mentioned in Section II-A, the switching speed of the EPC2034 devices has been shown to stay relatively constant over temperature. As a result, the FET overlap switching losses did not change significantly; but unlike the switching losses caused by parasitic capacitance, the overlap losses are proportional to load current and therefore have a reduced impact under light-load conditions. Other light-load sources of loss include the hysteretic losses in the inductor and capacitors, which are less dependent on temperature. Therefore, the light-load overall converter losses remain steady over the temperature range tested. A similar trend holds at the 10.8-A load as the loss curve is still roughly constant over temperature.

As the current is increased to 16.8 and 23.5 A, the ohmic losses in the converter account for a higher percentage of overall losses, so reduction in converter resistance with temperature has a larger impact on the overall converter losses. As shown in Fig. 3 and explained in Section II-A, the functional dynamic $R_{ds,ON}$ of the EPC2034 GaN FETs decreased to −80 °C and then tapered off with potentially a slight increase. In addition to the FETs, the ceramic capacitors exhibit increasing losses at low temperatures as shown in Fig. 4, and the inductor loss holds stable or slightly increases as documented in Fig. 6. In fact, only copper losses are reduced linearly by lowering temperature.

These trends, which primarily impact conduction losses, combine to cause the overall losses in the converter operating at high load to decrease over the first half of the temperature sweep until ≈ −60 °C and then increase slightly as the temperature is lowered further to −120 °C. At a cold plate temperature of −60 °C and rated 23-A load, a 16% reduction in losses was achieved compared to the room-temperature operation. This resulted in a 0.6% increase in efficiency from 96.1% to 96.7%. The highest efficiency of 98.2% was measured at −50 °C with an output load of 10.8 A or 500 W. As the converter is cooled below −60 °C, losses climb again.

In order to explore the trend in converter losses over temperature, a loss model was created taking component temperature dependencies into account. Power semiconductor loss calculations follow standard practice [71], [72], with appropriately scaled $R_{ds,ON}$ values to account for the temperature effect. A detailed description of the full loss calculations can be found in [70]. Because the losses of the switching devices are of special importance in this application, a description is included here for reference.

Referring to Fig. 1, it is clear that switch pairs A and B are forced to be complementary; therefore, the converter conduction losses for an $N-$level FCML converter are the result of the rms inductor current ($I_{L,RMS}$) flowing through the conduction resistance of $N-1$ switches, or one switch in each pair. The conduction losses ($P_{FET_{cond}}$) for the transistors can be

calculated as

$$P_{\mathrm{FET_{cond}}} = (N-1)\, R_{\mathrm{ds,ON}}(\mathrm{T_{FET}})\, I^2_{L,\mathrm{RMS}} \tag{3}$$

where the conduction resistance ($R_{\mathrm{ds,ON}}$) is a function of the temperature of the GaN FET ($\mathrm{T_{FET}}$).

The energy lost in the FET parasitic capacitance ($P_{\mathrm{FET_C}}$) is proportional to the switching frequency (f_{sw}) and roughly proportional to the output capacitance of the FET (C_{oss}). In reality, the output capacitance is nonlinear and typically plotted in the data sheet by the device manufacturer. The charge stored in the output capacitance (Q_{oss}) must be determined by an integration of the charge stored at each incremental voltage from zero to the blocking voltage (V_{ds}) at which the FET is operating [47]. For ($N-1$) complementary pairs of switches, the worst case loss can be calculated as

$$P_{\mathrm{FET_C}} = 2\,(N-1)\, Q_{\mathrm{oss}}(V_{\mathrm{ds}})\, f_{\mathrm{sw}} \approx (N-1)\, C_{\mathrm{oss}} V^2_{\mathrm{ds}} f_{\mathrm{sw}}. \tag{4}$$

As mentioned, this is the worst case condition. In operation, Q_{oss} is reduced through the discharge of the output capacitance during the dead time between switch transitions and therefore partial soft-switching occurs. This partial soft switching is accounted for in the loss assessment. The overlap losses per switch pair ($P_{\mathrm{FET_{SW}}}$) can be calculated over time (t) as

$$P_{\mathrm{FET_{SW}}} = (N-1)\, f_{\mathrm{sw}}\, (E_{\mathrm{ON}} + E_{\mathrm{OFF}}) \tag{5}$$

where the turn-ON and turn-OFF energy are calculated as

$$E_{\mathrm{ON/OFF}} = \frac{t_{\mathrm{ON/OFF}}\, V_{\mathrm{ds}}\, I_L}{2}. \tag{6}$$

The notation $t_{\mathrm{ON/OFF}}$ designates the turn-ON and turn-OFF transition periods of the switch. These times were estimated using

$$t_{\mathrm{ON/OFF}} = \frac{Q_{\mathrm{G}}}{I_{\mathrm{G_{ON/OFF}}}} \tag{7}$$

where Q_{G} is the gate charge of the GaN power FET, and $I_{\mathrm{G_{ON/OFF}}}$ are the gate turn-ON and turn-OFF currents, respectively, during the switching process, which are calculated from

$$I_{\mathrm{G_{ON}}} = \frac{V_{\mathrm{DR}} - V_{\mathrm{TH}}(\mathrm{T_{FET}})}{R_{\mathrm{ON}}} \tag{8}$$

and

$$I_{\mathrm{G_{OFF}}} = \frac{V_{\mathrm{TH}}(\mathrm{T_{FET}})}{R_{\mathrm{OFF}}} \tag{9}$$

where the term V_{DR} is the gate drive voltage, and R_{ON} and R_{OFF} are the turn-ON and turn-OFF resistances, respectively. Finally, V_{TH} is the threshold voltage, which is temperature dependent. The temperature dependence of V_{TH} was measured in [36]. The total switching interval estimated using this approach is comparable to the 10 ns switching time measured in [36] under the same gate-driving conditions.

The FET temperature was calculated based on the total power dissipated from the device ($P_{\mathrm{FET_{total}}}$), the temperature of the cold plate ($\mathrm{T_{plate}}$), and the thermal impedance of the gap filler (R_{TH}) between the FET and cold plate as

$$T_{\mathrm{FET}} = T_{\mathrm{plate}} + R_{\mathrm{TH}}\, P_{\mathrm{FET_{total}}} \tag{10}$$

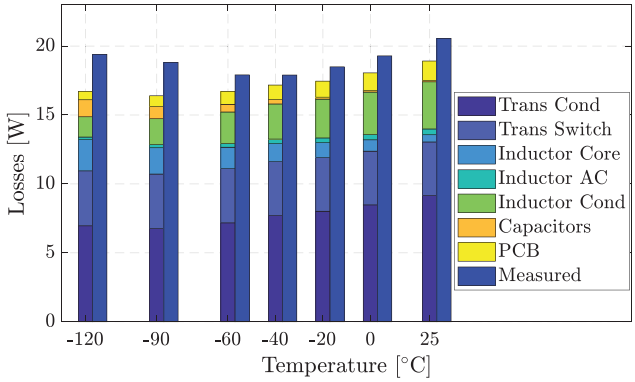

Fig. 14. Measured power losses and estimated losses versus temperature at (16.8 A_{RMS} output).

where $P_{\mathrm{FET_{total}}}$ is the summation of the losses discussed in (3)–(5) or

$$P_{\mathrm{FET_{total}}} = P_{\mathrm{FET_{cond}}} + P_{\mathrm{FET_{sw}}} + P_{\mathrm{FET_C}}. \tag{11}$$

In addition to the FET losses, losses in the capacitors, inductor, and PCB were also taken into account.

In this analysis, the total losses of the converter were calculated and averaged over a complete line cycle to determine the average loss. The bar graph in Fig. 14 shows a comparison between the measured loss at a load current of 16.8 A_{rms} and 45 V_{rms} and the calculated breakdown of loss. The trends leading the loss to fall and then stabilize are evident. In particular, the conduction losses of the inductor and PCB decrease over the temperature range tested, and the inductor core loss as well as the capacitor losses increase. Additionally, the conduction losses of the GaN FETs fall and then stabilize. Cumulatively, these trends lead to the hockey-stick trend in overall losses, although the exact replication of the trend would require additional knowledge of component properties and their internal operating temperature when the converter is operating.

Despite the smaller than expected gains in efficiency shown in Fig. 14, the concept of combined cooling and fuel in LNG powered systems still has the potential to improve system-level efficiency. If the power dissipated by each component (P_x) and the component area (A) is taken into account, the distance between the component and the LNG cooled heat sink (l_{gap}) can be adjusted to control the thermal impedance between the component and heat sink. Based on the thermal conductivity (R_θ) provided by the manufacturer for a given gap filler, the operating temperature of the device can then be calculated for a nominal converter operating point as

$$T_{\mathrm{Device}} = T_{\mathrm{sink}}(^\circ\mathrm{C}) + P_x(W) \times\ R_\theta \left(\frac{m-k}{W}\right) \times \frac{l_{\mathrm{gap}}(m)}{A(m^2)}. \tag{12}$$

By adjusting the distance between each component and the heat sink, each component could be operated at its optimal temperature for maximum efficiency while still utilizing the waste heat from the power electronics to warm the LNG from storage temperature towards the required combustion temperature, thereby improving system-level efficiency.

VI. Conclusion

This article has demonstrated the feasibility of operating a GaN-based FCML inverter at the reduced temperatures accessible in an LNG powered hybrid system. Building on prior work characterizing EPC 2034 GaN FETs, the experimental evaluation of a 1-kW single-phase inverter was completed from ambient down to $-140\,^{\circ}\mathrm{C}$ and from light to rated load. A reduction in losses was demonstrated down to $-60\,^{\circ}\mathrm{C}$, where a 16% reduction in losses compared to room temperature was observed. This trend reversed at lower temperature. An estimated power loss breakdown was also performed to provide further understanding of the components of inverter loss and opportunities for improvement in future systems.

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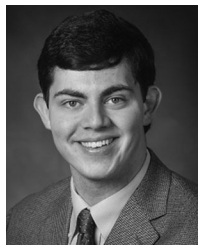
Christopher B. Barth (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Urbana, Illinois, USA, in 2012, 2014, and 2019, respectively.

He is currently an Aerospace Technologist with the NASA Glenn Research Center, Cleveland, OH, USA, working on electric power systems for space applications. His research focuses on high-density inverters for Photovoltaic and motor drive applications.

Dr. Barth is the first author of two IEEE prize papers.



Thomas Foulkes (Member, IEEE) received the B.S. degree in electrical engineering with a minor in applied mathematics from Rose-Hulman Institute of Technology, Terre Haute, IN, USA, in 2015, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Urbana, Illinois, USA, in 2017 and 2020, respectively.

As a National Science Foundation Graduate Research Fellow, his graduate research examined advanced cooling techniques, high-fidelity modeling and measurement of second-order loss mechanisms for both active and passive components, and hybrid multilevel switched-capacitor topologies in order to increase the power density and specific power of converters for electric vehicle applications.

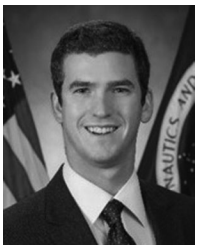
Dr. Foulkes is the author or co-author of five IEEE conference prize paper and best presentation awards. He was named one of the nine recipients globally to be a Siebel Scholar for energy science in 2020. Since graduating, he has founded a company to tackle problems related to the sustainable, secure, and reliable design of large electrical systems, such as data centers and the U.S. power grid.

Oscar Azofeifa was born in Costa Rica in 1992. He received the B.S. degree in mechatronics engineering from the Costa Rica Institute of Technology, Cartago, Costa Rica, in 2016, and the M.E. degree in energy systems from the University of Illinois Urbana–Champaign, Urbana, Illinois, USA, in 2018.

From 2018 to 2019, he was a Research Engineer with the Department of Electrical and Computer Engineering, University of Illinois. He is currently with a startup in the Boston area, where he develops controls for distributed energy resources and microgrids.

Juan Colmenares (Member, IEEE) was born in Maracaibo, Venezuela, in 1989. He received the Diploma degree in electronic engineering from the Universidad Simon Bolivar, Caracas, Venezuela, in 2012, and the Ph.D. degree in power electronics from the Department of Electrical Energy Conversion, KTH Royal Institute of Technology, Stockholm, Sweden, in 2016.

His research interests include design, implementation, and experimental evaluation of high-power high-efficiency high-temperature power electronic converters using WBG semiconductors, such as SiC and GaN, for various applications.



Keith Coulson received the B.S. degree in mechanical engineering from the Missouri University of Science and Technology, Rolla, MO, USA, in 2016, and the M.S. degree in mechanical science and engineering from the University of Illinois at Urbana–Champaign, Urbana, Illinois, USA, in 2018.

His research was focused on two-phase heat transfer and thermal management devices. He is currently an Aerospace Technologist with NASA Johnson Space Center, Houston, TX, USA, where he works in the propulsion systems branch.

Nenad Miljkovic (Member, IEEE) received the B.A.Sc. degree in mechanical engineering from the University of Waterloo, Waterloo, ON, Canada, in 2009, and the M.S. and Ph.D. degrees in mechanical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2011 and 2013, respectively.

He is currently an Assistant Professor of Mechanical Science and Engineering with the University of Illinois at Urbana–Champaign, Urbana, Illinois, USA, where he leads the Energy Transport Research Laboratory. He has courtesy appointments in Electrical and Computer Engineering and the Materials Research Laboratory. His research interests include the multidisciplinary fields of thermofluid science, interfacial phenomena, and renewable energy.

Dr. Miljkovic was the recipient of the National Science Foundation CAREER Award, the American Chemical Society Petroleum Research Fund Doctoral New Investigator Award, the Office of Naval Research Young Investigator Award, a Distinguished Visiting Fellowship from the United Kingdom Royal Academy of Engineering, a U.S. National Academy of Sciences Arab–American Frontiers Fellowship, the ASME ICNMM Young Faculty Award, the ASME Pi Tau Sigma Gold Medal, the CERL Research and Development Technical Achievement Award, and the UIUC Dean's Award for Excellence in Research.

Robert C. N. Pilawa-Podgurski (Member, IEEE) was born in Hedemora, Sweden. He received the dual B.S. degrees in physics, electrical engineering, and computer science, the M.Eng. degree in electrical engineering and computer science, and the Ph.D. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2005, 2007, and 2012, respectively.

He is currently an Associate Professor with the Electrical Engineering and Computer Sciences Department, The University of California, Berkeley, Berkeley, CA, USA. Previously, he was an Associate Professor of Electrical and Computer Engineering with the University of Illinois Urbana–Champaign, Urbana, Illinois, USA. He performs research in the area of power electronics. His research interests include renewable energy applications, electric vehicles, energy harvesting, CMOS power management, high-density and high-efficiency power converters, and advanced control of power converters.

Dr. Pilawa-Podgurski was the Student Activities Chair for IEEE Energy Conversion Congress & Exposition 2016 and 2017 conferences, and the Technical Co-Chair for the 4th IEEE Workshop on Wide Bandgap Power Devices and Applications in 2016. From 2014 to 2016, he was the Award Chair for IEEE PELS Technical Committee 6—High Performance and Emerging Technologies, where he is currently the Vice-Chair. From 2016 to 2019, he was the Chair for PELS Technical Committee 2—Power Conversion Systems and Components. From 2014 to 2019, he was an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He was the recipient of the Chorafas Award for Outstanding MIT EECS Master's thesis, the Google Faculty Research Award in 2013, and the 2014 Richard M. Bass Outstanding Young Power Electronics Engineer Award of the IEEE Power Electronics Society, given annually to one individual for outstanding contributions to the field of power electronics before the age of 35. In 2015, he received the Air Force Office of Scientific Research Young Investigator Award, the UIUC Dean's Award for Excellence in Research in 2016, the UIUC Campus Distinguished Promotion Award in 2017, and the UIUC ECE Ronald W. Pratt Faculty Outstanding Teaching Award in 2017. He was also the recipient of the IEEE Education Society Mac E. Van Valkenburg Award for outstanding contributions to teaching unusually early in his career in 2018. He is a co-author of ten IEEE prize papers.