Derivation of Single-Input Dual-Output Converters With Simple Control and No Cross Regulation

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***Abstract*—The design of power converter circuits is highly dependent on the types of the input and output terminations. Conventional dc–dc converters assume the input termination being a voltage source, and the converter circuits so developed are voltage-source-mode (VSM) converters which generally consist in switching an inductor between the input and the output with two complementary switches. However, when dealing with an input current source, the counterpart current-source-mode (CSM) converters are much less known. This article derives all single-input dual-output (SIDO) converters that inherently achieves no cross regulation using both VSM and CSM buck and boost converters, and provides a detailed comparison of the different SIDO configurations in terms of step-up and step-down functions, connection type, number of ground-referenced drivers, number of inductors, number of capacitors, voltage stress, and current stress. The control requirements for independent regulation of the two outputs are discussed. For illustration purposes, one specific CSM SIDO converter is presented and its detailed operation and design considerations are discussed. Finally, experimental results are presented to verify the analytical findings.**

***Index Terms*—Cross regulation, current-source-mode (CSM) converter, dc–dc converter, simple control, single-input dual-output (SIDO) converter.**

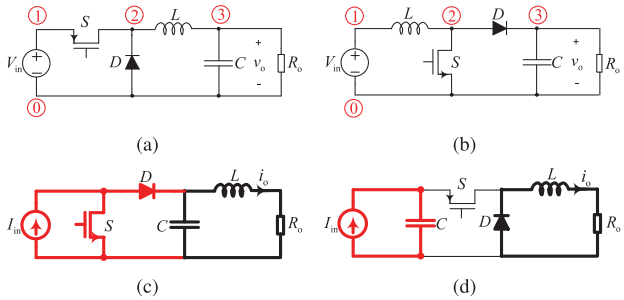

Fig. 1. VSM and CSM topologies. (a) VSM buck converter. (b) VSM boost converter. (c) CSM buck converter. (d) CSM boost converter.

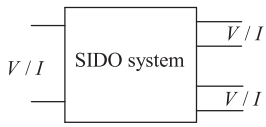

Fig. 2. Block diagram for SIDO converter.

I. Introduction

THE design of power converter circuits is highly dependent on the types of the input source and output load. Conventional dc–dc power converters assume the input being terminated by a voltage source while the output can be a regulated voltage or current subject to the appropriate use of control method. They operate by connecting a cyclically switched inductor to the input, as shown in Fig. 1(a) and (b). These well known dc–dc converters are herein referred to as *voltage-source-mode* (VSM) converters to clearly distinguish their input termination being voltage source. Moreover, when the input is a current source, circuit theory provides a tool to derive dual converter circuits that operate by connecting a cyclically switched capacitor to the input, as shown in Fig. 1(c) and (d). However, these dual versions of converters, therein called *current-source-mode* (CSM) converters, are rarely known and analyzed, let alone used in practical power conversion. The CSM converters work in exact dual fashion as their VSM counterparts by swapping voltage and current, capacitor and inductor, open and closed switches, resistance, and conductance [1], [2].

As shown in Fig. 1(a) and (b), the basic VSM switching cell consists of a switch, a diode, and an inductor. The output capacitor serves a filtering function, in contrast to the inductor in the switching cell which is the high-frequency switching storage component. Likewise, in the dual fashion [1]–[4], the CSM switching cell, as exemplified in Fig. 1(c) and (d), consists of a switch, a diode, and a capacitor. In Fig. 1, the corresponding nodes of the VSM converters and branches in the CSM converters involved in the switching operation are drawn in red for illustration. Here, the capacitor is the high-frequency switching storage component, whereas the inductor serves a filtering function [5], [6].

Single-input dual-output (SIDO) converters, as shown in Fig. 2, are popular power conversion modules serving

Manuscript received August 14, 2019; revised November 14, 2019 and January 29, 2020; accepted March 15, 2020. Date of publication March 31, 2020; date of current version July 20, 2020. This work was supported by Hong Kong Research Grants Council under Grant GRF15209617E. Recommended for publication by Associate Editor G. Moschopoulos. *(Corresponding author: Xiaolu Lucia Li.)*

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Digital Object Identifier 10.1109/TPEL.2020.2983618

applications that require two independently regulated outputs powered from a common power source, with minimum or no cross regulation. As mentioned above, conventional VSM converters have dominated the design of SIDO converters as voltage source is the common form of power [7]–[9]. However, with the emergence of new energy sources, power sources in the form of current sources are possible. This thus calls for the use of CSM converters from the circuit theoretic point of view. Also, until now, there is no systematic method for deriving SIDO converter circuits. In this article, we present a systematic derivation of SIDO converters, including both voltage and current sources as input power source. In the derivation of SIDO converters, we put equal emphasis on the use of VSM and CSM converters, addressing applications where the input is a voltage source and a current source, respectively. In addition, we emphasize the appropriate connection style that inherently leads to zero cross regulation, thus drastically simplifying the control problem. We will present systematic derivation of all SIDO topologies based on buck and boost topologies, first for applications where the input is a voltage source (using VSM converters), and then for applications where the input is a current source (using CSM converters). For each case, there are five fundamental types of SIDO converters based on the buck and boost topologies. Due to specific grounding (and floating) constraints, there are 9 VSM SIDO dc–dc converters and 12 CSM SIDO dc–dc converters. The corresponding circuit synthesis procedures for VSM and CSM SIDO dc–dc converters are presented. To achieve complete decoupling of the two outputs (i.e., no cross regulation), for the VSM version, we calculate the voltage difference between any two nodes, and find pairs of nodes with voltage difference being equal to the input voltage, hence guaranteeing no cross regulation. Using parallel connection, all VSM SIDO converters are derived. Likewise, for the CSM version, we calculate each branch current, and find the branches with current being equal to the input current. Using series connection, all CSM SIDO converters can be found. Application of duality clearly establish the relationship of VSM and CSM versions as exact circuit duals.

The rest of this article is organized as follows. Five basic types of SIDO configurations are presented in Section II. When using VSM buck and boost converters, the five types can be further developed into 9 VSM SIDO dc–dc converters. Moreover, when the CSM buck and boost converters are used, the five types can be developed into 12 CSM SIDO dc–dc converters. In Section III, we focus on the 12 CSM SIDO dc–dc converters and consider their control. A comparison in terms of step-up and step-down functions, connection type, number of ground-referenced drivers, number of inductors, number of capacitors, voltage stress, and current stress is presented. One specific type of CSM SIDO dc–dc converter is taken as an example for illustration. Guidelines for the extension from SIDO dc–dc converters to single-input multiple-output (SIMO) dc–dc converters are provided. In Section IV, practical configurations of specific CSM SIDO dc–dc converter are given, and experimental results are provided for verification purposes. Finally, Section V concludes this article.

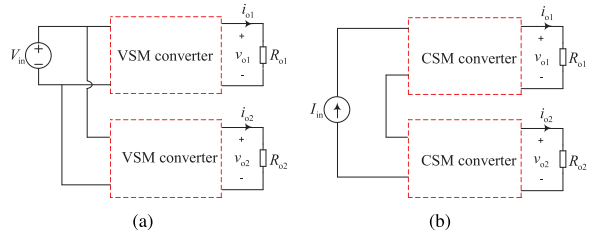


Fig. 3. Single-input dual-output converter configurations with inherently no cross regulation. (a) Parallel-connected converters for input being a voltage source. (b) Series-connected converters for input being a current source.

II. Synthesis Procedure

As shown in Fig. 3(a), the decoupling requirement for the two outputs can be achieved by connecting the inputs of the two VSM converters in parallel. Thus, the independent control of the two outputs (voltage or current) can be guaranteed. Likewise, as shown in Fig. 3(b), connecting the inputs of the two CSM converters in series achieves decoupling of the two outputs, thus guaranteeing the independent control of the two outputs (voltage or current). The derivation principle of the SIDO dc–dc converters is illustrated here with the buck and boost converters taken as the basic converters.

A. Basic VSM SIDO Configurations Based on Buck and Boost Converters

For the VSM buck and boost converters, there are four nodes involved in the switching operation, as labeled in red in Fig. 1(a) and (b). We assume V_{mn} is the voltage difference from nodes m and n, i.e., $V_{mn} = V_m - V_n$. For the VSM buck converter in ON state, V_{10} and V_{20} are equal to $V_{\rm in}$. For the VSM buck converter in OFF state, V_{10} and V_{12} are equal to $V_{\rm in}$. For the VSM boost converter at ON state, V_{10} and V_{12} are equal to $V_{\rm in}$. For the VSM boost converter at OFF state, V_{10} is equal to $V_{\rm in}$.

As we mentioned in Section I, when the input is a constant voltage source, parallel connection eliminates cross regulation and simple control strategy can be deployed. Therefore, through connecting another VSM cell in parallel to the pairs of nodes with the voltage difference equal to the input voltage, no cross regulation is guaranteed. Five basic types of VSM SIDO configurations are readily constructed, as shown in Fig. 4.

B. VSM SIDO Converters and Feasibility of Topologies

For each of the five types of VSM SIDO configurations shown in Fig. 4, the second VSM converter can either be a VSM buck converter or a VSM boost converter. Moreover, there is a redundancy for Types I and IV due to symmetry. Thus, a total of 9 (not 10) VSM SIDO converter circuits can be identified, which are referred here as VSM Type I–I, VSM Type I–II, VSM Type II–I, VSM Type II–II, VSM Type III–I, VSM Type III–II, VSM Type IV–II, VSM Type V–I, and VSM Type V–II, as shown in Fig. 5. From the output terminations, each VSM converter can be controlled to deliver regulated voltage to the load via

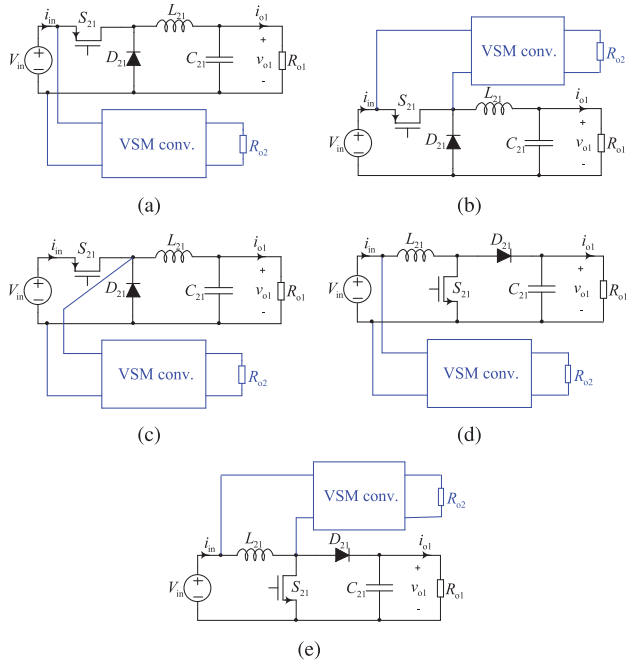


Fig. 4. Five basic types of VSM SIDO configurations based on buck and boost converters. (a) VSM Type I. (b) VSM Type II. (c) VSM Type III. (d) VSM Type IV. (e) VSM Type V.

TABLE I
VOLTAGE TRANSFER RATIOS OF FIVE FEASIBLE VSM SIDO DC–DC CONVERTERS

	Type I-I	Type I-II	Type III-I	Type III-II	Type IV-II
$\frac{V_{o1}}{V_{in}}$	D_{21}	D_{21}	D_{21}	D_{21}	$\frac{1}{1-D_{21}}$
$\frac{V_{o2}}{V_{in}}$	D_{22}	$\frac{1}{1-D_{22}}$	D_{22} *	$\frac{D_{21}}{1-D_{22}}$	$\frac{1}{1-D_{22}}$

*limited by $D_{22} < D_{21}$.

simple duty cycle control or regulated current via the standard current-programmed control.

It should be noted that practical operation of the switches may render some of the circuit configurations not feasible. Specifically, suppose that all VSM dc–dc converters operate in CCM, and we can readily check feasibility by inspection. For Type II–I VSM SIDO converter, when S_{22} is ON while D_{22} is OFF, there is no return path for inductor current of L_{22}, making this topology infeasible. Similarly, Type II–II VSM SIDO converter is infeasible. Moreover, Type V–I VSM SIDO converter is infeasible because D_{22} and the reverse diode of switch S_{22} would short inductor L_{21}. Furthermore, for Type V–II VSM SIDO converter, there is no return path for current of L_{22} when S_{21} is turned OFF, making the topology infeasible.

In summary, only five VSM SIDO dc–dc converters are operational. The voltage transfer ratios of the five VSM SIDO dc–dc converters as functions of duty cycle are summarized in Table I,

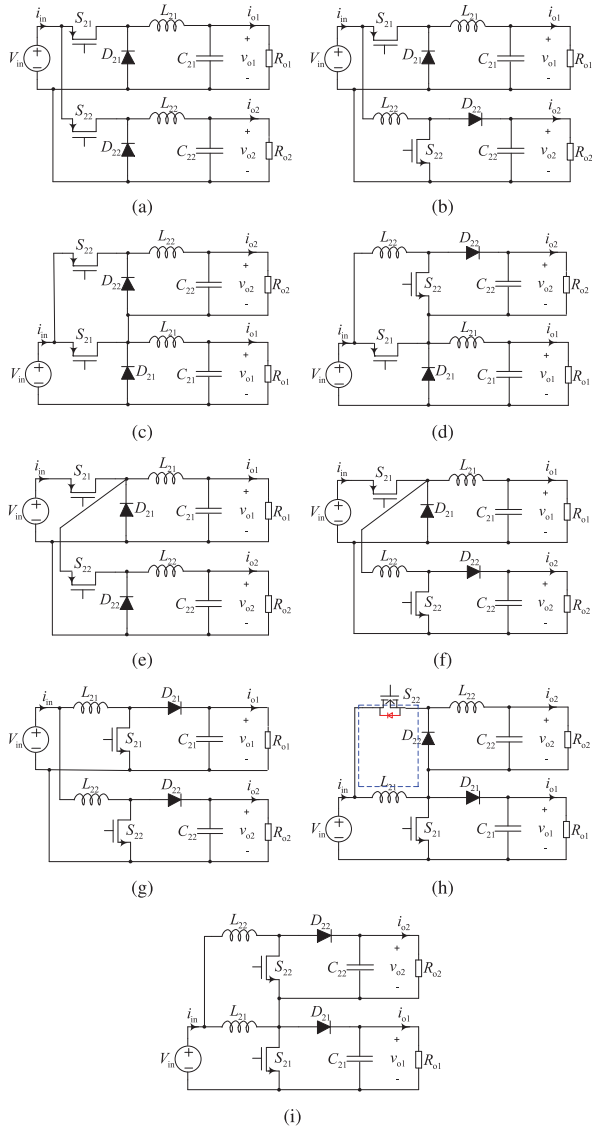


Fig. 5. Nine VSM SIDO circuit configurations based on buck and boost converters. (a) VSM Type I–I. (b) VSM Type I–II. (c) VSM Type II–I (infeasible). (d) VSM Type II–II (infeasible). (e) VSM Type III–I. (f) VSM Type III–II. (g) VSM Type IV–II. (h) VSM Type V–I (infeasible). (i) VSM Type V–II (infeasible).

where $V_{\rm in}$ is the input voltage; V_{o1} and V_{o2} are the output voltages of the first converter and the second converter, respectively; D_{21} and D_{22} are the duty cycles of the first and the second converters, respectively. As shown in Table I, the voltage transfer ratios of the five VSM SIDO dc–dc converters are independent of R_{o1} and R_{o2}. Thus, the variation of one output will not affect the other output.

C. Basic CSM SIDO Configurations Based on Buck and Boost Converters

For CSM buck and boost converters as given in Fig. 1(c) and (d), the branches having the same current as the input current when switch S is in the ON or OFF state are colored in red for ease of illustration.

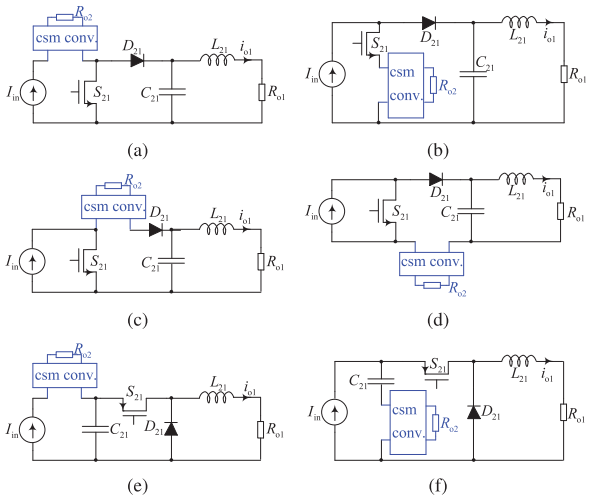


Fig. 6. Five types based on CSM converters. (a) CSM Type I (dual version of VSM Type I). (b) CSM Type II (dual version of VSM Type II). (c) CSM Type III-A (dual version of VSM Type III). (d) CSM Type III-B (dual version of VSM Type III). (e) CSM Type IV (dual version of VSM Type IV). (f) CSM Type V (dual version of VSM Type V).

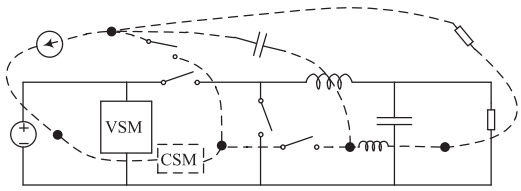


Fig. 7. Illustration of duality transformation. Solid line: VSM Type I converter [shown in Fig. 4(a)]. Dashed line: CSM Type I converter [shown in Fig. 6(a)]. Open switch is transformed to closed switch, and vice versa. Duty cycle D becomes $1 - D$ for any switch.

As we mentioned in Section I, when the input is a constant current source, the series connection can eliminate cross regulation, thus enabling the use of simple control strategy to achieve independently regulated outputs. Therefore, through connecting CSM cells in series with the branches shown by the red lines in Fig. 1(c) and (d), again, five types of CSM SIDO configurations, which are the exact duals of the VSM SIDO counterparts, can be constructed, as shown in Fig. 6. It should be noted that CSM Type III has two realizations, namely, CSM Type III-A [see Fig. 6(c)] and CSM Type III-B [see Fig. 6(c)], corresponding to two locations of the second CSM converter.

Remarks: The five types of CSM SIDO converter configurations can also be obtained through direct application of standard circuit duality transformation [1], as illustrated in Fig. 7 for Type I converters.

D. CSM SIDO Converters and Feasibility of Topologies

For each of the five types (six realizations) of CSM SIDO configurations shown in Fig. 6, the second CSM converter can either be a CSM buck converter or a CSM boost converter. Thus, a total of 12 CSM SIDO converter circuits, namely, CSM Type I–I, CSM Type I–II, CSM Type II–I, CSM Type II–II, CSM Type III-A-I, CSM Type III-A-II, CSM Type III-B-I, CSM Type III-B-II, CSM Type IV–I, CSM Type IV–II, CSM Type V–I, and CSM Type V–II, can be obtained, as shown in Fig. 8. For the output terminations, the CSM converters can be controlled to deliver regulated output current to the load by simple duty cycle control or regulated output voltage via a voltage-programmed control.

Similar to the VSM case, feasibility of the topologies should be validated assuming continuous capacitor voltage mode of operation. By inspection, for CSM Type V–II, when switch S_{21} is ON, the input current flows through the first converter. At this point, for the second converter, if switch S_{22} is ON, there is no current charging the load R_{o2}; if switch S_{22} is OFF, there is no current charging the capacitor C_{22}. Therefore, CSM Type V–II SIDO topology is infeasible.

The current transfer ratios of the 11 feasible CSM SIDO dc–dc converters as a function of duty cycle are summarized in Table II, where $I_{\rm in}$ is the input current; I_{o1} and I_{o2} are the output currents of the first and second converters, respectively; and D_{21} and D_{22} are the duty cycles of the first and second converters, respectively. As shown in Table II, the current transfer ratios of the 11 VSM SIDO dc–dc converters are independent of R_{o1} and R_{o2}, meaning that the variations of the outputs do not affect each other.

III. Analysis and Design Example

The VSM SIDO dc–dc converters have been used widely in practical applications [10]–[16]. However, the CSM SIDO converters are still relatively less known and analyzed. In this section, we focus on the CSM SIDO converters. In order to better understand the CSM SIDO converters and their characteristics, the control requirement is introduced first, followed by a comparison of the 11 feasible topologies. In particular, Type II–II CSM SIDO converter is analyzed in detail.

A. Control Requirements

For Type I–I, Type I–II, Type IV–I, and Type IV–II CSM SIDO converters, the two converters are connected in series and share the same input current source. The switching states of S_{21} and S_{22} would not affect the input current of each converter, leading to the independent control. In Fig. 9, the driving signal Q_{22} can be connected with Q'_{22} directly.

For Type II–I CSM SIDO converter, a NAND gate should be used in the control implementation, as indicated in the dashed box of Fig. 9. The reason will be presented in Section III-D.

For Type II–II CSM SIDO converter, a NOT gate should be used in the control implementation, as indicated in the dashed box of Fig. 9. The reason will be presented in Section III-D.

For Types III-A-I and III-B-I CSM SIDO converters, when switch S_{21} is OFF, switch S_{22} can operate in any state (ON or OFF state). When switch S_{21} is ON, switch S_{22} can only operate in the ON state to guarantee that the second converter does not occupy the input current source. Thus, an OR gate should be used in the control implementation, as indicated in the dashed box of Fig. 9.

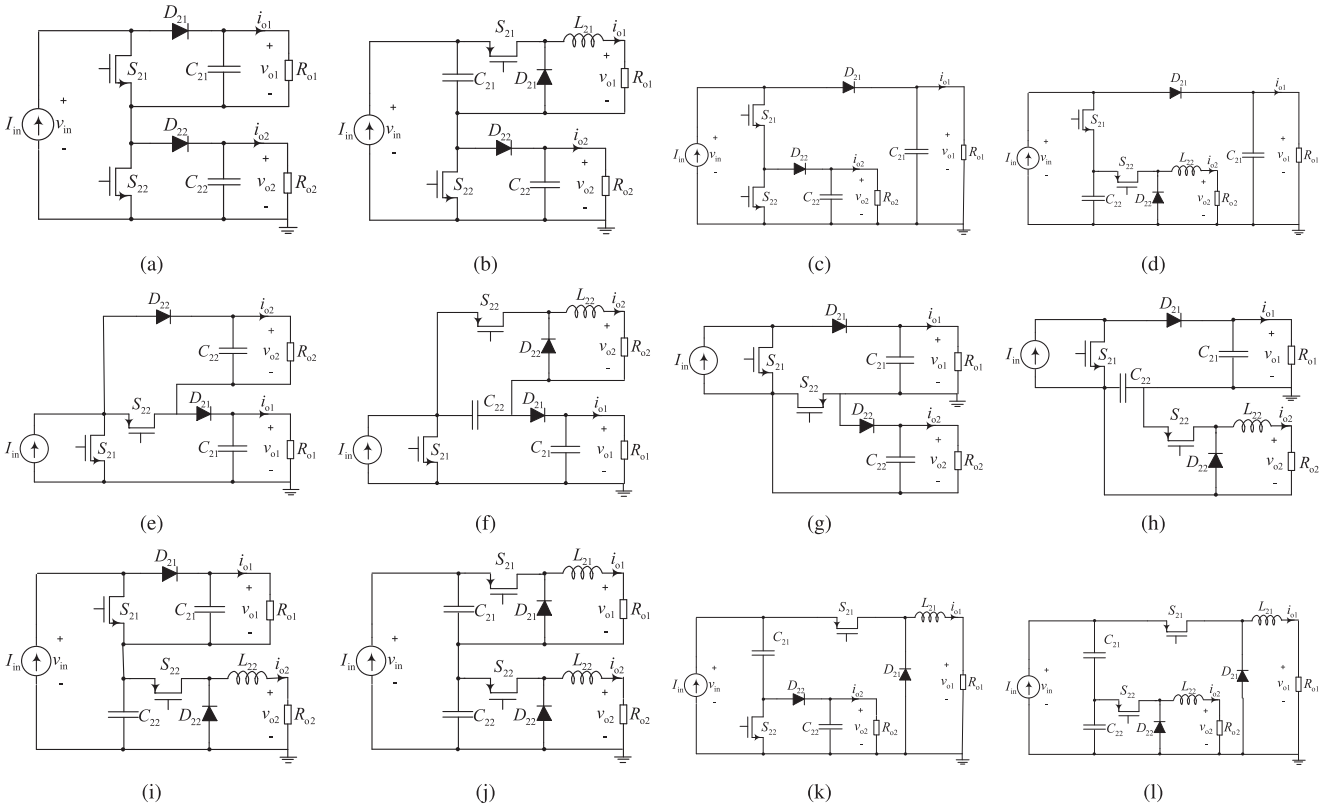


Fig. 8. Twelve CSM SIDO converter circuits based on CSM buck and boost converters. (a) CSM Type I–I. (b) CSM Type I–II. (c) CSM Type II–I. (d) CSM Type II–II. (e) CSM Type III-A-I. (f) CSM Type III-A-II. (g) CSM Type III-B-I. (h) CSM Type III-B-II. (i) CSM Type IV–I. (j) CSM Type IV–II. (k) CSM Type V–I. (l) CSM Type V–II (infeasible).

TABLE II
CURRENT TRANSFER RATIOS OF THE 11 FEASIBLE CSM SIDO DC–DC CONVERTERS SHOWN IN Fig. 8

	Type I-I	Type I-II	Type II-I	Type II-II	Type III-A-I	Type III-A-II	Type III-B-I	Type III-B-II	Type IV-I	Type IV-II	Type V-I
$\frac{I_{o1}}{I_{in}}$	$1\text{-}D_{21}$	$\frac{1}{D_{21}}$	$1\text{-}D_{21}$	$1\text{-}D_{21}$	$1\text{-}D_{21}$	$1\text{-}D_{21}$	$1\text{-}D_{21}$	$1\text{-}D_{21}$	$1\ \text{-}D_{21}$	$\frac{1}{D_{21}}$	$\frac{1}{D_{21}}$
$\frac{I_{o2}}{I_{in}}$	$1\text{-}D_{22}$	$1\text{-}D_{22}$	$1\text{-}D_{22}$ *	$\frac{D_{21}}{D_{22}}$	$1\text{-}D_{22}$ ⋆	$\frac{D_{21}}{1-D_{22}}$	$1\text{-}D_{22}$ ⋆	$\frac{D_{21}}{1-D_{22}}$	$\frac{1}{D_{22}}$	$\frac{1}{D_{22}}$	$1\text{-}D_{22}$ ⋆

*limited by $D_{22} > 1$ - D_{21}; ⋆ limited by $D_{22} > D_{21}$.

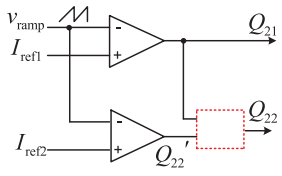


Fig. 9. Control strategy with appropriate logic gate in the dashed box.

For Types III-A-II and III-B-II CSM SIDO converters, the control logic is inverted version of that of Type II–II CSM SIDO converter. In Fig. 9, the driving signal Q_{22} can be connected with Q'_{22} directly.

For Type V–I CSM SIDO converter, when switch S_{21} is ON, the input current flows through switch S_{21}, and switch S_{22} can only operate in the ON state to guarantee that the second converter does not occupy the input current source. Thus, an OR gate should be used in the control implementation, as indicated in the dashed box of Fig. 9.

B. Comparison of CSM SIDO Converters

In comparing the different characteristics and properties of the different types of CSM SIDO converters, we focus on the current conversion, common ground connection, number of ground-referenced drivers, number of inductors, number of capacitors, voltage stress, and current stress. A summary of comparison is given in Table III.

It is worth noting that the CSM buck converter can eliminate the output inductor, while having adequate filtering function, as

TABLE III
COMPARISON OF DIFFERENT CSM SIDO CONVERTERS

	Current conversion	Common ground connection	No. of ground-referenced drivers	No. of inductors	No. of capacitors	Voltage stress	Current stress
Type I-I	Step down	No	1	0	2	$V_{S\,21}=V_{o\,1}$ $V_{S\,22}=V_{o\,2}$	$I_{S\,21}=I_{in}$ $I_{S\,22}=I_{in}$
Type I-II	Step up/down	No	1	1	3	$V_{S\,21}=V_{C\,21}$ $V_{S\,22}=V_{o\,2}$	$I_{S\,21}=I_{o\,1}$ $I_{S\,22}=I_{in}$
Type II-I	Step down	Yes	1	0	2	$V_{S\,21}=V_{o\,1}$ $V_{S\,22}=V_{o\,2}$	$I_{S\,21}=I_{in}$ $I_{S\,22}=I_{in}$
Type II-II	Step up/down	Yes	0	1	3	$V_{S\,21}=V_{o\,1}-V_{C\,22}$ $V_{S\,22}=V_{C\,22}$	$I_{S\,21}=I_{in}$ $I_{S\,22}=I_{o\,2}$
Type III-A-I	Step down	No	1	0	2	$V_{S\,21}=V_{o\,1}+V_{o\,2}$ $V_{S\,22}=V_{o\,2}$	$I_{S\,21}=I_{in}$ $I_{S\,22}=I_{in}$
Type III-A-II	Step up/down	No	1	1	3	$V_{S\,21}=V_{o\,1}+V_{C\,22}$ $V_{S\,22}=V_{C\,22}$	$I_{S\,21}=I_{in}$ $I_{S\,22}=I_{o\,2}$
Type III-B-I	Step down	No	2	0	2	$V_{S\,21}=V_{o\,1}+V_{o\,2}$ $V_{S\,22}=V_{o\,2}$	$I_{S\,21}=I_{in}$ $I_{S\,22}=I_{in}$
Type III-B-II	Step up/down	No	1	1	3	$V_{S\,21}=V_{o\,1}+V_{C\,22}$ $V_{S\,22}=V_{C\,22}$	$I_{S\,21}=I_{in}$ $I_{S\,22}=I_{o\,2}$
Type IV-I	Step up/down	No	0	1	3	$V_{S\,21}=V_{o\,1}$ $V_{S\,22}=V_{C\,22}$	$I_{S\,21}=I_{in}$ $I_{S\,22}=I_{o\,2}$
Type IV-II	Step up	No	0	2	4	$V_{S\,21}=V_{C\,21}$ $V_{S\,22}=V_{C\,22}$	$I_{S\,21}=I_{o\,1}$ $I_{S\,22}=I_{o\,2}$
Type V-I	Step up/down	Yes	1	1	3	$V_{S\,21}=V_{C\,21}+V_{C\,22}$ $V_{S\,22}=V_{C\,22}$	$I_{S\,21}=I_{o\,1}$ $I_{S\,22}=I_{in}$

analyzed in [3] and [17]. The inherent absence of inductors can reduce the number of inductors, thus reducing the volume and size of the circuit. The quantity statistics of inductors is given in Table III. Furthermore, the current ripple amplitude of the CSM boost converter is generally large. When an additional capacitor is connected at the output, the current ripple amplitude of the CSM boost converter can be reduced significantly. The quantity statistics of capacitors is given in Table III.

Based on the rated output voltages, the rated output currents, the input current, and the calculated capacitor voltage, we can easily select the type of switches.

C. Extension to Multiple-Output Converters

Using the synthesis procedure and the control logic mentioned above, it is possible to extend CSM SIDO configurations to CSM SIMO configurations. Fig. 10 shows one specific CSM SIMO configuration, which contains three CSM buck converters with the advantages of natural protection and common grounding. If one load is faulty, the current flowing through the load is still controlled to be constant, leading to the continuous increase of the capacitor voltage. When the capacitor voltage reaches the specified voltage limit, the protection circuit will set the corresponding switch to the ON state. Therefore, this converter is shorted, while other converters continue to work normally. For the control strategy, there are two restrictions for this configuration. First, when S_{21} is OFF, S_{22} and S_{23} can only operate in the ON state. Second, when S_{22} is OFF, S_{23} can only operate in the ON state.

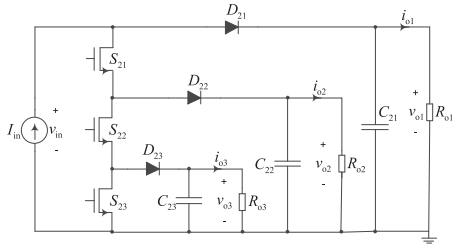


Fig. 10. CSM Single-input three-output converter.

D. Design Examples

1) Example 1. Type II–II CSM SIDO Converter: For Type II–II CSM SIDO converter with switches S_{21} and S_{22} turning ON at the same time, when D_{22} is larger than D_{21}, the capacitor is never charged throughout the switching cycle, resulting in the failure of the second output. In this article, switch S_{21} turns ON and S_{22} turns OFF at the same time. The range of duty cycle D_{22} can be widened. If (D_{21} + D_{22}) is larger than 1, the ampere-second balance of capacitor C_{22} gives

$$(1-D_{21})I_{o2}+(D_{21}+D_{22}-1)(I_{o2}-I_{\rm in})=(1-D_{22})I_{\rm in}. \quad (1)$$

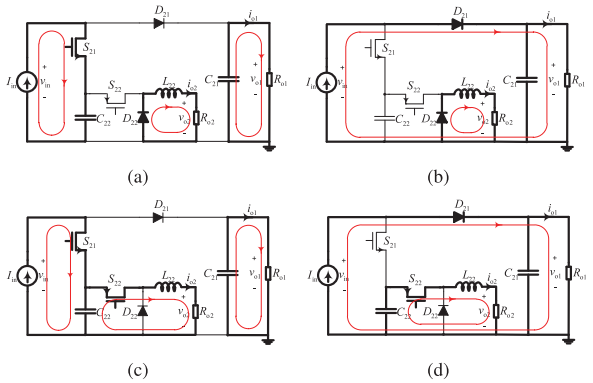


Fig. 11. Operating modes of Type II–II CSM SIDO converter. (a) S_{21} is ON and S_{22} is OFF. (b) S_{21} and S_{22} are OFF. (c) S_{21} and S_{22} are ON. (d) S_{21} is OFF and S_{22} is ON.

Upon simplification, the relationship between I_{o2} and $I_{\rm in}$ is identified as

$$I_{o2} = I_{\rm in}\frac{D_{21}}{D_{22}} = \frac{I_{\text{in-ave}}}{D_{22}} \tag{2}$$

If (D_{21}+ D_{22}) is smaller than 1, the relationship between I_{o2} and $I_{\rm in}$ is as given in (2). Thus, a NOT gate should be used in the control implementation. According to the control implementation, we can analyze the operating modes of Type II–II CSM SIDO converter.

Type II–II CSM SIDO converter contains two switches, namely, S_{21} and S_{22}. Each switch may operate in either ON or OFF state. Thus, there are four possible operating modes. Here, the two switches operate at the same frequency. The operating modes are shown in Fig. 11.

Mode 1: S_{21} is ON while S_{22} is OFF. In this mode, $I_{\rm in}$ charges up capacitor C_{22} and V_{C22} ramps up. Capacitor C_{21} and inductor L_{22} are discharged to their corresponding loads.

Mode 2: S_{21} and S_{22} are OFF. In this mode, $I_{\rm in}$ charges the load in the first converter and inductor L_{22} is discharged to the load in second converter. Capacitor voltage V_{C22} remains constant in this period.

Mode 3: S_{21} and S_{22} are ON. In this mode, $I_{\rm in}$ and capacitor C_{22} charge the load in the second converter. Capacitor C_{21} is discharged to the load in the first converter.

Mode 4: S_{21} is OFF while S_{22} is ON. In this mode, $I_{\rm in}$ charges the load in the first converter. Capacitor C_{22} is discharged to the load in the second converter.

For the first converter, the relationship between $I_{\rm in}$ and I_{o1} is given as

$$I_{o1} = (1 - D_{21})I_{\rm in}. \tag{3}$$

The output voltage of the first converter can be calculated as

$$V_{o1} = (1 - D_{21})I_{\rm in}R_{o1} \tag{4}$$

where R_{o1} is the load at the first converter output. The average input current $I_{\rm in-ave}$ of the second converter is

$$I_{\rm in-ave} = D_{21}I_{\rm in}. \tag{5}$$

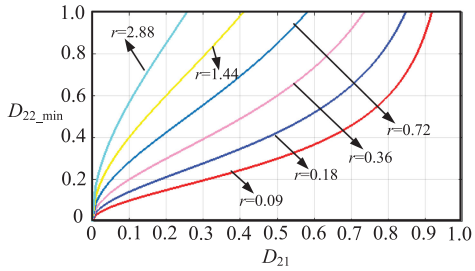


Fig. 12. Relationship between D_{21} and $D_{22-\rm min}$.

According to (2) in Section III-A, we get

$$I_{o2} = \frac{D_{21}I_{\rm in}}{D_{22}}. \tag{6}$$

The output voltage of the second converter can be calculated as

$$V_{o2} = \frac{D_{21}I_{\rm in}}{D_{22}}R_{o2} \tag{7}$$

where R_{o2} is the load at the second converter output.

For the second converter, ideally, the input power is equal to the output power. According to (6), we get

$$V_{C22} = \frac{{I_{o2}}^2 R_{o2}}{I_{\rm in-ave}} = \frac{(D_{21}I_{\rm in})^2 R_{o2}}{{D_{22}}^2 I_{\rm in}D_{21}} = \frac{D_{21}I_{\rm in}R_{o2}}{D_{22}^2}. \tag{8}$$

For the first converter, when switch S_{21} is ON, diode D_{21} is OFF. In this situation, if the capacitor voltage of C_{22} is higher than the output voltage V_{o1}, diode D_{21} will conduct, which will destroy the first converter. Thus, the capacitor voltage of C_{22} can be readily found as

$$V_{C22} < V_{o1}. \tag{9}$$

According to (4), (8), and (9), the limitation for duty cycle D_{22} is

$$D_{22} > \sqrt{\frac{D_{21}R_{o2}}{(1 - D_{21})R_{o1}}}. \tag{10}$$

We define $r = R_{o2}/R_{o1}$. With different r, the relationship between the duty cycle D_{21} and the minimum duty cycle $D_{22-\rm min}$ is plotted in Fig. 12. From (10) and Fig. 12, we see that the minimum duty cycle $D_{22-\rm min}$ is decided by D_{21}, R_{o1} and R_{o2}. In the design of circuit parameters, we should calculate the minimum duty cycle $D_{22-\rm min}$ based on the known parameters, thus controlling D_{22} within a reasonable range.

The maximum value of D_{22} is 1. Based on (10), the limitation for duty cycle D_{21} is

$$D_{21} < \frac{R_{o1}}{R_{o1} + R_{o2}}. \tag{11}$$

Fig. 13 plots the maximum duty cycle $D_{21-\rm max}$ against r, including the situations where r is smaller than 1 and r larger than 1, as given in Fig. 13(a) and (b), respectively. Taking r = 0.09 as an example, according to Fig. 13(a), the corresponding maximum duty cycle $D_{21-\rm max}$ is 0.92, which is consistent with the maximum value shown in Fig. 12.

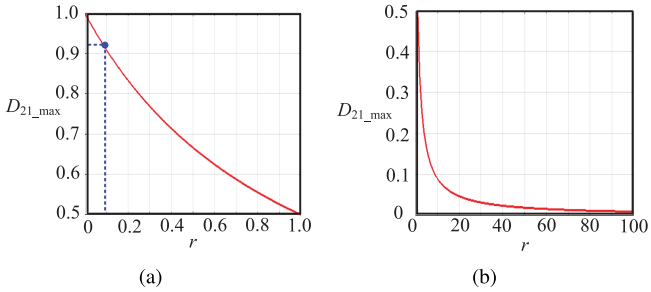


Fig. 13. Relationship between r and $D_{21-\max}$ under (a) r is smaller than 1, and (b) r is larger than 1.

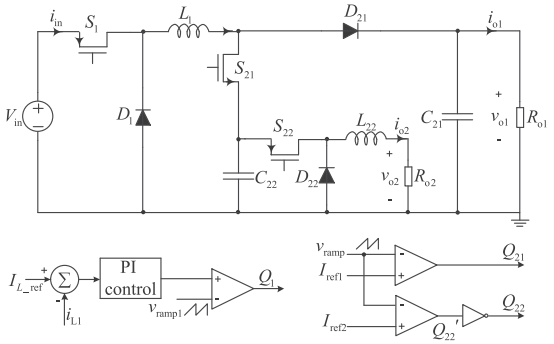


Fig. 14. Type II–II CSM SIDO converter preceded by the current source generator.

Type II–II CSM SIDO converter has following advantages: 1) It can achieve step-up and step-down functions simultaneously; 2) it can avoid cross regulation by simple control strategy; and 3) all ports are connected with a common ground.

In practice, the voltage source is a common input form. In order to deal with this situation, we add a current source generator. The function of the first stage is to produce a current source and feed the Type II–II CSM SIDO converter. A proper connection leads to the configuration shown in Fig. 14. It should be noted that an open-loop control for Type II–II CSM SIDO converter is sufficient to avoid the cross regulation issue, which means that the control circuit can be simplified greatly and the cost can be reduced.

For the practical configuration shown in Fig. 14, the input power is

$$P_{\text{in}} = V_{\text{in}} I_{L1} D_1. \tag{12}$$

According to (3), (4), (6), and (7), the output power is

$$P_{\text{out}} = \frac{{D_{21}}^2 {I_{L1}}^2}{{D_{22}}^2} R_{o2} + (1 - D_{21})^2 {I_{L1}}^2 R_{o1}. \tag{13}$$

The input power is ideally equal to the output power. Thus, we get

$$V_{\text{in}} I_{L1} D_1 = \frac{{D_{21}}^2 {I_{L1}}^2}{{D_{22}}^2} R_{o2} + (1 - D_{21})^2 {I_{L1}}^2 R_{o1}. \tag{14}$$

Regarding the practical configuration shown in Fig. 14, we can calculate the range of the load resistance based on the input voltage and the constant current value of inductor L_1.

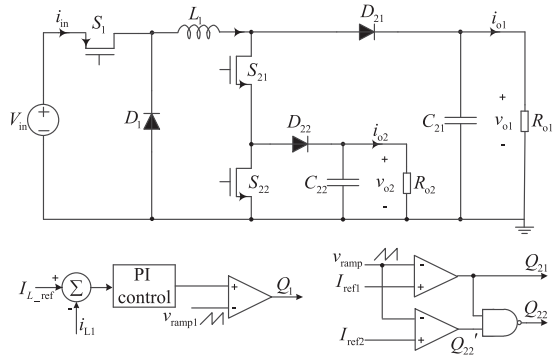


Fig. 15. Type II–I CSM SIDO converter preceded by the current source generator.

For instance, we set the parameters to the values in Table V. The input voltage is 48 V. The inductor current is 0.5 A. The duty cycles D_{21} and D_{22} are 0.5 and 0.4, respectively. When R_{o1} is 200 Ω, (14) can be simplified as

$$384 D_1 = 200 + 6.25 R_{o2}. \tag{15}$$

The maximum value of D_1 is 1. Thus, the maximum value of R_{o2} is 29.44. Equation (14) can be used to guide the parameter design of the circuit shown in Fig. 14.

2) Example 2. Type II–I CSM SIDO Converter: For Type II–I CSM SIDO converter, when switch S_{21} is ON, switch S_{22} can operate in any state (ON or OFF state). When switch S_{21} is OFF, switch S_{22} can only operate in the ON state to guarantee that the second converter does not occupy the input current source. Thus, a NAND gate should be used in the control implementation. Similar to the configuration in Fig. 14, Type II–I CSM SIDO converter employs a current generator to deal with the situation, where the input is voltage source, as shown in Fig. 15.

The converter in Fig. 15 contains only one inductor. By virtue of the constant inductor current, the second stage can employ an open-loop control. The lower magnetic component count and simple control strategy can reduce the cost significantly. Since the CSM buck converter inherently contains no inductor, it can be used in single-inductor multiple-output applications requiring minimum number of inductors.

For the practical configuration shown in Fig. 15, the input power is as given in (12). The maximum value of D_1 is 1. Thus, the maximum input power is

$$P_{\text{in}-\max} = V_{\text{in}} I_{L1}. \tag{16}$$

According to (3), the output power is

$$P_{\text{out}} = (1 - D_{21})^2 {I_{L1}}^2 R_{o1} + (1 - D_{22})^2 {I_{L1}}^2 R_{o2}. \tag{17}$$

Because (D_{21} + D_{22}) is larger than 1, the maximum output power is

$$P_{\text{out}-\max} = (1 - D_{21})^2 {I_{L1}}^2 R_{o1} + {D_{21}}^2 {I_{L1}}^2 R_{o2}. \tag{18}$$

The maximum input power should be larger than the maximum output power. Thus, we get

$$\frac{V_{\text{in}}}{I_{L1}} > (1 - D_{21})^2 R_{o1} + {D_{21}}^2 R_{o2}. \tag{19}$$

TABLE IV
COMPARISON OF DIFFERENT SIDO CONVERTERS

	Converter in Fig. 15	Converter in Fig. 14	CSM SIMO converter in [4]	Traditional SIDO converter under DCM operation [18]	Traditional SIDO converter under CCM operation [19]
Control strategy	Simple	Simple	Simple	Medium	Complicated
Controller cost	Low	Low	Low	Medium	High
No. of switches	3	3	3	3	3
No. of diodes	3	3	3	3	3
No. of capacitors	2	3	2	2	2
No. of inductors	1	2	1	1	1
No. of current sensors	1	1	1	2	2
Cross regulation	No	No	No	No	Yes
Common grounding	Yes	Yes	No	Yes	Yes
Current conversion	Step down	Step up/down	Step down	-	-

Equation (19) can be used to guide the parameter design of the circuit shown in Fig. 15.

In order to demonstrate the advantages of the converter circuits obtained, we compare the converter in Fig. 15, the converter in Fig. 14, the CSM SIDO converter presented in [4], the traditional SIMO converter under DCM operation [18] and CCM operation [19]. The differences are shown in Table IV.

In terms of the control requirement, the CSM-based SIDO converters require much simpler control circuits than the traditional SIDO converters. All converters need three switches and three diodes. Compared with other SIDO converters, the converter in Fig. 14 needs an extra capacitor and an extra inductor for performing the filtering function. Moreover, the CSM-based SIDO converters employ only one current sensor for producing a constant intermediate current, whereas traditional SIDO converters [18], [19] require two current sensors for regulating two output currents, resulting in increased power loss and cost. In terms of cross regulation performance, the CSM-based SIDO converters can alleviate cross regulation altogether. Furthermore, in terms of connection type, the two outputs of the CSM SIDO converter presented in [4] are connected in series, which limits its application. Finally, the converter in Fig. 14 can step up and down the current simultaneously.

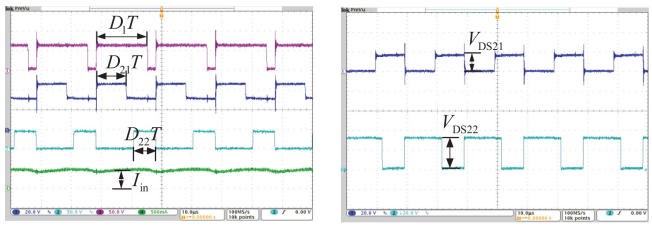
IV. EXPERIMENTAL RESULTS

A prototype of Type II–II CSM SIDO converter mentioned in Section III-D has been built for verifying the analytical results presented earlier. Parameters and components of our prototype are given in Table V.

Fig. 16(a) shows the driving waveforms and the input current waveform. The input current source is 500 mA. D_{21} and D_{22} represent the driving signals of switches S_{21} and S_{22}, respectively. According to Fig. 16(a), when switch S_{21} turns ON, switch S_{22} turns OFF, which agree well with the control logic shown in Fig. 9. In one period, we identify three subintervals. In the first subinterval, S_{21} is ON and S_{22} is OFF, and the input current source charges capacitor C_{22}. In the second subinterval, S_{21} and S_{22} are OFF, the capacitor voltage V_{C22} remains unchanged in this subinterval. In the third subinterval, S_{21} is OFF and S_{22} is ON. Capacitor C_{22} is discharged to the load in the second converter.

TABLE V
PARAMETERS OF TYPE II–II CSM SIDO DC–DC CONVERTER

Circuit Parameters	Value
Rated input current	500 mA
Inductor L_{22}	500 µH
Capacitor C_{21}	47 µF
Capacitor C_{22}	100 µF
Output currents I_{o1}	250 mA
Output currents I_{o2}	630 mA
Switch frequency of S_{21} and S_{22}	50 kHz
Load R_{o1}	200 Ω
Load R_{o2}	18 Ω
r	0.09
Switch frequency of S_{21} and S_{22}	50 kHz
MOSFETs S_{21} and S_{22}	IRF540NPBF
Diodes D_{2a} and D_{2b}	MBR20150CT



(a) (b)

Fig. 16. Experimental waveforms of (a) two driving signals and the input current; (b) voltage stress.

From Table III, the theoretical voltage stress of S_{21} is $(V_{o1} - V_{C22})$, and the theoretical voltage stress of S_{22} is V_{C22}. From (4), (8) and the parameters in Table V, the theoretical values of V_{DS21} and V_{DS22} are 21.9 and 28.1 V, respectively. Fig. 16(b) shows the voltage stress of switches S_{21} and S_{22}. The measured V_{DS21} and V_{DS22} are 19 and 30 V, respectively, which are generally in line with the theoretical results.

Fig. 17(a) presents the experimental waveforms of the input current and the two duty cycles. In this case, I_{in} is equal to 500 mA, and duty cycles D_{21} and D_{22} are set to 0.5 and 0.4, respectively. Fig. 17(b) presents the experimental waveforms of the two output currents. The measured output currents I_{o1} and

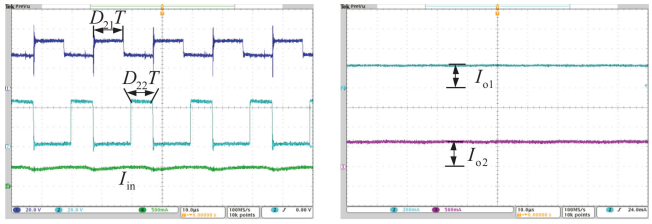


Fig. 17. Experimental waveforms of simultaneous step-up and step-down functions. (a) Input current and duty cycles. (b) Output currents.

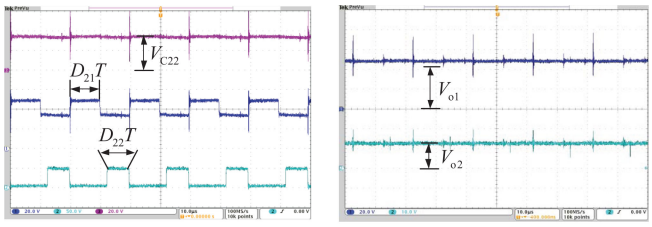


Fig. 18. Experimental waveforms of voltages V_{o1}, V_{o2} and V_{C22}. (a) V_{C22} and duty cycles. (b) Two output voltages.

I_{o2} are 250 and 630 mA, respectively, indicating the simultaneous step-up and step-down functions. The results are in perfect agreement with theoretical output currents calculated from (3) and (6). The advantage of Type II–II CSM SIDO converter is that it can achieve step-up and step-down functions with common ground connection.

Fig. 18(a) shows the experimental waveforms of capacitor voltage V_{C22} and the two duty cycles. The measured capacitor voltage V_{C22} is 30 V, and duty cycles D_{21} and D_{22} are set to 0.5 and 0.4, respectively. From (8), the theoretical voltage V_{C22} is 28.1 V. Notable error in V_{C22} can be found in Type II–II CSM SIDO converter due to the forward voltage drop of the diodes and the measurement error in the duty cycles. Fig. 18(b) presents the experimental waveforms of the two output voltages. The measured output voltages V_{o1} and V_{o2} are 52 and 12 V, respectively. According to (4) and (7), the theoretical voltage V_{o1} and V_{o2} are 50 and 11.3 V, respectively, which basically agree with the measured results. As shown in Fig. 18, V_{C22} is smaller than V_{o1}. The design consideration between V_{C22} and V_{o1}, as given in (9), is verified.

Fig. 19 shows the transient response when load R_{o2} steps between 18 Ω and 12 Ω. Details are shown in Fig. 19(b) and (c). The load R_{o1} is 200 Ω. According to Fig. 19, the output voltage V_{o2} steps from 12 to 7.5 V, and then return to 12 V. During the whole process, voltage V_{o1} is unaffected and maintained constant. The independent regulation can be achieved with simple duty cycle control in Type II–II CSM SIDO converter. Obviously, the configurations shown in Fig. 8 can eliminate cross regulation because of the series-connected structure and the constant current feeder. The decoupling performance of these CSM SIDO dc–dc converters is thus verified.

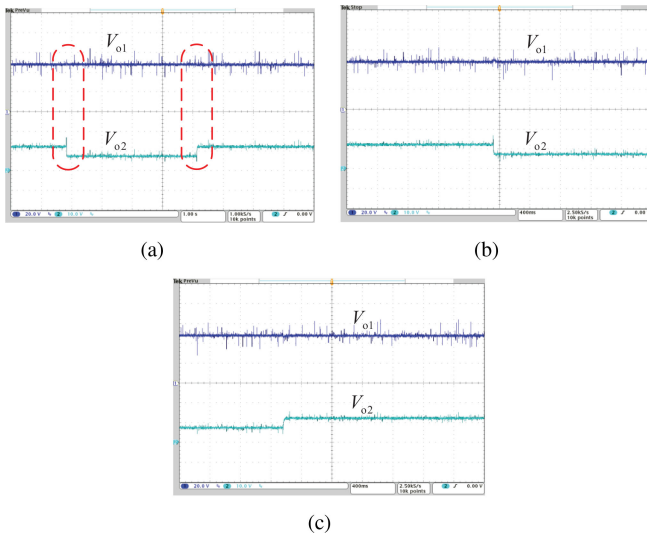


Fig. 19. Transient response showing independence of the two output voltage or cross regulation. (a) Transient response when R_{o2} steps between 18 Ω and 12 Ω. (b) 18 to 12 Ω. (c) 12 to 18 Ω. In both cases, the other voltage output is unaffected.

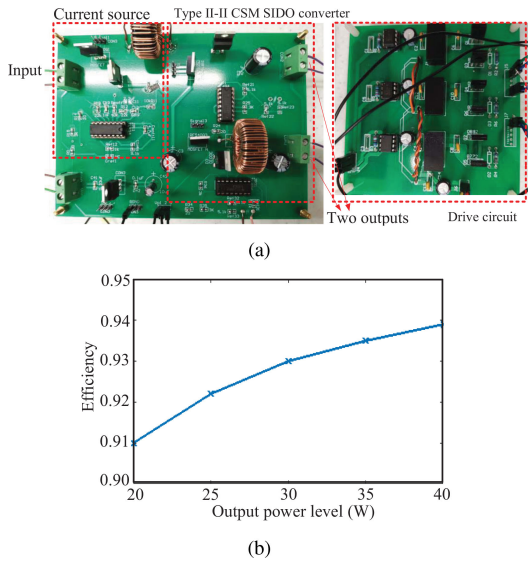
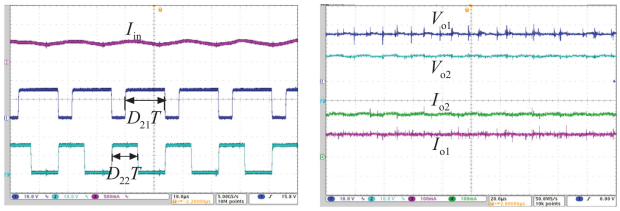


Fig. 20. (a) Prototype and (b) measured efficiency of Type II–II CSM SIDO converter.

Fig. 20(a) shows the prototype of the Type II–II CSM SIDO converter. The current source generator consists of a switch, a diode and an inductor. Fig. 20(b) shows the measured efficiency of this Type II–II CSM SIDO converter, which is not optimized for the power range of 30 W ± 33.3%.

We have also built a laboratory prototype of the converter which contains no inductor and has the advantages of simple control strategy, no cross regulation, common grounding, and natural protection. The experimental results are shown in Fig. 21. From Fig. 21(a), the input current is 500 mA, and the measured duty cycles D_{21} and D_{22} are 0.75 and 0.5, respectively. According to Table II, the two output currents should be 125 and



(a) (b)

Fig. 21. Experimental waveforms of Type II–I CSM SIDO converter. (a) Input current and duty cycles. (b) Output voltages and currents.

250 mA, which basically agree with the measured results shown in Fig. 21(b).

V. Conclusion

SIDO dc–dc converters are popular power conversion modules. Voltage source inputs have dominated the SIDO applications. However, systematic derivation of SIDO converters of all possible configurations is still not available. In addition, the potential use of current sources due to the advent of new energy sources has exposed the need for deriving current-source based SIDO converters. In particular, the CSM type of SIDO converters has apparently been completely missing from the literature. In this article, we attempt to fill this gap and present a systematic synthesis procedure for SIDO converters that achieve no cross regulation and allows the use of simple control strategy. Specifically, we have demonstrated how SIDO converters can be synthesized from basic boost and buck converters, for both VSM and CSM types. This work therefore represents a fundamental contribution to establishing SIDO converter configurations, and further to multiple-output converters.

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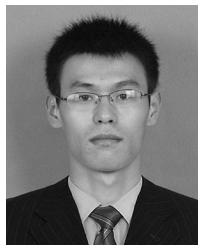

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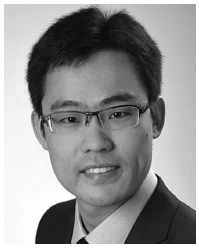

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