Analysis of Current Flowing Through Disabled Converters in Parallel AC/DC Power Conversion System

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***Abstract*—When not all the converters are enabled in a parallel ac/dc power conversion system, some current flows through the disabled converters. This current not only distorts the current waveform of the ac side but also causes extra loss and unintended power flow from the ac to the dc side. In this article, the reason for this current flow is identified, and the total current according to the number of paralleled converters and its operating conditions are analyzed. A new pulsewidth modulation (PWM) method is proposed to minimize the current. And, the zero-sequence voltage and the consequent current flowing through the disabled converters under the proposed PWM method are compared to those under the conventional PWM methods. As a result, it was identified that discontinuous space vector PWM (DPWM) is not a proper PWM method because it causes a large current at some operating conditions. According to both simulation and experimental results, the magnitude of the current flows through disabled converters under the proposed PWM was about 40% less than that under sine PWM and DPWM, and it was about 10% less than that under continuous space vector PWM.**

***Index Terms*—Circulating current, parallel three-phase converters, parallel ac/dc converters, diode conduction.**

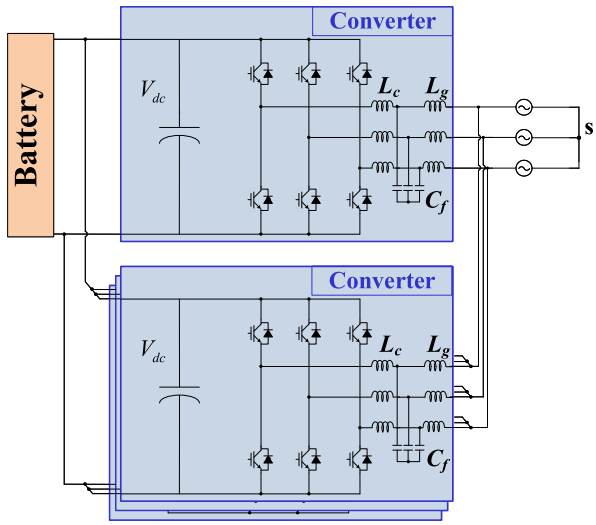

Fig. 1. Four parallel ac/dc converters sharing common dc and ac sources.

I. Introduction

An ac/dc conversion system composed of parallel-connected converters, as shown in Fig. 1, has been known to have several advantages [1]–[4]. First, the production and maintenance cost would be reduced owing to its modularity and mass production of a unit converter. Second, the efficiency at a light load would be conspicuously enhanced by deactivating some converters according to the load level. Finally, even if there are faults at some converters, the system can still be operated at a reduced power level with the remaining healthy converters.

Though a form of parallel converters sharing common dc and ac sources has the merits mentioned above, a nonnegligible amount of zero-sequence circulating current (ZSCC) inevitably flows between converters in this circuit configuration. Since the ZSCC degrades the overall efficiency and capacity of the converters, it should be minimized as much as possible.

Numerous studies have been carried out in order to suppress the ZSCC [5]–[16]. As analyzed in the literature, the reason that ZSCC flows is due to the zero-sequence voltage difference between the paralleled converters. Therefore, the ZSCC could have been controlled by adjusting the zero-sequence voltages of the paralleled converters or the corresponding switching duties. In [5], the ZSCC suppression method was proposed, in which, the zero-sequence voltage commands of slave converters follow the zero-sequence voltage of the master converter by utilizing communication. However, since the open-loop controller cannot perfectly suppress the ZSCC caused by communication delay and the slightly different dead time, switching characteristics, and impedance of filter between the converters, the closed-loop ZSCC controllers had been proposed. In [6], the hysteresis controller was adopted to improve the ZSCC suppression performance with discontinuous space vector PWM (DPWM). And, [7]–[13] utilized the proportional integral (PI)-type controller with various feed-forward terms and communication methods. A nonlinear control method was also utilized in [14]. Unlike the above-mentioned methods synchronizing the PWM carriers

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of the parallel converters, several studies had been conducted considering the case where the converters were interleaved to achieve multilevel output characteristics [15], [16].

However, all the conventional studies have focused on the circulating current that flows when all parallel converters are activated. But, another kind of unintended current exists as introduced in [17]. When not all converters are operating to enhance the efficiency of the system at a light load condition, the undesired current flows through the diodes of the disabled converters. This phenomenon has not been carefully addressed before. In [17], it was mentioned that the magnitude of the current converges as the number of paralleled converters increases. While, in this study, it is known that the magnitude does not converge but diverges. The reason for this discrepancy comes from the operating conditions of the converters. In [17], only the condition where one of the parallel converters is operating and others are disabled has been focused. While, in this study, a general operating condition, where *M* converters are operating and the remaining *N* converters are disabled, is considered.

Furthermore, this article proposes a new PWM method to minimize the magnitude of the undesired current. Since the ZSCC suppression methods of the conventional studies can be utilized with the proposed PWM method, the ZSCC can be also sufficiently suppressed when all converters are enabled. This article also identified DPWM as an inappropriate PWM method since it causes a significantly large current flowing through the disabled converters when the negative reactive power is flowing through the operating converters.

The remainder of this article is organized as follows. In Section II, the phenomenon that the current flows through the disabled converters is analyzed and the reason why such current flows is explained. The total current amount, according to the number of paralleled converters, is also identified in this section. In Section III, a new PWM method which minimizes the current is proposed, and the effectiveness of the proposed PWM is verified by the computer simulations. The current according to PWM methods are compared, and the reason why DPWM makes the current significantly large at some specific operating condition is also explained. In Section IV, the experimental test results are described. Finally, Section V concludes this article.

II. Circuit Analysis on Current Flowing Through Disabled AC/DC Parallel Converters

A. Reason for Current Flow Through Disabled Modules

In this section, the phenomenon that the current flows through the disabled converters in parallel ac/dc power conversion system is analyzed. First, the zero-sequence voltage of a single 2-level ac/dc converter is introduced. Then, the reason why the current flows through the disabled converters is explained with the example of a parallel converter system which consists of two converters. Finally, the total current amount flowing through *N*-disabled modules, where *M*-modules are operating among a parallel system that consists of $(M + N)$ converters, is analyzed.

1) Single AC/DC Converter: Fig. 2 illustrates a single 2-level ac/dc converter connected to the utility grid. With the assumptions of having balanced interface inductances and balanced

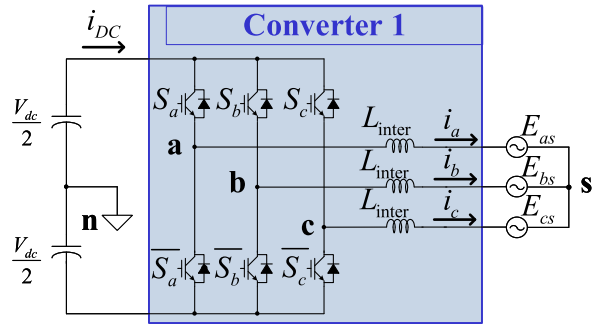

Fig. 2. Single 2-level ac/dc converter connected to the grid.

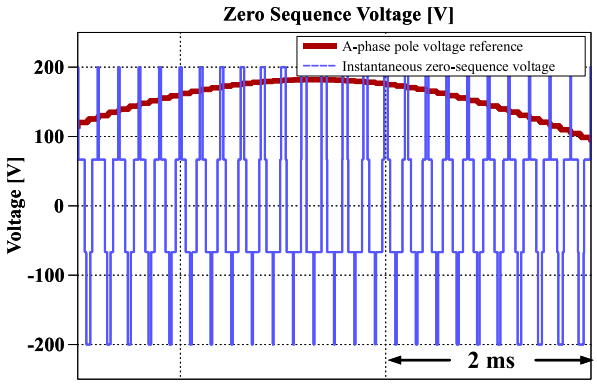

Fig. 3. Zero-sequence voltage of two-level ac/dc converter. $V_{\rm dc} = 400$ V, SPWM.

fundamental grid voltages, the pole voltages of the converter can be written as in (1) according to Kirchhoff's voltage law (KVL), and the zero-sequence voltage can be deduced as (2) by summing (1) for three phases

$$V_{xn} = E_{xs} + V_{sn} + L_{\rm inter}\frac{di_x}{dt}, \qquad \text{for } x = a, b, c \tag{1}$$

$$V_{sn} = \frac{\sum_{x=a,b,c} V_{xn}}{3} = \frac{\frac{V_{\rm dc}}{2}\sum_{x=a,b,c}(2S_x - 1)}{3} \subset \left\{-\frac{V_{\rm dc}}{2}, -\frac{V_{\rm dc}}{6}, \frac{V_{\rm dc}}{6}, \frac{V_{\rm dc}}{2}\right\} \tag{2}$$

where S_x stands for *x*-phase switching state, which is 1 when the corresponding upper switch is turned ON and 0 when the lower switch is turned ON. The sum of L_c and L_g of the *LCL* filter in Fig. 1 is simplified to $L_{\rm inter}$ in Fig. 2 for the simplicity of analysis.

According to (2), the instantaneous zero-sequence voltage of a 2-level ac/dc converter V_{sn} is always one of $V_{\rm dc}/2$, $V_{\rm dc}/6$, $-V_{\rm dc}/6$, $-V_{\rm dc}/2$. For instance, it is commonly said that the zero-sequence voltage of sinusoidal PWM (SPWM) is zero, but this is only true in the average concept for a sampling period. As depicted in Fig. 3, the zero-sequence voltage is not zero even for a moment.

2) Two Parallel AC/DC Converters: The circuit configuration of an ac/dc converter system under study is shown in Fig. 4, where two converters share the dc link and ac source together. The zero-sequence voltages of the converters, $V_{sn,1}$ and $V_{sn,2}$,

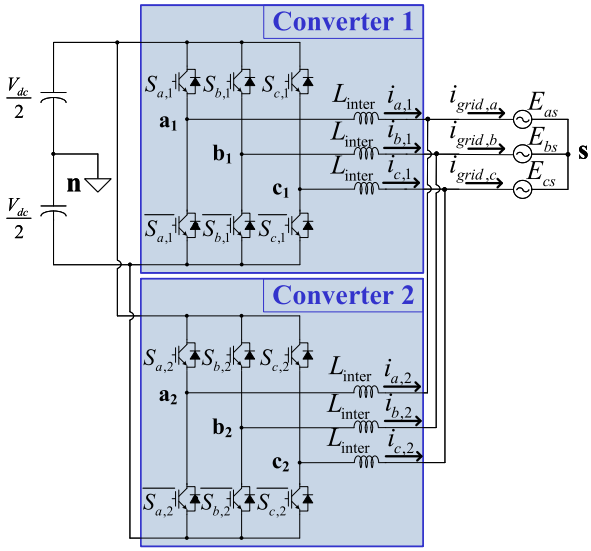

Fig. 4. Two ac/dc converters connected in parallel.

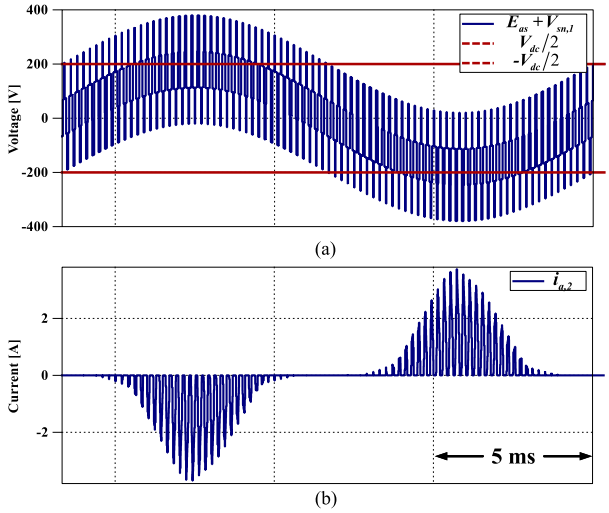

Fig. 5. Voltage and current waveform when only CONV 1 is operating. (a) Sum of E_{as} and $V_{sn,1}$. (b) $i_{a,2}$ of CONV 2. $V_{\rm dc} = 400$ V, pf $= 1$, SPWM.

can be defined as (3) in reference to (2). Equation (4) can be derived by KVL for each phase, and (5) can be deduced by summing (4) for $x = a, b, c$. Because the neutral point of the grid is isolated, there is no path for ZSCC through the grid so that '$i_{zscc,1} + i_{zscc,2} = 0$' holds according to Kirchhoff's current law (KCL). It should be noted that the variables in (3), $V_{sn,1}$ and $V_{sn,2}$, are defined for convenience of equation representation, but they are not measurable voltages between any nodes. On the other hand, the zero-sequence voltage of the parallel converter system in (4), V_{sn}, is a measurable voltage between node "s" and "n" in Fig. 4. The relation between V_{sn} and $V_{sn,1}$, $V_{sn,2}$ can be derived as (5) in the following:

$$V_{sn,1} \equiv \frac{\sum_{x=a,b,c} V_{xn,1}}{3} \quad V_{sn,2} \equiv \frac{\sum_{x=a,b,c} V_{xn,2}}{3} \tag{3}$$

$$V_{xn,1} = E_{xs} + V_{sn} + L\frac{di_{x,1}}{dt} \quad V_{xn,2} = E_{xs} + V_{sn} + L\frac{di_{x,2}}{dt}$$

$$\text{where } V_{sn} = \frac{\sum_{x=a,b,c} V_{xn,1} + \sum_{x=a,b,c} V_{xn,2}}{6} = \frac{V_{sn,1} + V_{sn,2}}{2} \tag{4}$$

$$V_{sn,1} = V_{sn} + L_{\rm inter}\frac{di_{zscc,1}}{dt} \quad V_{sn,2} = V_{sn} + L_{\rm inter}\frac{di_{zscc,2}}{dt}$$

$$\text{where } i_{zscc,k} \equiv \frac{\sum_{x=a,b,c} i_{x,k}}{3} \text{ for } k\text{th converter.} \tag{5}$$

The voltage and current waveforms of Converter 2, where Converter 1 (CONV 1) is enabled but Converter 2 (CONV 2) is disabled, are shown in Fig. 5. The reason why such current flows, that is, the conduction of the diode of the disabled converter, is very simple. It occurs because the pole voltages of CONV 2, V_{a2n}, V_{b2n}, and V_{c2n}, are outside the range of $-V_{\rm dc}/2$ to $V_{\rm dc}/2$ at some moments. Fig. 5(a) shows the sum of the A-phase grid voltage and the zero-sequence voltage of CONV 1, $E_{as} + V_{sn,1}$, which is the same as A-phase pole voltage of CONV 2 as long as

TABLE I
PARAMETERS OF SIMULATION AND EXPERIMENTS

Item		Value	Unit
$S_{rated,each}$		5	kVA
f_{sw}	DPWM	7.5	kHz
	Others	5	
L_c		1.2	mH
L_g		0.731	mH
C_f		9	μF
$V_{ll,grid}$		220	V_{rms}
$I_{rated,each}$		18.6	A_{peak}
V_{dc}		400	V

no current flows through CONV 2. As shown in Fig. 5(a), there are some moments that the A-phase pole voltage of CONV2 is outside the range of $-V_{\rm dc}/2$ to $V_{\rm dc}/2$, and the A-phase diodes of CONV 2 conduct at the same moment, as shown in Fig. 5(b). The simulation parameters for Fig. 5 are listed in Table I, and the *LCL* filter parameters in Table I are replaced by L filter, which is $L_{\rm inter}$ in Fig. 4, for simplicity of analysis. $L_{\rm inter}$ is the sum of L_c and L_g.

For quantitative analysis, the voltages applied to the interface inductors of CONV 2, to which the current is proportional, are calculated. The equations are developed in the case where the upper diode of A-phase is conducting without loss of generality. In the case, the voltage difference between $(E_{as} + V_{sn,1})$ and $V_{\rm dc}/2$ can be defined as "α" as (6), and the voltage drop at the A-phase interface inductor can be expressed as (7) in the following:

$$\alpha \equiv (E_{as} + V_{sn,1}) - V_{\rm dc}/2 \tag{6}$$

$$V_{L_a,2} = (E_{as} + V_{sn}) - V_{\rm dc}/2. \tag{7}$$

If current does not flow across CONV 2, the ZSCCs of both converters are zero, then, V_{sn}, $V_{sn,1}$, and $V_{sn,2}$ would

be identical according to (5), and the voltage of the A-phase inductor would be the same as α. However, V_{sn} and $V_{sn,1}$ are not identical because of the diode conduction of CONV 2. The pole voltages of CONV 2 can be expressed with respect to V_{sn} as (8) considering the diode conduction. If *x*-phase diodes are not conducting, then $D_{x,2}$ is 0, and (8) gives $V_{xn,2} = E_{as} + V_{sn}$. If not, then $D_{x,2}$ is 1, and $V_{xn,2}$ is $V_{\rm dc}/2$ or $-V_{\rm dc}/2$, depending on whether the *x*-phase upper diode conducts or the *x*-phase lower diode conducts

$$\begin{aligned} &V_{xn,2} = E_{xs} + V_{sn} + D_{x,2}(V_{xn,2} - E_{xs} - V_{sn}) \\ &\text{where } D_{x,2} = (\text{conduction state of CONV2 } x \\ &\qquad - \text{phase diode}) \in \{0,1\}. \end{aligned} \tag{8}$$

And, (9) can be derived by averaging (8) for three phases according to the definition of the zero-sequence voltage in (3). For instance, $D_{a,2} = 1$, $D_{b,2} = 0$, $D_{c,2} = 0$, and $m_2 = 1$ when the A-phase upper diode of CONV 2 would conduct

$$\begin{aligned} &V_{sn} = V_{sn,2} + \frac{\sum_{x=a,b,c} D_{x,2}(V_{xn,2} - E_{xs} - V_{sn,1})}{3 + m_2} \\ &\text{where } m_2 = \sum\nolimits_{x=a,b,c} D_{x,2}. \end{aligned} \tag{9}$$

From (9), the relation between V_{sn} and $V_{sn,1}$, considering the diode conduction state of CONV 2, can be derived as (10) with reference to (4)

$$\begin{aligned} &V_{sn} = V_{sn,1} - \frac{\sum_{x=a,b,c} D_{x,2}(E_{xs} + V_{sn,1} - V_{xn,2})}{3 + m_2} \\ &\text{where } m_2 = \sum\nolimits_{x=a,b,c} D_{x,2}. \end{aligned} \tag{10}$$

From the information of the conduction state of CONV 2 diodes, where only the A-phase upper diode is conducting, the voltage applied across the A-phase interface inductor of CONV 2, $V_{La,2}$, can be calculated as follows by substituting (10) into (7):

$$V_{La,2} = (E_{as} + V_{sn}) - \frac{V_{\rm dc}}{2} = \frac{3}{4}\alpha. \tag{11}$$

Equation (11) means that if the *x*-phase pole voltage of CONV 2 comes to exceed $V_{\rm dc}/2$ by α, the voltage applied to the *x*-phase inductor is three-quarters of α as the zero-sequence voltage changes according to diode conduction state. It can also be derived that the inductor voltage becomes three-quarters of α when the pole voltage of CONV 2 comes to fall below $-V_{\rm dc}/2$ by α.

3) (M + N) Parallel AC/DC Converters: To generalize the current flow through parallel converters, let us consider the situation where *M* converters are turned ON and the other *N* converters are turned OFF among (*M* + *N*) parallel ac/dc converters. The PWM carriers of paralleled converters are assumed to be synchronized, and the zero-sequence voltages of the enabled converters are assumed to be identical in the following analysis because huge ZSCCs flow between enabled converters if these conditions are not met [13]. The zero-sequence voltage of each converter $V_{sn,k}$ and the zero-sequence voltage of the parallel converter system V_{sn} can be expressed as (12). Without loss of generality, CONV 1 to CONV *M* can be assumed to be turned ON, then (13) can be derived in the same way that (10) was derived

$$\begin{aligned} &V_{sn,k} \equiv \frac{\sum_{x=a,b,c} V_{xn,k}}{3} \\ &V_{sn} = \frac{\sum_{k=1}^{(M+N)} \sum_{x=a,b,c} V_{xn,k}}{3(M+N)} = \frac{\sum_{k=1}^{(M+N)} V_{sn,k}}{(M+N)} \\ &V_{sn} = \frac{\sum_{k=1}^{M} V_{sn,k}}{M} \\ &\qquad - \frac{\sum_{k=M+1}^{M+N} \sum_{x=a,b,c} D_{x,k}(E_{xs} + V_{sn,1} - V_{xn,k})}{3M + \sum_{k=M+1}^{M+N} m_k} \end{aligned} \tag{12}$$

$$\begin{aligned} &\text{where } D_{x,k} = (\text{Conduction state of CONV } k\ x \\ &\qquad - \text{phase diode}/) \in \{0,1\} \\ &\text{and } m_k = \sum\nolimits_{x=a,b,c} D_{x,k}. \end{aligned} \tag{13}$$

Because diodes conduct passively, the diode conduction states of all disabled converters are identical. When only the A-phase upper diodes of the disabled converters conduct, the voltages applied to the A-phase interface inductors of the disabled converters can be calculated as (14) by substituting (13) into (7). Finally, the total current flowing through the diodes of *M* disabled converters among (*M* + *N*) parallel converters can be expressed as (15), which indicates the fact that the total current is proportional to 3*MN*/(3*M* + *N*)

$$\begin{aligned} &V_{La,k} = (E_{as} + V_{sn}) - \frac{V_{\rm dc}}{2} = \frac{3M}{3M+N}\alpha, \\ &\text{for } k = (M+1), \ldots, (M+N) \end{aligned} \tag{14}$$

$$I_{\rm diode,total} \propto \frac{3MN}{3M+N}\alpha \cdot \frac{T_{\rm cond}}{L_{\rm inter}} \tag{15}$$

where $T_{\rm cond}$ stands for diode conduction time. Equation (15) is verified by the computer simulation whose circuit parameters are listed in Table I. There is an exact correspondence between the total current by the simulation in Fig. 6 and that by (15) at the different number of parallel converters and its operating conditions as shown in Table II.

In the analysis of [13], it was assumed that only one of the paralleled converters is operating. Under the assumption, [13] concluded that the total current through the disabled converters converges to four times that with the two-paralleled case as the number of paralleled converters reaches infinity. However, (15) indicates the fact that the total current through the disabled converters diverges as the number of paralleled converter increases when all operating conditions are considered. Furthermore, it can be figured out from (15) that the magnitude of the current is inversely proportional to the switching frequency in that the diode current is proportional to the diode conduction time $T_{\rm cond}$. As the switching frequency of power semiconductors usually tends to be inversely proportional to its power rating, the current is more problematic as the power rating of the unit converter grows.

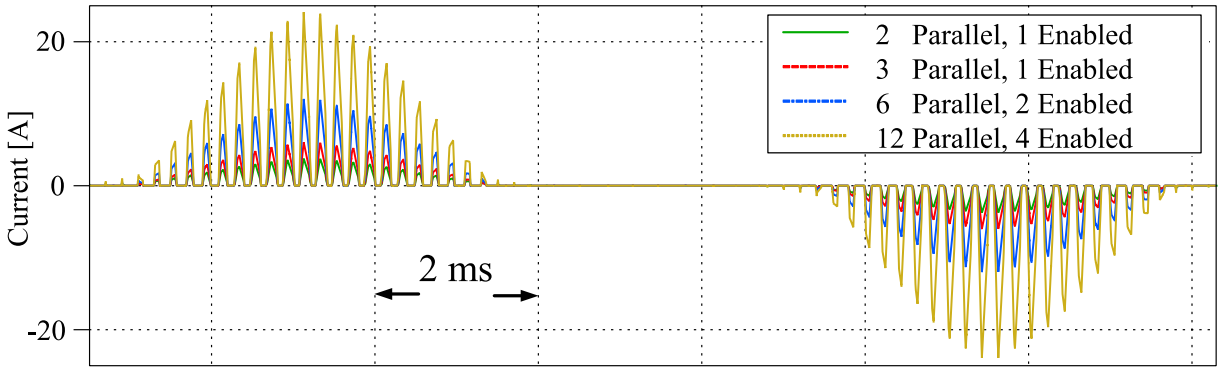

Fig. 6. Total A-phase current through disabled converters according to the number of converters and their operating conditions under SPWM.

TABLE II
TOTAL CURRENT THROUGH DISABLED CONVERTERS FROM SIMULATION AND (13) AT SEVERAL CASES UNDER SPWM

Parallel Number, (M+N)	Worst Case Combination (M,N)	Total Current by Simulation[A_{peak}]	Relative Magnitude of Total Current by Simulation (Fig. 6)	Relative Magnitude of Total Current by (15)
2	(1,1)	3.8	1	1
3	(1,2)	6.1	1.6	1.6
3	(2,1)	4.3	1.1	1.1
4	(2,2)	7.6	2.0	2.0
6	(2,4)	12.1	3.2	3.2
12	(4,8)	24.3	6.4	6.4

III. PROPOSED PWM MINIMIZING THE CURRENT

In this section, a new PWM method which minimizes the current through disabled converters is proposed. The proposed PWM minimizes the current under the following conditions. First, the proposed PWM is one of the continuous space vector PWM (CSVPWM) methods. Second, the voltage references are synthesized with the two nearest active voltage vectors and zero voltage vector so that the interface filter size can be optimized. Third, the maximum linear modulation index of the proposed PWM is the same as that of the conventional SVPWM, which is $2/\sqrt{3}$ [18].

According to the definition of "α" in (6), it can be figured out that the conduction current through diodes increases as the duration of the zero-voltage vector increases. For instance, the A-phase upper diode conducts where E_{as} is positive and the zero-voltage vector (1,1,1) is applied, and the lower one conducts where E_{as} is negative and the zero-voltage vector (0, 0, 0) is applied. Under this consideration, from (15), the maximum and minimum peak current of the disabled converter at a given switching period can be expressed as

$$i_{\max} \propto E_{\max} T_{0,+} \quad i_{\min} \propto E_{\min} T_{0,-} \tag{16}$$

where $i_{\max}$ stands for the maximum peak current of the disabled converter among three phases and $i_{\min}$ for the minimum one; $E_{\max}$ for the maximum voltage among three-phase ac voltages, $E_{\min}$ for the minimum one; $T_{0,+}$ for the time when the zero voltage vector (1,1,1) is applied, $T_{0,-}$ for the time when the zero voltage vector (0,0,0) is applied, as depicted in Fig. 7.

Considering the fact that the time for the active voltage vectors ($T_1 + T_2$) is decided by the current controller, the time for

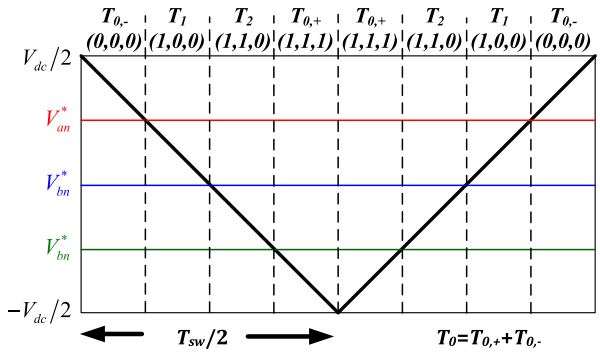

Fig. 7. Sequence of voltage vectors in carrier-based PWM.

the zero-sequence voltage ($T_{0,+} + T_{0,-}$) is not controllable but the ratio between $T_{0,+}$ and $T_{0,-}$ is controllable by determining the zero-sequence voltage of the converter V_{sn}. From (16), the relation between the zero-sequence voltage and the peak current through the disabled converter can be figured out. If the zero-sequence voltage increases under constant T_0, the increase of $T_{0,+}$ results in the larger $i_{\max}$, and the decrease of $T_{0,-}$ results in the smaller $i_{\min}$. It means that the higher zero-sequence voltage reduces the negative peak current but increases the positive peak current at the same time, and vice versa.

Finally, to balance the positive and negative current through the disabled converter, the zero-sequence voltage should be decided to satisfy (17), and the corresponding zero-sequence voltage can be calculated as (18). $V_{\max}$ in (18) stands for the maximum voltage among the phase voltage references from the current controller and $V_{\min}$ for the minimum voltage among

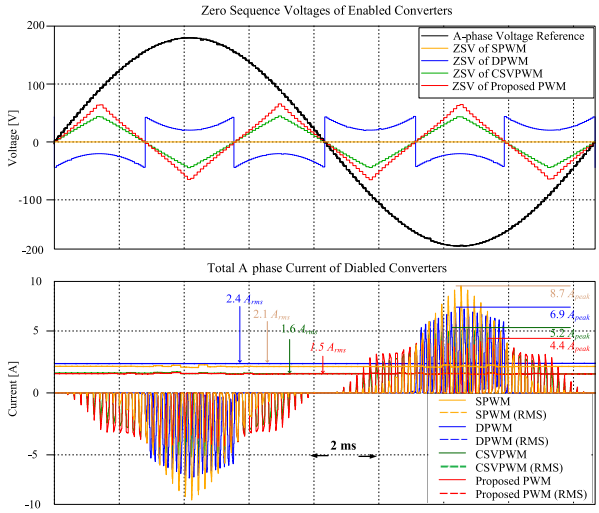

Fig. 8. Zero-sequence voltage according to PWM method. $P^* = 0$ W, $Q^* = 0$ VAR.

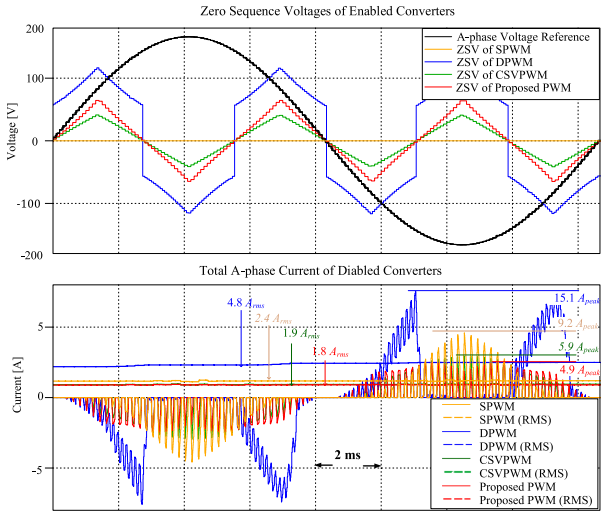

Fig. 9. Zero-sequence voltage according to PWM method. $P^* = 0$ W, $Q^* = -5$ kVAR.

them

$$E_{\max}T_{0,+} = -E_{\min}T_{0,-} \tag{17}$$

$$V_{sn} = V_{sn,\max} - (V_{sn,\max} - V_{sn,\min})\frac{E_{\max}}{E_{\max} - E_{\min}}$$

$$\text{where} \quad V_{sn,\max} = V_{\rm dc}/2 - V_{\max}, V_{sn,\min} = -V_{\rm dc}/2 - V_{\min}. \tag{18}$$

The zero-sequence voltage of the proposed PWM based on (18) for a period of the fundamental frequency is compared with those of SPWM and DPWM in Fig. 8. Fig. 8 also depicts the total A-phase current flowing through the disabled converters according to PWM methods where the number of the enabled converters M is 2, and the number of disabled converters N is 2. The circuit parameters for the simulation are listed in Table I, and the power references of the operating converters are 0 kVA. To make the effective switching frequencies identical among PWM methods, the switching frequency of the DPWM, which is widely applied to the grid-connected power conversion system, was set to 7.5 kHz while that of other methods was set to 5 kHz, as shown in Table I. The control block diagram is shown in Fig. 11.

As shown in Fig. 8, the peak current of the proposed PWM method is approximately half of those of SPWM and DPWM. Compared to CSVPWM, the zero-sequence voltage shape of the proposed method is similar to that of CSVPWM, and the rms current of the proposed method is almost the same as that of CSVPWM although the peak current of the proposed method is 15% smaller than that of CSVPWM.

Fig. 9 shows the current with a different operating point, where the power and reactive power reference of the operating converters are 0 kW and 5 kVAR each. The reason why the zero-sequence voltage shape of DPWM in Fig. 9 differs from that in Fig. 8 is that the minimum-loss DPWM (MLDPWM) is applied as a representative for DPWM [18]. As shown in the figure, the peak current flowing through the disabled converters is the minimum with the proposed PWM method. And, the rms current of the proposed method is also the minimum even though it is almost the same as that of CSVPWM.

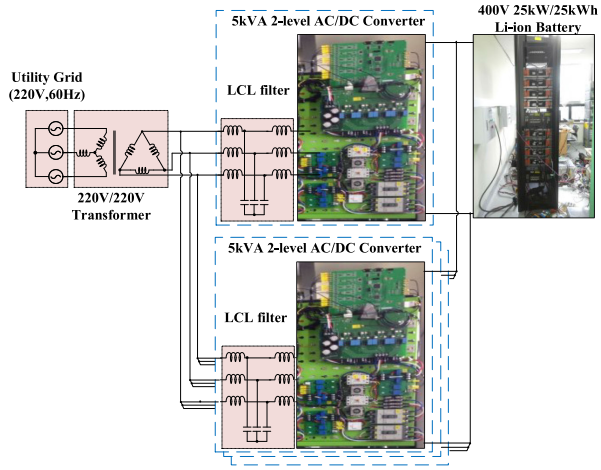

Fig. 10. Experimental setup: 5 kVA four-parallel grid-connected ac/dc converters.

The interesting thing with Fig. 9 is that the current of DPWM, which is 15.1 $A_{\rm peak}$ and 4.8 $A_{\rm rms}$, is significantly higher than those of other PWM methods. This large current, which flows regardless of the DPWM kinds when the operating converters supply negative reactive power, occurs because the volt–second balance of the interface inductors of the disabled converters is not met during a sampling period. Therefore, while the phase is not switching due to the inherent characteristic of DPWM, the current of the corresponding phase is stacked up as shown in the DPWM waveform in Fig. 9.

To be more specific, considering only A-phase upper diode conduction without loss of generality, the volt–second balance of the interface inductors breaks if the integral of $V_{La,k}$ during the switching period exceeds zero. By integrating (14), (19) can be derived under the condition the zero-sequence voltage of the

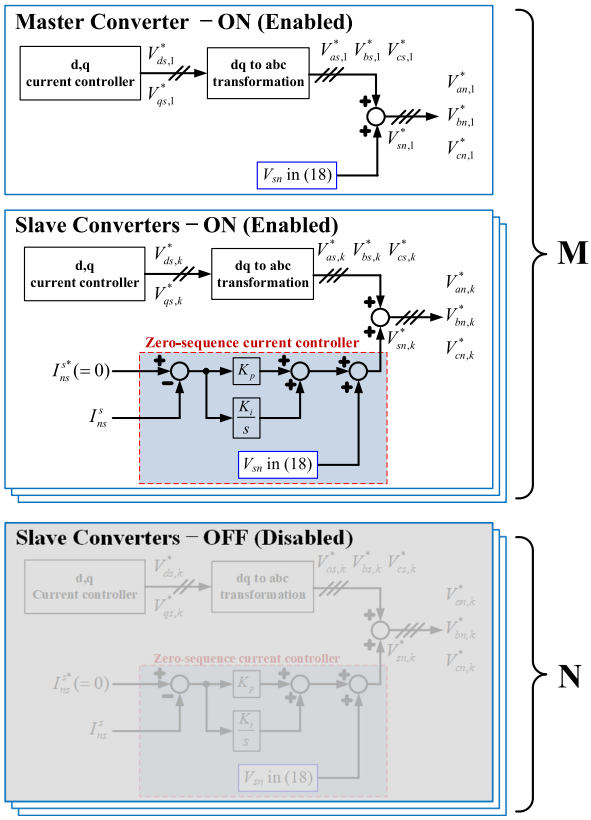

Fig. 11. Control block diagram of the paralleled converter system.

operating converter is set to the maximum, $V_{\rm dc}/2-V_{\rm max}$

$$\int_{T_{sw}} V_{La,k}dt = \int_{T_{sw}} \frac{3M}{3M+N}\{(E_{as}+V_{sn,1})-V_{\rm dc}/2\}\,dt$$
$$= \frac{3M}{3M+N}T_{sw}(E_{as}-V_{\rm max}). \quad (19)$$

Since the phase voltage reference at steady state can be written as (20) where only reactive power flows, (21) can be deduced from (19) under the condition that no active power flows

$$V^*_{xs} = (1+kL_{p.u.})E_{xs} \text{ for } x=a,b,c \quad (20)$$

where k stands for the per-unit value of reactive power and $L_{p.u.}$ for the per-unit inductance of the interface inductor. Therefore

$$\int_{T_{sw}} V_{La,k}dt = -\frac{3M}{3M+N}T_{sw}kL_{p.u.}E_{as}. \quad (21)$$

It can be figured out from (21) that the negative reactive power flow with DPWM breaks the volt–second balance and stacks up the current, as shown in Fig. 9 since the negative value of k in (21) makes the integral of $V_{La,k}$ during the switching period be positive. It should be noted that the A-phase grid voltage E_{as} is positive while the A-phase upper switch is not switching in DPWM.

IV. Experimental Results

An ac/dc power conversion system with four converters in parallel was set up, as shown in Fig. 10. Following the simulation

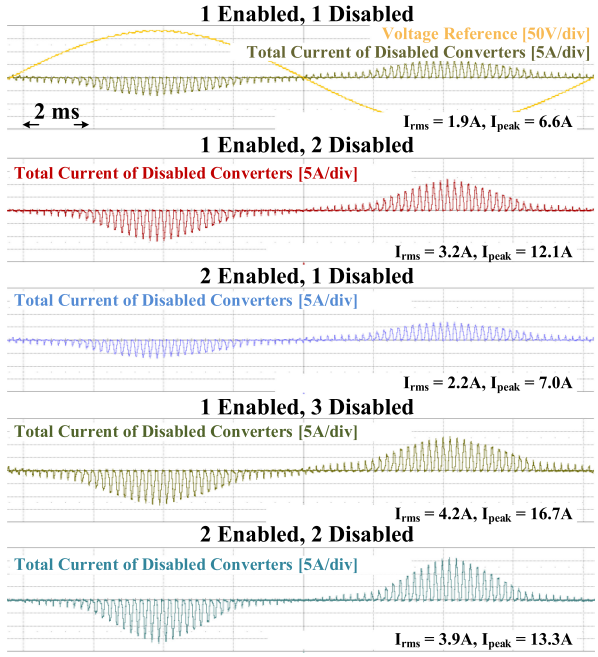

Fig. 12. A-phase total current flowing through disabled converters under SPWM. $P^*=0$ kW, $Q^*=0$ kVAR.

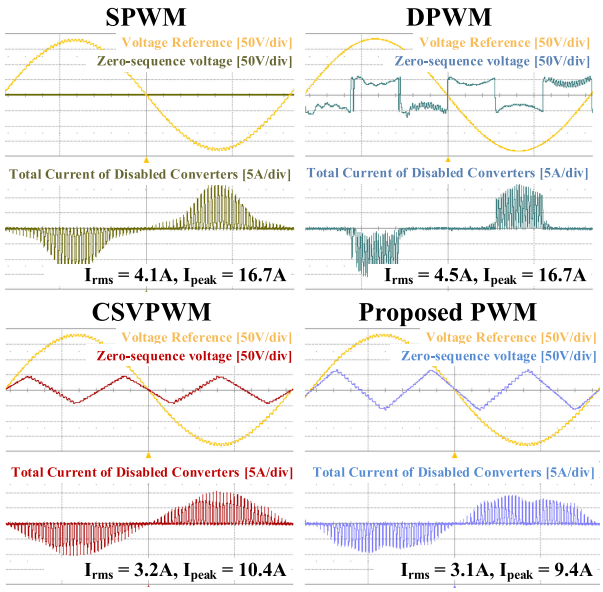

Fig. 13. A-phase total current flowing through disabled converters according to PWM methods. M = 1, N = 3, $P^*=0$ kW, $Q^*=0$ kVAR.

results shown in the previous sections, the experimental results also confirm the validity of the circuit analysis in Section II and the effectiveness of the PWM method proposed in Section III. The parameters of the experimental setup are the same as those in the simulation, whose parameters are listed in Table I, and the control block diagram of the experimental setup is depicted in Fig. 11. The zero-sequence voltages of the enabled converters are determined according to (18). And, as shown in Fig. 11, the slave converters have the additional PI controllers to suppress the ZSCC caused by the slightly different dead time, switching

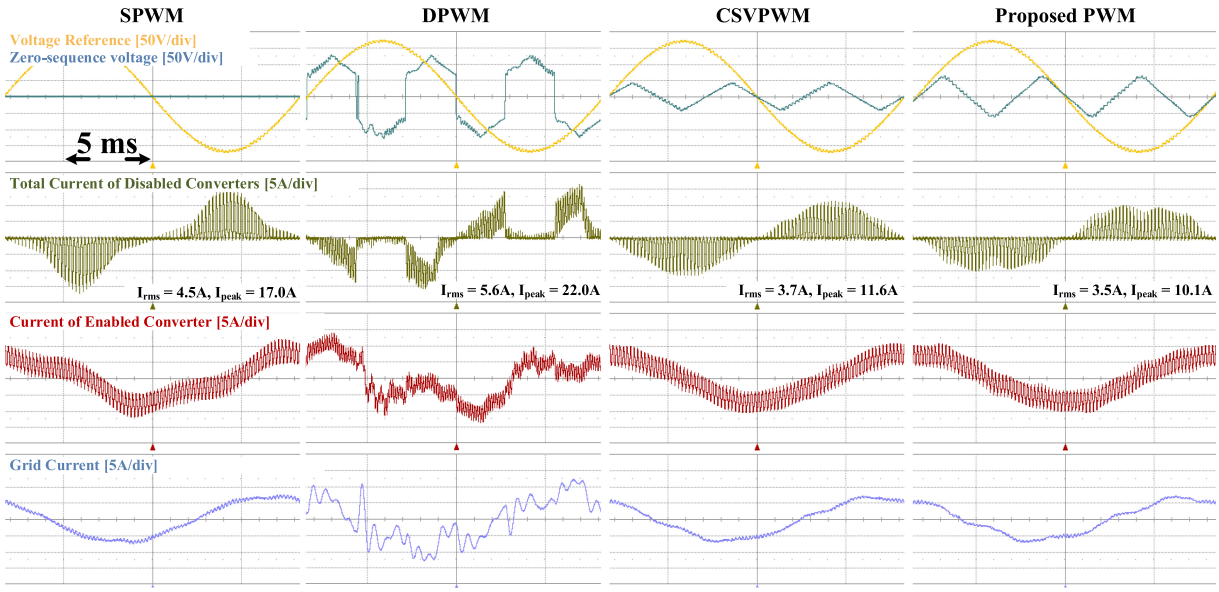

Fig. 14. A-phase total current flowing through disabled converters and converter current and grid current according to PWM methods. M = 1, N = 3, $P^* = 0$ kW, $Q^* = -2$ kVAR.

characteristics, and impedance of filter between the paralleled converters [13]. The bandwidth of the current controller is chosen as 500 Hz considering digital sampling frequency, which is 10 kHz.

Fig. 12 shows the A-phase total current flowing through the disabled converters where the number of parallel converters and its operating conditions vary. The number of paralleled converters ($M + N$) was varied from 2 to 4 by using circuit breakers, and the power reference of the enabled converters was 0 kVA and SPWM was applied in common. The waveforms in Fig. 12 show the validity of (15) and Table II, which indicated that the total current through the disabled converters is proportional to $MN/(3M + N)$. For instance, according to (15) and Table II, the current where both M and N are 2 is two times the current where both M and N are 1, and the experimental results correspond to the results from the theoretical analysis.

In Fig. 13, the effect of the PWM method on the current of disabled converters is compared where the power reference is 0 VA. The number of enabled converters and disabled converters were fixed to 1 and 3, i.e., $M = 1$, $N = 3$, and the switching frequency of DPWM was set to 7.5 kHz while both those of SPWM and the proposed PWM were set to 5 kHz to make the effective switching frequency equal for a fair comparison. As shown in Fig. 13, the total current through the disabled converters is the minimum where the proposed PWM method is engaged. In Fig. 13, the peak current with the proposed PWM, which is 9.4 A_{peak}, is 10% less than that with CSVPWM and 44% less than that with SPWM and DPWM.

Fig. 14 shows the A-phase total current of the disabled converters, the A-phase current of the enabled converter, and the grid current where reactive power reference is -2 kVAR. As the simulation results in Fig. 9, the current with DPWM, which is 5.6 A_{rms}, is significantly higher than that with other PWM methods. Furthermore, the current waveforms of the enabled converter and the grid are severely distorted with the DPWM method in this case. The reason the reactive power reference was set to -2 kVAR in Fig. 14 was that the enabled converter was tripped due to overcurrent fault with less reactive power. Therefore, DPWM cannot be even regarded as an appropriate PWM method if the parallel ac/dc power conversion system is required to have the operation mode compensating reactive power. If the phenomenon described in this article is not considered carefully, the ac/dc power conversion system with paralleled converters may not meet the grid codes regarding grid current waveform, such as IEEE Standard 519-1992 and IEC Standard 61000-3-6.

Another point that can be figured out from Fig. 14 is that the phase voltage reference and the current through the disabled converters of the fundamental frequency are in the same phase. It means that the active power from the ac side to the dc side flows through the disabled converters. Because of this power flow, even when the power reference of the operating converters is zero, the power flows from the utility grid to the dc link where the battery bank is connected in the experimental setup. This power flow should be additionally compensated by using the current information at the utility grid.

V. Conclusion

This article introduced a phenomenon related to the current flow through the disabled converters in parallel ac/dc power conversion system where each converter shares dc link and ac source. It was analyzed that the current flows because of the diode conduction of the disabled converter and the most current flows when the zero-vector voltage is applied to the operating converters. This article analytically proved the relation between the total current amount and the number of paralleled converters. According to the analysis, the total current does not converge as the number of parallel converters increases.

Also, this article proposed a new PWM method which minimizes the peak current flowing through the disabled converters, and it was confirmed with the simulation and experimental test that the proposed method reduces the peak current by 40%–60% compared with SPWM and DPWM methods and by 10%–15% compared with CSVPWM. Especially with the DPWM, the current reaches even the rated value where negative reactive power flows, and the reason for that was also analyzed. Thereby, the proposed PWM which suppresses the current steadily throughout all operating conditions would be more suitable PWM methods than DPWM method in the parallel ac/dc power conversion system. Also, since the current through the disabled converters cannot be perfectly removed even with the proposed PWM, which is theoretically the best PWM suppressing the current, the galvanic isolation of the disabled converters is highly recommended. According to the experimental results, the current deteriorates not only the current waveform of the operating converters but also the current waveform of the utility grid. Since the grid codes may not be satisfied because of this current, the phenomenon introduced in this article must be considered when the parallel converter system sharing dc link and ac source is designed.

REFERENCES

[1] J. L. Agorreta, M. Borrega, J. Lopez, and L. Marroyo, "Modeling and control of N-paralleled grid-connected inverters with *LCL* filter coupled due to grid impedance in PV plants," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 770–785, Mar. 2011.

[2] X. Wang, F. Zhuo, J. Li, L. Wang, and S. Ni, "Modeling and control of dual-stage high-power multifunctional PV system d-q-o coordinate," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1556–1570, Apr. 2013.

[3] R. Li and D. Xu, "Parallel operation of full power converters in permanent-magnet direct-drive wind power generation system," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1619–1629, Apr. 2013.

[4] F. Bovolini and H. Pinheiro, "Flexible arrangement of static converters for grid connected wind energy conversion systems," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4707–4721, Sep. 2014.

[5] T. P. Chen, "Circulating zero-sequence current control of parallel three-phase inverters," *IEE Proc. - Elect. Power Appl.*, vol. 153, no. 2, pp. 282–288, 2006.

[6] T. P. Chen, "Dual-modulator compensation technique for parallel inverters using space-vector modulation," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3004–3012, Aug. 2009.

[7] C. T. Pan and Y. H. Liao, "Modeling and coordinate control of circulating currents in parallel three-phase boost rectifiers," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 825–838, Apr. 2007.

[8] C. T. Pan and Y. H. Liao, "Modeling and coordinate control of circulating currents for parallel three-phase boost rectifiers with different load sharing," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2776–2785, Jul. 2008.

[9] S. K. Mazumder, "Continuous and discrete variable-structure controls for parallel three-phase boost rectifiers," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 340–354, Apr. 2005.

[10] Z. Ye, D. Boroyevich, J. Y. Choi, and F. C. Lee, "Control of circulating current in two parallel three-phase boost rectifiers," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 609–615, Sep. 2002.

[11] J. S. S. Prasad, R. Ghosh, and G. Narayanan, "Common-mode injection PWM for parallel converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 789–794, Feb. 2015.

[12] Z. Shao, X. Zhang, F. Wang, and R. Cao, "Modeling and elimination of zero-sequence circulating currents in parallel three-level T-type grid-connected photovoltaic inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1050–1063, Feb. 2015.

[13] Y. K. Son *et al.*, "Suppression of circulating current in parallel operation of three-level converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 2370–2375.

[14] A. Zorig, M. Belkheiri, S. Barkat, A. Rabhi, and F. Blaabjerg, "Sliding mode control and modified SVM for suppressing circulating currents in parallel-connected inverters," *Elect. Power Compon. Syst.*, vol. 46, no. 9, pp. 1059–1069, 2018.

[15] Z. Quan and Y. W. Li, "A three-level space vector modulation scheme for paralleled converters to reduce circulating current and common-mode voltage," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 703–714, Jan. 2017.

[16] A. Zorig, S. Barkat, M. Belkheiri, A. Rabhi, and F. Blaabjerg, "Novel differential current control strategy based on a modified three-level SVPWM for two parallel-connected inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1807–1818, Dec. 2017.

[17] Y. K. Son, S. J. Chee, and S. K. Sul, "Analysis on current flowing through deactivated modules in parallel connected AC/DC converters," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, 2016, pp. 761–767.

[18] D. W. Chung, J. S. Kim, and S. K. Sul, "Unified voltage modulation technique for real-time three-phase power conversion," *IEEE Trans. Ind. Appl.*, vol. 34, no. 2, pp. 374–380, Mar./Apr. 1998.

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