An Integrated Cascade Structure-Based Isolated Bidirectional DC–DC Converter for Battery Charge Equalization

Xianbin Qi, Yi Wang, *Member, IEEE*, and Mingzhu Fang

***Abstract*—In this article, an isolated bidirectional dc–dc converter with an integrated cascade structure is proposed for a centralized charge equalization system. Compared with existing architectures, the proposed converter structure is equivalent to the integration of polarity switches and a bidirectional dc–dc converter. Equalization of cells with different voltage polarities can be realized by controlling the working state of the converter, which further improves the reliability and integration of the equalization system. The integrated cascade structure can not only increase the equalization current and make it work in a continuous state but also achieve a high voltage conversion ratio to improve the efficiency of the transformer. Theoretical derivations of the converter and the conditions of soft-switch implementation are analyzed in detail. Finally, equalization experiments on a 13-cell lithium-ion battery string are carried out, and a quantitative and comprehensive comparison of different centralized equalizer is conducted. The experimental and comparison results validate the superiorities of the proposed equalizer and demonstrate obvious performance enhancement over the conventional method.**

***Index Terms*—Bidirectional dc-dc converter, integrated cascade, zero-voltage switching (ZVS), charge equalization.**

I. Introduction

TO MEET the voltage and power requirements of high-power applications, such as electric vehicles, lithium-ion battery cells are typically connected in series and in parallel to construct a battery pack. There are often performance differences among the cells in a battery pack, and these differences will be enlarged with the aging of the batteries. This will lead to a decline in the available capacity and lifetime of the batteries and even fire and explosion [1], [2]. Therefore, charge equalization technology should be adopted to realize balanced management of battery packs to ensure their efficient and safe operation.

Charge equalization technologies can be divided into passive and active methods. A passive method is to connect a resistor to each cell, but this approach has the problems of low equalization current and low efficiency. In contrast, active methods have the advantages of high efficiency and low energy consumption and can be divided into capacitor equalization, inductor equalization, transformer equalization and dc–dc converter equalization.

The switched-capacitor-based equalization technique has the advantages of high reliability and convenient control. However, the traditional scheme can only achieve balance between adjacent cells, and the equalization speed and efficiency will decrease significantly with an increase in the number of cells. In [3] and [4], an improved method based on a chain structure and double-layer switch capacitor was proposed that effectively reduces the equalization path of a battery pack and shortens the equalization time. A star-structured switched-capacitor equalization topology was proposed in [5]. Any two cells can be adjacent to each other, which improves the equalization efficiency and speed. In [6], a switching coupling capacitor equalizer was proposed that realizes global equalization of an entire battery pack without substantially increasing the hardware cost.

Equalization techniques based on inductor and transformer have high practicability; both components transmit energy between cells through inductance elements. In [7], an automatic equalizer based on a forward converter was proposed. Only one switch and one transformer winding are needed for each cell, and all switches can be controlled by one pulse width modulation (PWM) signal to realize automatic equalization of battery packs. However, to prevent saturation of the transformer core, this method needs an additional demagnetizing circuit to eliminate the magnetic bias of the transformer. Two equalization topologies based on forward and flyback conversion were presented in [8], [9] and can effectively reduce the size and cost of a circuit without additional demagnetizing circuits. The circuit proposed in [10] makes two adjacent cells share one transformer winding by buck–boost and flyback operations, thus reducing the number of windings and the circuit volume.

Charge equalization technologies based on dc–dc converters have the advantages of high equalization accuracy, high equalization current and high efficiency. According to the distribution of dc–dc converters, these equalization methods can be divided into distributed equalization [11]–[15] and centralized equalization [16]–[21]. In a distributed system, a dc–dc converter is connected to both ends of each cell. Common distributed dc–dc circuits include Cuk converters [11], buck–boost converters [12], and LC resonant converters [13]. In particular, the converter proposed in [13] realizes zero-voltage switching (ZVS) and zero-current switching (ZCS) of switches by resonant operation,

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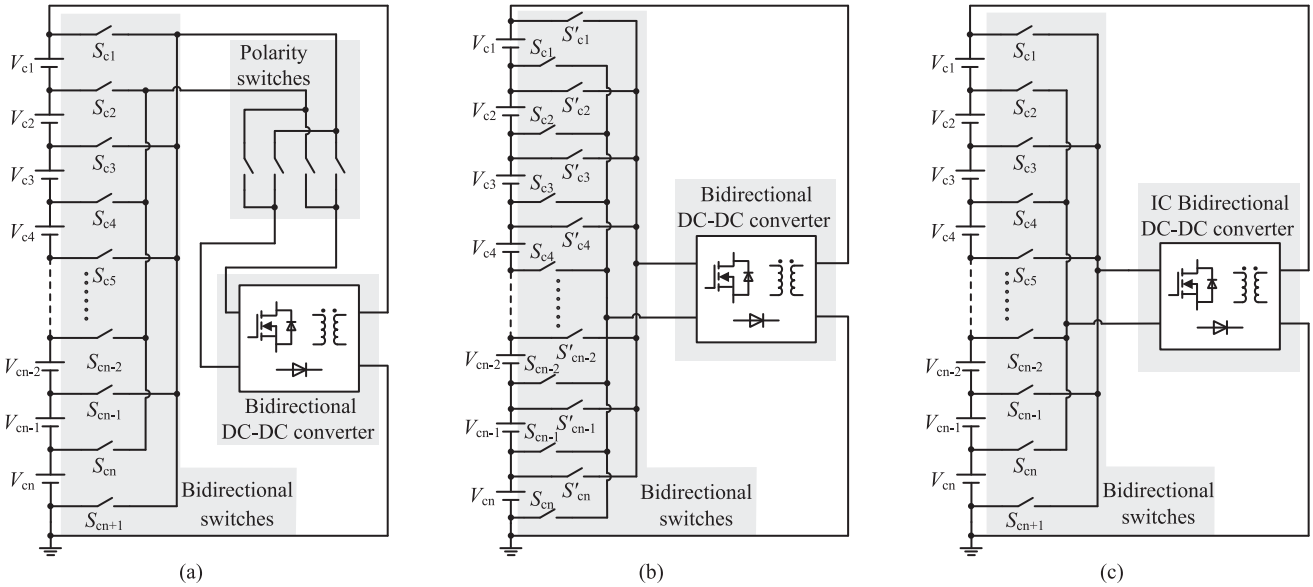

Fig. 1. Architectures of centralized charge equalization systems based on n cells. (a) and (b) Two traditional architectures. [16]–[21]. (c) Proposed architecture based on an integrated cascade (IC) bidirectional dc–dc converter.

thus reducing the switching loss of an equalization circuit. However, the complexity of the control system greatly improves the difficulty of this method. Reference [14] proposed a charge equalization circuit with a central cell structure. However, this structure has a high requirement for the reliability of the central cell. Reference [15] proposed a parallel multilayer charging equalization technology that uses multiple independent equalization circuits to achieve simultaneous equalization of different cells. According to the structure of a distributed dc–dc equalization system, each cell requires a dedicated equalizer, which increases the size and implementation cost, so this approach is not suitable for systems with a large number of cells.

Because of the small number of converters and the high reliability of the circuit, centralized charge equalization systems have developed rapidly. Compared with a distributed system, a centralized system has only one converter. The cells that need to be equalized are connected to the common converter by switch arrays. Therefore, a bidirectional dc–dc converter is a critical part of a centralized charge equalization system. In [16] and [17], bidirectional transmission of energy was realized by the anti-parallel connection of two flyback converters. An equalization system based on a bidirectional full-bridge converter was proposed in [19] and [20], but the efficiency and integration of the whole equalization system are obviously reduced by a large number of switches. In [21], a quasi-resonant bidirectional dc–dc converter was proposed that can realize soft switching by quasi-resonant operation in both boost mode and buck mode, thereby improving the conversion efficiency of the equalizer. The fly in the ointment is that to make the equalization current work in the current continuous state, an additional active filter circuit needs to be connected to prevent potential damage to the battery.

Fig. 1(a) and (b) show two traditional architectures of centralized charge equalization systems based on n cells. The switch array of the first architecture [18]–[21] consists of $N + 1$ bidirectional switches and 4 polarity switches, and the switch array of the second architecture [16], [17] contains a total of $2N$ bidirectional switches. When the number of cells in a battery string is large, fewer switches are utilized by the architecture shown in Fig. 1(a), which has certain expansion advantages. However, the bidirectional switches and polarity switches should ensure mutual coordination. If these two kinds of switches cannot be connected at the same time, the efficiency of the system will be affected to a certain extent, and there is even a risk of a short circuit between cells. The architecture shown in Fig. 1(b) does not have the problem of matching between switches and is more suitable for applications where the number of cells is small.

Fig. 1(c) shows the proposed architecture based on an integrated cascade (IC) bidirectional dc–dc converter. No additional polarity switches are needed, and cells with different voltage polarities can be equalized by controlling the operating state of the converter. The proposed converter improves the integration and reliability of a centralized equalization system and can achieve equalization with low cost and high efficiency for a long series-connected battery string. The rest of this article is organized as follows. Section II presents the operation principles of the proposed converter. Section III gives the theoretical derivations, parameters designs, and ZVS analysis. Section IV provides the experimental results. Section V compares and evaluates various converters that are employed in centralized systems. Finally, Section V concludes this article.

II. Operating Principles of the Proposed Converter

Fig. 2 shows the proposed bidirectional dc–dc converter with an integrated cascade structure in which the transformer T_r has a ratio of 1:N. V_{LV} represents the low-voltage side, which connects

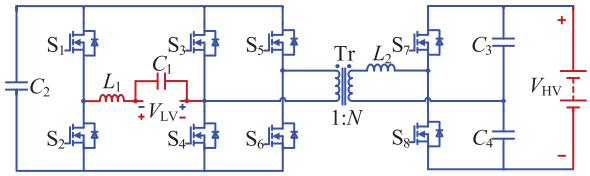

Fig. 2. Proposed integrated cascade bidirectional DC–DC converter.

the cells selected by the switch array. $V_{\rm HV}$ represents the high-voltage side, which connects the battery string.

The voltage polarities of the odd-numbered and even-numbered cells connected to the $V_{\rm LV}$ terminal are left-positive/right-negative and right-positive/left-negative, respectively. The converter is equivalent to a cascade of a bidirectional buck–boost converter and a bidirectional bridge converter. Cells that need to be equalized are connected to the bidirectional buck–boost converter, which can not only improve the equalization voltage gap to improve the equalization current but also make the equalization current work in a continuous state. The transformer leakage inductance L_r and the external inductor connected in series to the secondary winding constitute the inductor L_2, so the energy stored in L_r is contained in L_2. According to the circuit parameters, L_2 can operate in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM). Therefore, operation of the converter in CCM or DCM means L_2 works in the corresponding mode.

The proposed bidirectional dc–dc converter with an integrated cascade structure has the following characteristics:

1) Compared with traditional architectures, the proposed new converter significantly reduces the number of bidirectional switches and polarity switches and effectively improves the integration and reliability of the entire equalization system.
2) The converter effectively increases the equalization current and makes it work in a continuous current state, which not only improves the equalization speed but also avoids potential damage to the battery.
3) The integrated cascade structure enables the converter to achieve a high voltage conversion ratio when the turn ratio of the transformer is small. This feature can improve the efficiency of the transformer and equalize a battery string that contains more cells.
4) The energy in the leakage inductance can be released to the capacitors on the high-voltage side or the low-voltage side, thereby avoiding the voltage spikes caused by the leakage inductance.
5) The switching losses can be reduced by the soft-switching operation, which further improves the conversion efficiency of the equalizer.

A. Boost Mode

When an overcharged single cell releases energy to the entire battery string through the bidirectional dc–dc converter, the converter operates in boost mode. Regardless of the polarity of the $V_{\rm LV}$ terminal voltage, the cells can be equalized by controlling the operating state of the converter. Fig. 3(a) and (b) show switching sequence diagrams for when an overcharged odd-numbered cell is equalized; the difference is that the working mode of inductor L_2 is different. In Fig. 3(b), inductor L_2 operates in DCM, and the current i_{L2} decreases to zero before stages [t_3- t_5] and [t_8- t_{10}]. In addition, the converter operation in other stages is similar to that of CCM. Here, D_d is the percentage of dead time in switching period T_s, Δ_1 is the ratio of the interval [t_1- t_2] in T_s in CCM, and β_1 is the ratio of the interval [t_1- t_3] in T_s in DCM.

Fig. 4 shows the equivalent circuit when the converter operates in accordance with the switching sequence shown in Fig. 3(a). At this point, the converter equalizes the odd-numbered cells, inductor L_2 operates in CCM, and ten operation stages occur during one switching cycle.

Stage 1 [$t_0 - t_1$]*:* At t_0, S_2 and S_5 are turned ON. $V_{\rm LV}$ charges L_1 through S_2 and S_4, and i_{L1} increases linearly. Since L_2 operates in CCM, current i_{L2} freewheels through S_4, S_5, C_4 and the body diodes of S_8 until i_{L2} decreases to zero.

Stage 2 [$t_1 - t_2$]*:* At t_1, i_{L2} decreases to zero; V_{C2} charges L_2 through S_4, S_5, C_3 and the body diodes of S_7; and i_{L2} increases linearly in reverse. In this stage, the input voltage $V_{\rm LV}$ continues to charge L_1 through S_2 and S_4.

Stage 3 [$t_2 - t_3$]*:* At t_2, S_2 and S_5 are turned OFF. Because of the dead time, S_1 and S_6 will not be turned ON immediately. $V_{\rm LV}$ and L_1 release energy to C_2 through S_4 and the body diodes of S_1, and i_{L1} decreases linearly. L_2 freewheels through S_4, C_3 and the body diodes of S_6 and S_7, and current i_{L2} decreases linearly.

Stage 4 [$t_3 - t_4$]*:* At t_3, S_1 and S_6 are turned ON. Unlike the previous stage, S_1, S_4 and S_6 all work in a synchronous rectification state.

Stage 5 [$t_4 - t_5$]*:* At t_4, S_4 is turned OFF, and S_3 will not be turned ON immediately. During the dead time, $V_{\rm LV}$ and L_1 continue to release energy to C_2. The freewheeling channel of L_2 is changed; it freewheels through S_6, C_3 and the body diodes of S_3 and S_7; and i_{L2} decreases linearly with a larger slope.

Stage 6 [$t_5 - t_6$]*:* At t_5, S_3 is turned ON. $V_{\rm LV}$ charges L_1 through S_1 and S_3, and i_{L1} increases linearly. Since L_2 operates in CCM, i_{L2} continues to freewheel through S_3, S_6 and the body diodes of S_7 until i_{L2} decreases to zero.

Stage 7 [$t_6 - t_7$]*:* At t_6, i_{L2} decreases to zero, V_{C2} charges L_2 through S_3, S_6, C_4 and the body diodes of S_8, and i_{L2} increases linearly in reverse. In this stage, $V_{\rm LV}$ continues to charge L_1 through S_1 and S_3.

Stage 8 [$t_7 - t_8$]*:* At t_7, S_3 is turned OFF, and S_4 will not be turned ON immediately. $V_{\rm LV}$ and L_1 release energy to C_2 through S_1 and the body diodes of S_4, and i_{L1} decreases linearly. L_2 freewheels through S_6, C_4, and the body diodes of S_4 and S_8, and i_{L2} decreases linearly.

Stage 9 [$t_8 - t_9$]*:* At t_8, S_4 is turned ON. Unlike the previous stage, S_1 and S_4 work in a synchronous rectification state.

Stage 10 [$t_9 - t_{10}$]*:* At t_9, S_1, and S_6 are turned OFF, and S_2 and S_5 will not be turned ON immediately. $V_{\rm LV}$ and L_1 continue to release energy to C_2. The freewheeling channel of L_2 is changed; it freewheels through S_4, C_4, and the body diodes of S_5 and S_8; and i_{L2} decreases linearly with a larger slope.

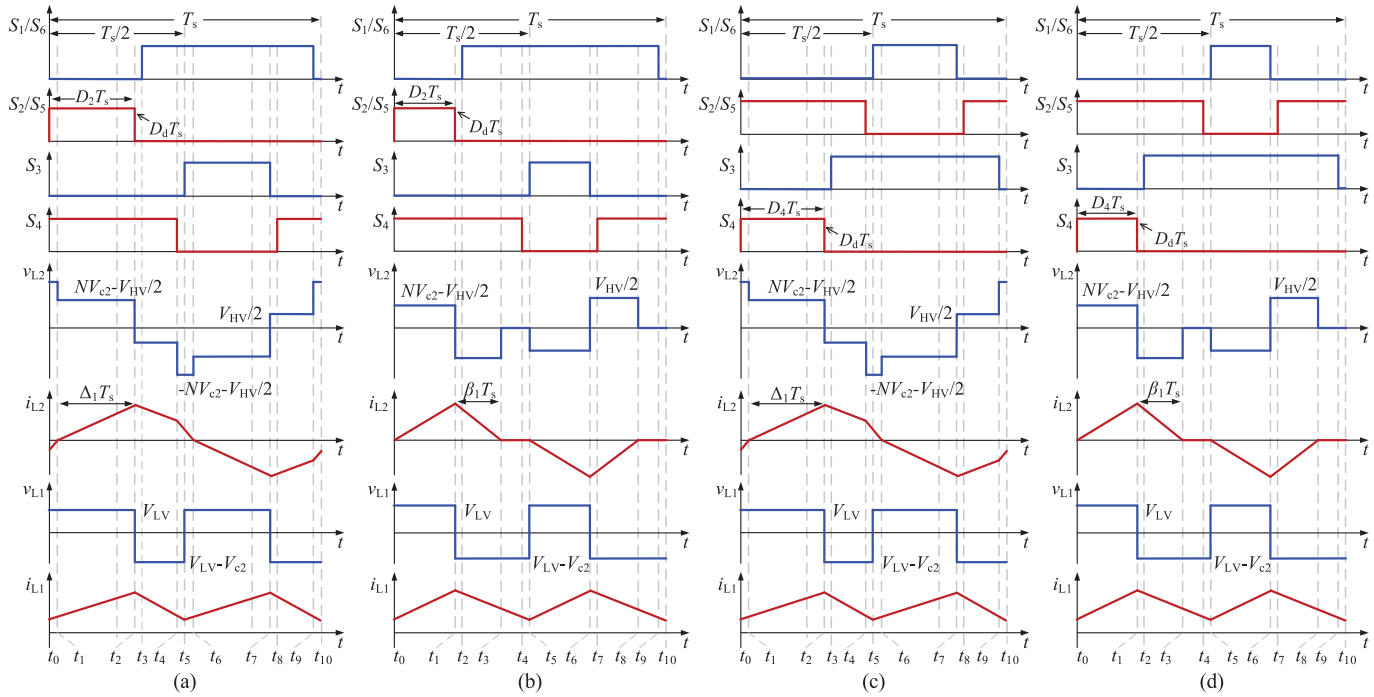

Fig. 3. Switching sequence diagrams when an overcharged cell is equalized. (a) Equalization of an odd-numbered cell in CCM. (b) Equalization of an odd-numbered cell in DCM. (c) Equalization of an even-numbered cell in CCM. (d) Equalization of an even-numbered cell in DCM.

Fig. 3(c) and (d) show switching sequence diagrams for when an overcharged even-numbered cell is equalized. Compared with Fig. 3(a) and (b), it is only necessary to adjust the switching sequence of several switches; that is, the cell can be equalized by the same working principle.

B. Buck Mode

When the entire battery string releases energy to an undercharged single cell through the bidirectional dc–dc converter, the converter operates in buck mode. Fig. 5(a) and (b) show switching sequence diagrams for when an undercharged odd-numbered cell is equalized. The difference is again that the working mode of inductor L_2 is different. Here, D_d is the percentage of dead time in switching period T_s. The duty cycles of switches S_1 and S_6 are D_1 in the first half-cycle and are always on during the second half-cycle. The on time of S_4 lags the on time of S_1 and S_6 by 180 degrees. It should be noted that S_3 and S_5 are always off in DCM to prevent power backflow after current i_{L2} drops to zero. However, in CCM, switches S_3 and S_5 can be turned on at t_8 and t_3, respectively, and operate in a synchronous rectification state, which further improves the efficiency of the converter.

Fig. 6 shows the equivalent circuit of the converter operating in buck mode to equalize the undercharged odd-numbered cells. At this point, L_2 operates in CCM, and ten operation stages occur during one switching cycle.

Stage 1 $[t_0 - t_1]$*:* At t_0, S_4, and S_7 are turned ON. Capacitor voltage V_{C2} charges L_1 through S_1, S_4 and V_{LV}, and i_{L1} increases linearly. Since inductor L_2 operates in CCM, current i_{L2} continues to freewheel through S_4, S_6, S_7 and C_3 until i_{L2} decreases to zero.

Stage 2 $[t_1 - t_2]$*:* At t_1, i_{L2} decreases to zero; capacitor voltage V_{C3} charges L_2 through S_4, S_6, and S_7; and i_{L2} increases linearly in reverse. In this stage, V_{C2} continues to charge L_1.

Stage 3 $[t_2 - t_3]$*:* At t_2, S_1 and S_6 are turned OFF. Because of the dead time, S_2, and S_5 will not be turned ON immediately. L_1 freewheels through S_4, V_{LV} and the body diodes of S_2, and i_{L1} decreases linearly. V_{C3} and L_2 release energy to C_2 through S_4, S_7 and the body diodes of S_5, and i_{L2} decreases linearly.

Stage 4 $[t_3 - t_4]$*:* At t_3, S_2, and S_5 are turned ON. Unlike the previous stage, S_2, S_4, and S_5 all work in a synchronous rectification state.

Stage 5 $[t_4 - t_5]$*:* At t_4, S_2, S_5, and S_7 are turned OFF, and S_1, S_6 and S_8 will not be turned ON immediately. During the dead time, L_1 freewheels through S_4, V_{LV} and the body diodes of S_2. The freewheeling channel of L_2 is changed; it freewheels through S_4, C_4 and the body diodes of S_8 and S_5; and i_{L2} decreases linearly with a larger slope.

Stage 6 $[t_5 - t_6]$*:* At t_5, S_1, S_6, and S_8 are turned ON. V_{C2} charges L_1 through S_1, S_4, V_{LV}, and i_{L1} increases linearly. Since L_2 operates in CCM, i_{L2} continues to freewheel through S_4, S_6, S_8, and C_4 until i_{L2} decreases to zero.

Stage 7 $[t_6 - t_7]$*:* At t_6, i_{L2} decreases to zero; V_{C4} charges L_2 through S_4, S_6 and S_8; and i_{L2} increases linearly in reverse. In this stage, V_{C2} continues to charge L_1.

Stage 8 $[t_7 - t_8]$*:* At t_7, S_4 is turned OFF, and S_3 will not be turned ON immediately. During the dead time, L_1 freewheels through S_1, V_{LV} and the body diodes of S_3, and i_{L1} decreases linearly. V_{C4} and L_2 release energy to C_2 through S_6, S_8 and the body diodes of S_3, and i_{L2} decreases linearly.

Stage 9 $[t_8 - t_9]$*:* At t_8, S_3 is turned ON. Unlike the previous stage, S_3 and S_6 work in a synchronous rectification state.

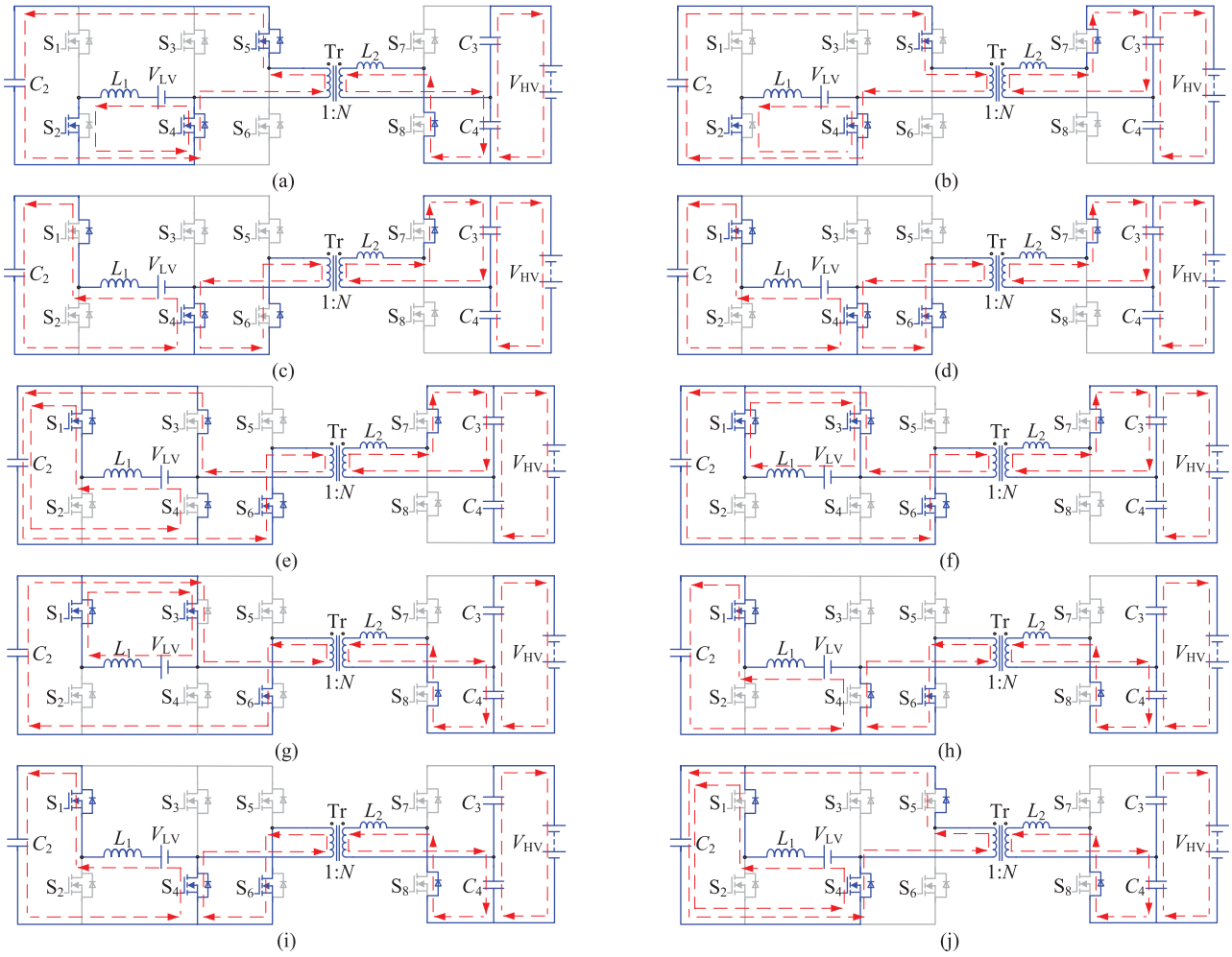

Fig. 4. Equivalent circuit when an overcharged odd-numbered cell is equalized in CCM. (a) Stage 1 [t_0- t_1]. (b) Stage 2 [t_1- t_2]. (c) Stage 3 [t_2- t_3]. (d) Stage 4 [t_3- t_4]. (e) Stage 5 [t_4- t_5]. (f) Stage 6 [t_5- t_6]. (g) Stage 7 [t_6- t_7]. (h) Stage 8 [t_7- t_8]. (i) Stage 9 [t_8- t_9]. (j) Stage 10 [t_9- t_{10}].

Stage 10 [t_9 – t_{10}]*:* At t_9, S_3 and S_8 are turned OFF, and S_4 and S_7 will not be turned ON immediately. During the dead time, L_1 continues to freewheel through S_4, V_{LV} and the body diodes of S_2. The freewheeling channel of L_2 is changed; it freewheels through S_6, C_3 and the body diodes of S_3 and S_7; and i_{L2} decreases linearly with a larger slope.

Fig. 5(c) and (d) show control sequence diagrams for the condition in which the battery string releases energy to an undercharged even-numbered cell. Compared with Fig. 5(a) and (b), only the switching sequence of the switches is different. In addition, the working principle of the converter and the conditions of soft switching are the same as those for odd-numbered cells.

III. Theoretical Derivation and Analysis

According to the above analysis, it is only necessary to adjust the switching sequence of several switches, and odd-numbered and even-numbered cells can be equalized by the same working principle. Therefore, the gain analysis and soft-switching analysis of the converter are consistent when cells with different voltage polarities are equalized. To simplify the analysis, the following is an example of the equalization of odd-numbered cells. The analysis methods and results are equally applicable to the equalization of even-numbered cells.

A. Derivation in Boost Mode

As shown in Fig. 3(a), when the converter operates in CCM, the volt-second balance relations of inductors L_1 and L_2 can be expressed as follows:

$$\begin{cases} V_{\mathrm{LV}} D_2 T_{\mathrm{s}} = (V_{\mathrm{C2}} - V_{\mathrm{LV}})(1-2D_2)\frac{T_{\mathrm{s}}}{2} \\ \left(NV_{\mathrm{C2}} - \frac{V_{\mathrm{HV}}}{2}\right)\Delta_1 T_{\mathrm{s}} = \left(NV_{\mathrm{C2}} + \frac{V_{\mathrm{HV}}}{2}\right)(D_2 - \Delta_1 + D_{\mathrm{d}})T_{\mathrm{s}} \\ \qquad\qquad + \frac{V_{\mathrm{HV}}}{2}(1-2D_2-2D_{\mathrm{d}})\frac{T_{\mathrm{s}}}{2} \end{cases}. \tag{1}$$

From this, the voltage gain in CCM can be derived as:

$$\frac{V_{\mathrm{HV}}}{V_{\mathrm{LV}}} = \frac{4N(2\Delta_1 - D_{\mathrm{d}} - D_2)}{1-2D_2}. \tag{2}$$

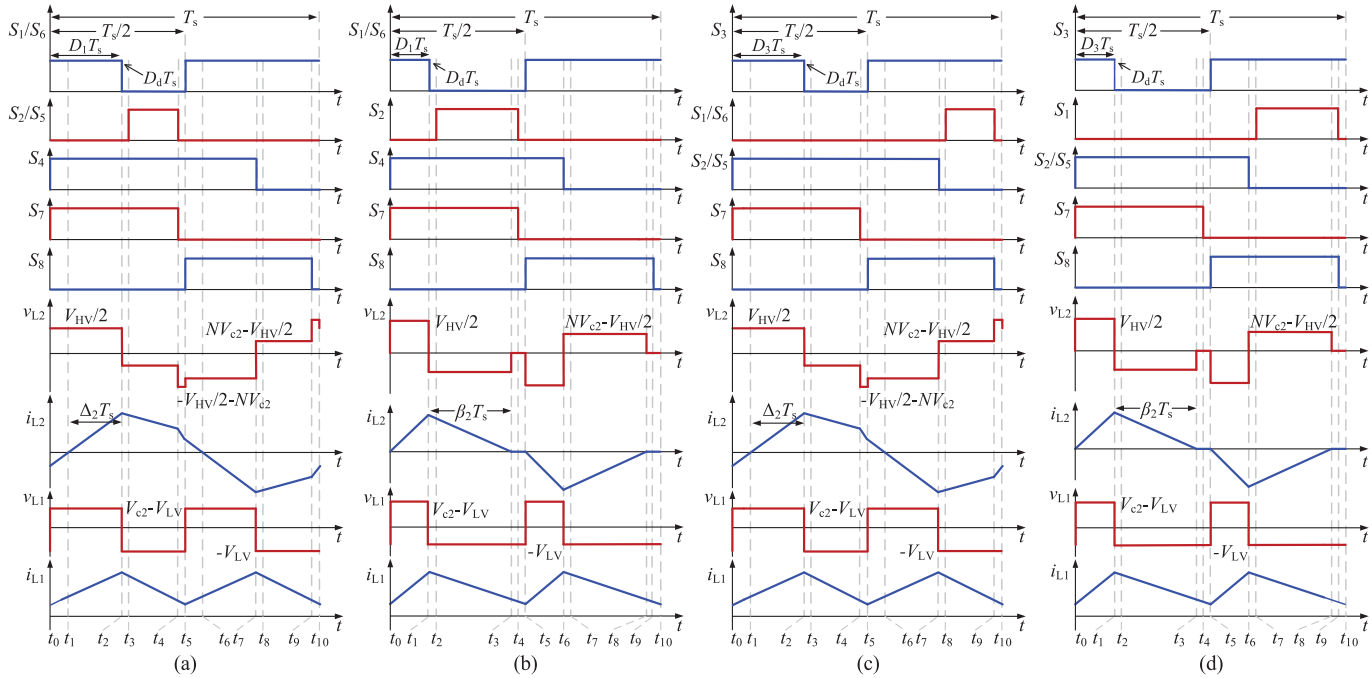

Fig. 5. Switching sequence diagrams when an undercharged cell is equalized. (a) Equalization of an odd-numbered cell in CCM. (b) Equalization of an odd-numbered cell in DCM. (c) Equalization of an even-numbered cell in CCM. (d) Equalization of an even-numbered cell in DCM.

At this point, the average current I_2 flowing into the high-voltage side can be calculated by:

$$I_2 = \frac{1}{T_s/2}\int_{t_1}^{t_6} i_2(t)dt = \frac{V_{HV}[2(D_2+D_d)^2 + 4\Delta_1(\Delta_1 - D_2 - D_d) - D_2 - D_d]}{8f_sL_2(D_2 - 2\Delta_1 + D_d)}. \tag{3}$$

By taking $\Delta_1 = D_2$ into (3) and combining with (2), the average current I_{2crit} flowing into the high-voltage side at the critical state can be obtained as:

$$I_{2crit} = \frac{V_{HV}(D_2 - 2{D_2}^2 + D_d - 2{D_d}^2)}{8f_sL_2(D_2 - D_d)}. \tag{4}$$

By substituting $V_{HV} = I_2\ R_2/2$ into (4), the conditions for operation in CCM are expressed as follows:

$$I_2 > I_{2crit} = \frac{I_2(D_2 - 2{D_2}^2 + D_d - 2{D_d}^2)}{K_{Boost}(D_2 - D_d)} \tag{5}$$

where the boost coefficient $K_{Boost} = 16\ L_2\ f_s/R_2$ and R_2 is the equivalent load resistor in boost mode.

By simplifying (5), the CCM condition can be obtained:

$$K_{Boost} > K_{Boost}(D_2) \tag{6}$$

where

$$K_{Boost}(D_2) = \frac{D_2 - 2{D_2}^2 + D_d - 2{D_d}^2}{D_2 - D_d}.$$

Since the dead time is small in practical applications, this article sets $D_d = 0.02$. Therefore, the boundary condition curves of CCM and DCM in boost mode can be drawn according to (6). As shown in Fig. 7, when $K_{Boost} = 0.455$, the critical duty cycle D_{2crit} is 0.317; that is, the converter works in CCM when $D_2 > 0.317$ and in DCM when $D_2 < 0.317$.

By combining (2) and (3), the voltage gain of the converter in CCM is:

$$\frac{V_{HV}}{V_{LV}} = \frac{2N\left(\sqrt{{K_{Boost}}^2 + 4D_2 + 4D_d - (2D_2 + 2D_d)^2} - K_{Boost}\right)}{1 - 2D_2}. \tag{7}$$

The same analysis method is used to derive the voltage gain in DCM. As shown in Fig. 3(b), when the converter operates in DCM, the volt-second balance relations of inductors L_1 and L_2 can be expressed as:

$$\begin{cases} V_{LV}D_2T_s = (V_{C2} - V_{LV})(1 - 2D_2)\frac{T_s}{2} \\ \left(NV_{C2} - \frac{V_{HV}}{2}\right)D_2T_s = \frac{V_{HV}}{2}\beta_1T_s \end{cases}. \tag{8}$$

Thus, the voltage gain in DCM can be derived as:

$$\frac{V_{HV}}{V_{LV}} = \frac{2ND_2}{(1 - 2D_2)(D_2 + \beta_1)}. \tag{9}$$

The average current I_2 flowing into the high-voltage side in DCM is:

$$I_2 = \frac{1}{T_s/2}\int_{t_0}^{t_3} i_2(t)dt = \frac{(D_2 + \beta_1)V_{HV}\beta_1}{2f_sL_2}. \tag{10}$$

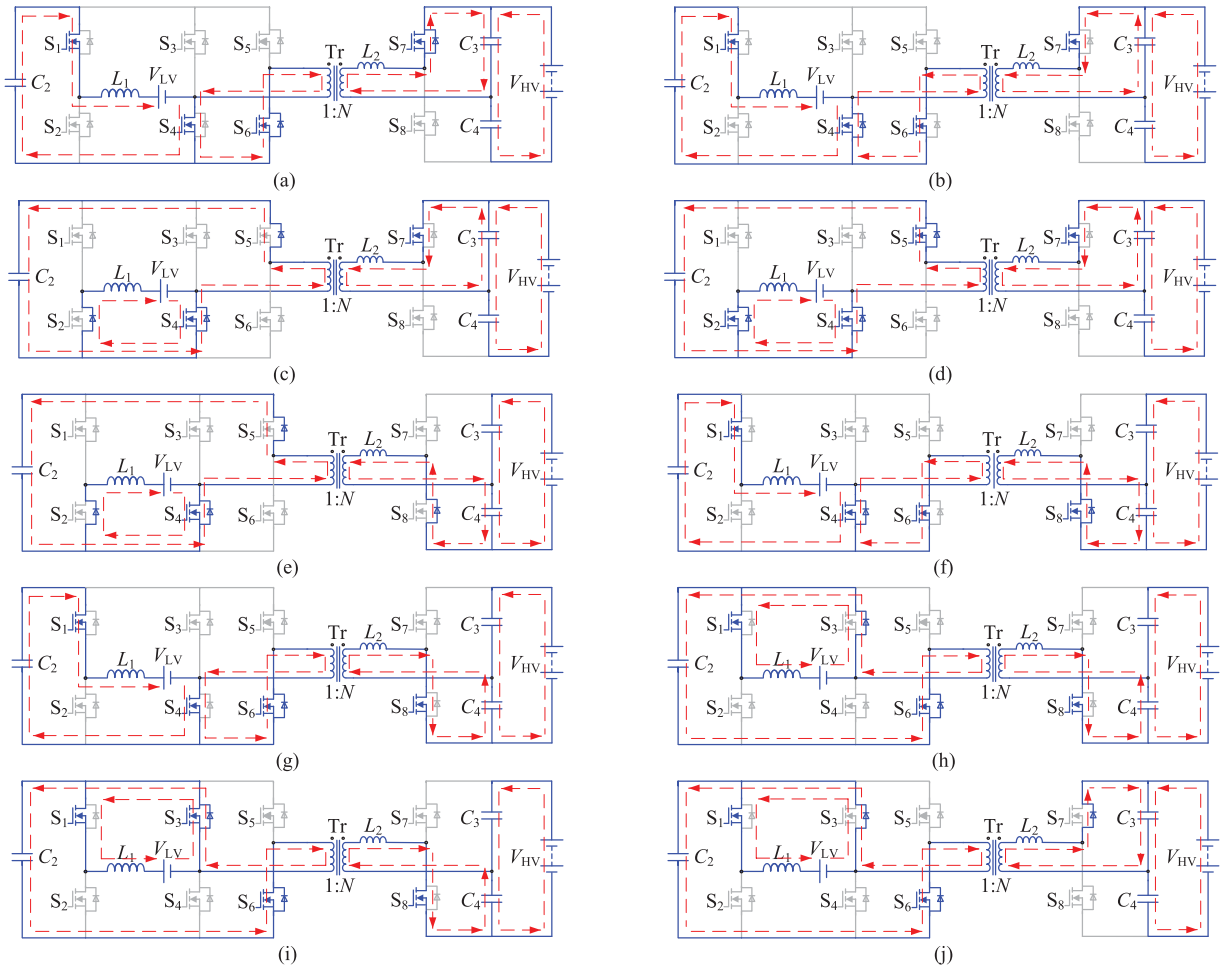

Fig. 6. Equivalent circuit when an undercharged odd-numbered cell is equalized in CCM. (a) Stage 1 [t_0- t_1]. (b) Stage 2 [t_1- t_2]. (c) Stage 3 [t_2- t_3]. (d) Stage 4 [t_3- t_4]. (e) Stage 5 [t_4- t_5]. (f) Stage 6 [t_5- t_6]. (g) Stage 7 [t_6- t_7]. (h) Stage 8 [t_7- t_8]. (i) Stage 9 [t_8- t_9]. (j) Stage 10 [t_9- t_{10}].

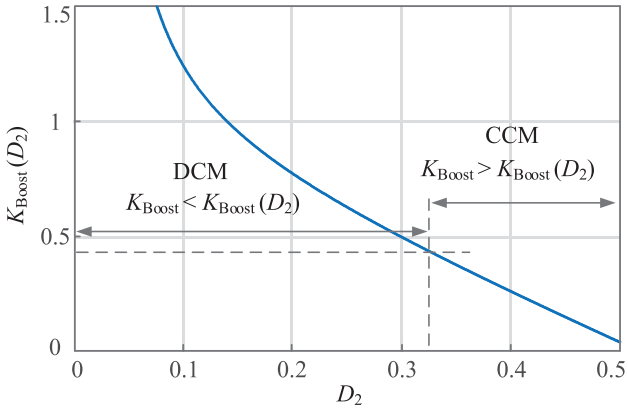

Fig. 7. Boundary between CCM and DCM in boost mode.

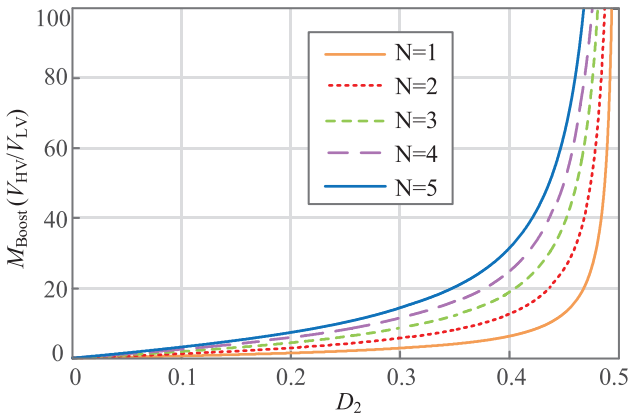

Fig. 8. Voltage gain that corresponds to different turn ratios in boost mode.

By combining (9) and (10), the voltage gain of the converter when operating in DCM mode is:

$$\frac{V_{\text{HV}}}{V_{\text{LV}}} = \frac{4ND_2(\sqrt{{D_2}^2 + K_{\text{Boost}}} - D_2)}{K_{\text{Boost}}(1 - 2D_2)}. \tag{11}$$

As shown in Fig. 8, by substituting $K_{\text{Boost}} = 0.455$, $D_{\text{d}} = 0.02$, and different transformer turns ratios N into (7) and (11), the voltage gain curves corresponding to different turns ratios in boost mode can be obtained. The proposed converter can achieve a high boost gain at a low transformer turns ratio, avoiding duty cycle operation in the limit state and effectively improving the efficiency of the transformer. Additionally, a high voltage gain can enable the converter to equalize a battery string that contains

more cells, which improves the integration of the equalization system.

B. Derivation in Buck Mode

As shown in Fig. 5(a), when the converter operates in CCM, the volt-second balance relations of inductors L_1 and L_2 can be expressed as:

$$\begin{cases} V_{\mathrm{LV}}(1-2D_1)\frac{T_\mathrm{s}}{2} = (V_{\mathrm{C2}}-V_{\mathrm{LV}})D_1T_\mathrm{s} \\ \frac{V_{\mathrm{HV}}}{2}\Delta_2 T_\mathrm{s} = \left(NV_{\mathrm{C2}}-\frac{V_{\mathrm{HV}}}{2}\right)(1-2D_1-2D_\mathrm{d})\frac{T_\mathrm{s}}{2} \\ \qquad\qquad + \left(NV_{\mathrm{C2}}+\frac{V_{\mathrm{HV}}}{2}\right)D_\mathrm{d}T_\mathrm{s} + \frac{V_{\mathrm{HV}}}{2}(D_1-\Delta_2)T_\mathrm{s}. \end{cases} \tag{12}$$

Thus, the voltage gain in CCM can be derived as:

$$\frac{V_{\mathrm{LV}}}{V_{\mathrm{HV}}} = \frac{D_1(1+4\Delta_2-4D_1-4D_\mathrm{d})}{N(1-2D_1)}. \tag{13}$$

At this point, the average output current I_2 on the high-voltage side can be calculated by:

By substituting $V_{\mathrm{HV}}\ I_2/2 = V_{\mathrm{LV}}\ I_1$ into (14) shown at the bottom of this page, and combining with (13), the average input current I_1 on the low-voltage side can be obtained as follows:

$$I_1 = \frac{V_{\mathrm{LV}}N^2(1-2D_1)[D_1+2D_\mathrm{d}-2{D_\mathrm{d}}^2-2(D_1+D_\mathrm{d})^2]}{8f_\mathrm{s}L_2{D_1}^2(1+4\Delta_2-4D_1-4D_\mathrm{d})}. \tag{15}$$

By substituting $\Delta_2 = D_1$ into (15), the average current $I_{1\mathrm{crit}}$ on the low-voltage side at the critical state can be obtained as:

$$I_{1\mathrm{crit}} = \frac{V_{\mathrm{LV}}N^2(1-2D_1)(D_1-2{D_1}^2+2D_\mathrm{d}-4{D_\mathrm{d}}^2-4D_1D_\mathrm{d})}{8f_\mathrm{s}L_2{D_1}^2(1-4D_\mathrm{d})}. \tag{16}$$

By substituting $V_{\mathrm{LV}} = I_1\ R_1$ into (16), the conditions for operation in CCM are expressed as

$$I_1 > I_{1\mathrm{crit}} = \frac{I_1(1-2D_1)(D_1-2{D_1}^2+2D_\mathrm{d}-4{D_\mathrm{d}}^2-4D_1D_\mathrm{d})}{8K_{\mathrm{Buck}}{D_1}^2(1-4D_\mathrm{d})} \tag{17}$$

where the buck coefficient $K_{\mathrm{Buck}} = L_2\ f_\mathrm{s}/R_1\ N^2$, and R_1 is the equivalent load resistor in the buck mode.

By simplifying (17), the CCM condition can be obtained:

$$K_{\mathrm{Buck}} > K_{\mathrm{Buck}}(D_1) \tag{18}$$

where $K_{\mathrm{Buck}}(D_1) = \frac{(1-2D_1)(D_1-2{D_1}^2+2D_\mathrm{d}-4{D_\mathrm{d}}^2-4D_1D_\mathrm{d})}{8{D_1}^2(1-4D_\mathrm{d})}$.

Similar to boost mode, the dead time $D_\mathrm{d} = 0.02$ is substituted into (18). Thus, the boundary condition curves of CCM and DCM under buck mode can be drawn. As shown in Fig. 9, when $K_{\mathrm{Buck}} = 0.289$, the critical duty cycle $D_{1\mathrm{crit}}$ is 0.2. Therefore, when $D_1 > 0.2$, the converter works in CCM, and when $D_1 < 0.2$, the converter works in DCM.

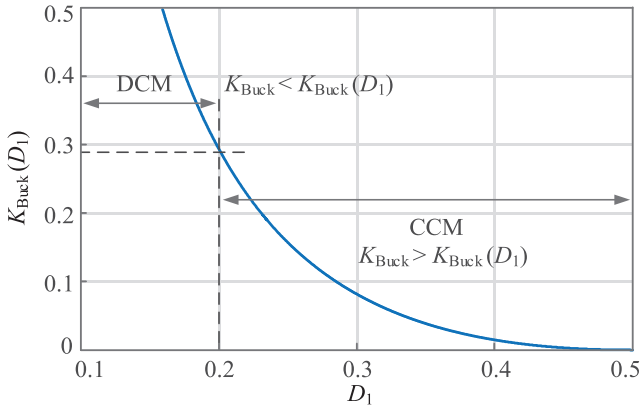

Fig. 9. Boundary between CCM and DCM in buck mode.

By combining (9) and (15), the voltage gain of the converter when operating in CCM is

$$\frac{V_{\mathrm{LV}}}{V_{\mathrm{HV}}} = \frac{D_1-2{D_1}^2+2D_\mathrm{d}-4{D_\mathrm{d}}^2-4D_1D_\mathrm{d}}{8ND_1K_{\mathrm{Buck}}}. \tag{19}$$

When the converter works in DCM, as shown in Fig. 5(b), the volt-second balance relations of inductors L_1 and L_2 can be expressed as:

$$\begin{cases} V_{\mathrm{LV}}(1-2D_1)\frac{T_\mathrm{s}}{2} = (V_{\mathrm{C2}}-V_{\mathrm{LV}})D_1T_\mathrm{s} \\ \frac{V_{\mathrm{HV}}}{2}D_1T_\mathrm{s} = \left(NV_{\mathrm{C2}}-\frac{V_{\mathrm{HV}}}{2}\right)\beta_2T_\mathrm{s}. \end{cases} \tag{20}$$

Thus, the voltage gain in DCM can be derived as:

$$\frac{V_{\mathrm{LV}}}{V_{\mathrm{HV}}} = \frac{D_1(D_1+\beta_2)}{N\beta_2}. \tag{21}$$

The average output current I_2 on the high-voltage side is

$$I_2 = \frac{1}{T_\mathrm{s}/2}\int_{t_0}^{t_3} i_2(t)dt = \frac{V_{\mathrm{HV}}D_1(D_1+\beta_2)}{2f_\mathrm{s}L_2}. \tag{22}$$

By substituting $V_{\mathrm{HV}}\ I_2/2 = V_{\mathrm{LV}}\ I_1$ into (22) and combining with (21), the average input current I_1 on the low-voltage side can be obtained as:

$$I_1 = \frac{V_{\mathrm{LV}}N^2{\beta_2}^2}{4f_\mathrm{s}L_2({D_1}^2+D_1\beta_2)}. \tag{23}$$

By combining (21) and (22), the voltage gain of the converter when operating in DCM is

$$\frac{V_{\mathrm{LV}}}{V_{\mathrm{HV}}} = \frac{D_1(K_{\mathrm{Buck}}+\sqrt{K_{\mathrm{Buck}}(1+K_{\mathrm{Buck}})})}{2NK_{\mathrm{Buck}}}. \tag{24}$$

By substituting $K_{\mathrm{Buck}} = 0.289$, $D_\mathrm{d} = 0.02$ and different transformer turns ratios N into (19) and (24), the voltage gain curves corresponding to different turns ratios can be obtained, as shown in Fig. 10. This figure shows that the integrated cascade

$$I_2 = \left|\frac{1}{T_\mathrm{s}/2}\int_{t_4}^{t_9} i_2(t)dt\right| = \frac{V_{\mathrm{HV}}(1+4\Delta_2-4D_1-4D_\mathrm{d})[D_1+2D_\mathrm{d}-2{D_\mathrm{d}}^2-2(D_1+D_\mathrm{d})^2]}{4f_\mathrm{s}L_2(1-2D_1)} \tag{14}$$

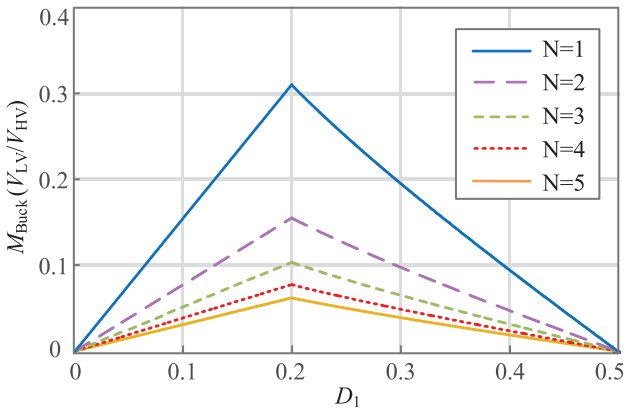

Fig. 10. Voltage gain that corresponds to different turn ratios in buck mode.

structure enables the converter to achieve a high buck gain with a low turn ratio, which not only improves the efficiency of the transformer but also enables the converter to have the ability to equalize long series-connected battery string.

C. Circuit Parameter Design

1) Inductor L_1 parameter design: The low-voltage side of the converter is connected to the cells that need to be equalized. To avoid potential damage to the cell, the equalization current i_{L1} needs to be operated in a continuous current state, that is, inductor L_1 is designed to operate in CCM. Therefore, the value of L_1 depends on the current ripple of i_{L1}. According to the actual charge and discharge characteristics of lithium-ion batteries, the maximum equalization charge current is set to 2 A, and the maximum equalization discharge current is set to 3 A. In boost mode, the ripple of current i_{L1} can be expressed as:

$$\Delta i_{L1\_boost} = \frac{V_{LV} D_2}{L_1 f_s} \tag{25}$$

where $\Delta i_{L1\_boost} = \alpha\, I_{L1}$, and the ripple coefficient α is 0.15.

The critical duty cycle expression of the converter in boost mode can be obtained by substituting $\Delta_1 = D_2$ into (2) as follows:

$$D_{2crit} = \frac{4NV_{LV}D_d + V_{HV}}{4NV_{LV} + 2V_{HV}}. \tag{26}$$

By substituting the parameters in Table I into (26), the critical duty cycle can be found as $D_{2crit} = 0.317$. By substituting the parameters in Table I and $D_{2crit} = 0.317$ into (25), it can be concluded that the range of inductor L_1 in boost mode is:

$$L_1 > \frac{V_{LV} D_2}{\alpha I_{L1} f_s} = \frac{3.7 \times 0.317}{0.15 \times 3 \times 20 \times 10^3} = 65\ \mu\text{H}. \tag{27}$$

Similarly, by substituting $\Delta_2 = D_1$ into (13), the critical duty cycle expression in buck mode can be determined as:

$$D_{1\_crit} = \frac{NV_{LV}}{2NV_{LV} - 4V_{HV}D_d + V_{HV}}. \tag{28}$$

Thus, the critical duty ratio in buck mode can be calculated as $D_{1crit} = 0.2$. The range of inductor L_1 in buck mode can be

TABLE I
PARAMETERS OF THE PROPOSED CONVERTER

Parameters		Values/Ratings
Rated voltage on low voltage side (V_{LV})		3.7 V
Rated voltage on high voltage side (V_{HV})		48.1 V
Switching frequency (f_s)		40 kHz
Inductors	L_1	100 μH
	L_2	210 μH
Capacitors	C_1	100 μF/16 V; multilayer ceramic capacitor
	C_2	100 μF/35 V; solid-state capacitor
	C_3	100 μF/100 V; aluminum electrolytic capacitor
	C_4	100 μF/100 V; aluminum electrolytic capacitor
Transformer	T_r	Turns ratio 1:4; Primary turns $N_1 = 5$; Secondary turns $N_2 = 20$; Magnetizing inductance L_{m1}=20 μH; Leakage inductance L_{s2}= 3.5 μH
MOSFETs	S_1-S_6	IRF1010Z; V_{DSS}=55V, I_D=75A; $R_{DS(on)}$=7.5mΩ
	S_7, S_8	IRF540Z; V_{DSS}=100V, I_D=36A; $R_{DS(on)}$=26.5mΩ
	S_{c1}-S_{c14}	IRF7862PbF; V_{DSS}=30V, I_D=21A; $R_{DS(on)}$=3.3mΩ

expressed as:

$$L_1 > \frac{(0.5 - D_1)V_{LV}}{\alpha I_{L1} f_s} = \frac{3.7 \times (0.5 - 0.2)}{0.15 \times 2 \times 20 \times 10^3} = 93\ \mu\text{H} \tag{29}$$

In summary, when the working frequency of the converter is 40 kHz, the inductor L_1 that satisfies the equalization current ripple can be considered 100 μH.

2) Inductor L_2 parameter design: The voltage gain curve in boost mode shows that the required voltage gain can be achieved by adjusting duty cycle D_2 regardless of the value of inductor L_2. A wider range of soft switching can be achieved when the converter is operating in CCM. Therefore, to ensure that the converter works in CCM at full load ($I_{discharge} = 3$ A), according to (4), the value range of inductor L_2 is

$$L_2 > \frac{V_{HV}(D_2 - 2{D_2}^2 + D_d - 2{D_d}^2)}{8 I_2 f_s (D_2 - D_d)} = 148\ \mu\text{H}. \tag{30}$$

From Fig. 9 and (19), when $D_{1crit} = 0.2$, the corresponding $K_{Buck} = 0.289$ and the voltage gain is 0.077. As shown in Fig. 10, the voltage gain in buck mode has a maximum at the critical duty cycle, and this value decreases as the load increases. Therefore, it is only necessary to ensure that the maximum voltage gain at full load ($R_1 = 1.85\ \Omega$) is 0.077. By adjusting duty cycle D_1, the voltage gain can meet the requirements under all load conditions. In other words, as long as the load resistance corresponding to the critical duty cycle is less than that at full load, the required voltage gain can be achieved under all loads. This condition can

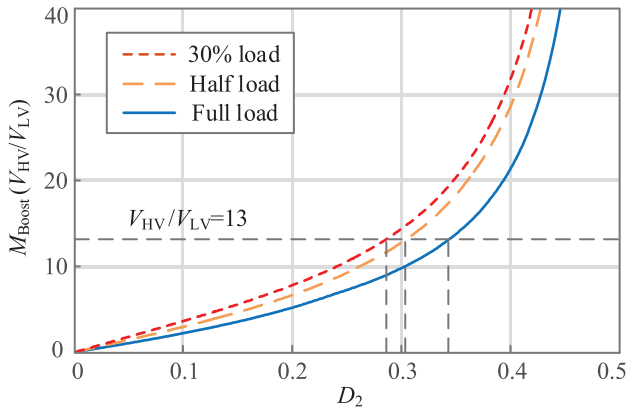

Fig. 11. Voltage gain under different loads in boost mode.

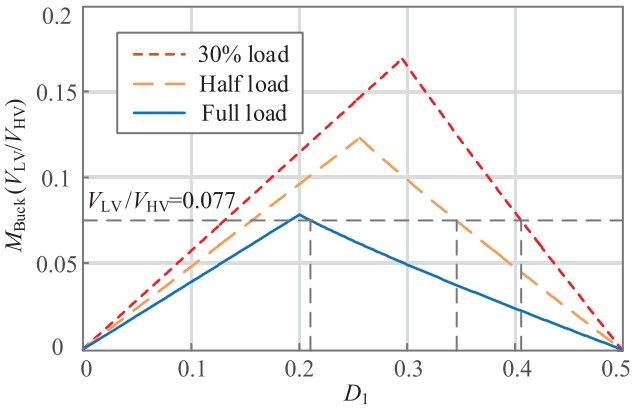

Fig. 12. Voltage gain under different loads in buck mode.

be expressed as:

$$R_1 = \frac{L_2 f_s}{N^2 K_{\text{Buck}}} < 1.85\ \Omega. \tag{31}$$

It can be calculated that:

$$L_2 < \frac{1.85 N^2 K_{\text{Buck}}}{f_s} = 214\ \mu\text{H}. \tag{32}$$

To ensure the equalization efficiency in a wider load range, the value of L_2 can be considered as large as possible. Therefore, L_2 in the experiment was considered 210 μH (where the transformer leakage inductance L_r is 3.5 μH). By substituting the parameters of L_2 and Table I into (7), (11), (19), and (24), the relationship curves between the voltage gain and load in boost mode and buck mode can be obtained. The voltage gain curve for $K_{\text{Boost}} = 0.645$ (full load), $K_{\text{Boost}} = 0.322$ (half load), and $K_{\text{Boost}} = 0.193$ (30% load) in boost mode are shown in Fig. 11. The voltage gain curve for $K_{\text{Buck}} = 0.284$ (full load), $K_{\text{Buck}} = 0.142$ (half load) and $K_{\text{Buck}} = 0.085$ (30% load) in buck mode are shown in Fig. 12. These different voltage gain curves show that the critical duty cycle and the actual duty cycle are different under different loads. After the value of L_2 is determined according to the set maximum charge/discharge current (full load), the equalization current can be adjusted by current closed-loop to make the converter work in different load conditions. When the set maximum equalization current increases, the value of L_2 also needs to be changed accordingly.

D. ZVS Analysis in Boost Mode

1) ZVS of S_1, S_4, and S_6: After S_2 and S_5 are turned OFF at t_2, currents i_{L1} and i_{L2} freewheel through the body diodes of S_1 and S_6, respectively. After S_3 is turned OFF at t_7, current i_{L2} freewheels through the body diode of S_4. This creates conditions for the ZVS operation of S_1, S_4, and S_6. Therefore, to realize the ZVS of these three switches, the energy stored in L_1 and L_2 must charge and discharge the junction capacitor of the switches completely during a suitable dead time. Thus, the ZVS conditions of S_1, S_4, and S_6 in boost mode are expressed as follows:

$$\frac{1}{2} L_1 [i_{L1}(t_2)]^2 > \frac{1}{2} (C_{oss1} + C_{oss2}) {V_{C1}}^2 \tag{33}$$

$$\frac{1}{2} L_2 [i_{L2}(t_2)]^2 > \frac{1}{2} (C_{oss3} + C_{oss4}) {V_{C1}}^2 \tag{34}$$

$$\frac{1}{2} L_2 [i_{L2}(t_7)]^2 > \frac{1}{2} (C_{oss5} + C_{oss6}) {V_{C1}}^2 \tag{35}$$

where C_{oss1}, C_{oss2}, C_{oss3}, C_{oss4}, C_{oss5}, and C_{oss6} are the junction capacitors of S_1, S_2, S_3, S_4, S_5, and S_6, respectively.

$i_{L1}(t_2)$ is the peak current of L_1 in each switching period, and L_1 works in CCM. Therefore, the condition in (33) must be satisfied in an actual circuit. Similarly, $i_{L2}(t_2)$ and $i_{L2}(t_7)$ are the peak currents of inductor L_2 in each switching period, and the values of the junction capacitors are generally very small, so the conditions in (34) and (35) are also satisfied. Therefore, switches S_1, S_4, and S_6 can realize ZVS in the full load range.

2) ZVS of S_3 and S_5: As shown in Fig. 3(a), since inductor L_2 operates in CCM, after switch S_4 is turned OFF at time t_4, current i_{L2} freewheels through the body diode of S_3. During the dead time [t_4- t_5], the junction capacitor of S_3 is completely discharged, which creates conditions for the ZVS operation of S_3 at t_5. The same operation takes place in [t_9- t_{10}], creating conditions for the ZVS operation of S_5 at t_{10}.

Thus, the ZVS condition of S_3 in boost mode is

$$i_{L2}(t_5) > 0 \tag{36}$$

where $i_{L2}(t_5)$ can be expressed as:

$$i_{L2}(t_5) = \frac{(N V_{C2} + \frac{V_{HV}}{2})}{L_2} (D_2 - \Delta_1) T_s. \tag{37}$$

By combining (3), (36) and (37), the ZVS range of S_3 and S_5 can be expressed as:

$$I_2 > \frac{V_{HV}(D_2 - 2{D_2}^2 + D_d - 2{D_d}^2)}{8 L_2 f_s (D_2 - D_d)}. \tag{38}$$

By substituting the parameters in Table I into (38), it can be concluded that when $L_2 = 210$ μH and $f_s = 40$ kHz, the ZVS range of S_3 and S_5 is $I_2 > 0.326$ A (I_2 is 0.462 A at full load). These results indicate that in boost mode, switches S_3 and S_5 can realize ZVS from 70.5% load to full load. The ZVS range curves of switches S_3 and S_5 are shown in Fig. 13, and the influence of inductor L_2 and switching frequency f_s on the ZVS regions can

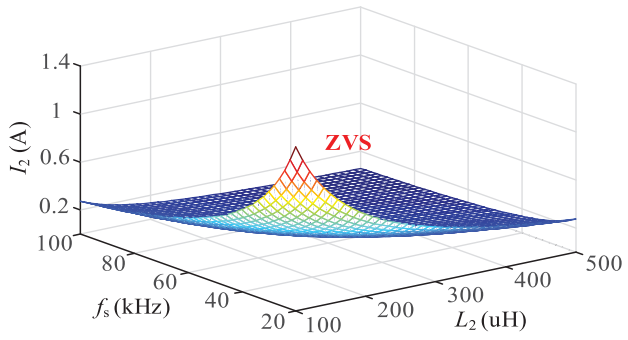

Fig. 13. ZVS boundary of S_3 and S_5 in boost mode.

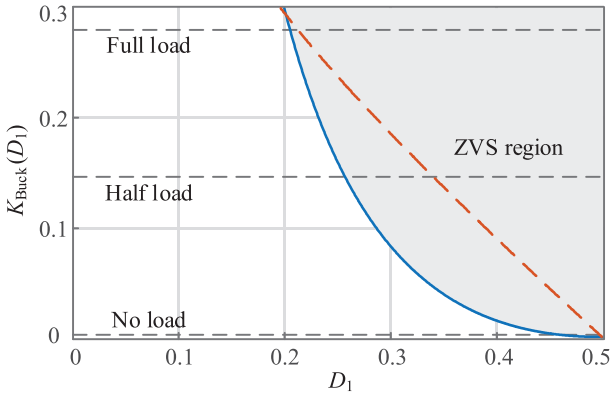

Fig. 14. ZVS boundary of S_7 and S_8 in buck mode.

be obtained from the diagram. When the working frequency is constant, a wider ZVS range can be obtained by increasing the value of L_2.

E. ZVS Analysis in Buck Mode

1) ZVS of S_2, S_3, *and* S_5: After S_1 and S_6 are turned OFF at t_2, currents i_{L1} and i_{L2} freewheel through the body diodes of S_2 and S_5, respectively. After S_4 is turned OFF at t_7, current i_{L2} freewheels through the body diode of S_3. This creates conditions for the ZVS operation of S_2, S_3, and S_5. Therefore, to realize the ZVS of these three switches, the energy stored in L_1 and L_2 must charge and discharge the junction capacitor of the switches completely during a suitable dead time. Thus, the ZVS conditions of S_2, S_3, and S_5 in buck mode are as follows:

$$\frac{1}{2}L_1[i_{L1}(t_2)]^2 > \frac{1}{2}(C_{oss1}+C_{oss2}){V_{C1}}^2 \tag{39}$$

$$\frac{1}{2}L_2[i_{L2}(t_2)]^2 > \frac{1}{2}(C_{oss5}+C_{oss6}){V_{C1}}^2 \tag{40}$$

$$\frac{1}{2}L_2[i_{L2}(t_7)]^2 > \frac{1}{2}(C_{oss3}+C_{oss4}){V_{C1}}^2 \tag{41}$$

where C_{oss1}, C_{oss2}, C_{oss3}, C_{oss4}, C_{oss5}, and C_{oss6} are junction capacitors of S_1, S_2, S_3, S_4, S_5, and S_6, respectively.

$i_{L1}(t_2)$ is the peak current of L_1 in each switching period, and L_1 works in CCM. Therefore, the condition in (39) must be satisfied in an actual circuit. Similarly, $i_{L2}(t_2)$ and $i_{L2}(t_7)$ are the peak currents of L_2 in each switching period, and the values of the junction capacitors are generally very small, so the conditions in (40) and (41) are also satisfied. Therefore, switches S_2, S_3, and S_5 can realize ZVS in the full load range.

2) ZVS of S_7 *and* S_8: As shown in Fig. 5 (a), since L_2 operates in CCM, after S_7 is turned OFF at time t_4, current i_{L2} freewheels through the body diode of S_8. During the dead time [t_4- t_5], the junction capacitor of S_8 is completely discharged, which creates conditions for the ZVS operation of S_8 at t_5. The same operation takes place in [t_9- t_{10}], creating conditions for the ZVS operation of S_7 at t_{10}.

Thus, the ZVS condition of S_8 in buck mode is:

$$i_{L2}(t_5) > 0 \tag{42}$$

where $i_{L2}(t_5)$ can be expressed as:

$$i_{L2}(t_5) = \frac{V_{HV}}{2L_2}(D_1-\Delta_2)T_s. \tag{43}$$

By combining (14), (42), and (43), the ZVS range of S_7 and S_8 can be expressed as:

$$K_{\mathrm{Buck}} > \frac{(1-2D_1)(D_1-2{D_1}^2+2D_d-4{D_d}^2-4D_1D_d)}{8{D_1}^2(1-4D_d)}. \tag{44}$$

It is known that the voltage gain of the converter operating in CCM is:

$$\frac{V_{LV}}{V_{HV}} = \frac{D_1-2{D_1}^2+2D_d-4{D_d}^2-4D_1D_d}{8ND_1K_{\mathrm{Buck}}}. \tag{45}$$

From this, the conditions of the converter when operating in CCM can be derived as follows:

$$K_{\mathrm{Buck}} = \frac{V_{HV}(D_1-2{D_1}^2+2D_d-4{D_d}^2-4D_1D_d)}{8ND_1V_{LV}}. \tag{46}$$

As shown in the shaded section of Fig. 14, the ZVS range of S_7 and S_8 under different load conditions can be obtained by substituting the parameters in Table I into (44). In addition, according to (46), the trajectories of the actual operating points under different loads can be obtained. The actual operating points from no load to full load all fall in the shaded area, indicating that the converter can realize the ZVS of S_7 and S_8 within the full load range.

IV. Experimental Results

A. Prototype of a Charge Equalization System for 13 Cells

Fig. 15 shows the main circuit part of the prototype. Fig. 16 shows a block diagram of the centralized charge equalization system employed in this article, and the experimental parameters are shown in Table I. The entire system consists of a bidirectional dc–dc converter, battery string, bidirectional switch array, voltage and current sampling circuit, driving circuit, and microcontroller. The voltage of each cell is detected in real time by the LTC6812, the currents on the high-voltage side and low-voltage side are detected by current sensors, and the

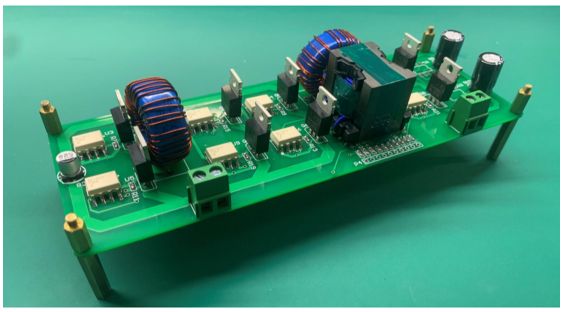

Fig. 15. Main circuit part of the prototype.

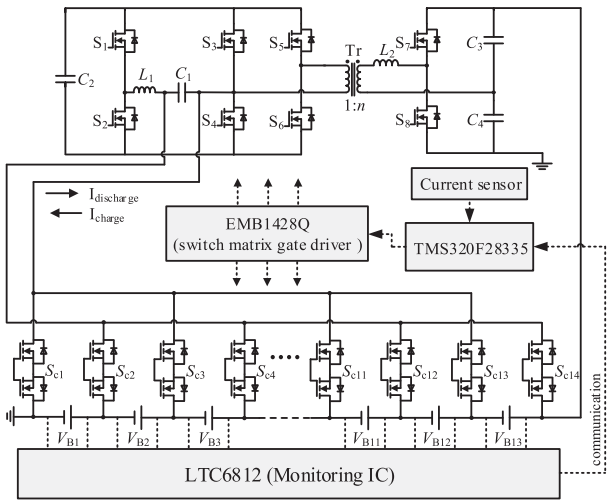

Fig. 16. Block diagram of the charge equalization system.

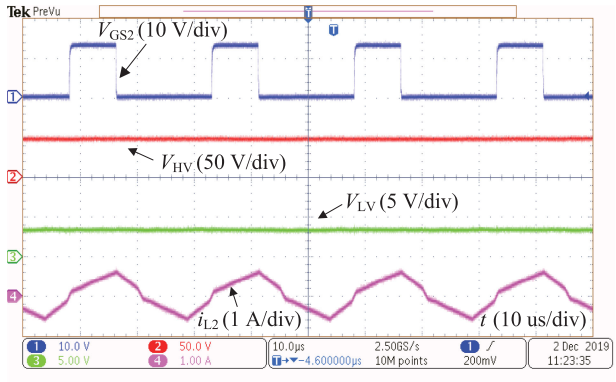

Fig. 17. Waveforms when an overcharged odd-numbered cell is equalized.

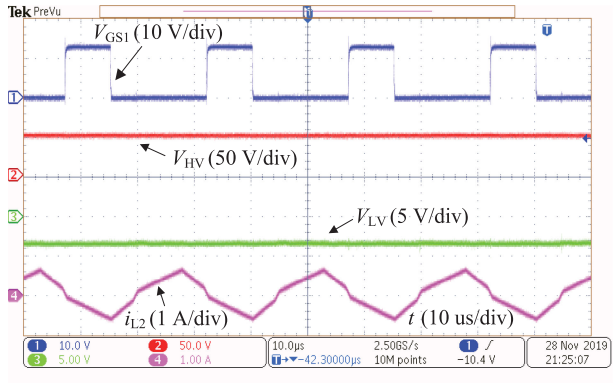

Fig. 18. Waveforms when an overcharged even-numbered cell is equalized.

sampling signals are in data communication with the microcontroller TMS320F28335. Since the number of PWM ports on the main controller is limited, when equalizing a battery string that contains more cells, the PWM port needs to be extended by the switch matrix gate driver EMB1428Q, and then an opt-coupler driver chip is connected to enhance the driving capability of the PWM signal.

When the charge equalization system operates, the DSP reads the voltage and current sampling values of each cell in real time to judge the working states of the cells and estimate their state of charge (SOC) values. The cells that need to be equalized are arranged according to the difference between their SOC and the average SOC of the battery string, and each cell is equalized according to the imbalance difference from large to small. When the SOC difference is greater than 2%, the overcharged single cell needs to release energy to the entire battery string. The maximum equalization discharge current is set to 3 A, and the converter works in boost mode. When the SOC difference is less than -2%, the entire battery string needs to release energy to the undercharged single cell. The maximum equalization charge current is set to 2 A, and the converter works in buck mode. In addition, overcharged cells are more susceptible to damage than undercharged cells, so the equalization priority of overcharged cells is higher than that of undercharged cells.

B. Experimental Results

To verify the equalization effect of the proposed equalizer, 13 series-connected lithium-ion cells are equalized, and the capacity of each cell is 3.5 Ah.

When equalizing an overcharged cell, the controller directly selects the corresponding switches in the switch array to connect the cell to the low-voltage side of the converter. The extra energy is released to the battery string by the converter working in boost mode. According to the experimental results, the conversion efficiency is approximately 84.3%. Figs. 17 and 18 show experimental waveforms for when odd-numbered and even-numbered cells are equalized. The oscilloscope channels represent the gate drive signals (V_{GS2}/V_{GS1}), low-voltage side voltage V_{LV}, high-voltage side voltage V_{HV} and inductance current i_{L2}, respectively. The polarities of the voltages on the low-voltage side (V_{LV}) of odd-numbered and even-numbered cells are different.

To simplify the analysis and correspond to the above theoretical analysis, the following also takes the equalization of odd-numbered cells as an example. According to the analysis shown in Fig. 19(a), the waveforms of V_{GS2}, V_{GS4}, and i_{L2} are consistent with the theoretical analysis, and the equalization discharge current is approximately 3 A. V_{Tr_L} and V_{Tr_H} in Fig. 19(b) represent the voltage waveforms on the low-voltage side and high-voltage side of transformer T_r, respectively. The relationship between the two voltages is in accordance with

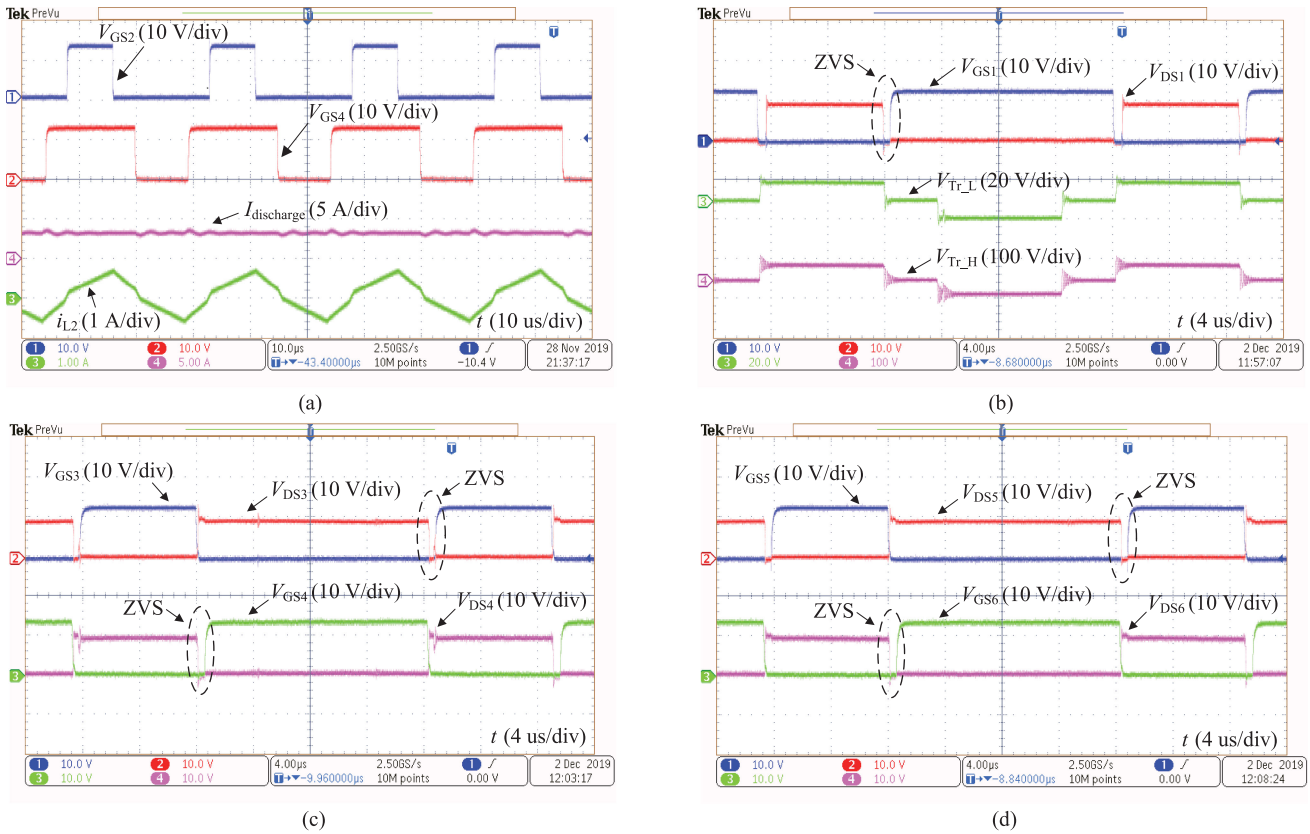

Fig. 19. Experimental waveforms of the proposed converter in boost mode. (a) V_{GS2}, V_{GS4}, i_{L2}, and $I_{discharge}$. (b) ZVS waveforms of S_1 and transformer voltage waveforms. (c) ZVS waveforms of S_3 and S_4. (d) ZVS waveforms of S_5 and S_6.

the transformer ratio of 1:4. Fig. 19(b) also shows the ZVS waveform of S_1, Fig. 19(c) shows the ZVS waveforms of S_3 and S_4, and Fig. 19(d) shows the ZVS waveforms of S_5 and S_6. According to the implementation principle of soft-switching in boost mode, inductor L_1 freewheels through its body diode before S_1 is turned on, and inductor L_2 freewheels through its body diode before S_4 and S_6 are turned on. Moreover, at the moment before S_1, S_4, and S_6 are turned on, inductor currents i_{L1} and i_{L2} are at the peak of each cycle. According to the conditions in (33), (34), and (35), L_1 and L_2 have sufficient energy to discharge the junction capacitors of S_1, S_4, and S_6. Therefore, switches S_1, S_4, and S_6 can realize ZVS in the full load range. In addition, according to the set parameters, the converter operates in CCM at full load. At this point, inductor L_2 freewheels through the body diode of S_3 in the positive half-cycle, which realizes ZVS of S_3. A similar work process occurs in the negative half-cycle, which achieves ZVS of S_5.

When equalizing an undercharged cell, the bidirectional converter operates in buck mode and releases energy from the battery string into the cell. According to the experimental results, the conversion efficiency is approximately 85.1%. Fig. 20 and 21 show the equalization experimental waveforms of odd-numbered and even-numbered cells, respectively. Similar to boost mode, only changing the switching sequence of several switches can equalize cells with different voltage polarities.

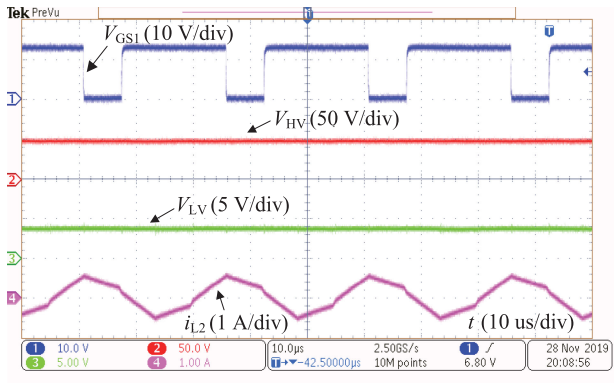

Fig. 20. Waveforms when an undercharged odd-numbered cell is equalized.

When the converter operates in buck mode, the equalization of odd-numbered cells is also analyzed as an example. According to Fig. 22(a), the waveforms of V_{GS1}, V_{GS7}, and i_{L2} are consistent with the theoretical analysis, and the equalized charge current is approximately 2 A. Because the value of inductor L_2 is larger, i_{L2} is close to a critical continuous state at full load. Fig. 22(b) shows the ZVS waveform of S_2, Fig. 22(c) shows the ZVS waveforms of S_3 and S_5, and Fig. 22(d) shows the ZVS waveforms of S_7 and S_8. In buck mode, L_1 freewheels through its body diode before S_2 is turned on, and L_2 freewheels through its body diode before

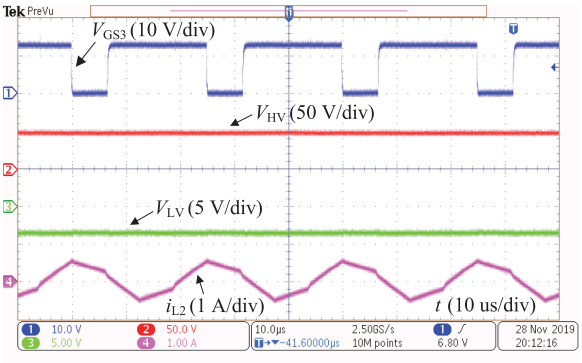

Fig. 21. Waveforms when an undercharged even-numbered cell is equalized.

S_3 and S_5 are turned on. Moreover, at the moment before S_2, S_3, and S_5 are turned on, inductor currents i_{L1} and i_{L2} are at the peak of each cycle. According to the conditions in (39), (40) and (41), inductors L_1 and L_2 have sufficient energy to discharge the junction capacitors of these three switches. Therefore, ZVS of switches S_2, S_3 and S_5 can be implemented in the full load range. In addition, according to the working principle of the converter in buck mode, current i_{L2} can work in CCM in the full load range, thus achieving ZVS of S_7 and S_8.

In the subsequent stage of equalization, the equalization current will be reduced to prevent over-charging or over-discharging of the cell. Figs. 23 and Fig. 24 are the experimental waveforms when the equalizing discharge current is 2.5 A and the equalizing charge current is 1 A, respectively. From Fig. 23(a) and (b), when $I_{\text{discharge}}$ is 2.5 A, current i_{L2} is close to the critical continuous state, and S_3 and S_5 can realize ZVS. Combined with Fig. 22(a), Fig. 24(a), and Fig. 24(b), when I_{charge} is reduced from 2 A to 1 A, current i_{L2} is not close to the critical continuous state. At this time, S_7 and S_8 can adequately implement ZVS.

To simulate a more serious unbalanced condition, before starting an equalization experiment, a cell was charged to states that exceed 10.5% of the average SOC value, and another cell was discharged to states below 6.8% with the average SOC value. According to the set equalization control principle, first, the overcharged cell will be equalized. The equalized SOC curve in Fig. 25 shows that the overcharged cell ($\Delta\text{SOC} = 10.5\%$) first releases energy to the battery string with a current of 3 A, and equalization is completed after 9 minutes. Second, the battery string releases energy to the undercharged cell ($\Delta\text{SOC} = -6.8\%$) with a current of 2 A, and the equalization is completed after 7.8 minutes.

It should be noted that in an actual system, equalization control is generally started at a later stage of battery charging. To focus on the performance of the equalizer, equalization in this experiment is carried out during an idle period of the battery string. When the difference value of the SOC is greater than 2%, the equalization control will be started; however, there is no such large SOC difference in an actual system, so the equalization time will be greatly reduced. In addition, the proposed topology has the ability to increase the equalization current. When the set equalization current is larger, the equalization time will be further reduced.

V. Comparison and Analysis

In this section, a quantitative and comprehensive comparison of different converters used in centralized charge equalization system is conducted and summarized. For a fair comparison, a virtual prototype of each equalizer has been designed for the same specification: the rated voltage of the single cell and the battery string are 3.7 V and 48.1 V, the maximum equalization discharge current is 3 A, the maximum equalization charge current is 2 A, the equalization current ripple coefficient α is 0.15, and the switching frequency is 40 kHz. To verify the design parameters of each virtual prototype and ensure their consistency with the original literatures, simulations have been carried out on PSIM 9.1.

A. Losses and Costs Comparison

The details of designed virtual prototypes have been listed in Table II. Based on this, the losses and costs of different centralized charge equalization systems are quantitatively analyzed, in which the losses model are referred in [22]–[24], and the costs calculation method are referred in [25], [26]. According to the numerical values of losses and costs, the performance of various equalizers will be comprehensively evaluated and analyzed.

The loss numerical values of various equalizers are listed in Table III. The quasi-resonant converter in [21] achieves the ZVS operation by quasi-resonant operation, which greatly reduces the switching loss. The converters presented in [16]–[20] can neither achieve soft-switching nor avoid the spike voltage caused by leakage inductance, which substantially affects the switching efficiency in boost mode. However, in buck mode, the converter in [18] can be soft-switched by active clamping, and the MOSFET of the converters in [16], [17] is located on the high-voltage side to ensure that the switching loss of these equalizers can be reduced. In boost mode and buck mode, the proposed converter can realize soft-switching of most MOSFETs, which can effectively reduce the total switching loss.

The conduction losses are mainly decided by the conduction current, number of switches, and on-state resistance. The total conduction loss of the equalizer is the sum of three kinds of switches: bidirectional switches, polarity switches and converter switches. Both the converter in [16], [17] and the converter in [21] have large current fluctuations, which cause an increase in the conduction loss. The equalization current of other converters is continuous, and their conduction loss will be reduced accordingly.

The transformer losses are split into the winding losses and core losses. In the case of the same core material, the larger is the volume and the greater is the current fluctuation, the greater is the transformer loss. The converters presented in [18]–[20] have a larger number of transformer turns. The converter in [16], [17] requires thicker litz wires due to the large current peak of the intermittent current. Therefore, the volume and loss of the transformers used for these equalizers are greatly increased. The proposed converter has a high voltage conversion ratio, and its transformer volume and turns are small, which can effectively reduce the transformer loss.

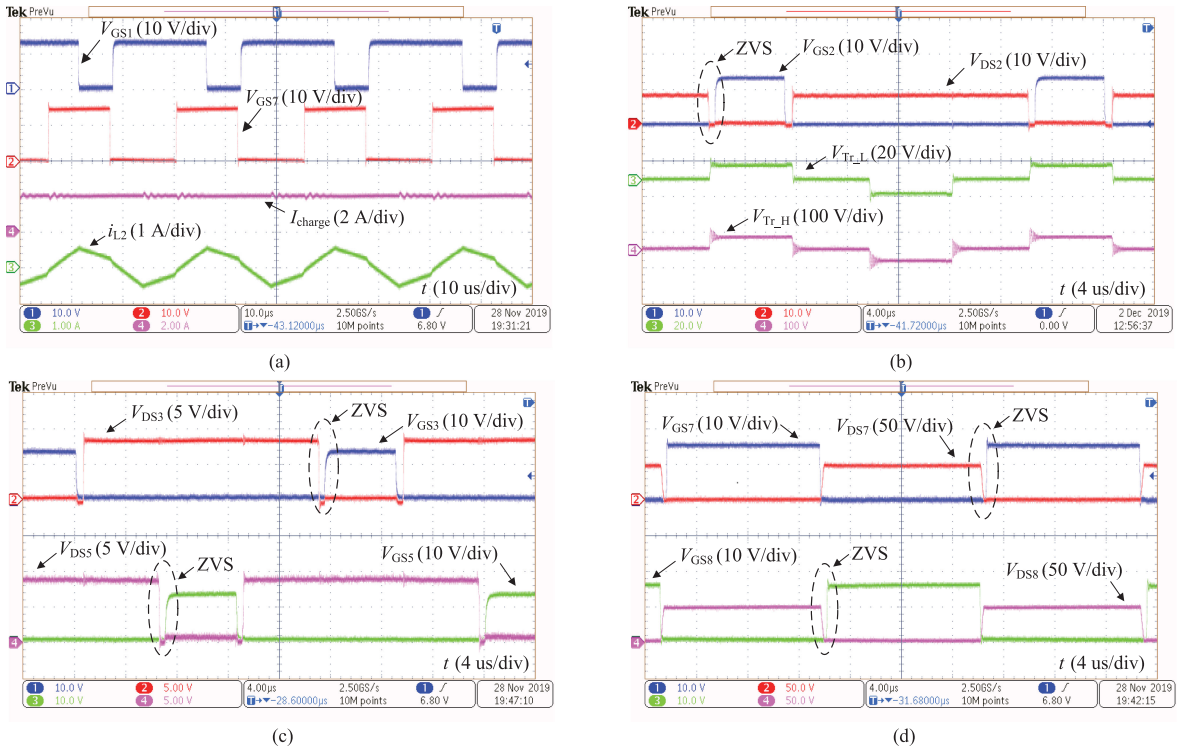

Fig. 22. Experimental waveforms of the proposed converter in buck mode. (a) V_{GS1}, V_{GS7}, i_{L2}, and I_{charge}. (b) ZVS waveforms of S_2 and transformer voltage waveforms. (c) ZVS waveforms of S_3 and S_5. (d) ZVS waveforms of S_7 and S_8.

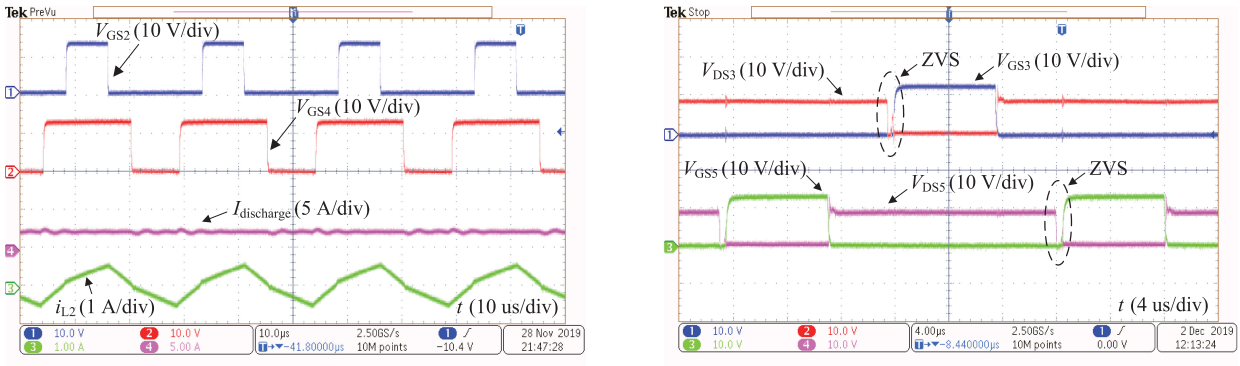

Fig. 23. Experimental waveforms with equalizing charge current of 2.5 A in the boost mode. (a) V_{GS2}, V_{GS4}, i_{L2}, $I_{discharge}$. (b) ZVS waveforms of S_3 and S_5.

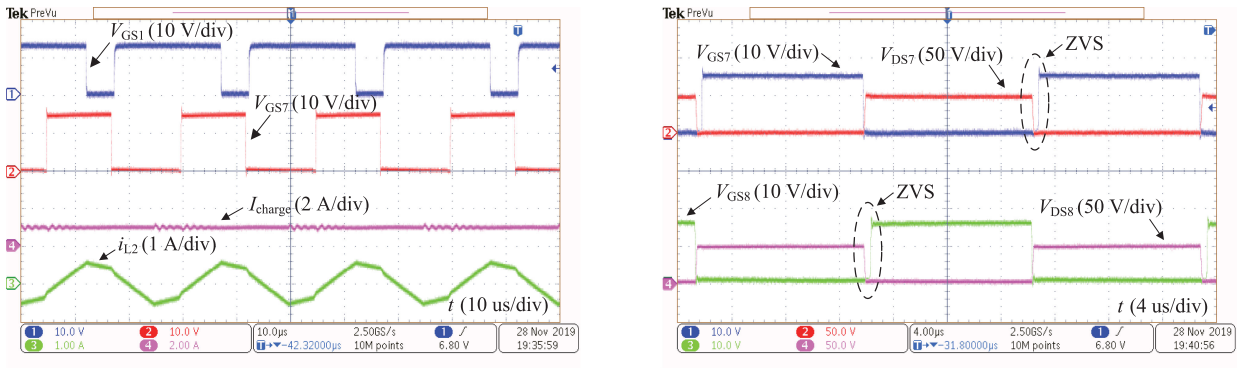

Fig. 24. Experimental waveforms with equalizing charge current of 1 A in the buck mode. (a) V_{GS1}, V_{GS7}, i_{L2}, and I_{charge}. (b) ZVS waveforms of S_7 and S_8.

TABLE II
COMPARISON OF THE DESIGN SPECIFICATIONS FOR CENTRALIZED CHARGE EQUALIZATION SYSTEMS CONSISTING OF 13 CELLS

Topology	Proposed equalizer	Quasi-resonant in [21]	Bidirectional forward in [18]	Bidirectional full-bridge in [19], [20]	Bidirectional flyback in [16], [17]
No. of switches	Convertor switches: 6×IRF1010Z, 2×IRF540Z Bidirectional switches: 28×IRF7862PbF	Convertor switches: 2×IRF1010Z, 2×IRF540Z Polarity switches: 4×IRF7862PbF Bidirectional switches: 28×IRF7862PbF	Convertor switches: 2×IRF1010Z, 2×IRF540Z Polarity switches: 4×IRF7862PbF Bidirectional switches: 28×IRF7862PbF	Convertor switches: 4×IRF1010Z, 4×IRF540Z Polarity switches: 4×IRF7862PbF Bidirectional switches: 28×IRF7862PbF	Convertor switches: 1×IRF1010Z, 1×IRF540 Bidirectional switches: 52×IRF7862PbF
Voltage stresses of switches	Primary: 15V Secondary: 55V	Primary: 35V Secondary: 80V	Primary: 15V Secondary: 80V	Primary: 5V Secondary: 60V	Primary: 15V Secondary: 90V
Inductor (sendust toroid core & litz wire)	a. Core:MS-090125-2 Winding: #18AWG, 33 turns (100μH) b. Core:MS-106125-2 Winding: #20AWG, 37 turns (210μH)	a. Core:MS-068060-2 Winding: #12AWG, 8 turns (2.7μH) b. Core:MS-068060-2 Winding: #18AWG, 26 turns (30μH)	Core:MS-106125-2 Winding: #18AWG, 35 turns (200μH)	Core:MS-090060-2 Winding: #18AWG, 37 turns (60μH)	Nil
Transformer (planar PQ core & copper foil winding)	Core: PQ2620-PC44 primary: #18AWG, 5 turns Secondary: #22AWG, 20 turns	Core: PQ2625-PC44 primary: #12AWG, 5 turns Secondary: #20AWG, 30 turns	Core: PQ3220-PC44 primary: #18AWG, 8 turns Secondary: #22AWG, 56 turns	Core: PQ3220-PC44 primary: #18AWG, 8 turns Secondary: #22AWG, 64 turns	Core: PQ3220-PC44×2 primary: #12AWG, 5 turns Secondary: #20AWG, 35 turns
	1:4	1:6	1:7	1:8	1:7, (7:1)
Capacitor	16V AC / 100μF; 35V DC / 100μF; 100V DC / 100μF; 100V DC / 100μF	16V DC / 100μF; 16V DC / 100μF; 100V AC / 220nF; 100V AC / 10μF; 100V DC / 100μF	16V DC / 100μF; 100V AC / 47nF; 100V DC / 100μF	16V DC / 100μF; 100V DC / 100μF	16V DC / 100μF; 100V DC / 100μF
Diodes	Nil	a. STPS40L45CG; b. STPS40L45CG	Nil	Nil	a. S1D; b. V12P10

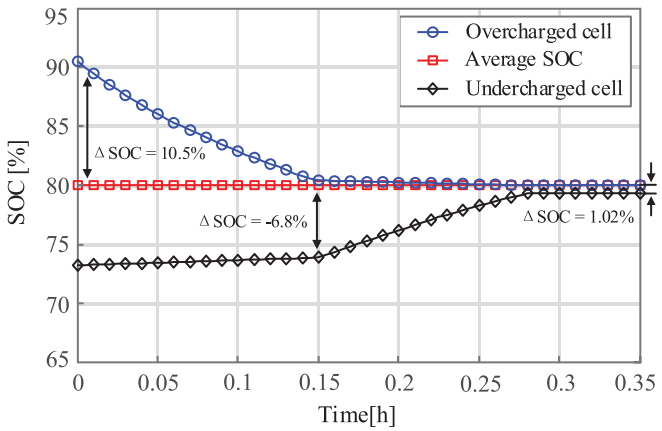

Fig. 25. SOC-based lithium-ion battery cell equalization results.

The inductor losses are also divided into the winding losses and core losses. Although the inductance value of the quasi-resonant converter in [21] is small, the large current ripple caused by the resonant operation will cause a large core loss. In [18], the filtering inductor of the converter is located on the low-voltage side, and the inductance value is large, which will cause a large winding loss. The proposed topology has two inductors, but the inductor with a large inductance value is located on the high-voltage side and the conduction current is small. In addition, the integrated cascade structure makes the high-voltage and low-voltage side currents work in a continuous state with small fluctuations, so that the inductor loss is not too large.

The bidirectional flyback converter in [16], [17] and the quasi-resonant converter in [21] have diode losses. In particular, the diode located in the low-voltage side of the bidirectional flyback converter in buck mode will cause a substantial number of losses.

According to the cost values of the various equalizers listed in Table III, the costs and even the size/weight of the equalizer mainly depends on the number of components, including MOSFETs, driver ICs, inductors, capacitors, diodes, and transformers. Specifically, the quantitative costs comparison can be achieved by calculating the total price of each equalizer, and the approximate comparison of the size and weight of the equalizer can be achieved according to the number and volume of components.

B. Performance Comparison

A comprehensive comparison of different converters used in centralized charge equalization systems is also conducted and summarized in Table III. This evaluation focuses on the impact

TABLE III
PERFORMANCE COMPARISON OF DIFFERENT CENTRALIZED CHARGE EQUALIZATION SYSTEMS

Topology		Proposed equalizer	Quasi-resonant in [21]	Bidirectional forward in [18]	Bidirectional full-bridge in [19], [20]	Bidirectional flyback in [16],[17]
Losses (W) in Boost mode	Switching	0.175	0.031	0.289	0.217	0.391
	Conduction	0.226	0.383	0.189	0.229	0.381
	Transformer	0.461	0.651	1.057	1.158	1.083
	Inductor	0.864	0.527	0.484	0.268	0
	Diode	0	0.263	0	0	0.249
Total		**1.726**	**1.855**	**2.019**	**1.872**	**2.104**
Losses (W) in Buck mode	Switching	0.187	0.041	0.041	0.204	0.092
	Conduction	0.095	0.185	0.151	0.102	0.101
	Transformer	0.368	0.537	0.883	0.941	0.898
	Inductor	0.629	0.325	0.269	0.121	0
	Diode	0	0.234	0	0	0.807
Total		**1.279**	**1.322**	**1.344**	**1.368**	**1.898**
Costs ($)	MOSFETs	72	72	72	80	108
	Gate driver ICs	33	33	33	39	42
	Transformer	5	5	5	5	10
	Inductor	8	8	4	4	0
	Capacitor	6	7.5	4.5	3	3
	Diode	0	4	0	0	4
Total		**124**	**129.5**	**118.5**	**131**	**167**
Voltage spike caused by leakage inductance		No	No	Yes	Yes	Yes
Costs		Low	Low	Low	Medium	High
Size / weight		Low	Medium	Low	Medium	High
Impact on state-of-health (SOH)		Excellent	Good	Excellent	Excellent	Good
Extendibility		Excellent	Good	Good	Good	Satisfactory
Conversion efficiency		High	High	Medium	Medium	Low
Control complexity		Good	Good	Excellent	Satisfactory	Satisfactory

Component cost per unit ($): MOSFET (2), Gate driver ICs (1.5), Transformer (5), Inductor (4), Capacitor (1.5), Diode (2) [25], [26].

on state-of-health (SOH), extendibility, equalization speed, conversion efficiency, and control complexity [27].

The first concern is the impact on the SOH of the battery. The proposed converter, bidirectional forward converter in [18] and bidirectional full-bridge converter presented in [19] and [20] enable the equalization current to work in a continuous current state with minimal impact on battery health. However, the equalization current of other converters works in a discontinuous current state, and large current peaks may cause potential damage to the battery.

Second, the extendibility of different equalizers is evaluated. The equalizer presented in [16] and [17] has a large number of bidirectional switches, which is not conducive to the expansion of the number of cells. Several other equalizers have greatly reduced the number of bidirectional switches by setting polarity switches, which improves the extendibility of the system. However, these two kinds of switches must cooperate with each other, and poor coordination will affect the efficiency of the system and even cause short circuits between cells. Compared with traditional architectures, the proposed new converter effectively reduces the numbers of bidirectional switches and polarity switches, greatly improving the extendibility and reliability of the centralized charge equalization system.

Unlike the non-centralized methods, the equalization speed of the centralized equalizer can be adjusted by setting the working current of the converter. The proposed converter improves the equalization voltage gap through the integrated cascade structure, which can significantly increase the equalization speed by increasing the equalization current.

The efficiency of the main converter and switch array are the two main factors that affect the equalizer efficiency. The proposed converter integrates the polarity switches, which are originally located in the switch array with the bidirectional dc–dc converter to realize a high voltage conversion ratio, continuous equalization current, and soft-switching of most switches. Thus, the transformer loss, conduction loss and switching loss of the equalizer are effectively reduced. At the same time, it also avoids the coordination problem of bidirectional switches and polarity

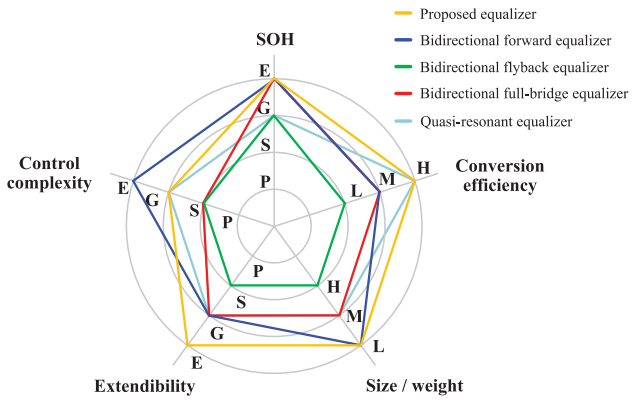

Fig. 26. Comparison of different centralized charge equalizers.

switches that exist in the traditional centralized equalization architecture, which can effectively reduce the efficiency loss caused by the switch array to improve the efficiency of the entire equalization system. The quantitative analysis and comparison of the losses verify that the proposed equalizer has significant advantages in terms of the conversion efficiency.

The final focus is on control complexity. The equalizer presented in [16] and [17] has a large number of bidirectional switches, which leads to increases in the number of driving circuits and control complexity. Similarly, the bidirectional full-bridge converter presented in [19] and [20] also has many switches, and the control is relatively complicated. The equalizer presented in [18] has a simple control system, but the driving capability of the control chip is very small, and an additional driving circuit needs to be provided to increase the driving capability. Fig. 3 and 5 show that the proposed converter has only one control variable in boost mode or buck mode, which greatly simplifies the complexity of the control system. In addition, the coordination problem between bidirectional switches and polarity switches is avoided, and the control performance of the entire equalization system is improved.

To make an intuitive comparison of the performance of several equalizers, a performance comparison diagram, as shown in Fig. 26, is drawn based on the above comparison results. The comparison results further show the superiorities of the proposed equalizer in terms of SOH, extendibility, size/weight and conversion efficiency.

VI. Conclusion

An isolated bidirectional dc–dc converter with an integrated cascade structure is proposed for a centralized charge equalization system. The operation principles, theoretical derivations, equalization experiments, and comparative studies are presented. The integrated cascade structure enables the proposed equalizer to have higher integration and higher reliability, and this converter solves the problem of achieving equalization with low cost and small volume for a long series-connected battery string. On the one hand, the experimental results of 13-cell lithium-ion battery string show that the proposed equalizer has excellent equalization performance (e.g., high voltage conversion ratio, continuous adjustable equalization current, ZVS of switches and good equalization speed). On the other hand, a quantitative and comprehensive comparison validate the superiorities of the proposed equalizer and demonstrate obvious performance enhancement over the conventional method.

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