Accurate Analytical Switching-ON Loss Model of SiC MOSFET Considering Dynamic Transfer Characteristic and Q_{gd}

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***Abstract*—Silicon carbide (SiC) devices enable more compact and efficient design of applications such as traction inverters and rectifiers. With miniaturization of power electronics, the volume and weight of heatsink or cold plate occupies a significant portion. So, thermal design, especially power loss evaluation, is crucial to the whole system. Analytical switching model based on datasheet parameters is usually adopted to evaluate devices' switching loss due to its convenience. However, when applied on SiC metal-oxide-semiconductor field-effect-transistors (MOSFETs), turn-ON waveforms of conventional analytical switching model show obvious discrepancy from experiments at both current rising and voltage falling stages. The transfer and capacitance characteristics from datasheet are responsible for that. Due to short channel effect and drain-induced barrier lowering, transfer characteristic during turn on period varies with different drain-to-source voltage v_{ds}. C_{gd} during actual turn on period is also different from that on the datasheet. So, considering the actual turn on process, dynamic transfer characteristic and Q_{gd} are proposed and measured in this paper. After these modifications, switching-on waveforms of the analytical switching loss model match the experiments very well, and error of the estimated loss is less than 5%.**

***Index Terms*—Analytical model, dynamic transfer characteristic, MOSFET, silicon carbide, Qgd.**

I. Introduction

As a kind of wide bandgap (WBG) power devices, silicon carbide (SiC) metal-oxide-semiconductor field-effect-transistor (MOSFET) is a promising alternative to silicon (Si) power devices [1], [2]. With superior material properties, SiC MOSFET switches faster, has lower switching loss, higher thermal conductivity and higher working temperature ability. So, switching frequency can be elevated to improve the power density, especially for those having strict requirements for volume and weight, e.g., electrical vehicle (EV) on-board charger (OBC) and traction drive systems (TDS) [3], [4]. A 100 kW integrated design with 100 kW/L at $2.7/kW for EV inverter is targeted by The United States (U.S.) Department of Energy (DOE) for 2025 [5]. As power density increases, thermal design will occupy 16%∼25% the total mass or volume of the whole implementation [6], [7] and faces more challenges. Design and molding of the heatsink or cold plate are time and cost consuming [8]. So, accurate devices' loss evaluation is of vital importance. Conduction loss of power devices can be calculated easily, so the key point falls at the accurate prediction of switching loss.

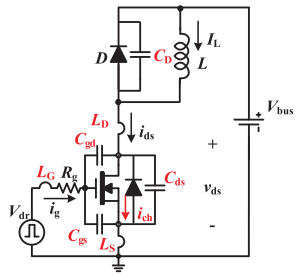

Fig. 1. Analytical switching loss model considering parasitic inductances and nonlinear characteristics.

Analytical switching loss model (also called mathematical model) is convenient and easy for designers to evaluate devices' switching performance. It is based on information from datasheet and adopts a series of equations to draw closed-form solutions for the circuit variables. The typical piecewise linear switching loss model with clamped inductive load for the power MOSFET is well-known for its simplicity [9], [10]. However, without consideration of circuit parasitic inductances and nonlinear characteristics of devices' parasitic capacitances, results of the piecewise linear switching loss model do not match experiment results very well, especially for high-speed switching and high frequency situations [11]. So, various literatures investigate the influence of parasitic inductances and nonlinear characteristics to improve the model, and apply it on Si low-voltage [11], [12] and high-voltage [13], [14] MOSFETs, gallium nitride (GaN) high-electron-mobility-transistors (HEMTs) [15], [16], and SiC MOSFETs [17]–[21]. In addition, considering the displacement current caused by the output capacitance C_{oss} during switching transitions, the channel current i_{ch} should be treated separately from the drain-to-source current i_{ds} [22]. So, a more reasonable and compact analytical switching loss model is fully established in Fig. 1, where L_S, L_G, L_D, and C_{gs}, C_{gd}, C_{ds} are the lumped parasitic inductances and capacitances, respectively. V_{bus}, v_{ds},

Manuscript received November 15, 2019; revised February 9, 2020; accepted April 8, 2020. Date of publication April 19, 2020; date of current version July 20, 2020. This work was supported in part by the National Natural Science Foundation of China under Grant 51877191, and in part by the Zhejiang Natural Science Outstanding Young Scholar Foundation LR18070001. Recommended for publication by Associate Editor D. G. Lamar. *(Corresponding author: Xinke Wu.)*

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Digital Object Identifier 10.1109/TPEL.2020.2988899

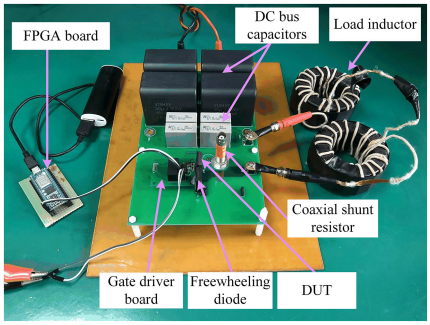


Fig. 2. Double pulse test platform.

$V_{\rm dr}$, $I_{\rm L}$, and $R_{\rm g}$ are the bus voltage, drain-to-source voltage, gate driving voltage, load current, and gate resistance. D represents the ideal freewheeling diode with the load inductor L in parallel. Parasitic capacitances of the freewheeling diode and the load inductor are integrated as a single value ($C_{\rm D}$ in Fig. 1) for the compactness of this model.

Nonetheless, when applied on SiC MOSFET, parameters from current datasheet may not be adequate for the analytical switching loss model. At first, conventional analytical switching model based on datasheet parameters for SiC MOSFETs is established according to previous publications [17]–[22]. Parasitic inductances, nonlinearity of both SiC transfer and parasitic capacitances are considered. However, compared to the experiments, the modeled switching-on waveforms show obvious discrepancies at both current rising and voltage falling stages.

So, insights of the current rising and voltage falling stages are provided. Analysis shows the transfer characteristic of SiC MOSFET varies under different $v_{\rm ds}$, which is caused by the short channel effect and drain-induced barrier lowering (DIBL) [23], [24]. This causes the inaccurate evaluation of $i_{\rm ch}$ and discrepancy at current rising stage. As for the voltage falling stage, the reverse transfer capacitance $C_{\rm rss}$ (namely $C_{\rm gd}$) from the capacitance verses $v_{\rm ds}$ (C-V) curve cannot be applied into the analytical switching loss model directly. The dynamic gate-to-drain charge $Q_{\rm gd}$ should be characterized for the model to derive a more accurate result.

Measurement methods of the dynamic transfer and $C_{\rm gd}$ characteristics are proposed. After adopting the modified characteristics in the analytical switching loss model, the predicted waveforms match the experiment results very well, and a quite accurate evaluation of SiC MOSFET's turn on loss can be done. Since turn off loss only contributes a small part of the total switching loss [25], [26], and even can be eliminated [27], only turn on loss is considered in this paper.

II. Inaccuracy of Conventional SiC MOSFET Analytical Switching Loss Model

At first, a double pulse test (DPT) platform is established to evaluate switching performance of SiC MOSFET.

A. Double Pulse Test Evaluation Platform

Fig. 2 shows the DPT platform. DC bus capacitors, device under test (DUT), freewheeling diode, and coaxial shunt resistor are placed on the main board, while the gate driver circuit is placed on a daughter board. A field programmable gate array (FPGA) board with control card (10M02SCM153) from Intel MAX 10 series is used as the generator of double pulse signals. Table I gives the main circuit parameters. A 1.2-kV SiC MOSFET (C2M0080120D [28]) and a 1.2-kV SiC Schottky diode (IDW20G120C5B [29]) are adopted as DUT and freewheeling diode, respectively. This SiC MOSFET adopts conventional packaging of TO-247, which is still widely used by many manufactories. This packaging introduces common source inductance $L_{\rm S}$, shared by power current loop and gate driving loop as shown in Fig. 1. $L_{\rm S}$ has a negative feedback on gate driving loop, slowing switching transients. Some new generation devices with Kelvin terminal would effectively eliminate $L_{\rm S}$, and much better switching performances can be obtained. If devices with Kelvin terminal are adopted, the proposed model in Fig. 1 can also be used with $L_{\rm S}$ set as 0, and it can be considered as a special case. In order to have a general understanding of the switching process, Devices with TO-247 packaging is used here.

TABLE I
Circuit Parameters

Parameters	Value
SiC MOSFET	C2M0080120D
SiC Diode	IDW20G120C5B
$V_{\rm bus}$	800 V
Load Inductor L	148 μH
$L_{\rm loop}$, $L_{\rm G}$, $L_{\rm S}$	16.4 nH, 28.6 nH, 2.8 nH
$V_{\rm dr}$ ($V_{\rm EE}$, $V_{\rm GG}$)	-4~20 V
$R_{\rm g}$ (Internal + External)	14.6 Ω (4.6 Ω+10 Ω)

As shown in Fig. 2, parasitic capacitance of the load inductor is minimized by sparse windings around the magnetic core and measured by the Model 200 Analog Network Analyzer. The value is about 19 pF, which is much less than that (about 100 pF) of the freewheeling diode. The printed circuit board (PCB) with component models are imported into the finite element analysis tool, Ansys Q3D [30]. Corresponding current loop can be selected and current excitation is applied to simulate the desired parasitic inductance. As shown in Fig. 3, $L_{\rm loop}$ (lumped power loop inductance, $L_{\rm D}+L_{\rm S}$), $L_{\rm G}$, and $L_{\rm S}$ extractions are done and marked. These values are also listed in Table I.

Usually, devices' transfer and C-V curves are extracted from datasheets. In order to be more accurate, characteristics of DUT are measured by curve tracer Keysight B1505A and adopted in the model. Multi-value approximation methods [18], [20], [21] are adopted to deal with the nonlinear characteristics.

B. Analysis of Turn-On Process

Then, turn-ON process is analyzed. It can be divided into four stages. The qualitative waveforms of corresponding parameters in Fig. 1 are shown in Fig. 4.

Stage 1: Turn-ON delay (t_0~t_1)

At t_0, gate driving voltage $V_{\rm dr}$ jumps from $V_{\rm EE}$ to $V_{\rm GG}$, and the input capacitance $C_{\rm iss}$ starts to be charged. The DUT keeps off-state until $v_{\rm gs}$ reaches $V_{\rm th}$. So, device's current remains zero

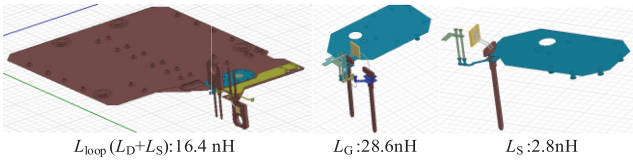


Fig. 3. Parasitic inductances extraction by Ansys Q3D.

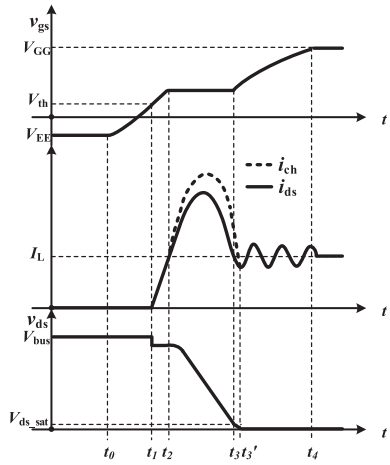


Fig. 4. Qualitative turn-ON waveforms.

and $v_{\rm ds}$ equals $V_{\rm bus}$. Equations of this stage are shown as

$$V_{\rm GG} = v_{\rm gs}(t) + R_{\rm g} i_{\rm g}(t) + (L_{\rm G} + L_{\rm S}) \frac{{\rm d}i_{\rm g}(t)}{{\rm d}t} + L_{\rm S} \frac{{\rm d}i_{\rm ds}(t)}{{\rm d}t} \tag{1}$$

$$i_{\rm g}(t) = C_{\rm iss} \frac{{\rm d}v_{\rm gs}(t)}{{\rm d}t} \tag{2}$$

Stage 2: Current rising (t_1~t_2)

When $v_{\rm gs}$ reaches $V_{\rm th}$ at t_1, the device starts conducting current. $I_{\rm L}$ is commutating from the freewheeling diode to the MOSFET. $v_{\rm ds}$ is clamped to $V_{\rm bus}$ by the freewheeling diode and keeps almost constant in this stage. So, the displacement current of $C_{\rm oss}$ is ignorable, and $i_{\rm ds}$ equals $i_{\rm ch}$. In conventional model, the relationship between $i_{\rm ds}$ (namely $i_{\rm ch}$) and $v_{\rm gs}$ is shown as the red solid line in Fig. 5. In order to show the nonlinearity of the transfer characteristic, fitting function (3) is adopted

$$i_{\rm ch}(t) = i_{\rm ds}(t) = f(v_{\rm gs}) = K(v_{\rm gs}(t) - V_{\rm th})^P \tag{3}$$

where $f(v_{\rm gs})$ represents function of the fitting curve, and K, $V_{\rm th}$, P are corresponding parameters. The fitting curve is also shown as the red dash-dot line in Fig. 5, which coincides with original curve accurately. This stage ends when $I_{\rm L}$ is totally transferred to the MOSFET, and the freewheeling diode begins to block voltage. If the freewheeling diode is the body diode of a MOSFET, then the reverse recovery should also be considered [19].

Stage 3: Voltage falling (t_2~t_3)

From t_2, the freewheeling diode begins to block voltage. Most of gate current $i_{\rm g}$ discharges $C_{\rm gd}$, and $v_{\rm ds}$ starts to fall simultaneously. So, the gate current should be represented as (4). The discharging current of $C_{\rm oss}$ should also be considered

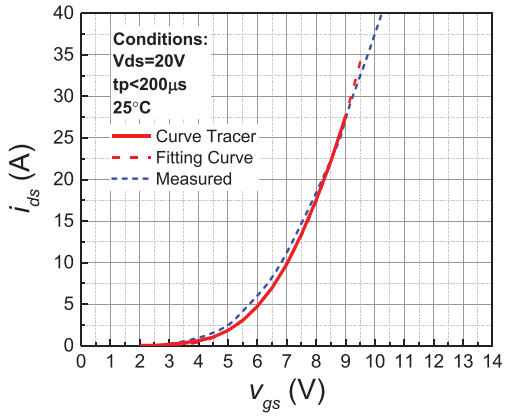


Fig. 5. Transfer characteristic of SiC MOSFET (C2M0080120D).

TABLE II
PARAMETERS OF THE DOUBLE PULSE TEST PLATFORM

Components	Vendor/Type	Spec.
Film Capacitors	Vishay	900V/50μF × 4
Film Capacitors	KEMET	1000V/0.47μF × 4
Ceramic Capacitors	MLCC	1000V/0.12μF × 2
Coaxial Shunt Resistor	T&M SSDN-015	15.013 mΩ
Low Voltage Probe	RIGOL RP3500A	350 MHz
High Voltage Probe	RIGOL RP1300H	300 MHz
Oscilloscope	RIGOL DS4034	350 MHz
Power Supply	Chroma 62150H-1000	1000V/15A
Signal Generator	Intel MAX® 10 FPGA	10M02SCM153

during the stage. Indicating different $i_{\rm ch}$ from $i_{\rm ds}$, as shown in (5)

$$i_{\rm g}(t) = C_{\rm iss} \frac{{\rm d}v_{\rm gs}(t)}{{\rm d}t} - C_{\rm gd} \frac{{\rm d}v_{\rm ds}(t)}{{\rm d}t} \tag{4}$$

$$i_{\rm ds}(t) = i_{\rm ch}(t) + C_{\rm oss} \frac{{\rm d}v_{\rm ds}(t)}{{\rm d}t} \tag{5}$$

This stage ends when $v_{\rm ds}$ falls to the saturation voltage $V_{\rm ds\_sat}$, namely $v_{\rm ds}$ equals $v_{\rm gs}$ at t_3.

Stage 4: Remaining period (t_3~t_4)

After t_3, $v_{\rm ds}$ continues dropping to the conduction voltage $v_{\rm ds\_on}$, and $i_{\rm ch}$ becomes equal to $i_{\rm ds}$ at t_3'. SiC MOSFET is fully turned ON, and the gate current continues to charge the input capacitance $C_{\rm iss}$ to $V_{\rm GG}$. $i_{\rm ds}$ will resonant due to the existing of power loop inductance and freewheeling diode's parasitic capacitance. When $v_{\rm gs}$ rises to $V_{\rm GG}$ and the ringing of $i_{\rm ds}$ is fully damped, the whole turn on process ends.

More detailed equations of the analytical model during each stage and their derivations are a little complicated and may be dull for readers, so they are introduced in the Appendix.

C. Turn On Waveforms Comparison

Corresponding parameters of the DPT platform and measuring instruments are shown in Table II. Turn on waveforms from the experiment and conventional analytical switching loss model at 800 V/25 A are shown and compared in Fig. 6. Obvious discrepancies can be observed at both current rising and voltage

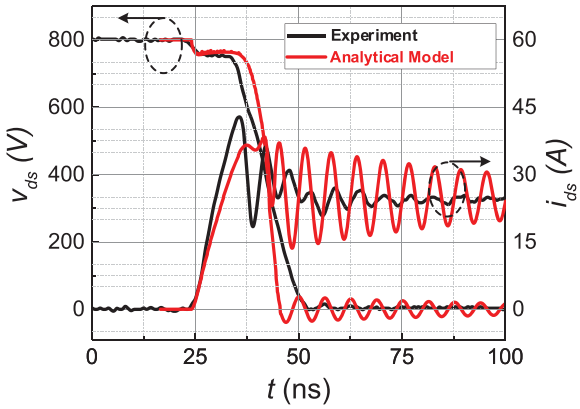


Fig. 6. Comparison of turn on waveforms between the experiment and conventional analytical switching loss model.

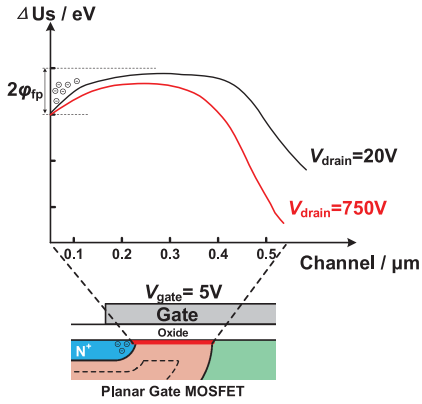


Fig. 7. Illustration of short channel effect and drain-induced barrier lowering (DIBL).

falling stages. i_{ds} of the conventional model rises slower and v_{ds} falls faster than the experiment results. So, loss evaluation is overestimated at current rising stage and underestimated at voltage falling stage. Total switching loss evaluation may be close to experiment results, but it is not reasonable. This indicates some parts of the analytical switching loss model needs to be improved or corrected. So, insights into the current rising and voltage falling stages are required.

III. Insight Into the Current Rising Stage

According to the analysis in Section II, i_{ds} equals i_{ch} during the current rising stage. At this stage, MOSFET is in saturation region and i_{ds} changes according to v_{gs}. Relationship between them can usually be described by the transfer characteristic, shown in Fig. 5 and (3).

However, it is noticed that during the current rising stage, v_{ds} keeps at a high voltage (around 750 V), while the transfer characteristic used in the analytical model is measured at a fixed 20 V v_{ds}, as shown in Fig. 5. Actually, transfer curve of SiC MOSFET changes with higher v_{ds}, which is quite different from that on the datasheet. This is caused by device's short channel effect and drain-induced barrier lowering (DIBL) [23], [24]. This phenomenon is briefly illustrated in Fig. 7 by the surface potential (ΔU_S) plots along the channel of the SiC MOSFET. Channel current is controlled by electron emission over a potential barrier at the source. When the channel length is short with a fixed gate voltage, the potential barrier will be lowered by the increased drain voltage, which means channel current will increase.

However, curve tracer cannot measure the transfer characteristic under high v_{ds} such as hundreds of volts. A single pulse test circuit according to [31] is proposed for the measurement of SiC MOSFET transfer characteristics under different v_{ds}, as shown in Fig. 8(a). During the measurement, junction temperature T_j is specified, and V_{bus} and V_{dr} are adjusted to specified values. Then, a single pulse on the gate is applied. i_{ds} is measured by a shunt resistor (15.013 mΩ) when the current is stable. Fig. 8(b) gives the typical measured waveforms at 100 V v_{ds} and 11.5 V v_{gs}. Transfer curve with v_{ds} fixed at 20 V is measured and plotted

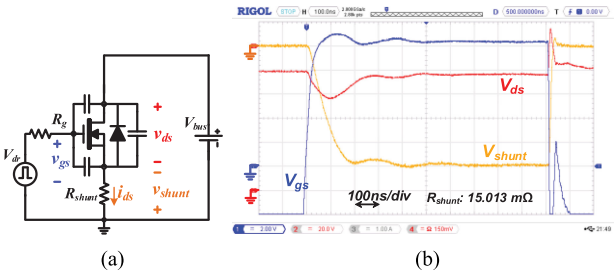


Fig. 8. Transfer characteristic measurement. (a) Circuit. (b) Typical waveforms (v_{ds}: 100 V; v_{gs}: 11.5 V).

as the blue dash line in Fig. 5. The measured curve is very close to that from curve tracer, which proves the accuracy of the measuring circuit. Then v_{ds} is adjusted to higher value and a series of transfer curves are measured.

Fig. 9(a) shows the measured i_{ds} under various v_{ds} when v_{gs} is fixed at 7.1 V. It is obvious that i_{ds} rises when the applied v_{ds} increases. The measured results coincide with the analysis about DIBL. Transfer curves under different v_{ds} is shown in Fig. 9(b). Due to the existing parasitic inductances of the measurement setup, ringing occurs on the measured current. So, the current should be measured when it is stable. However, the width of the pulse should not be too long because of devices' self-heating problem. As shown in Fig. 9(a), 1 μs is chosen. The current become almost stable at the end of the pulse, and average value during the period inside the dash line box is derived as the measured current for each curve. The junction temperature of DUT can be calculated by the transient thermal impedance curve from datasheet and the transient power applied on DUT. The calculated maximum temperature rise in Fig. 9(a) is around 16 °C at 500 V/25 A, which is tolerable and will not induce serious impact on the measurements.

Then, (3) is applied for different transfer curves in Fig. 9(b), and corresponding parameters (K, V_{th}, and P) with relation to v_{ds} are derived to obtain the desired transfer function under a certain v_{ds}. The calibrated transfer characteristic of SiC MOSFET is applied in the analytical model, and waveforms comparison is shown in Fig. 10. It shows that the current rising stage from

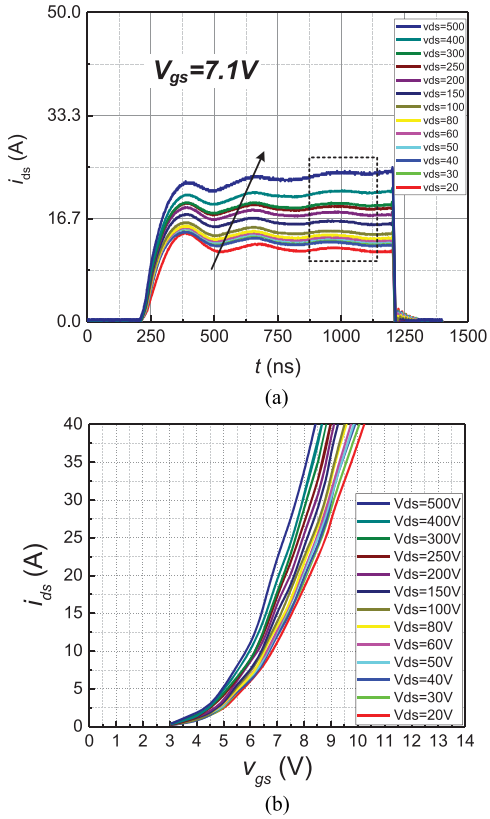


Fig. 9. Measurement results under various $v_{\rm ds}$. (a) $i_{\rm ds}$ when $v_{\rm gs} = 7.1$ V. (b) Transfer curves ($v_{\rm ds}$: 20–500 V).

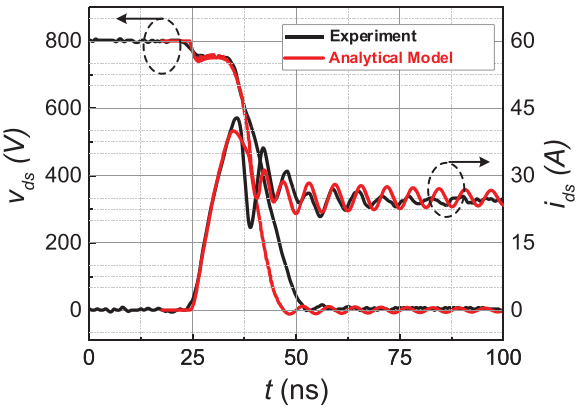


Fig. 10. Comparison of turn on waveforms between the experiment and loss model with dynamic transfer characteristic.

analytical switching loss model matches the experiment result perfectly. Besides of the current rising stage, dynamic change of transfer characteristic during voltage falling stage is also considered in the analytical switching loss model.

However, the voltage falling stage of the analytical switching loss model still do not coincide with the experiment well.

IV. Insight Into the Voltage Falling Stage

A. In-Depth Analysis of the Voltage Falling Stage

During the voltage falling stage, $v_{\rm gs}$ has reached the miller plateau voltage, and most of $i_{\rm g}$ flows through $C_{\rm gd}$. So, $C_{\rm gd}$ is

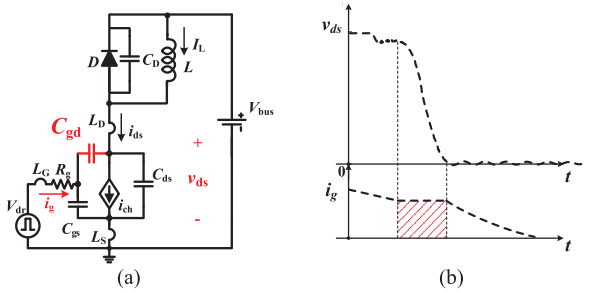


Fig. 11. (a) Equivalent circuit of the voltage falling stage. (b) Waveforms of key parameters.

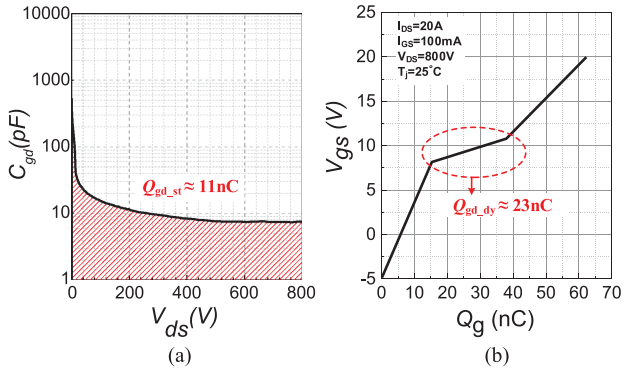


Fig. 12. Parameters from datasheet of SiC MOSFET (C2M0080120D). (a) Static $Q_{\rm gd}$ integrated from C–V curve. (b) Gate charge characteristic.

discharged and $v_{\rm ds}$ falls quickly, as shown in Fig. 11(a). The charge during this period can be defined as $Q_{\rm gd}$, highlighted as the shadow area in Fig. 11(b). Since $C_{\rm gd}$ is extracted from the static C-V characteristics, an integration along $v_{\rm ds}$ can be done to derive $Q_{\rm gd\_st}$, which is around 11 nC in Fig. 12(a). Another $Q_{\rm gd}$ can be found from the gate charge characteristic of device's datasheet, as shown in Fig. 12(b). According to [31], this value is measured during a dynamic process of SiC MOSFET, so it is named as $Q_{\rm gd\_dy}$, which is about 23 nC, and much larger than $Q_{\rm gd\_st}$. Considering the contradiction, in-depth analysis about detailed measurements of these two values are done.

A simplified measurement circuit of the $C_{\rm gd}$ is depicted in Fig. 13(a) [31]. During the measurement, junction temperature $T_{\rm j}$ is specified, and a constant $V_{\rm DD}$ is applied on the drain terminal of DUT. A constant $v_{\rm gs}$ (usually zero volt) is also applied, which means a closed channel. Then a high frequency small measuring signal (usually 1 megahertz, tens of millivolts) is applied on $C_{\rm gd}$ through C_1 and C_2. C_1, C_2 are adopted here to separate dc voltage and their values are much larger than $C_{\rm gd}$, presenting short circuit for the measuring signal. Different capacitances under various drain voltage are measured and plotted to derive the C-V curve. Fig. 13(b) shows the test current $i_{\rm gd}$ flowing through $C_{\rm gd}$ (consisting of the oxide capacitance $C_{\rm gd\_1}$ and the depletion capacitance $C_{\rm gd\_2}$ in series) inside SiC MOSFET.

The simplified measurement circuit of the gate charge characteristic is shown in Fig. 13(c). $V_{\rm DD}$ and a resistor R_1 is placed in series with the DUT. A constant gate current $I_{\rm GG}$ charges $v_{\rm gs}$

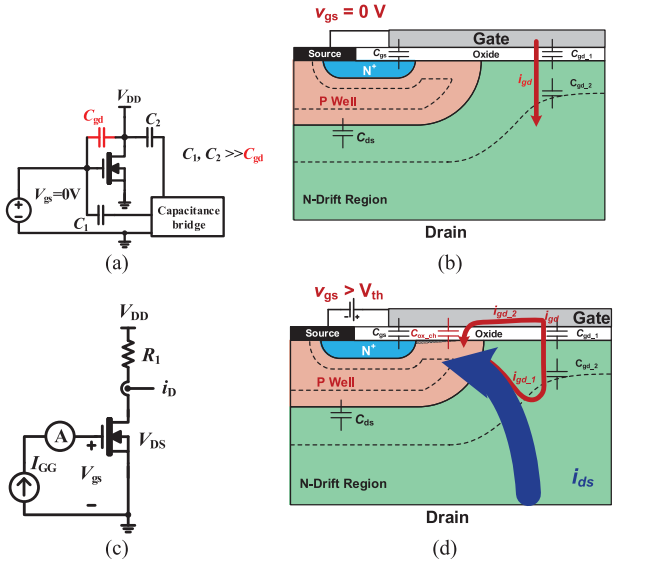


Fig. 13. Measurement of C–V characteristic. (a) Simplified circuit. (b) i_{gd} inside the device; and measurement of gate charge characteristic. (c) Measurement circuit. (d) Current flows inside the device.

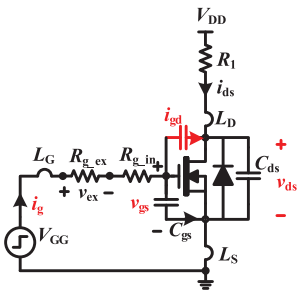


Fig. 14. Evaluation circuit of the dynamic Q_{gd}.

from a low voltage level to a high voltage level. v_{gs} verses the gate charge during this process is the gate charge characteristic in Fig. 12(b). The whole process is a dynamic turn on process. Current flows inside SiC MOSFET during this measurement is illustrated in Fig. 13(d). The channel is turned on and besides of the original current i_{gd_1} flowing through C_{gd}, extra current i_{gd_2} also flows through the channel oxide capacitance C_{ox_ch}. So, Q_{gd_dy} is larger than Q_{gd_st}, and this is the reason why v_{ds} of conventional analytical model falls faster than the experiment.

The static C_{gd} extracted from C-V curve is not accurate for the dynamic turn on process, while the dynamic Q_{gd} in the gate charge characteristic is more reasonable for the turn on evaluation. However, Fig. 12(b) only shows the characteristic of v_{gs} verses Q_g with no information concerning the variation of v_{ds}.

So, the dynamic v_{ds} verses Q_g or Q_{gd} should be evaluated.

B. Evaluation of the Dynamic Q_{gd} *Characteristic*

Based on the measurement of gate charge in Fig. 13(c), a modified circuit is proposed in Fig. 14 to evaluate the dynamic Q_{gd}. The constant current is replaced by a constant voltage for

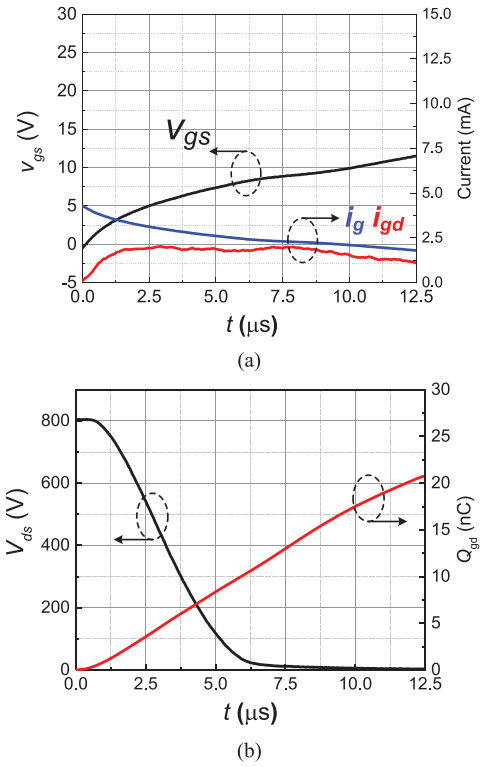


Fig. 15. (a) Waveforms of gate circuit parameters. (b) Waveform of v_{ds} and Q_{gd}.

convenience. Three parameters i_g, v_{gs}, and v_{ds} are measured. In order to minimize the influence of the parasitic inductance during the measurement, the external gate resistor R_{g_ex} is chosen large enough to slow down the measurement time. With minimized di/dt in the gate loop and power loop, the induced voltages on these parasitic inductances can be ignored.

R_{g_ex} is selected as 1.5 kΩ in the test circuit. V_{DD} is 800 V, and R_1 is set as 33.3 Ω, which means the conduction current is 24 A. i_g is too small to be measured directly and accurately. However, voltage v_{ex} on R_{g_ex} can be measured to derive i_g. With the measured v_{gs} and constant C_{gs} value, then i_{gd} can also be calculated.

Then, v_{gs}, i_g, and i_{gd} are plotted in Fig. 15(a). i_g is less than 5 mA; so, the voltage on the 4.6 Ω internal gate resistance can be ignored. di_g/dt is so small that the induced voltage on the gate inductance is far less than 1mV and is also ignored. It means the measured v_{gs} is almost same to the actual internal gate voltage of the device.

As analyzed before, the integration of i_{gd} during the voltage falling stage is the gate-to-drain charge Q_{gd}. Waveform of v_{ds} and Q_{gd} are plotted in Fig. 15(b). When Q_{gd} increases, v_{ds} falls simultaneously. In order to show the relation between Q_{gd} and variation of v_{ds}, v_{ds} vs. Q_{gd} is plotted as the black solid line in Fig. 16, and defined as dynamic Q_{gd} characteristic. The total dynamic Q_{gd} of the falling stage is around 21 nC, which is close to that on the datasheet and confirms the accuracy of the measurement. At the same time, the static Q_{gd} characteristic based on Fig. 12(a) is also plotted as the red dash line in Fig. 16 for comparison. The static Q_{gd} is obviously lower than the

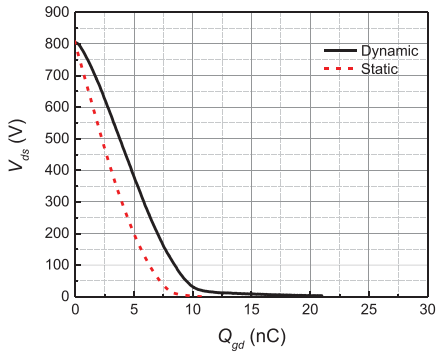


Fig. 16. Comparison of the dynamic and static $Q_{\rm gd}$ characteristic.

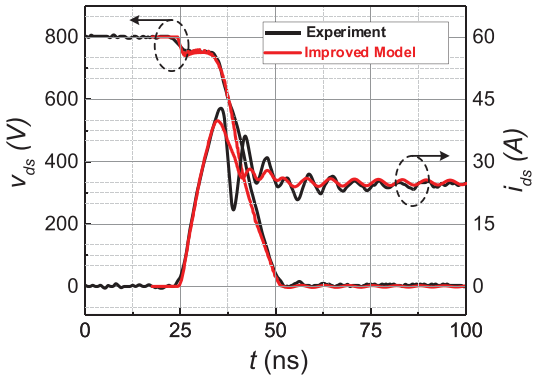


Fig. 17. Comparison of turn on waveforms between the experiment and improved loss model with dynamic transfer and $Q_{\rm gd}$ characteristics.

dynamic $Q_{\rm gd}$. The comparison is consistent with voltage falling stage of the waveforms in Fig. 10.

C. Loss Evaluation of SiC MOSFET With Dynamic Transfer and Q_{gd} Characteristics

Based on the measured dynamic $Q_{\rm gd}$ characteristic, corresponding dynamic $C_{\rm gd}$ can be derived. Then, the dynamic $C_{\rm gd}$ is adopted in the analytical switching loss model to evaluate the switching performance. Waveforms comparison of the improved model and experiment are shown in Fig. 17. The waveforms predicted by the improved model matches the experiment very well at both current rising and voltage falling stages. Only a little difference of the resonating current during voltage falling stage can be observed. This is may cause by the simplification of lumped parasitic parameters. In actual prototype, these parasitic parameters distribute in an extensive layout, and will affect the resonating waveforms of $i_{\rm ds}$ during the fast changing of $V_{\rm ds}$. A compromise is adopted in the model to have a clearer and compact illustration. The predicted turn on loss is about 340 μJ, which is only 4.5% lower than the measured value, 356 μJ.

Different load currents are tested, and loss comparison is shown in Fig. 18. Loss calculated by conventional model is always lower the experiment. The error is more than 5% and increases with increasing current. In comparison, losses calculated by the improved model match the experiment results very

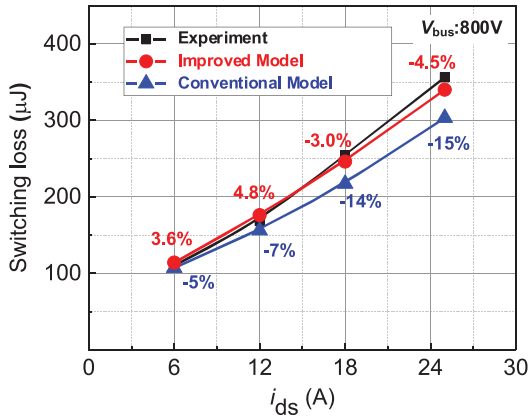


Fig. 18. Turn ON loss comparison under different load current.

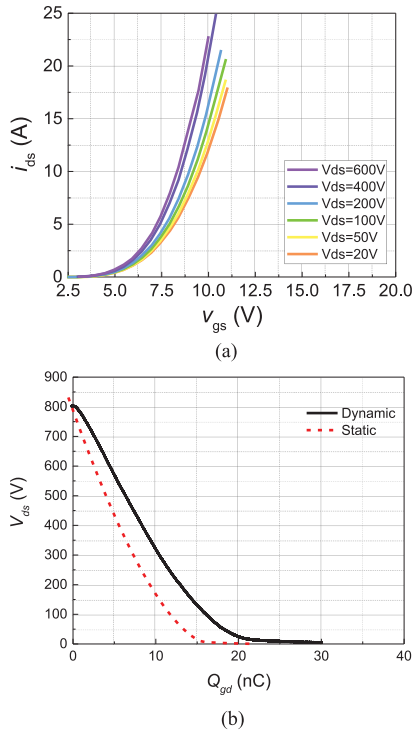
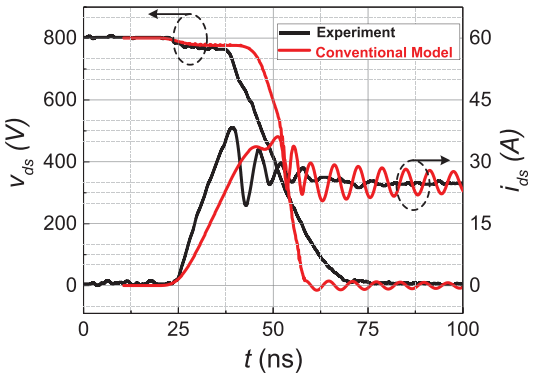


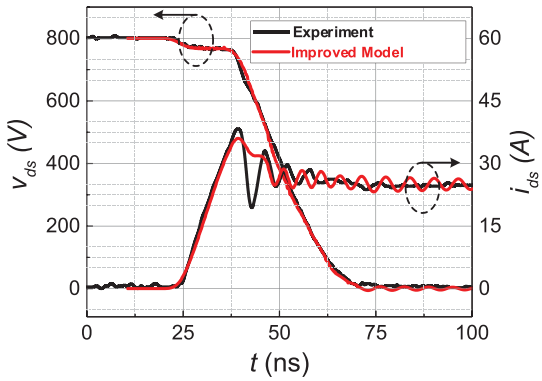
Fig. 19. SiC MOSFET (device B). (a) Transfer characteristics under different $v_{\rm ds}$ @25 °C. (b) Comparison of the static and dynamic $Q_{\rm gd}$ characteristic.

well, and the error is always less than 5% under different load current.

Besides that, another 1.2 kV/80 mΩ SiC MOSFET (device B, *LSIC1MO120E0080* [32]) from Littelfuse is also tested with the same processes. Fig. 19(a) and (b) show the transfer and $Q_{\rm gd}$ characteristics, respectively. In Fig. 19(a), the transfer characteristic also varies under different $v_{\rm ds}$, and this causes slower current rising for conventional analytical model shown in Fig. 20(a). The dynamic $Q_{\rm gd}$ characteristic is also plotted in Fig. 19(b), and shows larger value to static $Q_{\rm gd}$ derived by integrating C-V curve. Fig. 20(b) gives the waveforms comparison between experiments and the improved analytical switching loss model with dynamic transfer and $Q_{\rm gd}$ characteristics. Waveforms match much better with each other at both current rising



(a)



(b)

Fig. 20. Turn on waveforms comparison of SiC MOSFET (device B) between the experiment and loss model. (a) Conventional model. (b) Improved model with dynamic transfer and Q_{gd} characteristics.

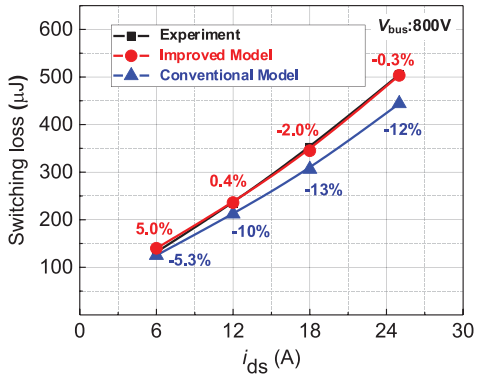


Fig. 21. Turn ON loss comparison under different load current of SiC MOSFET (device B).

and voltages falling stages than that from conventional analytical switching loss model. Loss comparison under different current load is shown in Fig. 21. Compared to conventional model, the error of the improved model is all within 5% over whole current load and it further verifies the accuracy of the analysis and the improved model.

V. Conclusion

This article analyzes the impact of dynamic transfer and Q_{gd} characteristic on the turn on process evaluation of SiC MOSFETs.

Firstly, the transfer characteristic from current SiC MOSFET's datasheet ignores the short channel effect and DIBL phenomena. Without this consideration, conventional analytical switching loss model predicts slower current rising speed of DUT and overestimate the loss during this stage. Secondly, due to different circuit conditions, the static C_{gd} from C-V curves cannot be directly adopted to predict the voltage falling stage of SiC MOSFET's turn on process. Static C_{gd} from C-V curves causes faster voltage falling prediction and underestimates loss during this stage.

Detailed analyses of these two parameters based on planar gate SiC MOSFETs are done to offer a better understanding of the turn on process, and it is suggested that parameters from current SiC MOSFET datasheet is not adequate to fully explicit characteristics of the device. Measurement circuits of transfer characteristics and dynamic Q_{gd} are proposed. Measured parameters from these circuits are applied in the analytical model and the waveforms show good consistency with experiments. The error of loss evaluation with the improved analytical model is always less than 5%, which is quite accurate to be used for the design of thermal dissipation and whole system.

Appendix

Stage 1

$$V_{\mathrm{GG}} = v_{\mathrm{gs}}(t) + R_{\mathrm{g}} i_{\mathrm{g}}(t) + (L_{\mathrm{G}} + L_{\mathrm{S}}) \frac{\mathrm{d}i_{\mathrm{g}}(t)}{\mathrm{d}t} + L_{\mathrm{S}} \frac{\mathrm{d}i_{\mathrm{ds}}(t)}{\mathrm{d}t} \tag{1}$$

$$i_{\mathrm{g}}(t) = C_{\mathrm{iss}} \frac{\mathrm{d}v_{\mathrm{gs}}(t)}{\mathrm{d}t}. \tag{2}$$

Laplace transform is done, and (6) can be derived as

$$\left(\tau_{\mathrm{m}} s^2 + \tau_{\mathrm{n}} s + \tau_{\mathrm{o}}\right) V_{\mathrm{gs}}(s) = \frac{AA}{s} + BB + sCC \tag{6}$$

where

$$\tau_{\mathrm{m}} = (L_{\mathrm{G}} + L_S) C_{iss} \quad \tau_{\mathrm{n}} = R_{\mathrm{g}} C_{iss} \quad \tau_{\mathrm{o}} = 1$$

$$AA = V_{\mathrm{GG}} \quad BB = \tau_{\mathrm{m}} \frac{\mathrm{d}v_{\mathrm{gs}}(0)}{\mathrm{d}t} + \tau_{\mathrm{n}} v_{\mathrm{gs}}(0) \quad CC = \tau_{\mathrm{m}} v_{\mathrm{gs}}(0)$$

$\frac{\mathrm{d}v_{\mathrm{gs}}(0)}{\mathrm{d}t}$, $v_{\mathrm{gs}}(0)$ are the initial value.

Stage 2

Linear approximation for (3) is needed and (7) is proposed.

$$i_{\mathrm{ch}}(t) = g_{fs}\left(v_{gs}(t) - v_{gs}(0)\right) + i_{\mathrm{ch}}(0) \tag{7}$$

$$g_{\mathrm{fs}} = \frac{f^{-1}\left(i_{\mathrm{ch}}(0) + \Delta I_{\mathrm{ref}}\right) - f^{-1}\left(i_{\mathrm{ch}}(0)\right)}{\Delta I_{\mathrm{ref}}} \tag{8}$$

where $v_{\mathrm{gs}}(0)$ and $i_{\mathrm{ch}}(0)$ are initial values, and g_{fs} is transconductance. $f^{1}(i_{\mathrm{ch}})$ is the inverse function of (3). When ΔI_{ref} approaches the limit "0", g_{fs} is the real transconductance at corresponding i_{ch}. In this model, piecewise linearization is done with ΔI_{ref} set as 0.1–0.2 I_{L}. So, the linear equation (7) is adopted with different g_{fs} at different current intervals. Substituting (7) and (2) into (1), the same form of (6) can be derived with different term coefficients as

$$\tau_{\mathrm{m}} = (L_{\mathrm{G}} + L_{\mathrm{S}}) C_{\mathrm{iss}} \quad \tau_{\mathrm{n}} = R_{\mathrm{g}} C_{\mathrm{iss}} + L_{\mathrm{S}} g_{\mathrm{fs}} \quad \tau_{\mathrm{o}} = 1$$

and

$$v_{\rm ds}(t) = V_{\rm bus} - L_{\rm loop}\frac{{\rm d}i_{\rm ds}(t)}{{\rm d}t}. \tag{9}$$

Stage 3

$$i_{\rm g}(t) = C_{\rm iss}\frac{{\rm d}v_{\rm gs}(t)}{{\rm d}t} - C_{\rm gd}\frac{{\rm d}v_{\rm ds}(t)}{{\rm d}t} \tag{4}$$

$$i_{\rm ds}(t) = i_{\rm ch}(t) + C_{\rm oss}\frac{{\rm d}v_{\rm ds}(t)}{{\rm d}t}. \tag{5}$$

Displacement current of $C_{\rm D}$ should also be considered.

$$i_{\rm ds}(t) = I_{\rm L} + C_{\rm D}\frac{{\rm d}v_{\rm Diode}(t)}{{\rm d}t} \tag{10}$$

$$v_{\rm ds}(t) = V_{\rm bus} - L_{\rm loop}\frac{{\rm d}i_{\rm ds}(t)}{{\rm d}t} - v_{\rm Diode}(t). \tag{11}$$

Considering the nonlinear characteristic of parasitic capacitances, piecewise linearization is also done. This stage is divided into multiple intervals based on the falling $v_{\rm ds}$, e.g., 20 volts for each interval. Charge equivalent value of capacitances during each interval is adopted. $v_{\rm ds}$ is assumed falling linearly during each interval, and (12) is proposed.

$$v_{\rm ds}(t) = v_{\rm ds}(0) - \int_0^t \delta \cdot {\rm d}t \tag{12}$$

where δ is assumed constant. When (4), (5), (7), and (12) are substituted into (1), we obtain

$$V_{\rm GG} = v_{\rm gs}(t) + (R_{\rm g}C_{\rm iss} + L_{\rm S}g_{\rm fs})\frac{{\rm d}v_{\rm gs}(t)}{{\rm d}t} + (L_{\rm G} + L_{\rm S})C_{\rm iss}\frac{{\rm d}^2v_{\rm gs}(t)}{{\rm d}t^2} + R_{\rm g}C_{\rm gd}\delta. \tag{13}$$

When (7) and (12) are substituted into (5), we derive

$$i_{\rm ds}(t) = g_{\rm fs}(v_{\rm gs}(t) - v_{\rm gs}(0)) + i_{\rm ch}(0) - C_{\rm oss}\delta. \tag{14}$$

Equations (14) and (11) are substituted into (10) to derive (15)

$$i_{\rm ds}(t) = I_{\rm L} - L_{\rm loop}C_{\rm D}g_{\rm fs}\frac{{\rm d}^2v_{\rm gs}(t)}{{\rm d}t^2} + C_{\rm D}\delta. \tag{15}$$

Equations (14) and (15) are substituted into (13), eliminating δ and $i_{\rm ds}(t)$. The same form of (6) can be derived with different term coefficients as

$$\tau_{\rm m} = (L_{\rm G} + L_{\rm S})C_{\rm iss} + \alpha L_{\rm loop}C_{\rm D}g_{\rm fs}$$
$$\tau_{\rm n} = R_{\rm g}C_{\rm iss} + L_{\rm S}g_{\rm fs} \quad \tau_{\rm o} = 1 + \alpha g_{\rm fs}$$
$$\alpha = \frac{R_{\rm g}C_{\rm gd}}{C_{\rm oss} + C_{\rm D}}$$

and

$$AA = V_{\rm GG} - \alpha\left[i_{ch}(0) - g_{\rm fs}v_{\rm gs}(0) - I_{\rm L}\right]$$
$$BB = \tau_{\rm m}\frac{{\rm d}v_{\rm gs}(0)}{{\rm d}t} + \tau_{\rm n}v_{\rm gs}(0)$$
$$CC = \tau_{\rm m}v_{\rm gs}(0).$$

When $v_{\rm gs}(t)$ is derived, $i_{\rm ch}(t)$ can be obtained by (3), then $i_{\rm ds}(t)$ can be derived by solving (5), (10), and (11)

$$i_{\rm ds}(t) = i_{\rm ds}(0)\cos s_3 t + \frac{1}{s_3}\frac{{\rm d}i_{\rm ds}(0)}{{\rm d}t}\sin s_3 t + \frac{C_D}{\tau_a s_3}\int_0^t i_{\rm ch}(\tau)\sin(t-\tau){\rm d}\tau + \frac{C_{oss}I_{\rm L}}{\tau_b}2\sin^2\frac{s_3}{2}t \tag{16}$$

where

$$\tau_a = L_{\rm loop}C_{\rm oss}C_{\rm D} \quad \tau_b = C_{\rm oss} + C_{\rm D} \quad s_3 = \sqrt{\frac{\tau_b}{\tau_a}}.$$

Stage 4

$$v_{gs}(t) = (V_{\rm GG} - v_{gs}(0))\left(1 - e^{-\frac{t}{R_{\rm g}C_{\rm iss}}}\right) + v_{gs}(0) \tag{17}$$

$$v_{\rm Diode}(t) + R_{\rm loop}i_{\rm ds}(t) + L_{\rm loop}\frac{{\rm d}i_{\rm ds}(t)}{{\rm d}t} = V_{\rm bus} \tag{18}$$

$$i_{\rm ds}(t) - I_{\rm L} = C_{\rm D}\frac{{\rm d}v_{\rm Diode}(t)}{{\rm d}t}. \tag{19}$$

$R_{\rm loop}$ is the power loop damping resistance.

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