A Single Carrier-Based Pulsewidth Modulation Technique for Three-to-Three Phase Indirect Matrix Converter

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***Abstract*—In this article, a new carrier-based pulsewidth modulation (CBPWM) technique is presented for three-to-three phase indirect matrix converter (IMC). The main feature of this technique is the use of single triangular carrier to obtain the switching signals for both converter stages of the IMC. Simplified modulation equations calculated independently from the sector judgements and space vector pulsewidth modulation (SVPWM) technique are proposed for the bidirectional rectifier and inverter stages of the IMC. As a result, the presented CBPWM technique is implemented easily with the reduced complexity as compared to the conventional single carrier-based CBPWM techniques developed based on the SVPWM technique. This new technique features all the benefits associated with the conventional CBPWM techniques of the IMC, i.e., sinusoidal input/output waveforms, voltage transfer ratio of 0.866 and generation of the switching signals independent of the lookup tables. The simulation model of the IMC is developed in the PSIM environment to verify the performance of the proposed CBPWM technique. The laboratory prototype for the IMC is developed based on the proposed scheme using the DSP and FPGA devices. The experimental results are included to support the simulation results.**

***Index Terms*—Carrier-based pulsewidth modulation (CBPWM), FFT, matrix converter (MC), modulation index, overmodulation, space vector PWM, voltage transfer ratio.**

I. Introduction

THE matrix converter (MC) is an "all semiconductor" device first introduced by Alesina and Venturini [1] in the 1980s for direct ac–ac conversion. The interesting features of the MC are bidirectional power flow, sinusoidal input/output waveforms, compact design, and the adjustable input power factor. Two MC topologies, namely, direct MC (DMC) and indirect MC (IMC) are alternatively used to accomplish the ac–ac conversion process [2]–[4]. The topology of three-to-three phase (3×3) DMC consists of nine bidirectional switches in form of matrix connecting the three input phases with the three output phases [2]. In the 3×3 IMC, the three-phase bidirectional current source rectifier (BCSR) (six bidirectional switches) and conventional two-level voltage source inverter (VSI) (six unidirectional switches) stages are connected back to back forming the virtual dc-link between the two converter stages [3], [4]. Both topologies provide the similar performances with the reference to input/output waveforms, number of switches and the voltage transfer ratio (VTR).

The IMC topology is receiving more recognition recently owing to some important benefits over the DMC topology. The IMC provides the benefits of simple commutation and protection as compared to complex commutation and protection of the DMC topology. Also, the IMC topology provides the possibility of modifying the structures of current source rectifier (CSR) or VSI stages. The research in the field of IMC is mainly concentrated on the topological structures, control algorithms, commutation strategies, common mode voltages, performance under unbalanced supply, and improving the VTR [5]–[11].

The control of the IMC has also remained an interesting topic for the researchers owning to the decoupled rectification and inversion stages [12]–[26]. The modulation strategies of the IMC are classified in two categories: 1) space vector pulsewidth modulation (SVPWM); and 2) carrier-based pulsewidth modulation (CBPWM). The SVPWM for the IMC topology was first presented in [3]. It has become the most extensively used control technique for the IMC because of its superior performance [12]–[16]. However, the SVPWM method is difficult to implement on the account of complex calculations based on the sector judgements and lookup tables.

On the other hand, the CBPWM techniques have been widely examined to control the IMC topology [17]–[21]. The CBPWM techniques overcome the abovementioned problem of SVPWM method up to some extent. These CBPWM techniques generate the gating signals by comparison of the modulation waves with the carrier of high frequency and therefore provides the simple implementation as compared to the SVPWM technique. Wang and Venkataramanan [17] proposed a new CBPWM algorithm for the IMC with the aim of reducing the computational complexity by using the simple and robust commutation. A digital CBPWM technique is proposed in [18] for reducing the switching commutation count and smooth sextant transitions in the IMC. Chiang and Itoh [19] presented a carrier-based scheme to expand the VTR beyond 0.866 for the IMC. The carrier-based discontinuous pulsewidth modulation (PWM) schemes are presented in [20] and [21] to minimize the switching losses of IMC.

However, the above CBPWM methods use the different carriers for the both conversion stages of the IMC. The BCSR

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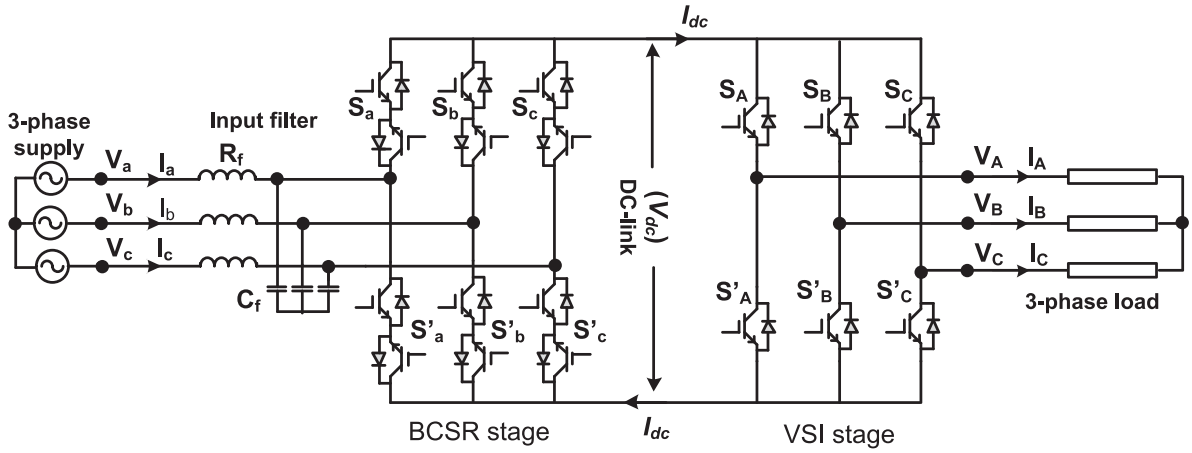

Fig. 1. IMC topology.

stage uses the symmetrical triangular carrier whereas the VSI stage uses the carrier with the variably increasing and decreasing slopes in accordance with the BCSR stage switching instants. This leads to the poor stability and complex implementation. The concept of using a single triangular carrier to overcome the abovementioned drawback of the conventional CBPWM is presented in [22]–[26]. Among these, the CBPWM method presented in [22] is developed for 3×3 IMC topology. Whereas the CBPWM schemes presented in [23] and [24] are developed for the dual output IMC topologies. The CBPWM schemes in [25] and [26] are developed for three-to-five phase IMC and three-level IMC topologies, respectively. These single carrier-based techniques derive their required modulation equations using the duty ratios calculated based on the SVPWM technique.

In this article, a new single CBPWM technique is presented to solve the aforementioned constraint of the standard single CBPWM technique of the IMC topology. The simple modulation equations are derived in this technique without using the duty ratios calculated based on the SVPWM technique and the sector judgements. Therefore, this new technique can be easily implemented without complex calculations as compared to existing single CBPWM methods. The modulations of the BCSR and VSI stages are based on the dead-band PWM (DPWM) and third harmonic injection PWM (THIPWM) techniques initially developed for the conventional PWM voltage/current source converters. Both these techniques are characterized by the increased voltage gain and the simplicity of gate pulse generation. The presented modulation technique provides the similar performance to that of the existing CBPWM techniques with reference to input/output waveform qualities and VTR.

The rest of this article is organized as follows. The 3×3 IMC topology is explained with the operation in Section II. Section III includes the derivation of the proposed CBPWM technique for the IMC based on the DPWM and THIPWM schemes of the conventional converters. Sections IV and V include the simulation and the experimental test results, respectively, to validate the presented new CBPWM technique. Finally, Section VI concludes this article.

II. 3×3 Phase IMC Topology With Operation Principle

The 3×3 phase IMC topology with the BCSR and the VSI stages is shown in Fig. 1 [3]. The BCSR stage is analogous to the conventional CSR consisting of upper and lower group of bidirectional switches represented by S_k and S'_k, respectively, for $k \in \{a, b, c\}$. The six bidirectional switches of the BCSR stage are controlled to synthesize the positive dc-link voltage ($V_{\rm dc}$) and the sinusoidal supply currents. The VSI stage of IMC is analogous to the standard two-level VSI with the upper and lower group of unidirectional switches represented by S_j and S'_j, respectively, for $j \in \{A, B, C\}$. The controlling of the six VSI stage switches produces the desired output voltages. The *LC* filter connected on the supply side of the IMC is shown in Fig. 1. The output of the IMC is connected with the three-phase star connected inductive load.

The three-phase balanced supply voltages applied to the IMC are represented by the following expression:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = V_m \begin{bmatrix} \sin(\omega_i t) \\ \sin(\omega_i t - \frac{2\pi}{3}) \\ \sin(\omega_i t + \frac{2\pi}{3}) \end{bmatrix} \tag{1}$$

where V_m and ω_i represent the peak amplitude and the angular frequency of the supply voltages.

The main contribution of BCSR stage in the IMC is to furnish the positive dc voltage ($V_{\rm dc}$) to the VSI stage. The voltage produced on the dc-link of IMC is related with the input voltages $[V_a, V_b, V_c]^T$ by the rectifier switching function which is expressed as [27]

$$\begin{bmatrix} +\frac{1}{2}V_{\rm dc} \\ -\frac{1}{2}V_{\rm dc} \end{bmatrix} = \begin{bmatrix} S_a & S_b & S_c \\ S'_a & S'_b & S'_c \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}. \tag{2}$$

The safe operation of the BCSR stage of IMC is ensured by considering the following conditions while developing the rectifier switching functions:

$$\begin{cases} S_a + S_b + S_c = 1 \\ S'_a + S'_b + S'_c = 1. \end{cases} \tag{3}$$

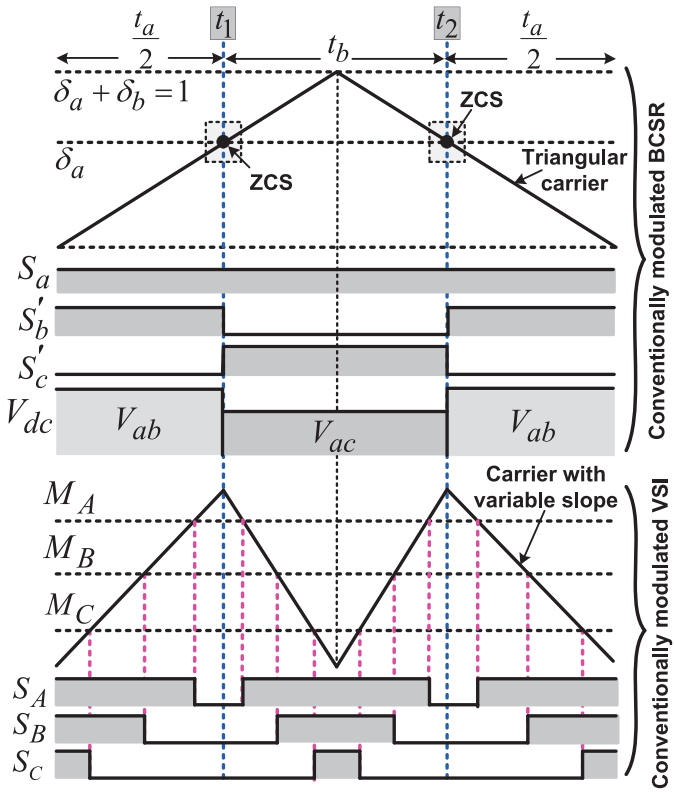

Fig. 2. Modulation of IMC using conventional carrier-based schemes.

The VSI stage of IMC produces the required output voltages with the required frequency. The output voltages $[V_A, V_B, V_C]^T$ are related with the dc voltage by the inverter switching function as represented by the following expression [27]:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \begin{bmatrix} S_A & S'_A \\ S_B & S'_B \\ S_C & S'_C \end{bmatrix} \begin{bmatrix} +\frac{1}{2}V_{\rm dc} \\ -\frac{1}{2}V_{\rm dc} \end{bmatrix}. \tag{4}$$

The safe operation of the VSI stage of IMC is ensured by considering the following conditions while developing the inverter switching function:

$$\begin{cases} S_A + S'_A = 1 \\ S_B + S'_B = 1 \\ S_C + S'_C = 1. \end{cases} \tag{5}$$

Finally, the output voltages $[V_A, V_B, V_C]^T$ and the input voltages $[V_a, V_b, V_c]^T$ of the IMC are related by the following expression [20]:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \begin{bmatrix} S_A & S'_A \\ S_B & S'_B \\ S_C & S'_C \end{bmatrix} \begin{bmatrix} S_a & S_b & S_c \\ S'_a & S'_b & S'_c \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{6}$$

where the switch S_x is turned ON when $S_x = 1$ and turned OFF when $S_x = 0$.

Fig. 2 shows the modulation of IMC for the one sampling period when the switching functions of BCSR and VSI stages are determined by the conventional CBPWM schemes [3], [17], [18]. The synchronization between input and output stages of the IMC is required in order to obtain the balance between input and output quantities. By aligning the peak of the VSI stage carrier with the switching instants of the BCSR stage, as shown in the Fig. 2, the synchronization is established between two stages. The generation of the switching pulses S_a, S'_b, and S'_c for the BCSR stage are shown by the comparison of two duty cycles δ_a and $\delta_a + \delta_b$ with the triangular carrier [17], [18]. Whereas the switching pulses S_A, S_B, and S_C for the VSI stage are shown to be produced by comparison of modulation signals M_A, M_B, and M_C with the carrier having the variable rising and falling slopes [17], [18]. It is clearly observed that the switching instants created at t_1 and t_2 on the BCSR stage are aligned with the zero voltage states of the VSI stage due to the synchronization of both stages. This enables the BCSR stage swtiches to commutate at the zero currents which is termed as zero current switching (ZCS) operation. The ZCS provides the high efficiency operation of the IMC by eliminating the switching losses of the BCSR stage. In addition, the ZCS allows the two-step commutation which reduces the complexity of implementation [3]. The ZCS operation of the BCSR stage requires the VSI stage to operate with the modulation index less than unity in order to produce the zero voltage stages, as shown in Fig. 2.

The synthesize of dc voltage by the BCSR stage in the given sampling period is also shown in Fig. 2. It is assumed that the maximum and medium line voltages available in the given sampling period are V_{ab} and V_{ac}, respectively. In the duration t_a, the switches S_a and S'_b are operated to synthesize $V_{\rm dc}$ from the input line voltage V_{ab}. Similarly, in the duration t_b, the dc-link voltage is synthesized from the input line voltage V_{ac} by the operation of the switches S_a and S'_c. The zero switching states are eliminated from the BCSR stage to obtain the maximum dc voltage for the VSI stage as shown in Fig. 2. For this, the duty cycles δ_a and δ_b of the BCSR stage are modified (normalized) such that the addition of δ_a and δ_b becomes unity [17], [18].

III. Proposed Single CBPWM Technique

In the proposed CBPWM technique, the BCSR and the VSI stages of IMC are analyzed by the two independent carrier-based modulation techniques. These carrier-based techniques are originally developed for the conventional PWM rectifier (CSR) and two-level inverter (VSI) topologies. Section III-A derives the modulation scheme for the BCSR stage based on the DPWM scheme of CSR presented in [28]. Similarly, Section III-B includes the derivation of modulation scheme for the VSI stage based on the THIPWM scheme of the traditional VSI [29], [30].

A. Derivation of Modulation Scheme for BCSR Stage of IMC

The DPWM scheme presented in [28] for the conventional CSR is explained in Section III-A1. Section III-A2 explains the modifications incorporated in the original scheme to extend its application for the BCSR stage of IMC.

1) Modulation of Conventional CSR: Three input dead-band modulation waves are calculated from the balanced supply voltages which are given as follows:

$$M_{cabc}=\begin{cases} m_c \cdot \sin\left(\omega_i t-\frac{2\pi k}{3}+\phi\right), \text{for } \frac{2\pi k}{3}\le\omega_i t\le\frac{2\pi(k+1)}{3} \\ -m_c \cdot \sin\left(\omega_i t-\frac{2\pi(k+2)}{3}+\phi\right), \text{for } \\ \qquad\qquad \frac{2\pi(k+1)}{3}\le\omega_i t\le\frac{2\pi(k+2)}{3} \\ 0, \text{for } \frac{2\pi(k+2)}{3}\le\omega_i t\le\frac{2\pi(k+3)}{3} \end{cases} \tag{7}$$

where M_{cabc} represents the three input modulation signals M_{ca}, M_{cb}, and M_{cc} obtain for $k \in \{0, 1, 2\}$. m_c and ϕ represent the modulation index and the required displacement angle between supply voltages and currents, respectively. The modulation index is defined as the ratio of the peak input current to the dc-link current $\frac{I_m}{I_{\rm dc}}$ for the CSR. As the modulation waves are derived directly from the supply voltages, ϕ is zero resulting in the unity power factor.

Fig. 3 shows the modulation scheme presented in [28] for the conventional CSR. Following are the steps to obtain the gate pulses for the CSR switches as per the scheme.

1) The modulation signals M_{ca}, M_{cb}, and M_{cc} are compared with the sawtooth carrier to obtain the three corresponding switching patterns represented by s_{ik} for $k \in \{a, b, c\}$.
2) The basic switching pulses for the six CSR switches are determined by combining the switching patterns of two phases obtained in step-1 to produce the expected PWM line currents. Switching pulses s_a, s_b, s_c belong to the upper switches and s'_a, s'_b, s'_c belong to the corresponding lower switches.
3) The shorting pulses s_{sc} are produced using the basic switching pulses obtained in the step-2, as shown in Fig. 3. The generation of the shorting pulses s_{sc} indicates the absence of switching pulses either on the upper group of switches ($S_a = 0, S_b = 0, S_c = 0$) or on the lower group of switches ($S'_a = 0, S'_b = 0, S'_c = 0$). In order to avoid this situation to ensure the safe operation of CSR and to satisfy (3), the shorting pulses are required to be distributed uniformly among all the switches. The distribution pulses s_{d1}, s_{d2}, and s_{d3} obtained based on the modulation signals, as shown in Fig. 3 are used to distribute s_{sc} uniformly among all the six switches of CSR.
4) Finally, the gate pulses S_a, S_b, S_c for the upper and S'_a, S'_b, S'_c for the lower CSR switches are determined, as shown in Fig. 3.

The modulation of conventional CSR topology with the above modulation scheme provides the required output dc-voltage with the sinusoidal supply currents.

2) Modulation of BCSR Stage of IMC: The dc-link voltage of the IMC, $V_{\rm dc}$ pulsates at the frequency six times the supply frequency due to the lack of energy storing element. Therefore, the modulation waves of (7) are modified in order to use it for the BCSR stage of IMC. The modulation index m_c in (7) assumes the constant instantaneous value due to the fixed amplitudes of input and dc-link currents in the conventional CSR modulation. To compensate the effect of pulsating $V_{\rm dc}$ on the supply currents,

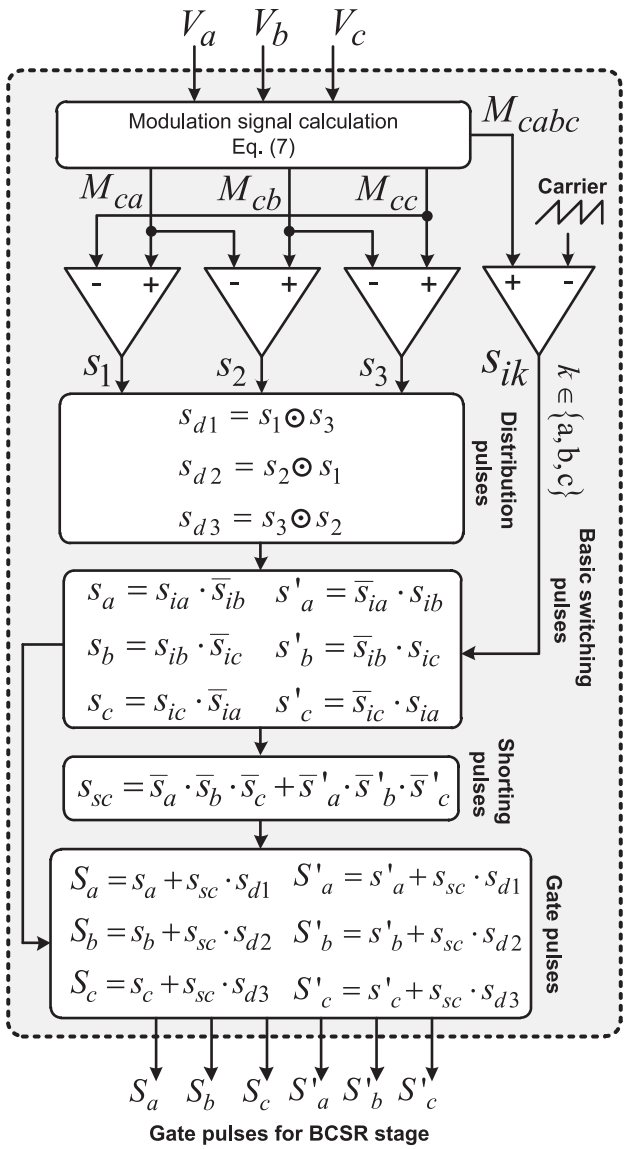

Fig. 3. Dead-band modulation scheme of conventional CSR topology.

m_c is modified based on its relation with the dc-link voltage. For that, the following relation between input and output powers of the BCSR stage is considered assuming the ideal converter

$$\begin{cases} 3V_{in}I_{in}\cos\phi = V_{\rm dc}I_{\rm dc} \\ \therefore \frac{3}{2}V_m I_m \cos\phi = V_{\rm dc}I_{\rm dc} \quad \left(\because V_{in}=\frac{V_m}{\sqrt{2}}, I_{in}=\frac{I_m}{\sqrt{2}}\right) \\ \therefore \frac{I_m}{I_{\rm dc}} = \frac{2V_{\rm dc}}{3V_m} = m_c \quad (\because \cos\phi = 1) \end{cases} \tag{8}$$

where $V_{\rm dc}$ and $I_{\rm dc}$ are the dc-link voltage and current, respectively. V_{in} and I_{in} are the rms values of input phase voltages and currents, respectively. Similarly, V_m and I_m represent the peak amplitudes of input phase voltages and currents, respectively. The symbols "$\therefore$" and "$\because$" used in (8) represent "therefore" and "because," respectively. Equation (8) yields the relation between m_c and dc voltage $V_{\rm dc}$. Therefore, in order to consider the effect

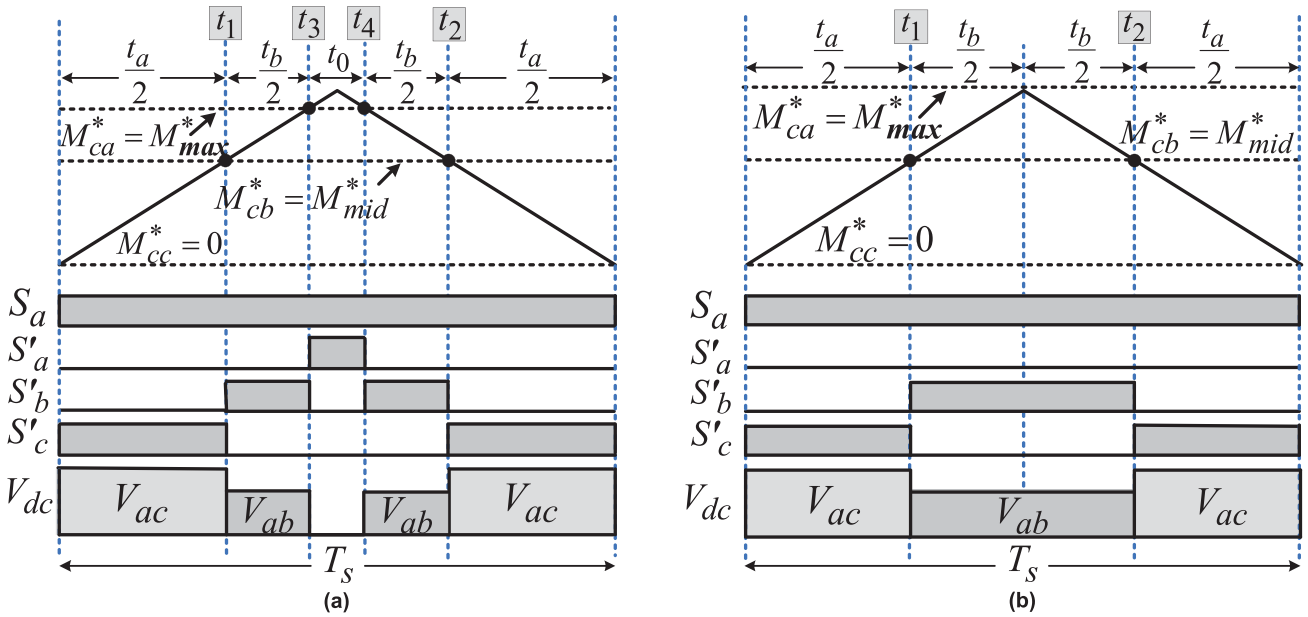

Fig. 4. Carrier-based modulation of BCSR stage with (a) linear modulation range ($0 \le m'_c \le 1$) and (b) overmodulation ($m'_c = 1.07$).

of the ripple present in the V_{dc}, modulation signals of (7) are modified as given

$$M^*_{cabc} = \begin{cases} m'_c \cdot \sin\left(\omega_i t - \frac{2\pi k}{3} + \phi\right), \text{for } \frac{2\pi k}{3} \le \omega_i t \le \frac{2\pi(k+1)}{3} \\ -m'_c \cdot \sin\left(\omega_i t - \frac{2\pi(k+2)}{3} + \phi\right), \text{for } \frac{2\pi(k+1)}{3} \le \omega_i t \le \frac{2\pi(k+2)}{3} \\ 0, \text{for } \frac{2\pi(k+2)}{3} \le \omega_i t \le \frac{2\pi(k+3)}{3} \end{cases} \tag{9}$$

where $m'_c = m_c \cdot V_{\text{rip}}$. V_{rip} represents the per unit dc voltage with the ripple component which is similar to the output voltage of three-phase diode rectifier. V_{rip} is calculated using the input line voltages, as given by (10). M^*_{cabc} represents the three modified input modulation signals M^*_{ca}, M^*_{cb}, and M^*_{cc} for the BCSR stage of IMC. Considering the relation between m_c and m'_c, the modified modulation signals M^*_{cabc} are related with M_{cabc} by the expression given in (11)

$$V_{\text{rip}} = \frac{\max|V_{ab}, V_{bc}, V_{ca}|}{\sqrt{3} \cdot V_m} \tag{10}$$

where V_{ab}, V_{bc}, and V_{ca} are the input line voltages

$$M^*_{cabc} = V_{\text{rip}} \cdot M_{cabc}. \tag{11}$$

Now, according to step-1 of the modulation scheme presented in Section III-A1, M^*_{cabc} are compared with the carrier wave to obtain the three switching patterns for the BCSR stage. However, in the present work, the unipolar triangular carrier is used instead of sawtooth carrier. Then, following the steps-2–4 given in Section III-A1, the six gate signals for the bidirectional switches of the BCSR stage are obtained. Fig. 4(a) represents the PWM of the BCSR stage using the modulation procedure explained above in the linear modulation range ($0 \le m'_c \le 1$).

DC-link voltage produced by the modulation of BCSR is expressed as follows, which is derived based on (8)

$$V_{\text{dc}} = \frac{3}{2} V_m m'_c \cos\phi. \tag{12}$$

According to the above equation, the maximum average value of V_{dc} is $1.5V_m$ obtained at unity modulation index ($m'_c = 1$) and input power factor ($\cos\phi = 1$). However, due to the presence of zero switching states for the linear range of m'_c, as shown in Fig. 4(a), the available dc voltage for the VSI stage is reduced. Therefore, it is required to eliminate the zero voltage states from the dc-link voltage which provides the performance similar to that obtained by the conventional control of the BCSR stage of IMC as discussed in Section II.

Fig. 4(a) shows the PWM of BCSR stage by the comparison of modulation signals M^*_{ca}, M^*_{cb}, and M^*_{cc} with the triangular carrier. In the given sampling period, M^*_{ca} and M^*_{cc} assume the highest ($M^*_{ca} = M^*_{\max}$) and lowest ($M^*_{cc} = 0$) amplitudes, respectively. It is observed that due to the intersection of M^*_{ca} with the carrier wave, the gating signals for the upper and lower switches S_a and S'_a of the BCSR leg are produced. Turning ON of the switches in the same BCSR leg for the duration t_0 produces the zero dc voltage, as verified from Fig. 4(a). Therefore, it is required to prevent the intersection of modulation signal having the highest amplitude ($M^*_{\max}$) with the carrier wave to eliminate the zero voltage states from V_{dc}. Modulation signal with the highest amplitude among M^*_{cabc} are represented as $M^*_{\max}$ and calculated as

$$M^*_{\max} = \max(M^*_{ca}, M^*_{cb}, M^*_{cc}). \tag{13}$$

In order to avoid the intersection of $M^*_{\max}$ with the carrier wave, one alternative is the overmodulation operation of BCSR stage. However, the purpose of increasing m'_c here is not to produce the maximum possible value of dc voltage similar to the

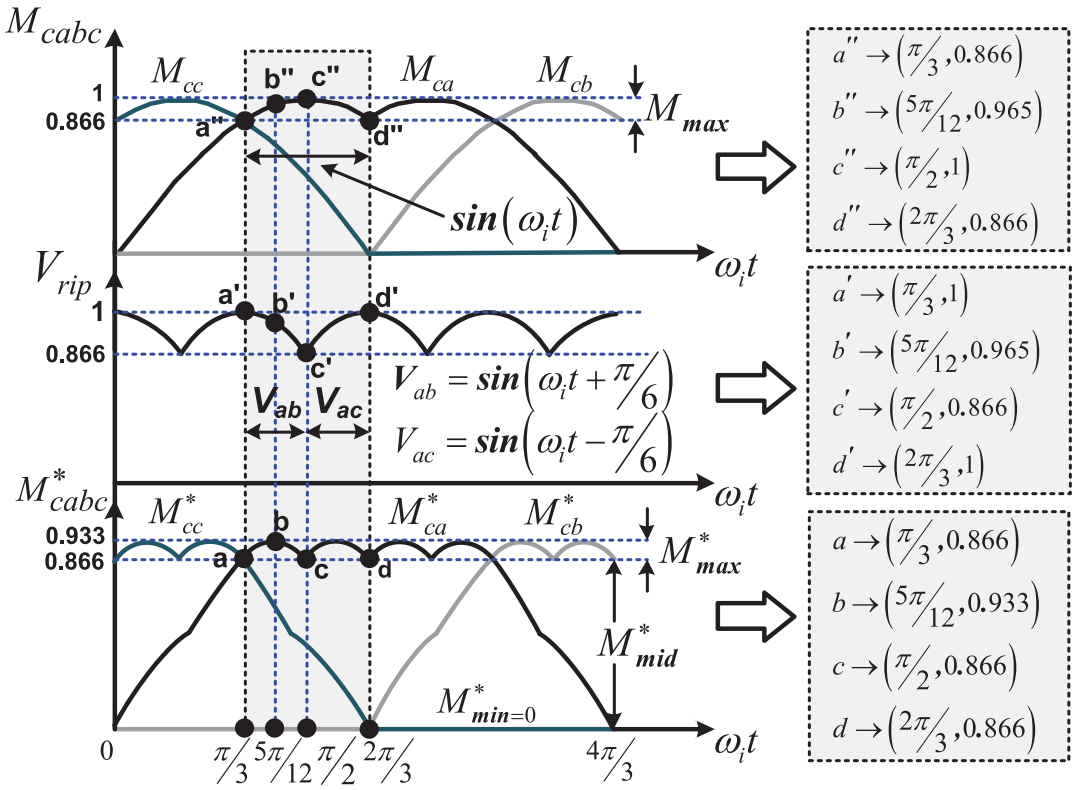

Fig. 5. Estimation of $M^*_{\max}$ range using M_{cabc} and $V_{\rm rip}$.

diode rectifier. Therefore, it is interesting to find the minimum value of overmodulation which is enough only to eliminate the zero voltage states from $V_{\rm dc}$. This value of overmodulation can be estimated by finding the range of M^*_{cabc} amplitudes which constitutes $M^*_{\max}$.

The derivation of M^*_{cabc} using M_{cabc} and $V_{\rm rip}$, based on the relation given in (11), is represented graphically in Fig. 5. To find the range of maximum amplitudes $M^*_{\max}$ of M^*_{cabc}, the interval $[\frac{\pi}{3}, \frac{2\pi}{3}]$ is considered, as shown in Fig. 5. $M^*_{\max}$ is shown to be obtained from $M_{\max}$ (maximum amplitudes of M_{cabc}) and $V_{\rm rip}$. The waveforms of M_{cabc} are considered with the peak amplitude of unity ($m_c = 1$). The peak amplitude of $V_{\rm rip}$ is also unity, according to (10).

For the given interval $[\frac{\pi}{3}, \frac{2\pi}{3}]$, $M_{\max}$ follows V_a whereas $V_{\rm rip}$ follows V_{ab} in interval $[\frac{\pi}{3}, \frac{\pi}{2}]$ and V_{ac} in interval $[\frac{\pi}{2}, \frac{2\pi}{3}]$ as shown in Fig. 5. Therefore, for the given interval, $M^*_{\max}$ is expressed by the following:

$$f(\omega_i t) = \begin{cases} \sin(\omega_i t) \cdot \sin\left(\omega_i t + \dfrac{\pi}{6}\right), \text{for } \dfrac{\pi}{3} \le \omega_i t \le \dfrac{\pi}{2} \\ \sin(\omega_i t) \cdot \sin\left(\omega_i t - \dfrac{\pi}{6}\right), \text{for } \dfrac{\pi}{2} \le \omega_i t \le \dfrac{2\pi}{3} \end{cases} \tag{14}$$

where $f(\omega_i t) = M^*_{\max}$.

Now, to derive the range of $M^*_{\max}$ graphically, various test points a'', b'', c'', and d'' are considered on M_{cabc} at $\omega_i t = \frac{\pi}{3}$, $\frac{5\pi}{12}$, $\frac{\pi}{2}$ and $\frac{2\pi}{3}$, respectively. Corresponding points a', b', c', and d' on $V_{\rm rip}$ are also shown in Fig. 5. The calculated amplitudes of the corresponding points a, b, c, and d of M^*_{cabc} according to (11) belong to $M^*_{\max}$, as shown in Fig. 5. The highest and lowest amplitudes obtained for $M^*_{\max}$ are 0.933 and 0.866 for the given amplitudes of M_{cabc} and $V_{\rm rip}$.

Theoretically, the extreme (highest and lowest) amplitudes of $M^*_{\max}$ for the given interval are obtained by applying the condition $f'(\omega_i t) = 0$ to (14). $f'(\omega_i t)$ represents the derivative of $f(\omega_i t)$ with respect to $\omega_i t$. For the intervals $[\frac{\pi}{3}, \frac{\pi}{2}]$ and $[\frac{\pi}{2}, \frac{2\pi}{3}]$, the conditions to find the extreme points of $M^*_{\max}$ are expressed by

$$f'(\omega_i t) = \frac{d}{d(\omega_i t)} \left\{ \sin(\omega_i t) \cdot \sin\left(\omega_i t + \frac{\pi}{6}\right) \right\} = 0 \tag{15}$$

$$f'(\omega_i t) = \frac{d}{d(\omega_i t)} \left\{ \sin(\omega_i t) \cdot \sin\left(\omega_i t - \frac{\pi}{6}\right) \right\} = 0. \tag{16}$$

The solution of (15) and (16) provide $\omega_i t = \frac{5\pi}{12}$ and $\frac{7\pi}{12}$ respectively. The extreme amplitudes obtained for $M^*_{\max}$ at $\omega_i t = \frac{5\pi}{12}$ and $\frac{7\pi}{12}$ ($f(\frac{5\pi}{12})$ and $f(\frac{7\pi}{12})$) are equal to 0.933. The amplitudes obtained for $M^*_{\max}$ at the ends of two intervals $[\frac{\pi}{3}, \frac{\pi}{2}]$ and $[\frac{\pi}{2}, \frac{2\pi}{3}]$ are equal to 0.866. By comparing the amplitudes of $M^*_{\max}$ obtained at the extreme points ($\omega_i t = \frac{5\pi}{12}$ and $\frac{7\pi}{12}$) and at the ends of the two intervals ($\omega_i t = \frac{\pi}{3}$, $\frac{\pi}{2}$ and $\frac{2\pi}{3}$), the highest and lowest amplitudes obtained are 0.933 and 0.866, respectively.

Thus, the graphical as well as theoretical methods provide the same highest and lowest amplitudes of $M^*_{\max}$ equal to 0.933 and 0.866, respectively. As a result, the range in which the amplitudes of $M^*_{\max}$ varies is 0.067 which amounts 7% portion of M^*_{cabc}.

Therefore, in order to eliminate the intersection of $M^*_{\max}$ with the carrier wave, this 7% part of M^*_{cabc} requires to be raised above the carrier wave by increasing m'_c to 1.07.

At $m'_c = 1.07$, $M^*_{\max}$ completely rises above the carrier wave (saturates at unity) and consequently no zero voltage states are created in the dc voltage. This is an easy alternative to eliminate the zero voltage states from $V_{\rm dc}$ without complex modifications in the modulation waves. With $m'_c = 1.07$, the value of average dc-link voltage is slightly more than $1.5V_m$ as per (12).

It is known that the overmodulation operation of the converter injects the lower order harmonics into the converter output voltages and supply currents [31]–[36]. As the unmodulated portion of the modulation signal increases with the increase in modulation index, the harmonic injection into the output voltage and supply current waveforms are increased. The harmonic injection is highest when CSR and VSI operate in the six-step mode. For the traditional CSR, the range of variation obtained for the maximum amplitudes of M_{cabc} ($M_{\max}$) is 14% as verified from Fig. 5. Therefore, m_c required to eliminate the zero voltage states from the CSR operation is 1.14 with the same reason explained previously for the BCSR operation. The overmodulation operation of the CSR injects the lower order harmonics into the supply currents due to this 14% unmodulated portion of M_{cabc}. On the other hand, the elimination of zero voltage states from $V_{\rm dc}$, the BCSR operation requires 7% overmodulation as compared to 14% overmodulation of the traditional CSR. As a result, the unmodulated portion of the modulation signals in the BCSR operation remains less as compared to conventional CSR operation. Therefore, the harmonic injection into the supply currents of the BCSR stage is less as compared to the conventional CSR. Also, with $m'_c = 1.07$, the BCSR stage does not reach to the six-step operating mode and therefore the current distortion is not in the highest amount.

Fig. 4(b) illustrates the PWM of the BCSR stage with the overmodulation operation as explained above. For the given sampling period T_s, the switching signals S_a, S'_b, and S'_c are shown to be generated by comparison of M^*_{ca}, M^*_{cb}, and M^*_{cc} with the triangular carrier. Here, $M^*_{\max}$ (M^*_{ca}) is saturated at unity due to the overmodulation operation. It is observed that the intersection of modulation signal having the medium amplitude ($M^*_{cb} = M^*_{\rm mid}$) with the carrier wave creates the switching instants t_1 and t_2 for the generation of S'_b and S'_c. $M^*_{\rm mid}$ represents the medium amplitudes of the modulation waves M^*_{cabc} and is obtained by (17). The ON durations of the switching signals S'_b and S'_c are represented by t_a and t_b as shown in Fig. 4(b). Knowing the values of $M^*_{\rm mid}$ and T_s, the switching durations t_a and t_b are easily calculated using the expressions of (18) and (19). t_a and t_b obtained here are used to produce the carrier wave of VSI stage in the conventional modulation schemes to synchronize both converter stages of the IMC

$$M^*_{\rm mid} = \text{mid}(M^*_{ca}, M^*_{cb}, M^*_{cc}) \tag{17}$$

$$t_a = T_s \cdot M^*_{\rm mid} \tag{18}$$

$$t_b = T_s - t_a = T_s \cdot (1 - M^*_{\rm mid}). \tag{19}$$

The CBPWM scheme developed in this section provides a simple control for the BCSR stage of IMC without using the complicated duty cycle calculations, lookup tables and sector judgments.

B. Derivation of Modulation Scheme for VSI Stage of IMC

The THIPWM scheme of the conventional VSI presented in [29] and [30] is explained in Section III-B1. The new modulation scheme developed for the VSI stage of IMC is explained in Section III-B2.

1) Modulation of Conventional VSI: The modulation signals for the traditional VSI are calculated using (20) according to THIPWM scheme. Here, the offset value 0.5 is added to the modulation signals to enable its comparison with the unidirectional carrier wave

$$M_{vABC} = \frac{m_v}{2}\left\{\sin\left(\omega_o t - \frac{2\pi k}{3}\right) + 0.17\sin 3\omega_o t\right\} + 0.5 \tag{20}$$

where M_{vABC} represents the three output modulation signals M_{vA}, M_{vB}, and M_{vC} for $k \in \{0, 1, 2\}$. ω_o represents the required angular frequency of the output voltages. m_v represents the modulation index which is defined as the ratio of peak amplitude of the required output voltage (phase quantity) to the input dc voltage $\frac{V_{om}}{V_{\rm dc}}$. For the specific output voltage condition in the conventional VSI, V_{om} is constant in addition to the constant input dc voltage $V_{\rm dc}$. As a result, the instantaneous amplitude of m_v is considered constant for a given output voltage.

The comparison of modulation signals M_{vABC} with the unidirectional carrier wave produces the required gate pulses for the traditional VSI switches.

2) Modulation of VSI Stage of IMC: In the IMC, as discussed in the previous section, pulsating $V_{\rm dc}$ is produced due to the absence of energy storing element. Therefore, it is necessary to modify the modulation signals of (20) to compensate the effect of $V_{\rm dc}$ ripple from the output voltages. The modified modulation signals $M^*_{\rm VABC}$ are obtained by modifying m_v based on its relation with $V_{\rm dc}$ as given in

$$M^*_{\rm VABC} = \frac{m'_v}{2}\left\{\sin\left(\omega_o t - \frac{2\pi k}{3}\right) + 0.17\sin 3\omega_o t\right\} + 0.5 \tag{21}$$

where $m'_v = \frac{m_v}{V_{\rm rip}}$ as per the definition of m_v described in Section III-B1. In order to create the zero voltage states on the VSI stage and hence enabling the ZCS operation of the BCSR switches, m'_v is always selected in the range $0 \le m'_v < 1$, as discussed in Section II.

As discussed in Section II, in order to produce the balance between input and output voltages as well as to obtain the ZCS on the BCSR stage, it is required to synchronize both stages of the IMC. In the conventional CBPWM techniques, this target is achieved by aligning the peak of the VSI carrier wave with the switching instants created on the BCSR stage. Fig. 6(a) illustrates the PWM of VSI stage synchronized with the BCSR stage operation for the one sampling period T_s. It is shown that the switching durations t_a and t_b of the BCSR stage are used to produce the rising and falling slopes of the VSI stage carrier wave. The comparison of the modulation wave M^*_{VA} with this carrier wave producing the switching signal S_A for the VSI stage

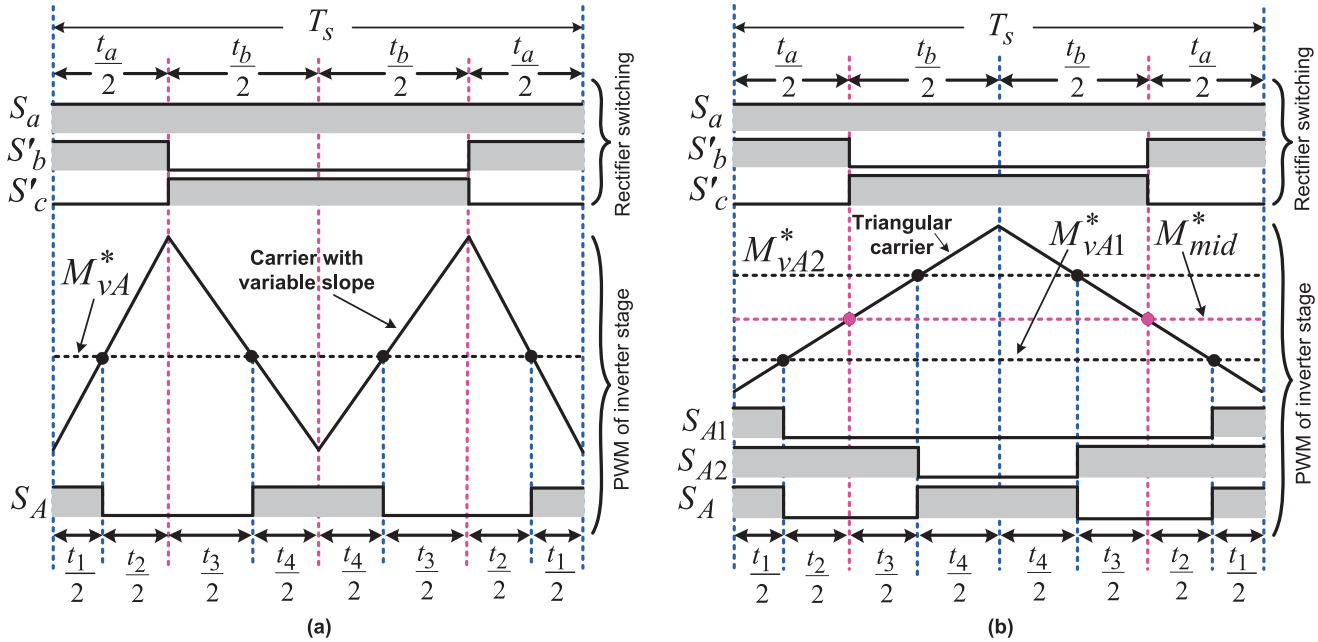

Fig. 6. PWM of VSI stage with (a) conventional carrier-based modulation technique and (b) proposed modulation technique.

is shown in Fig. 6(a). Corresponding pulse durations of S_A are represented by t_1 and t_4 which are also shown in Fig. 6(a). t_1 and t_4 are obtained by the comparison of M^*_{VA} with the carrier slopes derived based on the switching duration t_a and t_b of the BCSR stage, respectively. Therefore, for the given switching durations t_a and t_b as well as modulation signal M^*_{VA}, the ON state switching durations t_1 and t_4 of S_A can be calculated as given by

$$t_1 = t_a \cdot M^*_{VA} = T_s \cdot M^*_{\text{mid}} \cdot M^*_{VA} \tag{22}$$

$$t_4 = t_b \cdot M^*_{VA} = T_s \cdot (1 - M^*_{\text{mid}}) \cdot M^*_{VA}. \tag{23}$$

The proposed modulation technique establishes the synchronism between the two stages of IMC without producing the carrier with variable slopes for the VSI stage. For that, the switching durations t_a and t_b of the BCSR stage are used to modify the modulation signals of VSI stage instead of modifying the carrier wave of VSI. The new modulation signals should be able to produce the switching signals for the VSI stage with the same pulse durations as produced in the conventional modulation schemes.

Consider the switching durations t_1 and t_4 expressed by (22) and (23) obtained by the conventional modulation of the VSI stage. The new modulation signals M^*_{VA1} and M^*_{VA2} corresponding to the durations t_1 and $T_s - t_4$ are calculated in (24) and (25), respectively, for M^*_{VA}. In the similar way, the new modulation equations M^*_{VB1} and M^*_{VB2} as well as M^*_{VC1} and M^*_{VC2} corresponding to M^*_{VB} and M^*_{VC} are derived for phase-B and C, respectively.

Now, M^*_{VA1} and M^*_{VA2} are compared with the triangular carrier which generates the two switching signals S_{A1} and S_{A2}, as shown in Fig. 6(b). The ON switching state of S_{A1} and OFF switching state of S_{A2} correspond to the durations t_1 and t_4, respectively. Therefore, S_{A1} and S_{A2} are combined appropriately (X-NOR operation) according (26) to obtain the switching pattern S_A which is similar to that obtain by the conventional modulation scheme shown in Fig. 6(a). Similarly, the switching patterns of S_B and S_C for phase-B and C are determined, respectively

$$M^*_{VA1} = \frac{t_1}{T_s} = M^*_{\text{mid}} \cdot M^*_{VA} \tag{24}$$

$$M^*_{VA2} = 1 - \frac{t_4}{T_s} = 1 - ((1 - M^*_{\text{mid}}) \cdot M^*_{VA}) \tag{25}$$

$$S_A = S_{A1} \cdot S_{A2} + \overline{S}_{A1} \cdot \overline{S}_{A2}. \tag{26}$$

The modulation equations derived in (24) and (25) are simple and require only M^*_{mid} of BCSR stage and basic modulation signal M^*_{VA}. The new control schemes developed in this article for the BCSR and VSI stages of IMC are included in Fig. 7. The various modulation signals obtained corresponding to the BCSR and VSI stage control are also represented in Fig. 7.

The voltage gain of the BCSR stage (ratio of average dc-link voltage to the peak input phase voltage, q_R) attains the value of $3/2$ (slightly more than $3/2$ at $m'_c = 1.07$) due to the elimination of zero voltage states as discussed in the previous section. The introduction of the third harmonic in the fundamental modulating wave increases the voltage gain of the VSI stage (ratio of peak output phase voltage to the average dc-link voltage, q_V) to $1/\sqrt{3}$ [30]. Therefore, overall VTR (q_T) of the IMC is obtained by the following expression:

$$q_T = q_R \cdot q_V = \frac{3}{2} \cdot \frac{1}{\sqrt{3}} = \frac{\sqrt{3}}{2}. \tag{27}$$

The control of BCSR and VSI stages of the IMC does not require any complex calculations based on the lookup tables or space vector modulation. The CBPWM of both converter stages

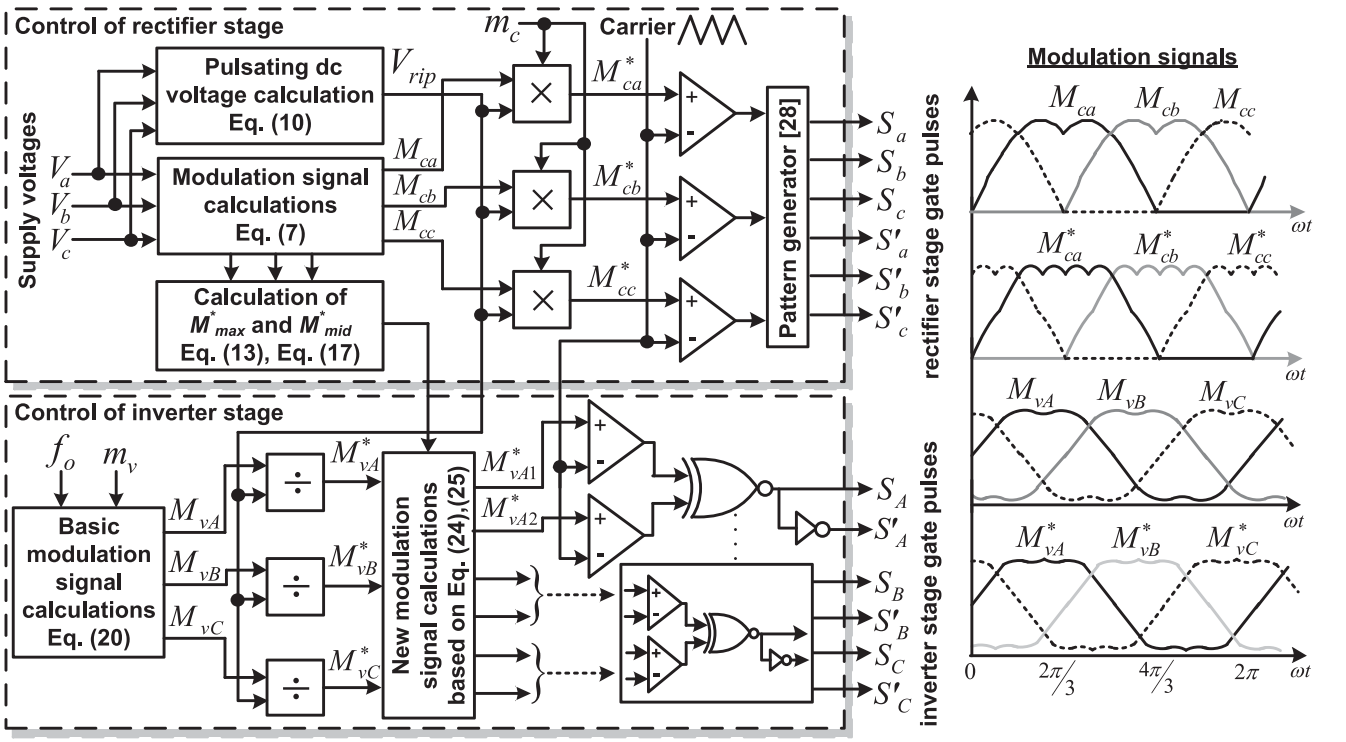

Fig. 7. Proposed single carrier-based modulation technique for IMC.

TABLE I
SIMULATION PARAMETERS

Parameter	Value
Supply voltages (V_s)	80 V
Supply frequency (f_s)	50 Hz
Input filter resistance (R_f)	58 Ω
Input filter inductance (L_f)	1 mH
Input filter capacitance (C_f)	15 μF
Load resistance (R_L)	10 Ω
Load inductance (L_L)	10 mH
Voltage transfer ratio (q_T)	0.75
Load frequency (f_o)	50 Hz
Carrier frequency (f_c)	5.7 kHz

using the simple modulation equations and a single triangular carrier reduces the complexity of implementation up to the great extent.

IV. SIMULATION RESULTS

The simulation of the IMC topology with the proposed modulation technique is carried out using PSIM environment. The input and output performances of the IMC obtained with the presented technique are compared with those obtained by the SVPWM technique of IMC in this section. The selection of the various parameters used in the simulation are according to Table I.

The simulation waveforms of the various control circuit signals generated by the presented CBPWM scheme are represented in Fig. 8. The modulation waves of the BCSR stage (M^*_{ca})

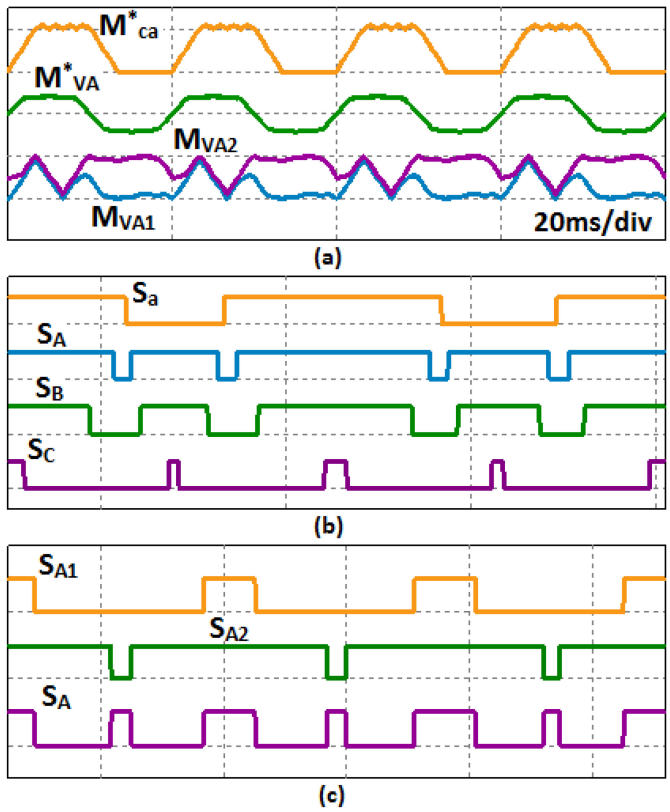

Fig. 8. Simulation results. (a) BCSR and VSI stage modulation signals. (b) BCSR stage switching signal S_a and VSI stage switching signals S_A, S_B, S_C. (c) VSI stage switching signals S_{A1}, S_{A2}, and S_A.

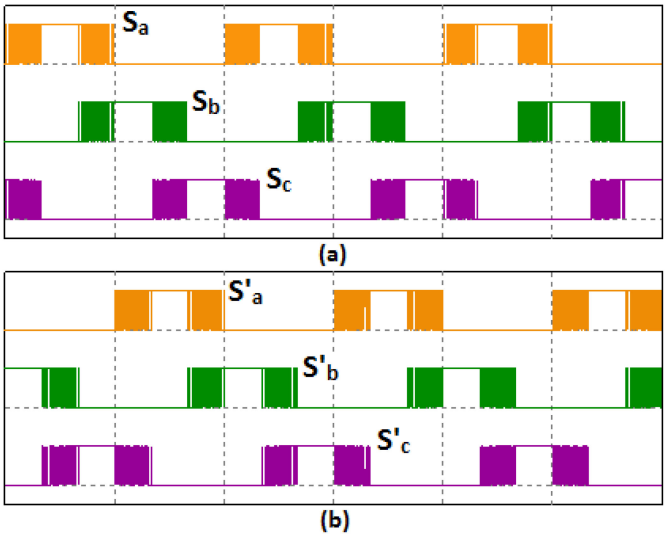

Fig. 9. Simulation results. (a) Switching signals S_a, S_b, and S_c for the upper group of BCSR switches. (b) Switching signals S'_a, S'_b, and S'_c for the lower group of BCSR switches.

and the VSI stage ($M^*_{\rm VA}$, $M^*_{\rm VA1}$, $M^*_{\rm VA2}$) are depicted in Fig. 8(a). Fig. 8(b) depicts the commutation of the BCSR switch S_a with reference to the upper inverter switches S_A, S_B, and S_C. The ZCS of the switch S_a is clearly observed. The switching signals S_{A1}, S_{A2}, and S_A of the VSI stage are shown in Fig. 8(c). It is shown that the switching signal S_A is obtained by the logical operation of S_{A1} and S_{A2}, as given in (26). The switching pulses obtained for the upper and lower group of BCSR switches are shown in Fig. 9(a) and (b), respectively.

The simulation results of the power circuit obtained for the presented CBPWM technique and SVPWM technique are illustrated in Figs. 10 and 11, respectively. Fig. 10(a) includes the simulation results of the supply voltage (V_a), supply current (I_a), and dc-link voltage ($V_{\rm dc}$) waveforms obtained by the new CBPWM technique. It is observed that the waveforms of Fig. 10(a) are nearly equal to the waveforms represented in Fig. 11(a). The supply current is near to sinusoidal nature and in phase with the supply voltage for the both techniques. The zero voltage states are completely eliminated from the dc-link voltage due to the overmodulation operation ($m'_c = 1.07$) of the BCSR stage, as per the discussion of Section III-A2. Whereas, the zero voltage states in the SVPWM technique are eliminated by normalizing the duty cycles of BCSR stage, as discussed in Section II.

Figs. 10(b) and 11(b) represent the load side waveforms of phase voltage (V_A), line voltage (V_{AB}), and current (I_A) for the presented new CBPWM and SVPWM techniques, respectively. As observed, the load current waveform is nearly sinusoidal for the both modulation techniques. The waveforms of V_A and V_{AB} are also similar in nature for the both cases.

Figs. 10(c) and 11(c) represent the harmonic spectrums of supply and load currents for the new CBPWM and SVPWM techniques, respectively. The supply current THD are 5.5% and 4.9% in the new CBPWM and SVPWM techniques,

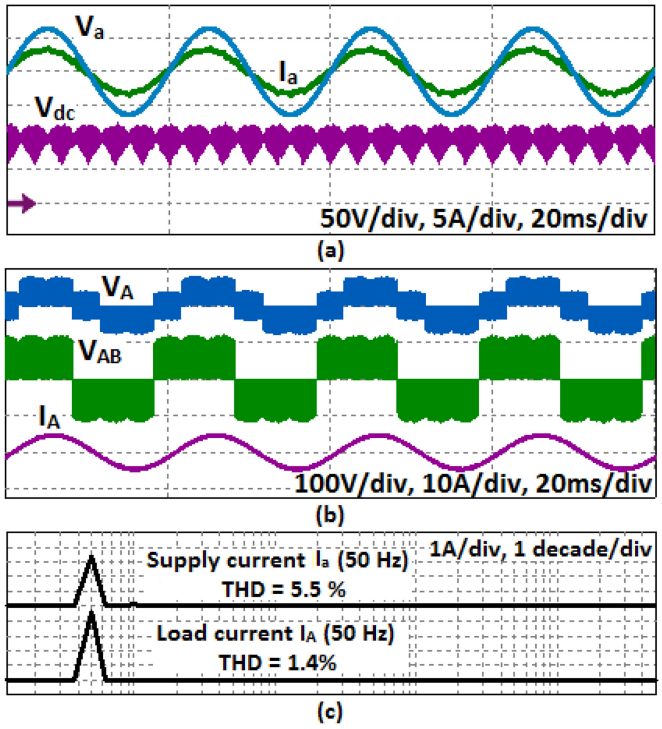

Fig. 10. Simulation results of proposed CBPWM technique. (a) Supply voltage (V_a), supply current (I_a), dc-link voltage ($V_{\rm dc}$). (b) Load side phase voltage (V_A), line voltage (V_{AB}), load current (I_A). (c) Harmonic spectrums of supply current (I_a) and load current (I_A).

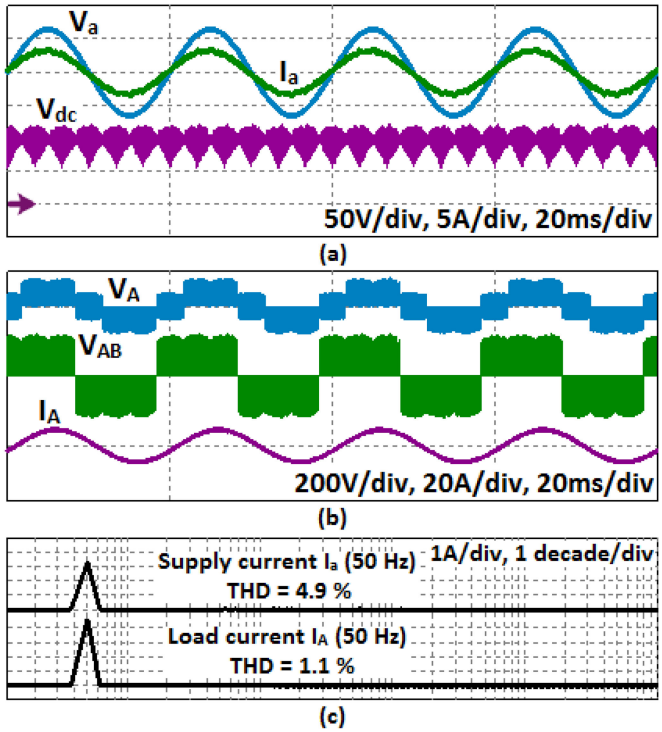

Fig. 11. Simulation results of SVPWM technique. (a) Supply voltage (V_a), supply current (I_a), dc-link voltage ($V_{\rm dc}$). (b) Load side phase voltage (V_A), line voltage (V_{AB}), load current (I_A). (c) Harmonic spectrums of supply current (I_a) and load current (I_A).

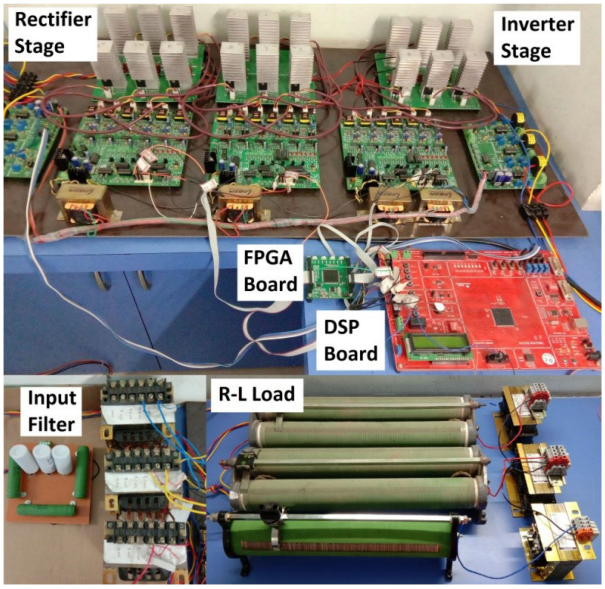

Fig. 12. Experimental setup of IMC implemented with the proposed CBPWM method.

respectively. The load current THD measured for the CBPWM and SVPWM techniques are 1.4% and 1.1%, respectively. The supply and load current THD for the new CBPWM technique are little more than those obtained in the SVPWM technique. This is due to the overmodulation operation of the BCSR stage of the IMC adopted for the elimination of the zero voltage states from the dc voltage. However, there is no significant difference between THDs of the supply and load currents in presented CBPWM and SVPWM techniques.

From the simulation results presented in this section, it is confirmed that the presented CBPWM technique yields the required input and output performances same as the conventional modulation techniques of the IMC.

V. Experimental Results

The experimental setup of the IMC is developed in the laboratory to approve the performance of the proposed CBPWM technique, as shown in Fig. 12. The control part of the proposed technique is implemented by using the 32-bit DSP (TMS320F28335) and FPGA (SPARTAN-6). The various calculations required to generate the modulation waves as well as PWM signals of the BCSR and VSI stages are performed by the DSP. The various logical operations and the commutation delay required to apply on the PWM signals of the BCSR and VSI stages are performed in the FPGA. The BCSR and VSI stages of the IMC have been built using the power IGBTs-FGA25N120ANTD. The parameter values used in the experimental setup are indicated in Table II.

The experimental results of the control circuit are shown in Figs. 13 and 14. Fig. 13(a) shows the modulation signals M^*_{ca} and M^*_{VA} of the BCSR and VSI stages. The ZCS operation of the BCSR stage as well as the relation of the switching signal S_A with S_{A1} and S_{A2} of the VSI stage are clearly verified in the Fig. 13(b) and (c), respectively. The switching signals for the upper and lower group of BCSR switches are shown in Fig. 14(a) and (b), respectively.

TABLE II
Experimental Parameters

Parameter	Value
Supply voltages (V_s)	80 V
Supply frequency (f_s)	50 Hz
Input filter resistance (R_f)	68 Ω
Input filter inductance (L_f)	2.7 mH
Input filter capacitance (C_f)	10 μF
Load resistance (R_L)	10 Ω
Load inductance (L_L)	10 mH
Voltage transfer ratio (q_T)	0.75
Load frequency (f_o)	50 Hz
Carrier frequency (f_c)	5.7 kHz

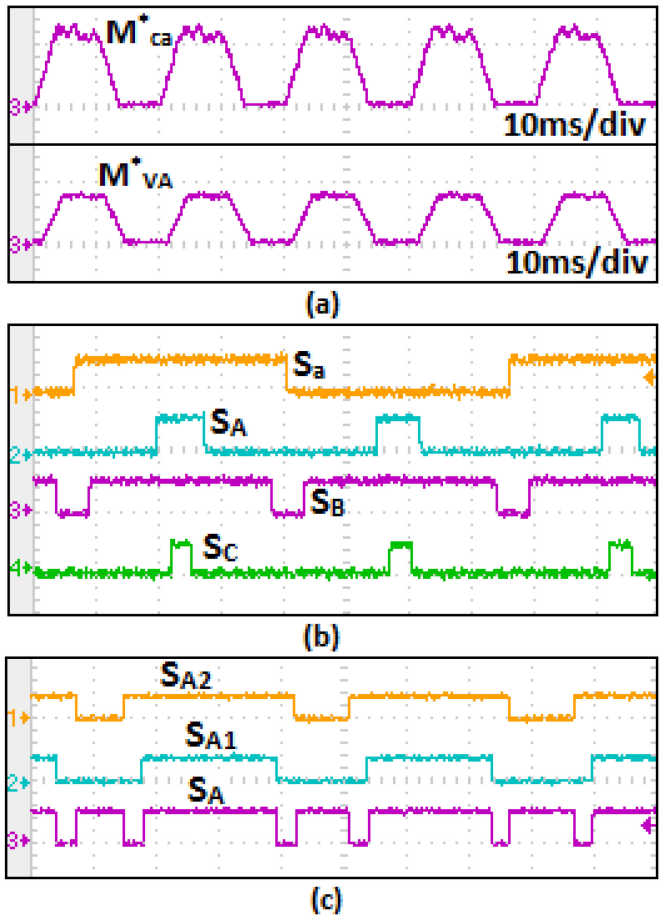

Fig. 13. Experimental results. (a) BCSR and VSI stage modulation signals. (b) BCSR stage switching signal S_a and VSI stage switching signals S_A, S_B, S_C. (c) VSI stage switching signals S_{A1}, S_{A2}, and S_A.

Fig. 15(a) shows the experimental waveforms of supply voltage (V_a), supply current (I_a), and dc-link voltage ($V_{\rm dc}$). The sinusoidal nature of the supply current, near to unity power factor and the elimination of zero voltage states from $V_{\rm dc}$ are the expected results as explained in the previous section. The load side waveforms of phase voltage (V_A), line voltage (V_{AB}), and current (I_A) are depicted in Fig. 15(b). The load current waveform is near to sinusoidal nature as obtained in the simulation results. It is noticed that all the waveforms obtained by the

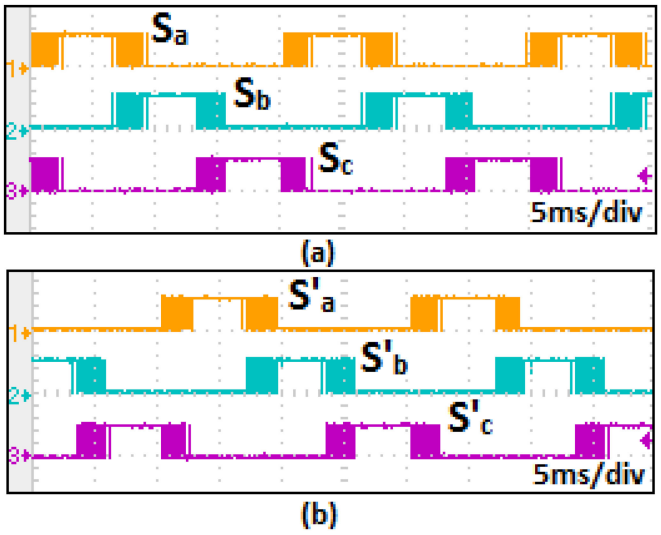

Fig. 14. Experimental results. (a) Switching signals S_a, S_b, and S_c for the upper group of BCSR switches. (b) Switching signals S'_a, S'_b, and S'_c for the lower group of BCSR switches.

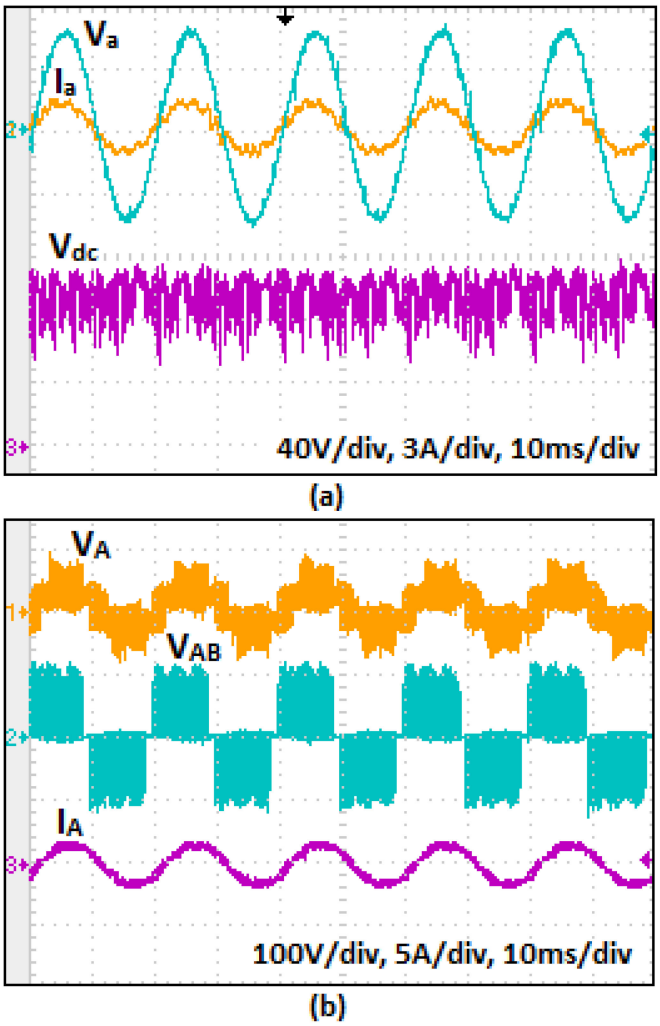

Fig. 15. Experimental results. (a) Supply voltage (V_a), supply current (I_a), and dc-link voltage ($V_{\rm dc}$). (b) Load side phase voltage (V_A), line voltage (V_{AB}), and load current (I_A).

experimental testing are approximately close to the waveforms obtained by the simulation.

The various mathematical, logical, and conditional operations required to implement the proposed CBPWM technique are less as compared to those required for the SVPWM technique. The total time required for the execution of the proposed CBPWM technique is approximately 10 μs, as compared to 16 μs required by the SVPWM technique of the IMC. The low value of execution time as compared to the SVPWM technique clearly indicates the less computational burden offered by the presented CBPWM scheme.

In this section, the performance of IMC with the proposed CBPWM technique is approved by the experimental testing. The coherence between simulation and experimental results of the IMC prove the effectiveness of the new CBPWM technique of providing the required input and output performances.

VI. Conclusion

This article develops a new CBPWM technique for controlling the IMC with the reduced complexity. The proposed technique employs a single triangular carrier for producing the PWM signals for the BCSR and VSI stages. The simple modulation equations are derived in this technique to enable the use of single triangular carrier on both stages of the IMC. In comparison with the previously introduced single CBPWM techniques, the proposed technique provides the very simple modulation equations which do not require any reference of SVPWM technique and sector judgements. As a result, the presented CBPWM technique is more easily implemented in comparison with the existing single carrier-based modulation techniques. The IMC control with the given modulation technique provides the sinusoidal input/output waveforms, VTR of 0.866 and zero current commutation on the rectifier stage similar to the conventional modulation methods. The proposed work is supported by the simulation and the experimental results.

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