A High Conversion Ratio and High-Efficiency Bidirectional DC–DC Converter With Reduced Voltage Stress

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***Abstract*—A dc–dc converter is proposed to achieve a high voltage conversion ratio for bidirectional power flow applications. The nonisolated topology is optimally designed to integrate both the switched capacitor and coupled inductor techniques for high efficiency. The windings of the coupled inductor are stacked at the low voltage source, which transfers any leakage energy of the coupled inductor directly into the output port and simplifies the clamping circuit. The optimal design keeps the voltage stress on the main switches low for the entire duty cycle operation. Thus, the converter demonstrates the advantage of wide-voltage gain based on common ground and low and steady voltage stress in both buck and boost modes of its operation. Furthermore, the converter can realize zero-voltage switching through the synchronous rectifiers without requiring extra hardware circuitry to enhance conversion efficiency. The operation principle, including the steady-state analysis, dynamic modeling, controller design, efficiency analysis, and optimization, are discussed in detail and verified by the experimental test. The prototype substantiates the theoretical analysis and soft-switching operation. The converter exhibits the capability for load and line regulation and demonstrates a peak efficiency of 96.38% in the boost mode and 95.61% in the buck mode of operation.**

***Index Terms*—Bidirectional power flow, dc-dc power converters, energy storage, switched capacitor circuits.**

I. Introduction

BIDIRECTIONAL dc–dc converters become key system components for modern and distributed energy systems when energy storage is integrated [1]. High voltage conversion ratio is required to accommodate the voltage difference between the rechargeable battery side and dc grid. Research focuses on the development of low-cost, high efficiency, and reliable topologies to meet the increasing requirement [2]. The bidirectional dc–dc converters are classified into two categories: isolated, and nonisolated versions.

Manuscript received January 9, 2020; revised March 8, 2020; accepted April 6, 2020. Date of publication April 12, 2020; date of current version July 20, 2020. Recommended for publication by Associate Editor B. P. McGrath. *(Corresponding author: Waqas Hassan.)*

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Digital Object Identifier 10.1109/TPEL.2020.2987083

The isolated converters usually utilize a high-frequency transformer to support a high conversion ratio of voltage. The gain of these converters depends on the turns ratio of the transformer with the utilization of the half-bridge [3] and full-bridge [4], [5]. For a high voltage conversion ratio, the transformer design becomes challenging with the consideration of high-frequency core losses and harmful leakage inductance. One well-known topology is the dual active bridge (DAB), which typically requires eight (8) active switches to maintain the bidirectional operation. It shows the capability of zero-voltage switching (ZVS) and power flow controllability [6]. However, high conduction loss and high cost can be expected due to the high component count. Moreover, the efficiency of DAB is challenging to be maintained high for a full power range due to the existing circulating power and potential loss of soft switching [7], [8]. When galvanic isolation becomes unnecessary, the nonisolated topologies can be considered, thanks to low cost and high efficiency.

The nonisolated bidirectional dc–dc converters are commonly derived from the conventional topologies, such as the buck/boost, SEPIC/Cuk/Zeta, multiple levels, switched capacitor, and coupled inductor. A nonisolated bidirectional dc–dc converter consisting of two conventional boost converters is proposed in [9]. The converter attains high voltage gain but reveals high voltage stress on switches. The SEPIC/Cuk/Zeta converters show constraints on conversion efficiencies due to the cascaded structures. The switched capacitors bidirectional converters [10], [11] can achieve a high voltage gain. Also, their structure and control schemes are simple to implement. However, the drawback of the switched capacitors technique is the high current stress and switching loss. A switched capacitor bidirectional converter proposed in [12] can achieve a wide voltage gain range with four switches but has lower efficiency due to high conduction losses.

The coupled inductor dc–dc converter received considerable attention to attain high voltage gain due to its simple structure comprising a fewer number of components compared to other topologies [13]. By tapping or coupling the inductor of the conventional boost/buck converter, the high voltage gain can be realized [14]. The coupled inductor topologies exchange energy at a different time instant and utilize the turn ratio of the coupled inductor to achieve high voltage gain. By optimizing the design of magnetic components, the size and volume of the

coupled inductor can be significantly reduced; therefore, a high power density can be realized [15]. The bipolar excitation of the magnetic core makes these topologies suitable even for high power applications [16]. The bidirectional converter presented in [16] was constructed for the nominal 48–360 V voltage conversion at 2 kW, and achieve 95% peak efficiency and 92.5% average efficiency both in buck and boost modes of operation. A significant challenge in coupled inductor topologies is to clamp the leakage energy of the coupled inductor and reduce the voltage spike and stress across the switches. The clamp/snubber circuits are usually utilized to constrain voltage stress. The active clamp circuits can also realize ZVS operation [17]. The leakage energy can be recycled to increase the conversion ratio and efficiency further. The high step-up converter reported in [18] employs an active clamp circuit, which enhances the conversion efficiency by 3% compared to the hard switching counterpart. Furthermore, combing coupled inductor technique with switched capacitor ultralarge gain can be attained [19], [20].

The early development of the unidirectional power converters for the high conversion gain is commonly utilized to develop bidirectional topologies for high efficiency. A bidirectional converter proposed in [21] can achieve a high conversion ratio, but it requires five active switches and three intermediate capacitors for the operation. A soft-switching bidirectional converter presented in [22] integrates a dual-active half-bridge converter with a conventional buck–boost converter to attain a high conversion ratio. However, the voltage stress on the low side switch is relatively high compared to other converters with the same component count. Moreover, the voltage stress on the switch connected with the high voltage terminal is about 75% of the output voltage. The converter presented in work in [23] and [24] utilizes antiparallel diodes of the active switches to realize soft-switching to improve efficiency further. A nonisolated high step-up/down bidirectional converter presented in [25] can realize high efficiency and high gain; however, the utilization of switches in boost mode is limited, and the floating high voltage side ground limits its applications. In [23] and [25], the low and high voltage sides are separated by a power switch; thus, the uncommon ground is faced. The high-frequency pulsewidth modulation voltage is the potential difference between the high and low voltage terminal, which results in added EMI and *du/dt* issues. In [24] and [26], the coupled inductor is connected in a reverse manner to realize high voltage gain at a lower turn ratio. However, the voltage stress on the high voltage side switch is almost half of the high output voltage. The configuration proposed in [26] is based on a cascaded structure with integrated three winding and diode-capacitor multiplier to achieve ultralarge voltage gain, but the additional winding increases the size and cost of the converter. Moreover, the efficiency decreases at high power due to the cascaded structure. The bidirectional converter presented in [27] is SEPIC derived which utilizes charge pump and tapped inductor techniques to attain high voltage gain. However, the high voltage side switch suffers from high voltage stress, which is equal to the output voltage. Moreover, it has three intermediate capacitors and two magnetic cores; thus, high component count. In [28], the converter utilizes two coupled inductors and switched capacitor circuit for an ultrahigh step-up and down conversion ratio; therefore, it shows the high cost and large size. A new family of high gain converters derived from impedance source dc–dc converters are also proposed in the literature for high step-up applications [29]. These converters have relatively lower voltage stresses on devices compared to impedance source converters. A coupled inductor bidirectional dc–dc converter with soft-switching capability consisting of four switches and two intermediate capacitors is proposed in [30], but the gain is moderate, and the efficiency is relatively lower than other topologies. In all topologies, the voltage stress on the switch connected with high voltage terminal is higher than the low voltage side switch.

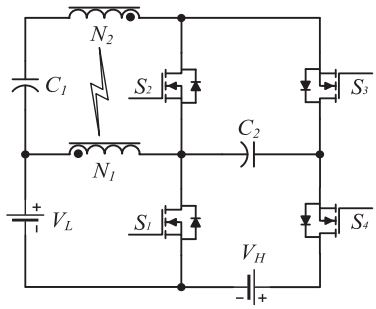

Fig. 1. Proposed bidirectional converter.

In this article, a bidirectional dc–dc converter is proposed adopting the technologies of the switched capacitor and coupled inductor techniques, which have shown effectiveness in unidirectional power conversion. It utilizes four switches and two intermediate capacitors. The secondary winding of the coupled inductor is stacked at the input side that is different from the conventional cascaded and stacked coupled inductor topologies. Thus, the configuration does not require any snubber/clamp circuit to mitigate harmful voltage spike across the switch. The leakage energy is directly transferred to the output port. The voltage stress on the high voltage side switch is significantly lower than that of other topologies. The converter can realize the ZVS in boost and buck mode through the synchronous rectifiers, thus switching losses are reduced. Furthermore, the topology realizes a common ground for both terminals.

The principle of the operation is discussed in Section II. The steady-state analysis of both buck and boost modes is explained in Section III. Moreover, efficiency and loss analysis are carried out thoroughly for efficiency optimization in both buck and boost mode of operation. The dynamic modeling and controller design are elaborated for closed-loop design. The circuit parameters designs, including conditions for ZVS operation and power density calculations, are discussed in Section III. The detailed experimental results, including dynamic performance and voltage regulation capability, are demonstrated in Section IV.

II. Topology Introduction and Operating Principle

The proposed bidirectional topology is illustrated in Fig. 1, which consists of four active switches, S_1–S_4, two intermediate capacitors C_1 and C_2, and one coupled inductor with the winding turns ratio, N_1: N_2. The secondary winding is stacked with the

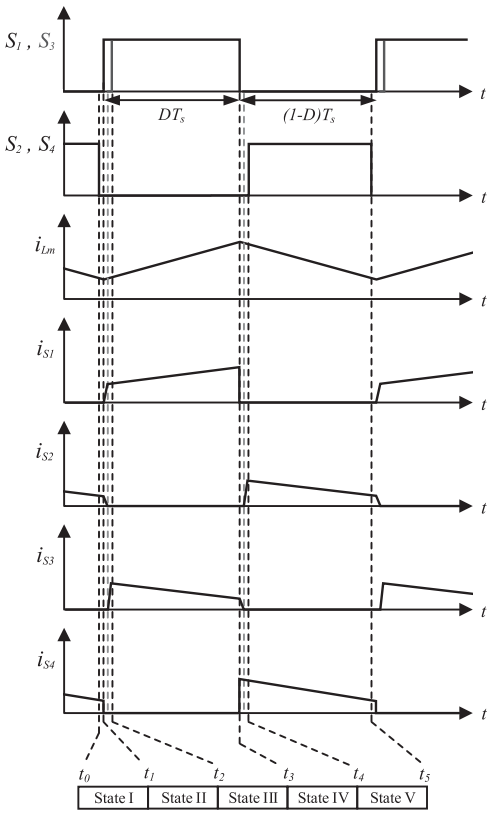

Fig. 2. Vital converter waveforms in boost mode.

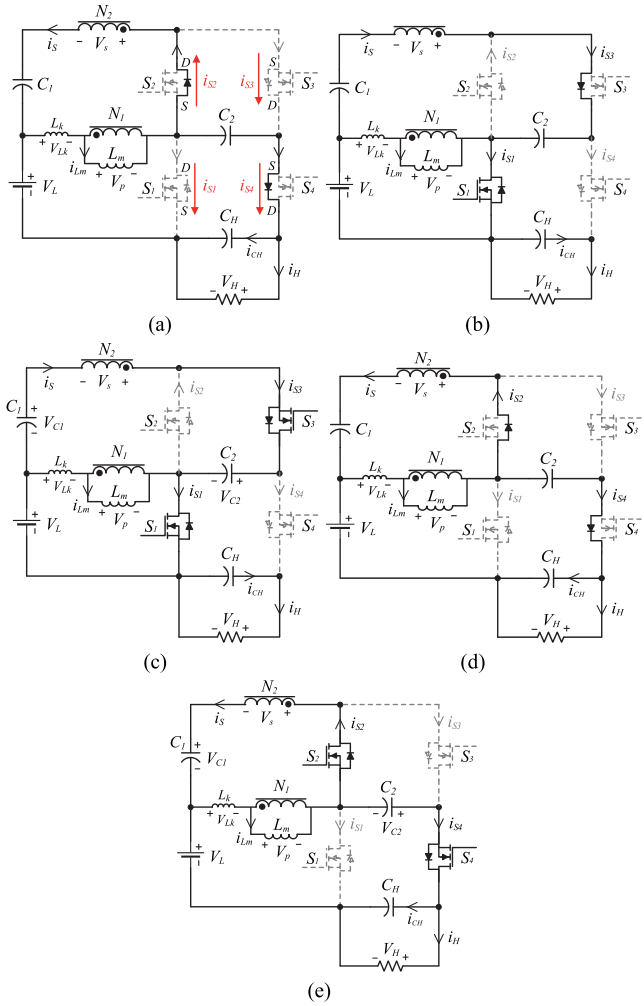

Fig. 3. Operational states in the boost mode. (a) State I $[t_0 - t_1]$. (b) State II $[t_1 - t_2]$. (c) State III $[t_2 - t_3]$. (d) State IV $[t_3 - t_4]$. (e) State V $[t_4 - t_5]$.

lower side terminal, V_{L}, and the capacitor, C_1. The intermediate capacitor, C_2, is utilized for the switched-capacitor technique to realize high conversion gain for the high side, V_{H}. The switched capacitor also clamps the voltage stress on switches. Thus, an additional snubber circuit is not required in the topology for clamping the leakage energy. The leakage energy directly goes to the output port. The steady-state operation characteristics in both boost and buck mode are analyzed and based upon the following assumptions.

1) All the power devices are considered ideal, i.e., zero resistance. However, the parasitic capacitance of power switches is considered in the analysis.
2) All passive components are ideal, i.e., zero resistance.
3) All capacitance is significant to maintain the cross-voltage constant in the following steady-state analysis.
4) The magnetizing inductance L_m, the leakage inductance L_k, and an ideal transformer models the coupled inductor.

A. Boost Mode

Five operating states are defined in the boost mode of operation, which is illustrated by the vital waveforms in Fig. 2. Fig. 3 illustrates the equivalent circuits in coordination with the five operating states. The zero-voltage switching (ZVS) can be realized by synchronous rectifiers in this mode. The reference direction of current for the MOSFET S_1 is defined from drain (D) to source (S). The reference direction of current for the switches, S_2, S_3, and S_4, is defined from source (S) to drain (D), as shown in Fig. 3(a). The current in S_2, S_3, S_4, is flowing from source to drain in boost mode of operation and indicated as the positive value, as shown in Fig. 2. In the boost mode, the power source is the low-voltage side, V_{L}, and the high-voltage side is modeled as a resistor in parallel with a capacitor.

State I [t_0–t_1]: At $t = t_0$, the switches S_2 and S_4 are turned OFF, as shown in Fig. 3(a). The current flowing through switches shifts into the respective antiparallel diodes. Thus, both switches are turned OFF under the ZVS condition. This operating state ends with the switching-ON of S_1.

State II [t_1–t_2]: At $t = t_1$, S_1 is turned ON, as illustrated in Fig. 3(b). The antiparallel diode of S_4 becomes reverse biased. The current passing through the antiparallel diode of S_2 decreases linearly due to the leakage inductance. The antiparallel diode of S_2 becomes reverse biased when the secondary side current of the coupled inductor is zero. Then, the secondary side current changes direction and discharges output capacitance, C_{S3}, and turns ON the antiparallel diode of S_3 and increases linearly, as shown in Fig. 2. The conduction of the antiparallel diode of S_3 clamps the drain to source voltage close to zero. The current flowing from source to drain discharges C_{S3}. The

dc voltage source, V_{L}, charges the magnetizing and leakage inductors. The state ends with the reverse-biasing status of the antiparallel diode in S_3.

State III [t_2–t_3]: At $t = t_2$, S_3 is turned ON with ZVS due to the early conduction of its antiparallel diode, as illustrated in Fig. 3(c). The capacitor C_1 discharges and transfers its stored energy to C_2 through the coupled inductor. The capacitor C_{H} sustains the load; meanwhile, the magnetizing and leakage inductors continue to be charged by input dc voltage source. This operating state ends, when switches S_1 and S_3 are turned OFF.

State IV [t_3–t_4]: At $t = t_3$, S_1 and S_3 are turned OFF, as shown in Fig. 2. The leakage energy quickly discharges the output capacitance, C_{S4}, and antiparallel diode of S_4 becomes forward biased instantaneously, which clamps the drain to source voltage of S_4 close to zero. The current flowing from source to drain discharges C_{S4}. The leakage energy directly clamps to capacitor C_{H}. The secondary side current decreases linearly and continues to flow through the antiparallel diode of S_3. Hence, S_3 is turned OFF at ZVS. When the current of the secondary winding is zero, the antiparallel diode of S_3 becomes reverse-biased. The secondary side current of the coupled inductor changes direction and discharges output capacitance, C_{S2}, and then turns ON the antiparallel diode of S_2, as shown in Fig. 3(d). The current flowing from source to drain discharges C_{S2}. The conduction of the antiparallel diode of S_2 clamps the drain to source voltage close to zero. The magnetizing inductor charges C_1. Meanwhile, C_2 is discharged and delivers its energy to the output capacitor. This operating state ends with the turn-on of switches S_2 and S_4.

State V [t_4–t_5]: At $t = t_4$, S_2 and S_4 are turned ON, as shown in Fig. 3(e). The current passing through antiparallel diodes shifts into the respective switches S_2 and S_4 for continuous conduction. Therefore, both switches are turned ON at ZVS. The input voltage source and coupled inductor charge C_{H}. The capacitor C_2 continues to be discharged. This state is switched to State I when switches S_2 and S_4 are turned OFF, and their respective antiparallel diodes become forward biased.

B. Buck Mode

Seven operating states are defined in the buck mode of operation, which is illustrated by the critical waveforms in Fig. 4. Fig. 5 illustrates the equivalent circuits in coordination with the seven operating states. In the buck mode, the reference direction of current for the switches, S_2, S_3, S_4, is defined from drain (D) to source (S), as shown in Fig. 5(a). The reference direction of current for the MOSFET S_1 is defined from source (S) to drain (D). The current in S_1 is flowing from source to drain in buck mode of operation and indicated as the positive value, as shown in Fig. 4. In the buck mode, S_4 becomes the main switch, and the power source is switched to the high-voltage side, V_{H}, and the low-voltage side is modeled as a resistor in parallel with a capacitor.

State I [t_0 –t_1]: At $t = t_0$, S_1 and S_3 are turned OFF, as shown in Fig. 5(a). The current flowing through switch S_1 shifts into its antiparallel diode. Thus, S_1 turns OFF at ZVS. The current flowing through S_3 is zero. The secondary side current discharges output capacitance, C_{S2}, and shifts into the anti-parallel diode of S_2 for continuous conduction, which clamps the drain to source voltage close to zero. The secondary winding current continues through the antiparallel diode of switch S_2. This operating state ends with the switching-ON of S_2.

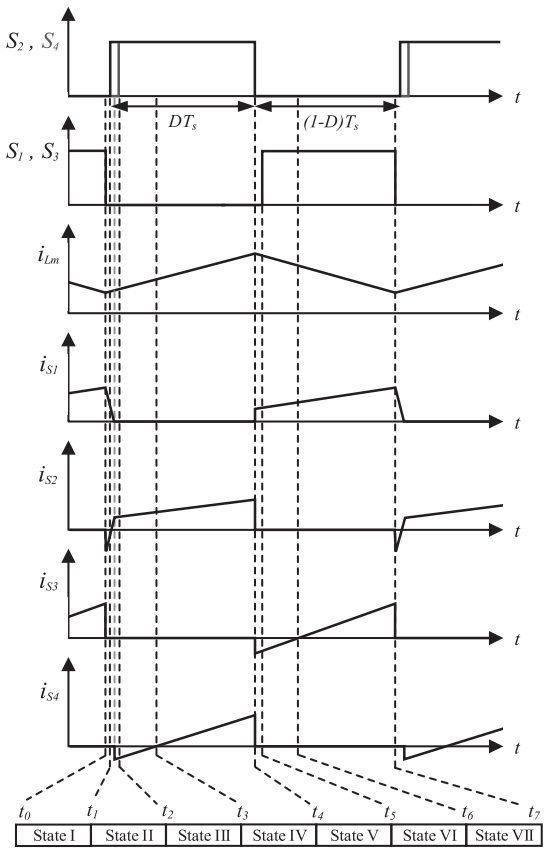

Fig. 4. Vital converter waveforms in buck mode.

State II [t_1–t_2]: At $t = t_1$, S_2 is turned ON at ZVS due to the early conduction of its antiparallel diode, as illustrated in Fig. 4. The current passing through the antiparallel diode of S_1 decreases. The antiparallel diode of S_1 is reverse biased when the secondary side current changes direction. Now the secondary side current discharges output capacitance, C_{S4}, and then continues through antiparallel diode of S_4. The conduction of the antiparallel diode of S_4 clamps the drain to source voltage of S_4 close to zero. Then, both C_1 and C_2 start to be discharged, as shown in Fig. 5(b). This operating state ends with the switching-ON of S_4.

State III [t_2–t_3]: At $t = t_2$, S_4 is turned ON at ZVS due to the early conduction of its antiparallel diode, as illustrated in Fig. 5(c). The capacitors C_1 and C_2 are discharged; meanwhile, C_{H} provides energy to the load. The magnetizing and leakage inductors are charged by capacitor C_1. This operating state ends when the current through S_4 changes its direction.

State IV [t_3–t_4]: At $t = t_3$, the current passing through switch S_4 becomes positive, as shown in Fig. 4. The high voltage

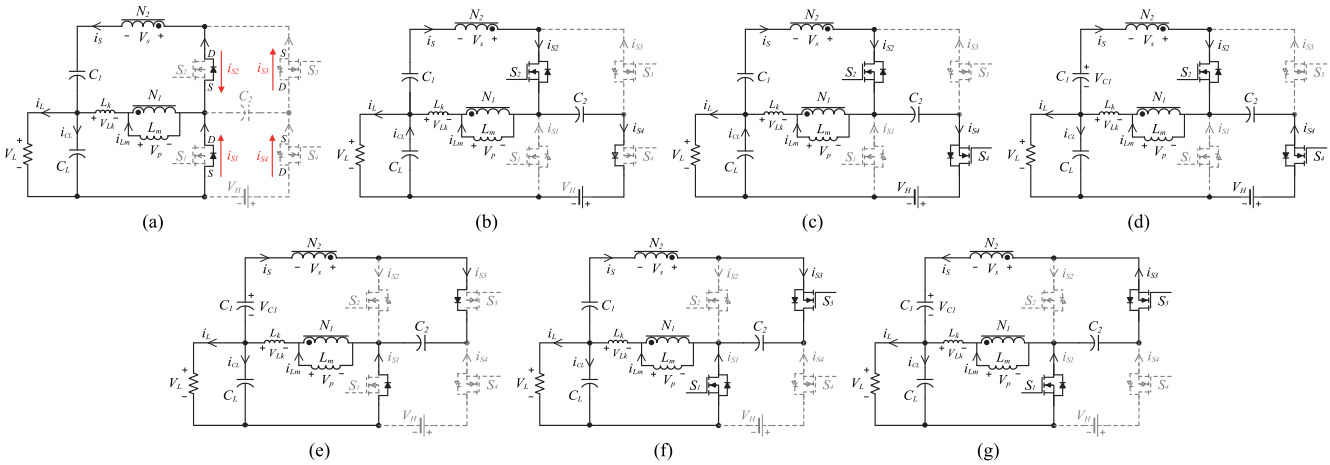

Fig. 5. Operational states in the buck mode. (a) State I [$t_0 - t_1$]. (b) State II [$t_1 - t_2$]. (c) State III [$t_2 - t_3$]. (d) State IV [$t_3 - t_4$]. (e) State V [$t_4 - t_5$]. (f) State VI [$t_5 - t_6$]. (g) State VII [$t_6 - t_7$].

source $V_{\rm H}$ charges C_2, magnetizing and leakage inductors. The capacitor C_1 continues to charge the magnetizing and leakage inductors of the coupled inductor. This state ends when switches S_2 and S_4 are turned OFF.

State V [t_4–t_5]: At $t = t_4$, S_2 and S_4 are turned OFF, as shown in Fig. 5(e). The current passing through switch S_2 is zero. The secondary side current discharges output capacitance, $C_{\rm S3}$, and continues through antiparallel diode of S_3, which clamps drain to source voltage close to zero. The current passing through switch S_4 is zero at $t = t_4$. The leakage inductor current discharges output capacitance, $C_{\rm S1}$, and continues through antiparallel diode of S_1, which clamps drain to source voltage close to zero. The current flowing from source to drain discharges $C_{\rm S1}$ in this state. The magnetizing and leakage inductors discharge and transfer their stored energies to $C_{\rm L}$. The capacitor C_1 discharges and moves its energy to C_2 through the coupled inductor. This state ends with the turn-ON of switches S_1 and S_3.

State VI [t_5–t_6]: At $t = t_5$, S_1 and S_3 are turned ON, as shown in Fig. 5(f). The current passing through antiparallel diodes shifts into respective switches S_1 and S_3 for continuous conduction. Therefore, both switches are turned ON at ZVS. The magnetizing inductor continues to be discharged and transfer its energy to capacitor $C_{\rm L}$. Capacitor C_1 continues to charge C_2 through the coupled inductor. This state ends when the current through switch S_3 changes its direction.

State VII [t_6–t_7]: At $t = t_6$, the current passing through S_3 becomes positive, as shown in Figs. 4 and 5(g). The capacitor C_2 discharges and transfers its energy to capacitor C_1 through the secondary side of the coupled inductor. The magnetizing inductor continues to be released to supply $C_{\rm L}$. This state is switched to State I when switches S_1 and S_3 are turned OFF.

III. Steady-State Analysis

In this section, steady-state analysis in both boost and buck modes is performed. The turns ratio is defined as $n = N_2/N_1$. The leakage inductance is $L_{\rm k}$, and the coupling coefficient is defined as $k = L_m/(L_m + L_k)$.

A. Boost Mode

In the boost mode, States I, II, and IV occur at a small fraction of each switching period. Therefore, they are neglected in the steady-state analysis. States III and V are considered for steady-state analysis.

In operating State III, according to Fig. 3(c), the following voltage equations can be written as follows:

$$V_p^{III} = kV_L = V_S^{III}/n \tag{1}$$

$$V_{C2} = V_L + V_{C1} + V_s^{III}. \tag{2}$$

In operating State V, according to Fig. 3(e), the following voltage equations can be written as follows:

$$V_{C1} = -V_{Lk}^V - V_p^V - V_s^V \tag{3}$$

$$V_H = V_L + V_s^V + V_{C1} + V_{C2}. \tag{4}$$

The volt-second balance (VSB) principle on the magnetizing and leakage inductances results in the following voltage equations across capacitors:

$$\begin{cases} V_{C1} = \frac{(1+nk)}{1-D} D V_L \\ V_{C2} = \frac{(1+nk)}{1-D} V_L. \end{cases} \tag{5}$$

The voltage gain of the converter in boost mode can be derived by substituting (5) into (4)

$$M_{\rm boost} = \frac{V_H}{V_L} = \frac{2+nk}{1-D}. \tag{6}$$

The gain primarily is a function of the duty cycle and the number of the turns ratio. The characteristics of voltage gain in boost mode of operation are shown in Fig. 6. It depicts that the leakage inductance degrades the voltage gain; however, its impact is minimal, particularly at lower turns ratio and duty cycle. According to Fig. 3, the voltage stress on the main power switch S_1 is expressed as follows:

$$V_{DS1} = \frac{V_L}{1-D} = \frac{V_H}{2+n}. \tag{7}$$

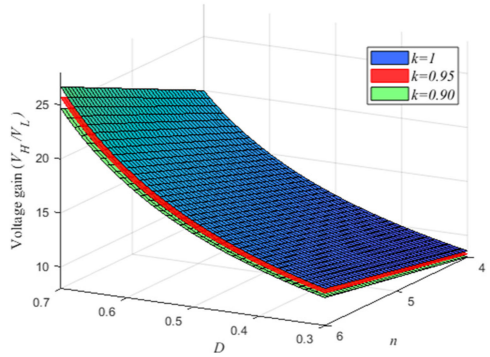

Fig. 6. Voltage gain characteristics in boost mode.

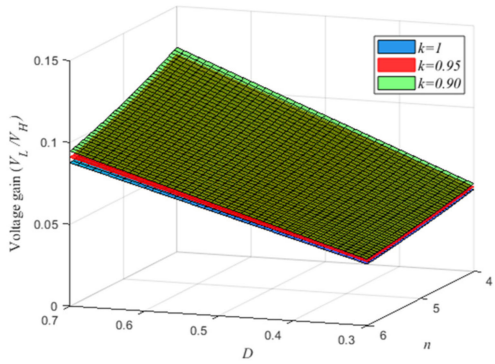

Fig. 7. Voltage gain characteristics in buck mode.

In the boost mode, the voltage stress on the main switch S_1 is clamped at a lower value compared to the high output voltage besides clamping the leakage energy at the output without utilizing any clamp circuit. Thus, the conversion efficiency can be enhanced by employing a low voltage rating MOSFET.

B. Buck Mode

In the buck mode, States I, II, and V only occur at a small fraction of each switching period. Therefore, they are neglected in the steady-state analysis. States III, IV, VI, and VII are considered for the analysis.

According to Fig. 5(c) and (d), the voltage equations in States III and IV are equal. In State III, the following voltage equations can be written as follows:

$$V_L = V_H - V_{C2} - V_{C1} - V_s^{III} \tag{8}$$

$$V_{C1} = -V_{Lk}^{III} - V_p^{III} - V_s^{III}. \tag{9}$$

According to Fig. 5(f) and (g), the voltage equations in States VI and VII are analogous. In State VI, the following voltage equation can be written:

$$V_p^{VI} = V_p^{VII} = kV_L = V_S^{VI}/n \tag{10}$$

$$V_{C2} = V_L + V_s^{VI} + V_{C1}. \tag{11}$$

Similarly, by applying the VSB principle on the magnetizing and leakage inductance, the voltage gain in the buck mode can be computed and expressed as follows:

$$M_{\text{buck}} = \frac{V_L}{V_H} = \frac{D}{2+nk}. \tag{12}$$

The voltage gain characteristics of the proposed converter in buck mode are illustrated in Fig. 7. It depicts that leakage inductance has an insignificant impact on the voltage conversion gain, particularly at the high turns ratio and low duty cycle. The voltage stress in buck mode on the main switch S_4 is expressed as follows:

$$V_{DS4} = \frac{V_H}{2+n}. \tag{13}$$

The voltage stress is clamped at a lower value compared to the high voltage side, unlike a conventional buck converter and other coupled inductor topologies. Thus, a switch with a low voltage rating can be used to reduce the conduction and switching loss. The voltage stress on intermediate switches is expressed as follows:

$$V_{DS2} = V_{DS3} = \frac{1+n}{2+n}V_H. \tag{14}$$

The voltage stress on S_2 and S_3 are also lower than the high voltage $V_{\text{H,}}$ unlike conventional buck/boost converters.

C. Performance Evaluation

In this section, a performance evaluation of the proposed topology in comparison with other bidirectional topologies is performed. A comparison in terms of high step-up/step-down conversion ratio, voltage stress, number of switches, and efficiency is shown in Table I. The proposed bidirectional topology demonstrates a relatively higher conversion ratio than other topologies except for the topology in [21], which utilizes five switches and more intermediate capacitors. It shows a high component count. The salient feature of the proposed configuration lies in the reduced voltage stress on the high voltage side switch (S_4). The high side switch voltage stress is significantly lower than the high voltage, unlike other topologies. A comparison of high side switch voltage stress with other converters is depicted in Fig. 8(a). It clearly distinguishes the proposed topology from other topologies in terms of reduced voltage stress on the switch connected with high output voltage. A comparison of low side switch voltage stress with other converters is revealed in Fig. 8(b). In the proposed configuration, the voltage stress on the low voltage side is also relatively lower than other topologies except [21], which utilizes more intermediate capacitors to reduce voltage stress. Therefore, low voltage rating switches can be used to decrease the switching and conduction losses; thus, efficiency can be enhanced.

D. Theoretical Efficiency and Loss Analysis

The efficiency and loss analysis is conducted in this section to calculate the theoretical efficiency curve and compute losses in the converter. The analysis is useful to identify lossy components to optimize conversion efficiency. The ripple in the inductor current and capacitors voltage is neglected to simplify the mathematical analysis. The conduction losses in passive components

TABLE I
PERFORMANCE EVALUATION

Converters	Switches	Voltage Gain		Switch Voltage Stress			Reported Peak Efficiency		Power Density
		Boost	Buck	Low voltage side	High voltage side	Maximum	Boost	Buck	Buck/Boost
[21]	5	$\frac{1+2n-nD}{1-D}$	$\frac{D}{1+2n+nD}$	$\frac{V_H}{1+2n-nD}$	$\frac{nV_H}{1+2n-nD}$	$\frac{nV_H}{1+2n-nD}$	97.33%	96.23%	-
[22]	4	$\frac{1+n}{1-D}$	$\frac{D}{1+n}$	$\frac{V_H}{1+n}$	$\frac{n}{1+n}V_H$	$\frac{n}{1+n}V_H$	96%	96%	-
[24]	4	$\frac{2n-1}{(n-1)(1-D)}$	$\frac{(n-1)D}{2n-1}$	$\frac{n-1}{2n-1}V_H$	$\frac{n}{2n-1}V_H$	$\frac{n}{2n-1}V_H$	96.41%	95.44%	-
[27]	4	$\frac{1+n}{1-D}$	$\frac{D}{1+n}$	$\frac{V_H}{1+n}$	V_H	V_H	96.4%	95%	-
[30]	4	$\frac{1+n}{1-D}$	$\frac{D}{1+n}$	$\frac{V_H}{1+n}$	$\frac{n}{1+n}V_H$	$\frac{n}{1+n}V_H$	94.5%	94%	-
[15]	4	-	$\frac{nD}{1+2n+D}$	$\frac{n}{1+2n+D}V_H$	$\frac{(1+n)V_H}{1+2n+D}$	$\frac{(1+n)V_H}{1+2n+D}$	-	93.2%	144 W/ 9040 mm^3
Proposed converter	4	$\frac{2+n}{1-D}$	$\frac{D}{2+n}$	$\frac{V_H}{2+n}$	$\frac{V_H}{2+n}$	$\frac{1+n}{2+n}V_H$	96.38%	95.61%	300 W/ 41471 mm^3

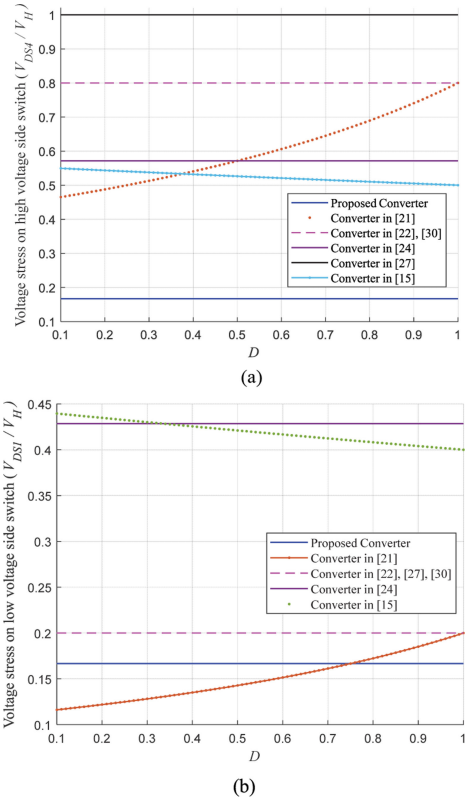

Fig. 8. Voltage stress on switches. (a) High voltage side switch. (b) Low voltage side switch.

and semiconductors, switching losses in the switches, and core losses in the coupled inductor are obtained to calculate the efficiency of the proposed converter. The root mean square (rms) value is obtained to compute the conduction losses in the components. The rms value of the current is obtained as follows:

$$I_{x(\mathrm{rms})} = \sqrt{\frac{1}{T_s}\int_0^{T_s} (i_x)^2\, dt}. \tag{15}$$

In the boost mode of operation, the rms values of current are calculated with the help of theoretical plots in Fig. 2. Therefore, the corresponding rms values for different components are as follows:

$$I_{S1(\mathrm{rms})} = \frac{1+n+D}{(1-D)\sqrt{D}} I_H \tag{16}$$

$$I_{S2(\mathrm{rms})} = I_{S4(\mathrm{rms})} = \frac{I_H}{\sqrt{1-D}} \tag{17}$$

$$I_{S3(\mathrm{rms})} = \frac{I_H}{\sqrt{D}} \tag{18}$$

$$I_{Lk(\mathrm{rms})} = I_H \sqrt{\left(\frac{n+2D}{1-D}\right)^2 \frac{1}{D} + \frac{4}{1-D}} \tag{19}$$

$$I_{C1(\mathrm{rms})} = I_{C2(\mathrm{rms})} = I_{S(\mathrm{rms})} = \frac{I_H}{\sqrt{D\,(1-D)}} \tag{20}$$

$$I_{CH(\mathrm{rms})} = I_H \sqrt{\frac{D}{1-D}}. \tag{21}$$

The conduction losses are obtained by using these equations in the corresponding components. In the boost mode of operation, switch S_1 is operating under hard switching condition; therefore, the switching loss in S_1 is obtained as follows:

$$P_{\mathrm{sw1\_loss}} = \frac{1}{2} V_{DS1} \left[i_{s1-\min} \times t_{\mathrm{on1}} + i_{s1-\max} \times t_{\mathrm{off1}} \right] f_s \tag{22}$$

where f_s is the switching frequency, t_{on1} and t_{off1} are the rise and fall time of the switch, respectively.

During the delay time, the switches output capacitance discharges as a result drain to source voltage drops to zero for ZVS turn ON. Therefore, the output capacitance loss of switches is considered in the efficiency and loss analysis. According to [31], it is obtained as

$$P_{\mathrm{sw1}} = P_{\mathrm{sw4}} = \frac{2}{3} f_s C_{S1} {V_{DS1}}^2 = \frac{2}{3} f_s C_{S1} \left(\frac{V_H}{2+n}\right)^2 \tag{23}$$

$$P_{\mathrm{sw2}} = P_{\mathrm{sw3}} = \frac{2}{3} f_s C_{S2} \left(\frac{V_H (1+n)}{2+n} \right)^2 \tag{24}$$

where C_{Sx} donates the output capacitance of the respective switch.

The core losses are calculated by using the ferrite data sheet curve. The typical curve indicates the core power loss density (mW/cm^3) against peak to peak flux density for a given switching frequency. The peak to peak flux density, according to Faraday's Law, is obtained as follows:

$$\Delta B = \frac{D (1-D) V_H}{(2+n) N_1 A_c f_s} \tag{25}$$

where N_1 is the number of turns around the primary side of the core, and A_c is a cross-sectional area of the core. Therefore, the core losses are computed as follows:

$$P_{\mathrm{core}} = [\text{core loss density}] \times V_e \tag{26}$$

where V_e denotes the volume of the core.

Considering the switching, core, and conduction losses, the efficiency of the proposed converter in boost mode is formulated as follows:

$$\eta_{\mathrm{Boost}} = \frac{P_o}{P_{\mathrm{in}}} = \frac{1}{1 + A_1 + A_2 + A_3 + (A_4 + A_5) R_L}$$

$$A_1 = \frac{(1+n+nD)^2 r_{DS1} + (n+2D)^2 D R_P}{D^2 (1-D)^2 R_L}$$

$$A_2 = \frac{R_S + r_{C1} + r_{C2} + r_{DS3} (1-D) + D^2 r_{CH}}{D (1-D) R_L} + \frac{4R_P + r_{DS2} + r_{DS4}}{(1-D) R_L}$$

$$A_3 = \frac{1+n+D}{2(2+n) D (1-D)} \left[\left(1 - \frac{V_H D (1-D)}{(2+n) L_m f_s} \right) t_{\mathrm{on1}} + t_{\mathrm{off1}} \right] f_s$$

$$A_4 = \frac{2 f_s}{3(2+n)^2} \left[C_{S1} + C_{S4} + (1+n)^2 (C_{S2} + C_{S3}) \right]$$

$$A_5 = \frac{P_{\mathrm{core}}}{{V_H}^2} \tag{27}$$

where r_{DSx} donates the ON-state resistance of the respective switches, r_{Cx} represents the equivalent series resistance of individual capacitors, and R_P and R_S represents the series resistance of primary and secondary windings, respectively. The parameters of each component are taken from the datasheet.

In the buck mode of operation, the rms values of current are calculated with the help of theoretical plots in Fig. 4. Therefore, the corresponding rms values for different components are as follows:

$$I_{S1(\mathrm{rms})} = \frac{2+n-D}{(2+n)\sqrt{1-D}} I_L \tag{28}$$

$$I_{S2(\mathrm{rms})} = I_{S4(\mathrm{rms})} = \frac{\sqrt{D}}{2+n} I_L \tag{29}$$

$$I_{S3(\mathrm{rms})} = \frac{D}{(2+n)\sqrt{1-D}} I_L \tag{30}$$

$$I_{Lk(\mathrm{rms})} = \frac{I_L}{2+n} \sqrt{4D + \frac{(2+n-2D)^2}{1-D}} \tag{31}$$

$$I_{C1(\mathrm{rms})} = I_{C2(\mathrm{rms})} = I_{S(\mathrm{rms})} = \frac{I_L}{2+n} \sqrt{\frac{D}{1-D}} \tag{32}$$

$$I_{CL(\mathrm{rms})} = \frac{n I_L}{2+n} \sqrt{\frac{D}{1-D}}. \tag{33}$$

In buck mode, all switches can realize the ZVS turn-ON operation. The turn OFF losses are calculated as follows

$$P_{\mathrm{sw\_loss}} = \sum_{x=2}^{4} \frac{1}{2} V_{DSx} \left[i_{sx-\max} \times t_{\mathrm{off}x} \right] f_s \tag{34}$$

where $t_{\mathrm{off}x}$ represents the fall time of switch x.

The output capacitance loss of switches is obtained as follows:

$$P_{\mathrm{sw1}} = P_{\mathrm{sw4}} = \frac{2}{3} f_s C_{S1} {V_{DS1}}^2 = \frac{2}{3} f_s C_{S1} \left(\frac{V_L}{D} \right)^2 \tag{35}$$

$$P_{\mathrm{sw2}} = P_{\mathrm{sw3}} = \frac{2}{3} f_s C_{S2} \left(\frac{V_L (1+n)}{D} \right)^2. \tag{36}$$

The core losses can be obtained by (25) and (26). Thus, the efficiency of the proposed converter in the buck mode of operation can be formulated as follows:

$$\eta_{\mathrm{Buck}} = \frac{P_o}{P_{\mathrm{in}}} = \frac{1}{1 + B_1 + R_L (B_2 + B_3) + B_4 {R_L}^2}$$

$$B_1 = \frac{1}{(2+n)^2 (1-D)} [D (1-D) (r_{DS2} + r_{DS4}) + D^2 r_{DS3} + (2+n-D)^2 r_{DS1} + R_P (4D (1-D) + (2+n-2D)^2) + D (R_S + r_{C1} + r_{C2}) + n^2 D r_{CL}$$

$$B_2 = \frac{2 f_s}{3D^2} \left[C_{S1} + C_{S4} + (1+n)^2 (C_{S2} + C_{S3}) \right]$$

$$B_3 = \frac{P_{\mathrm{core}}}{{V_L}^2}$$

$$B_4 = \frac{(1+n) f_s}{2(2+n)} \left[\frac{t_{\mathrm{off2}}}{\sqrt{D}} + \frac{t_{\mathrm{off3}}}{1-D} + \frac{t_{\mathrm{off4}}}{\sqrt{D} (1+n)} \right]. \tag{37}$$

The efficiency of the proposed converter against the duty cycle in both boost and buck mode is illustrated in Fig. 9 in order to find the optimal range of duty ratio for efficiency optimization. The proposed converter shows high conversion efficiency at a lower duty cycle close to 0.5 in both operating modes. The optimal duty cycle range is 0.3–0.6.

E. Dynamic Modeling and Controller Design

The small-signal model is derived in this section to find the control to the output transfer function in boost and buck mode of operation. The proposed converter consists of four energy storage elements, which includes a coupled inductor and three capacitors. The voltage across intermediate capacitors, C_1 and C_2, is constant and depends on input or output voltage. Therefore, they are not counted as the state variables [26]. The state variables are coupled inductor and output capacitors. Thus,

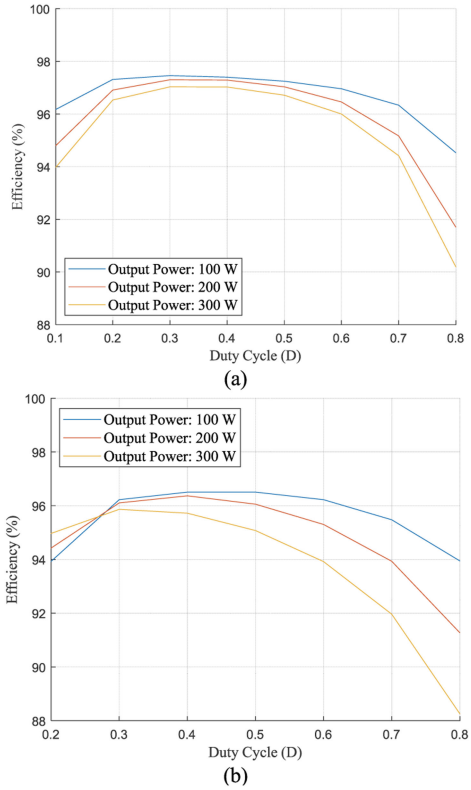

Fig. 9. Efficiency of the proposed converter as a function of duty ratio. (a) Boost mode. (b) Buck mode.

the resulting small-signal model is transformed into a reduced second-order system. In the boost mode, the voltage across the high side output capacitor (v_H) and the current flowing through the primary side of the coupled inductor (i_L) are two state variables. Therefore, the circuit equations in ON and OFF switching states can be written as follows:

$$\begin{cases} L_1 \frac{di_L}{dt} = V_L \\ C_H \frac{dv_H}{dt} = -\frac{v_H}{R_L} \end{cases} \qquad S = 1 \qquad (38)$$

$$\begin{cases} L_1 \frac{di_L}{dt} = V_L + V_{C2} - v_H \\ C_H \frac{dv_H}{dt} = \frac{n-1}{n} i_L - \frac{v_H}{R_L} \end{cases} \qquad S = 0. \qquad (39)$$

The state-space averaging method is applied, and the model comes out to be nonlinear. Therefore, the linearization process is utilized to develop the small-signal model.

$$\begin{bmatrix} \frac{d\tilde{i}_L}{dt} \\ \frac{d\tilde{v}_H}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-D)}{L_1} \\ \frac{(n-1)(1-D)}{nC_H} & -\frac{1}{R_L C_H} \end{bmatrix} + \begin{bmatrix} \frac{V_H}{L_1} - \frac{(1+n)}{L_1(1-D)} V_L \\ -\frac{(n-1)I_L}{nC_H} \end{bmatrix} \left[\tilde{d}\right]. \qquad (40)$$

Finally, by taking the Laplace transform, the control to the output transfer function in the boost mode is obtained as follows:

$$G(s)_{\text{Boost}} = \frac{\tilde{v}_H(s)}{\tilde{d}(s)} = \frac{K_o(-\beta_1 s + 1)}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

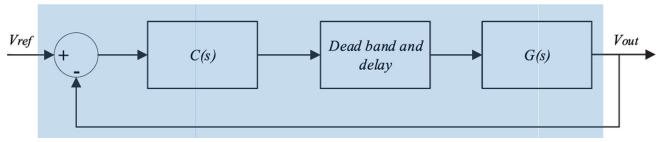

Fig. 10. Control block diagram of the proposed converter.

where

$$K_o = (n-1)\left[\frac{V_H(1-D) - V_L(1+n)}{nL_1 C_H}\right]$$

$$\beta_1 = \frac{I_L L_1}{V_H(1-D) - V_L(1+n)}$$

$$\omega_n = (1-D)\sqrt{\frac{n-1}{nL_1 C_H}},\ \xi = \frac{1}{2R(1-D)}\sqrt{\frac{nL_1}{C_H(n-1)}}. \qquad (41)$$

In the buck mode, the voltage across the low side output capacitor (v_L) and the current flowing through the primary side of the coupled inductor (i_L) are two state variables. Therefore, the circuit equations in ON and OFF switching states can be written as follows:

$$\begin{cases} L_1 \frac{di_L}{dt} = V_H - V_{C2} - v_L \\ C_L \frac{dv_L}{dt} = \frac{n-1}{n} i_L - \frac{v_L}{R_L} \end{cases} \qquad S = 1 \qquad (42)$$

$$\begin{cases} L_1 \frac{di_L}{dt} = -v_L \\ C_L \frac{dv_L}{dt} = \frac{n-1}{n} i_L - \frac{v_L}{R_L} \end{cases} \qquad S = 0. \qquad (43)$$

The average small-signal model is expressed as follows:

$$\begin{bmatrix} \frac{d\tilde{i}_L}{dt} \\ \frac{d\tilde{v}_L}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_1} \\ \frac{n-1}{nC_L} & -\frac{1}{R_L C_L} \end{bmatrix} + \begin{bmatrix} \frac{V_H}{(2+n)L_1} \\ 0 \end{bmatrix} \left[\tilde{d}\right]. \qquad (44)$$

Finally, by taking the Laplace transform, the transfer function in the buck mode is obtained as follows:

$$G(s)_{\text{Buck}} = \frac{\tilde{v}_L(s)}{\tilde{d}(s)} = \frac{K_o}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

where

$$K_o = \frac{(n-1)V_H}{n(2+n)L_1 C_L},$$

$$\omega_n = \sqrt{\frac{n-1}{nL_1 C_L}},\ \xi = \frac{1}{2R}\sqrt{\frac{nL_1}{C_H(n-1)}}. \qquad (45)$$

The control block diagram is illustrated in Fig. 10. The controller $C(s)$ is designed by using Affine parameterization approach [32] according to the desired closed-loop system performance by specifying the close loop undamped natural frequency ω_{cl} and the damping ratio ξ_{cl}. The controller is expressed in PID format for realization in a digital microcontroller

$$C(s) = \frac{s^2 + 2\xi\omega_n s + \omega_n^2}{K_o s(\alpha_2 s + \alpha_1)}$$

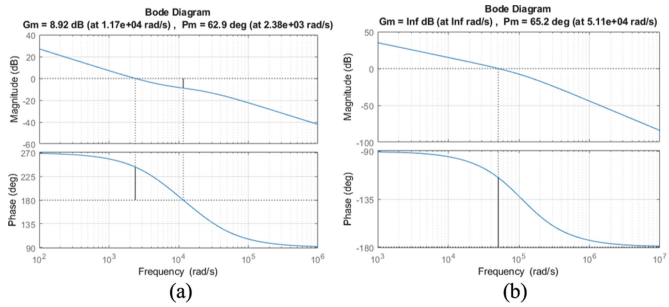

Fig. 11. Frequency response of the proposed converter. (a) Boost mode. (b) Buck mode.

where

$$\alpha_1 = \frac{2\xi_{cl}}{\omega_{cl}},\ \alpha_2 = \frac{1}{\omega_{cl}^2}. \tag{46}$$

The relative stability of $C(s)G(s)$ is analyzed and ensured for a stable closed-loop system. Following the case study, the bode diagram of the closed-loop system for boost and buck mode is shown in Fig. 11 to demonstrate the system's robustness. The bode plot shows a good phase margin for both boost and buck mode of operation. The phase margins are 62.9° and 65.2° for boost and buck modes, respectively.

F. Design of Circuit Parameters

The coupled inductor is a critical component of the converter. The turns ratio of the coupled inductor is determined by selecting the optimal duty cycle. In the proposed design, the nominal duty cycle is set as 0.5. The turns ratio is calculated as follows:

$$n = \frac{V_H\,(1-D) - 2V_L}{2V_L}. \tag{47}$$

The magnetizing inductance is designed to ensure the CCM operation. The magnetizing inductance at the boundary condition is obtained as follows:

$$L_{mB} \geq \frac{D^2(1-D)^2 R_L}{(2+n)\,(1+n+D)\,f_s}. \tag{48}$$

The value of magnetizing inductance should be selected 20% to 30% higher than the critical boundary value. The choice of the magnetic core is crucial to keep the core losses low in the coupled inductor. For high-frequency operation, the ferrite magnetic core is preferred due to comparatively low losses at high frequencies. A ferrite core is available in different geometries such as E, U, RS, and pot cores. In the proposed converter, the ETD 44 ferrite core is used. The switches are selected according to maximum voltage stress and rms current according to corresponding equations derived in previous sections. The adequate rating margin should be ensured. The capacitors are chosen based on voltage rating and specified allowed voltage ripple (ΔV_{Cx}). The voltage rating of capacitors is obtained by (5). The value of capacitors is computed as follows:

$$C_H \geq \frac{I_H D}{f_s \Delta V_H} \tag{49}$$

$$C_L \geq \frac{V_L\,(1-D/2+n)}{8{f_s}^2 L_m \Delta V_L} \tag{50}$$

$$C_1 \geq \frac{I_L D}{n f_s \Delta V_{C1}} \tag{51}$$

$$C_2 \geq \frac{I_L D}{(2+n)\,f_s \Delta V_{C2}}. \tag{52}$$

G. Soft Switching Conditions

The ZVS turn-ON is realized in both boost and buck mode of operation. However, ZVS operation is subject to some constraints. The following conditions must be fulfilled for the realization of ZVS in both modes.

1) The adequate dead time should be added between gate signals to discharge the parasitic capacitances of respective switches before applying gate signals.
2) The energy stored in magnetizing and leakage inductances must be high enough to discharge the parasitic capacitances of switches.

In the boost mode, when S_1 is turned OFF, the leakage and magnetizing inductances are fully charged, and their stored energies discharge the parasitic capacitance of S_2 and S_4. Therefore, ZVS can be realized for a wide range of loads by synchronous rectification provided adequate energy in the coupled inductor. At $t = t_1$, the secondary side leakage energy is minimum, which discharges the parasitic capacitance of S_3. The following condition must be fulfilled in boost mode

$$\frac{1}{2}L_k i_{Lk}^2\,(t_1) \geq \frac{1}{2}C_{S3}V_{DS3}^2. \tag{53}$$

The ZVS turn ON for S_3 is critical. Thus, the minimum boundary value of load current to realize ZVS can be expressed as follows:

$$I_{H\ \min\_ZVS} = \sqrt{\frac{C_{S3}}{L_k}} \times \frac{(1+n)\,(1-D)\,V_H}{(2+n)^2}. \tag{54}$$

The converter can realize ZVS turn ON down to 40% of full load at $L_k = 1\,\mu$H. However, the other switches can realize ZVS for a wide range of loads. In the buck mode, ZVS turn-ON of S_2 is critical. All other switches can realize ZVS for wide load conditions. Thus, the following condition must be fulfilled for ZVS turn-ON of S_2 in buck mode

$$\frac{1}{2}L_k i_{Lk}^2\,(t_0) \geq \frac{1}{2}C_{S2}V_{DS2}^2. \tag{55}$$

The minimum boundary value of load current to realize ZVS can be expressed by

$$I_{L\ \min\_ZVS} = \sqrt{\frac{C_{S2}}{L_k}} \times \frac{(1+n)\,V_L}{D}. \tag{56}$$

A high value of leakage inductance expands the ZVS range but degrades the voltage conversion ratio. Therefore, the tradeoff should be considered in the design. The dead time (T_d) is maintained long enough between the gate signal to discharge parasitic capacitance to guarantee antiparallel diode conduction, which assures ZVS turn-ON condition. The dead time is given

TABLE II
VOLUME AND POWER DENSITY CALCULATION

Components	Specification		Volume
Switches	IPB027N10N5 × 2/ SIHP25N40D × 2 Size: D^2 PAK/TO220AB Length: 9.5/18 mm Width: 9.8/10 mm Thickness: 4.5/5 mm		838/1800 mm^3
Capacitors	C_1: 24 μF × 2 Diameter: 10 mm Height: 20 mm	C_2: 15 μF × 2 Diameter: 12.5 mm Height: 20 mm	3140 mm^3 4906 mm^3 1570 mm^3 11398 mm^3
	C_L: 470 μF Diameter: 10 mm Height: 20 mm	C_H: 100 μF Diameter: 22mm Height: 30 mm	
Coupled Inductor	ETD 44 Ferrite core Length: 300 mm Area: 173 mm^2		17819 mm^3
Total Volume: 41471 mm^3			
Power Density: 7.23 mW/mm^3			

by

$$T_d \geq \frac{\pi}{2}\sqrt{L_k C_{s4}}. \tag{57}$$

H. Power Density

Following the early study in [15], the volume and size distribution of the proposed converter is computed and given in Table II. The coupled inductor contributes a significant portion in total volume size. The capacitors weigh the second considerable portion in volume, which is dominated by the high voltage side capacitor. The semiconductor devices contribute a relatively small portion compared to other elements. The power density is also included in Table I for comparison. The proposed converter attains the theoretical power density of 300 W/41 471 mm^3, which is less than the density attained by [15]. However, the high side voltage in [15] is set at a lower value of 72 V compared to 380 V in the proposed converter. Thus, the comparison is not based on the same standard. The power density data in other converters have not been reported. At this stage, the prototype has not been optimized for high power density, which is expected in the future.

IV. EXPERIMENTAL EVALUATION

A 300-W prototype circuit has been built in the laboratory, which is tested in boost and buck modes to validate the theoretical analysis and performance expectations. A picture of the prototype is illustrated in Fig. 12. The nominal low voltage is 30 V, and the high side voltage is regulated at 380 V. The switching frequency is 50 kHz. The nominal value of the duty cycle is set to 0.5 for optimal operation. The turns ratio is calculated from (47) according to the input and output voltages, which is designed at 4.5. The components used in the experiment are as follows:

1) coupled inductor: ETD 44, N97 Ferrite Core; $n = 4.5$;
2) MOSFET S_1 and S_4: IPB027N10N5, MOSFET S_2 and S_3: SiHP25N40D;
3) capacitors: C_1—48 μF/250 V, C_2 —30 μF/450 V.

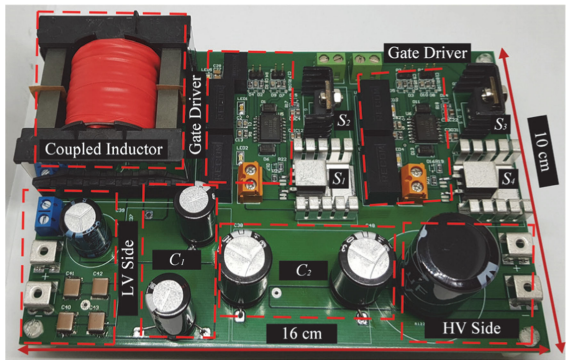

Fig. 12. Prototype picture.

The key converter waveforms of current and voltage are recorded to demonstrate the performance in boost and buck modes of operation. Fig. 13 shows the experimental waveforms of the proposed bidirectional converter in boost mode. Fig. 13(a) depicts voltage stress on the main switch is clamped at a low level, 62 V, which is almost 16% of the high voltage.

Fig. 13(b) and (c) show that the switches S_2 and S_3 are operating under the ZVS condition. The voltage stress on the high side switch S_4 is shown in Fig. 13(d). The voltage stress on the high side switch is significantly minimized compared to the voltage level on the high side. Furthermore, the high side switch S_4 is operating under ZVS in both turn ON and turn OFF conditions. Thus, the switching loss is reduced, and the low voltage rating MOSFETs can be employed as the main switches to minimize the conduction loss to improve the efficiency further. Fig. 14 illustrates a more precise and better picture of the ZVS operation for S_2–S_4. It depicts that during the delay time, the current discharges the output capacitance (C_s) of respective switches. When the output capacitors fully discharged, then diodes become forward biased, which clamps drain to source voltage close to zero. After that, the gate signal is applied to turn ON respective switches under zero drain to source voltage to realize the ZVS turn on. Thus, the switching loss is minimized to enhance conversion efficiency. The current in switches S_2, S_3, and S_4 is flowing from source to drain in the boost mode of operation, which always realize ZVS. The current in S_2–S_4 is negative from standard drain to source reference direction in order to discharge output capacitors (C_s) to realize ZVS. All the experimental waveforms tally with the theoretical analysis. The dynamic response of the proposed configuration is illustrated in Fig. 15. The load is changed from full load to 110 W to observe the converter dynamics. The output voltage is stable with a change in load. The load and line regulation are evaluated to see the performance of the proposed converter under different load and line conditions. The percentage load and line regulations are calculated by the following equations:

$$\%LOR = \frac{V_{o(\min L)} - V_{o(FL)}}{V_{o(FL)}} \times 100\% \tag{58}$$

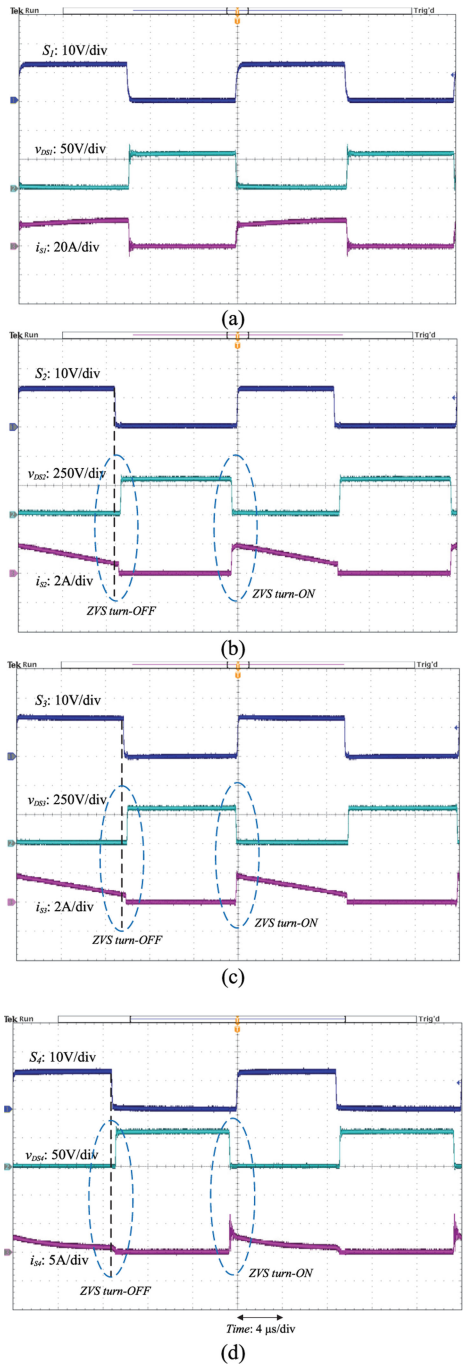

Fig. 13. Experimental results in boost mode.

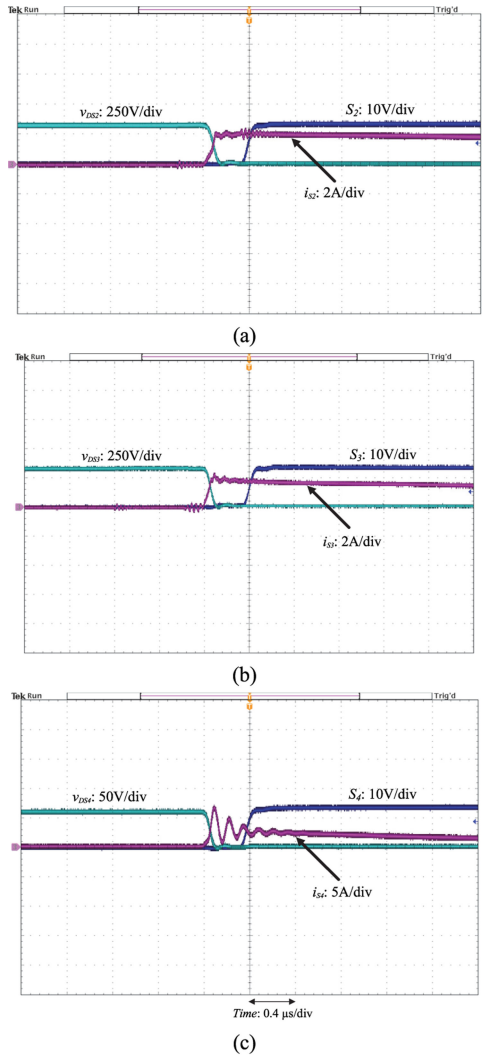

Fig. 14. ZVS in boost mode.

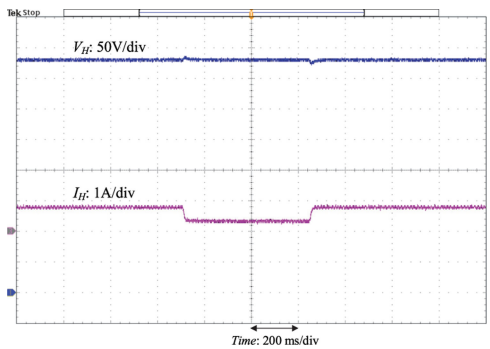

Fig. 15. Dynamic performance of the proposed converter in boost mode.

where $V_{o(\min L)}$ indicates output voltage at minimum load, and $V_{o(FL)}$ represents output voltage at full rated load

$$\%LNR = \frac{\frac{\Delta V_o}{V_{o(\text{nom})}} \times 100}{\Delta V_{\text{in}}}\% \tag{59}$$

where $V_{o(\text{nom})}$ indicates output voltage at nominal load, and ΔV_x represents a change in the voltage. Table III shows the parameters for line and load regulation in boost mode. At the full load condition, the output voltage is regulated at 380 V. When the load is changed from full load to minimum load, the output voltage is measured 383.67 V. For line regulation measurement, the input voltage is changed from minimum to maximum range, and the output voltage is measured accordingly. The proposed converter shows load and line regulation of 0.96% and 0.15%, respectively, in boost mode of operation. The practical and theoretical conversion efficiencies at the different output power levels

TABLE III
REGULATION PARAMETERS IN BOOST MODE

Parameters	Symbols	Values
Low Side Voltage	V_L	24~34 V
Nominal Low Side Voltage	$V_{L(nom)}$	30 V
High Side Voltage	V_H	380 V
Full Load Power	P_O	300 W
Minimum Load	$P_{O(min)}$	20% of full load
Load Current Range	I_H	0.16~0.79 A

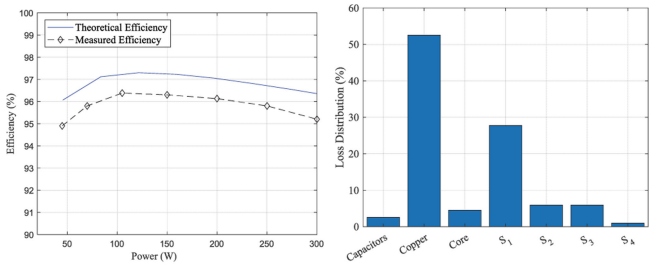

Fig. 16. (a) Experimental and theoretical efficiency in the boost mode. (b) Percentage losses of the proposed converter in boost mode.

in boost mode of operation are demonstrated in Fig. 16(a). The converter achieves a peak efficiency of 96.38% and a full-load efficiency of 95.20%, which are slightly less than theoretical efficiencies obtained from the efficiency analysis. Both efficiency curves follow the same pattern. The losses are calculated from the loss analysis, and percentage loss distribution at full power is illustrated in Fig. 16(b). The loss analysis indicates that copper losses are highest in the proposed converter. Switch S_1 is the second major lossy element due to hard switching. The losses in other components are comparatively low.

The experimental waveforms in the buck mode of operation are illustrated in Fig. 17. It clearly shows all switches realized ZVS operation at turn ON. The voltage stress on high and low side switches, S_1 and S_4, are clamped at 0.16 times the voltage level of V_{H}. Therefore, like the boost mode of operation, the low voltage switches can be utilized to enhance the efficiency of the converter. Fig. 18 illustrates a precise picture of ZVS performance for S_1 and S_4. It depicts the ZVS operation in buck mode of operation. The current in switch S_1 is flowing from source to drain in the buck mode of operation, which always realize ZVS. All switches can realize ZVS turn ON in the buck mode of operation. The dynamic response of the proposed converter in buck mode is depicted in Fig. 19. The output voltage is stable with the change in load. In general, all waveforms are consistent with the theoretical analysis presented in Section II. Table IV shows the parameters for line and load regulation in buck mode. At full load, the output voltage is regulated at 30 V. When the load is changed from full load to minimum load, the output voltage is measured 30.57 V. For line regulation measurement, the input voltage is changed from minimum to maximum range, and the output voltage is measured accordingly. The proposed converter shows load and line regulation of 1.9% and 0.36%, respectively, in buck mode

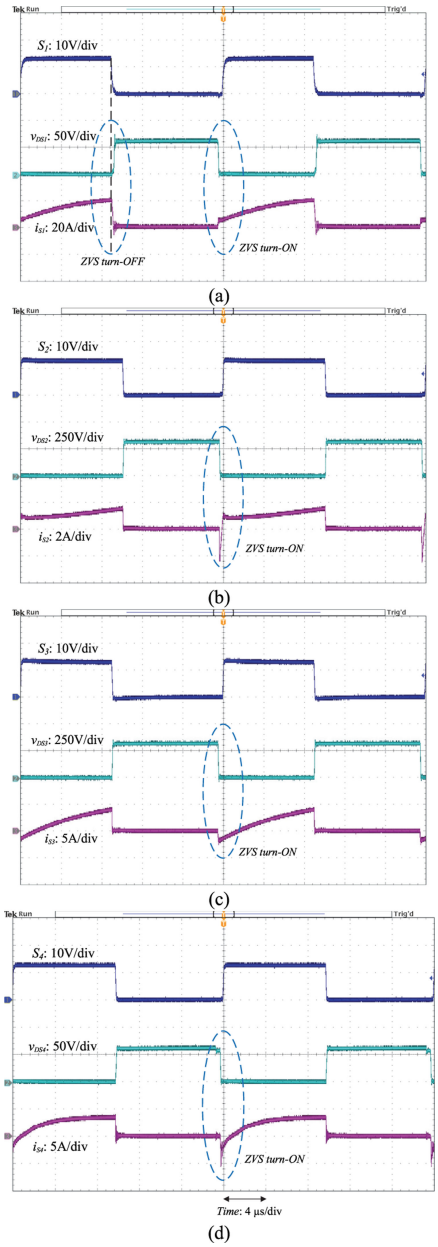

Fig. 17. Experimental results in buck mode.

of operation. The practical and theoretical conversion efficiency at different output power levels in the buck mode of operation is demonstrated in Fig. 20(a). In the buck mode, the converter attains a maximum practical efficiency of 95.61%, and full-load efficiency is 94.24%. The practically measured efficiencies are slightly less than theoretical efficiencies. However, both practical and theoretical efficiency curves follow the same pattern. The losses are computed from the loss analysis, and percentage loss distribution at full power is illustrated in Fig. 20(b). The loss analysis indicates that copper losses are also dominating in buck mode of operation. The capacitors show a second significant portion of the converter's losses. The capacitor connected with a low voltage side relatively shows higher losses due to the high current at full power.

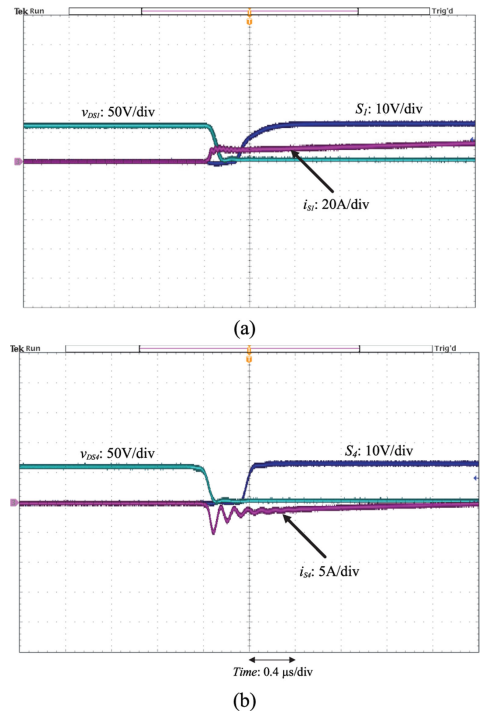

Fig. 18. ZVS in buck mode.

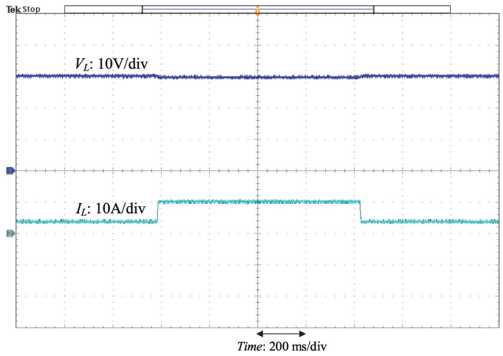

Fig. 19. The dynamic performance of the proposed converter in buck mode.

TABLE IV
REGULATION PARAMETERS IN BUCK MODE

Parameters	Symbols	Values
High Side Voltage	V_H	370~390 V
Nominal High Side Voltage	$V_{H(nom)}$	380 V
Low Side Voltage	V_L	30 V
Full Load Power	P_O	300 W
Minimum Load	$P_{O(min)}$	20% of full load
Load Current Range	I_L	2~10 A

The losses in the switches are small due to the ZVS operation. Moreover, low voltage stress allows us to choose switches with low ON-state resistance resulting in lower conduction losses; therefore, the conversion efficiency is improved. The design of the coupled inductor can be optimized in the future to reduce the losses; hence, the conversion efficiency can be further enhanced.

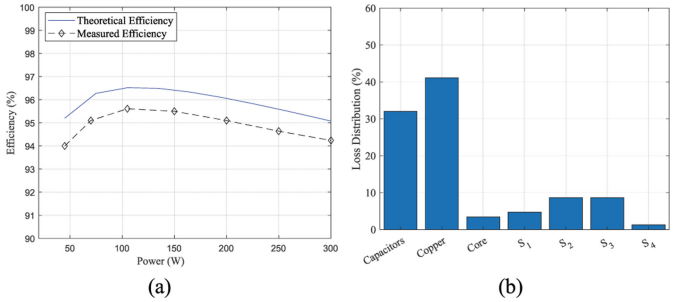

Fig. 20. (a) Experimental and theoretical efficiency in the buck mode. (b) Percentage losses of the proposed converter in buck mode.

V. CONCLUSION

This article analyzes a bidirectional dc–dc converter, which is capable of achieving high voltage conversion ratio and high efficiency. The topology is based on the coupled inductor technique with the optimization of circuit design, which stacks the winding of coupled inductors at the low voltage side. Hence, the clamp circuit is not needed to recycle leakage energy of the coupled inductor since the leakage energy is directly transferred to the output port. Furthermore, the voltage stress on the main switches, S_1 and S_4, is maintained low during the operating range, which is measured by almost one-sixth of the highest voltage in the circuit. This salient feature allows the utilization of MOSFETs with low voltage rating and low ON-state resistance to decrease the conduction loss; thus, yielding higher efficiency. Furthermore, the inherent soft-switching capability (ZVS) of the proposed converter minimized switching loss to enhance the conversion efficiency further. The operating principle and steady-state analysis are elaborated in detail. The theoretical efficiency, loss, and dynamic analysis are presented thoroughly. A prototype of 300 W was built and tested for a 30–380 V conversion ratio to validate the performance and capability. The experimental results substantiated the theoretical analysis demonstrating the soft-switching characteristics, capability for load and line regulation, and enhanced efficiency curve in both boost and buck modes of operation. The converter has shown the peak efficiency of 96.38% in boost mode and 95.61% in buck mode of operation.

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