A General Constant-Switching-Frequency Model-Predictive Control of Multilevel Converters With Quasi-PS-PWM/LS-PWM Output

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***Abstract*—Classical model-predictive control (MPC) of multilevel converters experiences poor steady-state performance owing to the noninterleaved and variable-frequency switching manner. To improve the steady-state performance of MPC, this article presents a general constant-switching-frequency MPC scheme for multilevel converters that can generate quasi-phase-shifted pulsewidth modulation (PWM)/quasi-level-shifted PWM output waveforms and the dc voltage utilization that compares well to that of the space vector modulation. In the proposed MPC scheme, parts of switching pairs of the multilevel converter are determined using the finite-control-set MPC using a hexagon selection approach, while the rest of the switching pairs of the multilevel converter are determined using the multiple-vector MPC for the constant-switching-frequency operation. The deadbeat approach is employed to reduce the computation burden of finite-control-set MPC. The basic concept of the proposed MPC is evaluated in both simulation and experimental tests on a five-level active-neutral-point-clamped converter.**

***Index Terms*—Level-shifted pulsewidth modulation (LS-PWM), model-predictive control (MPC), multilevel converter, phase-shifted pulsewidth modulation (PS-PWM).**

NOMENCLATURE

N	Number of carriers.
x	Phase $x \in [a, b, c]$.
$u_{\rm dc}, \Delta u_{\rm dc}$	DC-link voltage and its difference.
$u_{\rm dc1}, u_{\rm dc2}$	DC-link capacitor voltages.
u_{fx}	FC voltages.
$u_f^*, \Delta u_{\rm dc}^*$	DC-link voltage difference and FC voltage reference.
$i_{{\rm NP}x}, i_{fx}$	Neutral point and FC current of phase x.
$i_{\rm NP}$	Total neutral point current.
i_x, u_{xo}	Phase current and voltage.
L, R	Load inductance and resistance.
T_s	Sampling period.
$C_{\rm dc}, C_f$	DC-link and flying capacitance.
$S_{x1}, \ldots, S_{x4}$	Switching states in phase x.
$S'_{x1}, \ldots, S'_{x4}$	Complementary switching states of $S_{x1}, \ldots, S_{x4}$.
S_{vx}	Virtual switching state by considering S_{x3} and S_{x4} as a whole.
S_{xm}, S_{xn}	Switching states ($m, n \in \{3, 4\}, m \neq n$).
d_{xm}, d_{xn}	Duty cycles of S_{xm}, S_{xn}.
d_{x3}, d_{x4}, d_{vs}	Duty cycles of S_{x3}, S_{x4}, S_{vx}.
$\boldsymbol{v}, \boldsymbol{i}$	Voltage and current vector in the $\alpha\beta$ frame.
$v_\alpha^*, v_\beta^*, i_\alpha^*, i_\beta^*$	Voltage and current reference in the $\alpha\beta$ frame.
$\boldsymbol{v}^*, \boldsymbol{i}^*$	Voltage and current vector reference in the $\alpha\beta$ frame.
$\boldsymbol{v}_s^*$	Voltage vector reference in the selected middle hexagon.
v_a^*, v_b^*, v_c^*	Voltage reference in the abc frame.
$v_{sa}^*, v_{sb}^*, v_{sc}^*$	Voltage reference in selected hexagon in the abc frame.
h, h_s	Selected middle and smallest hexagon number ($h, h_s \in \{1, 2, \ldots, 6\}$).
$\boldsymbol{v}_{c1}, \boldsymbol{v}_{c2}$	Voltage vectors lie in the selected middle and smallest hexagon.
$\boldsymbol{v}_i, \boldsymbol{v}'_i, \boldsymbol{v}''_i$	Eight voltage vectors lie in the center and vertex of the original, middle, smallest hexagon ($i \in \{0, 1, \ldots, 7\}$).
$\boldsymbol{v}'_0, \boldsymbol{v}'_7, \boldsymbol{v}''_0, \boldsymbol{v}''_7$	Voltage vector pairs lie in the center of the selected hexagon h, h_s.
$x(k), x(k+1)$	Variable x at $k, k+1$ time instant.
J_i, g_i	Cost function values and their adjacent sum values ($i \in \{1, 2, \ldots, 6\}$).
$\boldsymbol{v}_{o1}, \boldsymbol{v}_{o2}$	Selected two adjacent optimal vectors.
$\boldsymbol{s}_1, \boldsymbol{s}_2, \boldsymbol{s}_0$	Current slopes of two adjacent optimal vectors and $\boldsymbol{v}_{c1}/\boldsymbol{v}_{c2}$.
$s_{\alpha 1}, s_{\beta 1}$	Current slope of $\boldsymbol{v}_{o1}$ in the $\alpha\beta$ frame.
$s_{\alpha 2}, s_{\beta 2}$	Current slope of $\boldsymbol{v}_{o2}$ in the $\alpha\beta$ frame.
$s_{\alpha 0}, s_{\beta 0}$	Current slope of $\boldsymbol{v}_{c1}/\boldsymbol{v}_{c2}$ in the $\alpha\beta$ frame.
t_1, t_2, t_0	Optimal duty cycles for $\boldsymbol{v}_{o1}$, $\boldsymbol{v}_{o2}$, and $\boldsymbol{v}_{c1}/\boldsymbol{v}_{c2}$.
$\tilde{i}_\alpha, \tilde{i}_\beta$	Differences between current references and their measured values in the $\alpha\beta$ frame.
$\varepsilon_\alpha, \varepsilon_\beta$	Differences between current references and their predicted values in the $\alpha\beta$ frame.
t_n, t_p	Duty cycle for $\boldsymbol{v}'_0, \boldsymbol{v}'_7$.
k_{bnp}, k_{bfcx}	Proportional control parameters.
d_{bnp}, d_{bfcx}	Duty cycles for capacitor voltage balancing.

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I. Introduction

MULTILEVEL converters have been extensively employed in industrial applications, such as grid-tied inverters [1], energy storage systems [2], medium-voltage motor drive systems [3], and so on [4], thanks to their advantages of better output voltage quality, reduced switching losses, lower dv/dt, and so on.

However, the design of modulation schemes, which map the reference voltage to the duty cycle for each switching pair of the multilevel converters, is always a challenging topic. Carrier-based pulsewidth modulation (PWM), such as phase-shifted PWM (PS-PWM) [5], [6] and level-shifted PWM (LS-PWM) [7], and space vector modulation (SVM) [8], [9] are extensively investigated in the literature.

The carrier-based PWM scheme is widely adopted because of the simple implementation process. However, carrier-based PWM has its intrinsic drawbacks. The utilization of dc voltage is only 87% compared to SVM. To increase the dc-link voltage utilization, zero-sequence voltage is always injected. However, the calculation of the required zero-sequence voltage becomes more complicated when the level of the converter gets higher. Iterations of sorting and comparison must be processed [10].

An alternative to carrier-based PWM is the SVM, which can also achieve good utilization of the dc-link voltage. However, SVM is a more complex modulation scheme as compared to the carrier-based PWM, especially when the number of switching states is large. The control of the neutral voltage in SVM is indirect and complicated. For example, the space vector diagram for a five-level converter is divided into 96 small triangles. The possible switching sequence should be individually analyzed for neutral voltage balance [9]. Considering the massive computation required to locate the reference vector and determine the dwell time calculation for each vector, the SVM design for the multilevel converter becomes quite difficult.

Like modulation scheme design, the controller design is also a challenging task. In the multilevel converter, the neutral point voltage and phase voltage balance are always required in addition to output current control. Therefore, a multiobjective control issue is always formulated to guarantee the stable operation of the multilevel converter. To address this issue, the linear-system-theory-based multiple proportional-integral (PI) or proportional-resonant (PR) loops with PWM may be a possible choice [7], [9], [11]. However, multiple PI/PR loops lead to tedious tuning work, and the interactions of the different PI/PR loops may lead to poor control performance.

Model-predictive control (MPC) can realize the optimal control of multiple objectives and has attracted growing interest because of its advantages such as fast dynamic response, straightforward realization, and easy inclusion of nonlinear constraints [12]–[16]. However, classical MPC realizes the multiobjective control of the multilevel converter by exhaustive searching all the switching states in an online computational stage. A flexible cost function, which includes all the control objectives, is evaluated and minimized to determine the optimal switching state. As a result, classical MPC provides good dynamic performance and easy inclusion of nonlinearity and constraint [17], [18].

However, as the optimal switching state is selected in each control period and applied to the multilevel converter during the next entire control period, the classical MPC is featured with a variable switching frequency that leads to voltage and current spectra that are spread over a wide range of frequencies. The resulting switching frequency changes as the sampling frequency and reference are changed, and the maximum value is limited to half the sampling frequency. Moreover, the switching states of the classical MPC update in a noninterleaved manner, which leads to inferior output waveform quality than that of the linear controller with PS-PWM/LS-PWM.

As the constant-switching-frequency scheme brings several advantages in the filter and heat sink size design, several works on constant-switching-frequency MPC of the multilevel converter are investigated [6], [16], [19]–[25]. The reference voltage is calculated using the MPC scheme, while the duty cycle for each switching pair was generated using PWM techniques [21]–[24]. The modulation stage was excluded from the optimization stage, and the complicated modulation scheme is also required. In [19], the cost functions for the 27 vectors produced by the three-level converter were evaluated, and the duty cycles for each of the 24 sectors were calculated. Because of its heavy computation burden, this method was complicated to extend to other multilevel converters with a high number of voltage levels. A multiobjective optimization MPC for load current tracking and circulating current suppression was proposed for the single-phase modular multilevel converter [6]. However, the dc voltage utilization was only 87.5% of the SVM, since the three-phase system is modeled as three single-phase systems. A constant switching frequency was obtained by selecting an optimal set of concatenated voltage vectors that were stored in a lookup table as precalculated sequences [20]. The voltage vector sequences were chosen over a fixed period, which resulted in a fixed switching frequency. As the voltage level becomes large, it became impractical as a huge table should be built. A constant-switching-frequency MPC using the finite-control-set MPC concept was presented in [16]. However, it was only applicable to the controller evaluated at a very high sampling frequency, typically 400 kHz to achieve 10 kHz switching frequency, which imposed a high requirement on the microprocessor.

By investigating the essence of PS-PWM and LS-PWM, this article proposes a general constant-switching-frequency MPC with quasi-PS-PWM/LS-PWM output for the multilevel converter. It presents the dc voltage utilization that compares well to that of the SVM. Combined with the deadbeat approach, the proposed MPC method is easy to implement with a low computation burden. The results of a five-level active-neutral-point-clamped (5L-ANPC) converter are utilized as a case study to validate the effectiveness of the proposed MPC methods.

II. Features of PS-PWM and LS-PWM

To achieve a quasi-PS-PWM/LS-PWM output waveform, the switching features of PS-PWM and LS-PWM should be analyzed. In PS-PWM, the carriers are interleaved with an angle of $2\pi/N$. For LS-PWM, several carrier configurations can be implemented, namely the phase disposition PWM (PD-PWM),

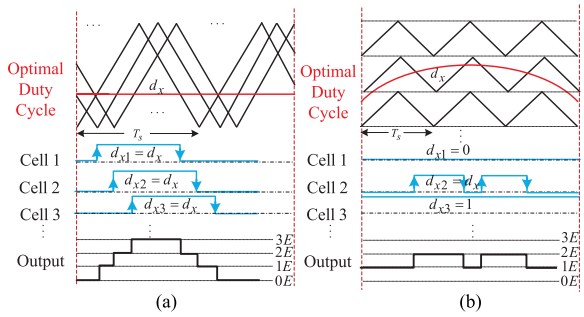

Fig. 1. Illustration pulse train generation of (a) PS-PWM and (b) LS-PWM.

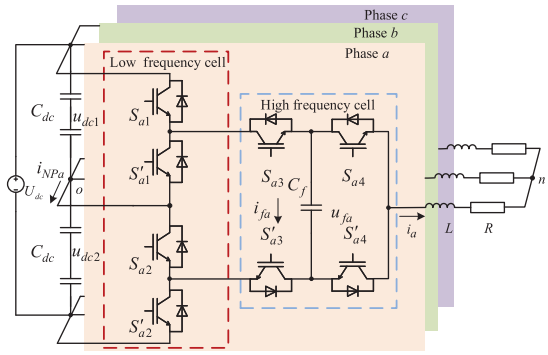

Fig. 2. Topology of a 5L-ANPC converter.

the phase opposition disposition PWM, and the alternative phase opposition disposition PWM.

In the application of multilevel converters, the PS-PWM features balanced power loss and natural balancing of the flying capacitor (FC) voltage. On the other hand, all three methods of LS-PWM require active FC voltage balancing at switching frequency. However, PD-PWM can produce higher output quality than PS-PWM [26]. As such, both PS-PWM and PD-PWM have been popular choices for multilevel converters depending on the requirements of applications. In this article, PD-PWM is selected as an example of LS-PWM in the analysis. The implementation processes of both PS-PWM and PD-PWM are given in Fig. 1.

To implement PS-PWM, the voltage across different switching pairs should be the same. As presented in Fig. 1(a), the duty cycle for each switching pair in PS-PWM is the same. Therefore, the duty cycle generation process is simple. To achieve a comparable output waveform of PS-PWM, the optimal duty cycle obtained by the multiple-vector MPC algorithm [27], [28] should be equally distributed to each switching pair. In the multiple-vector MPC, the voltage vector is adopted to calculate the optimal duty cycles, which leads to the same dc-link voltage utilization as that of the SVM.

The pulse train generation process of LS-PWM is illustrated in Fig. 1(b). As shown, the duty cycles of some switching pairs are equal to 0 and 1. Only the optimal duty cycle for one switching pair should be determined. To achieve a comparable output waveform of LS-PWM, the classical finite-control-set MPC is utilized to generate the gating signals of the switching pairs with duty cycles of 0 and 1, and the multiple-vector MPC algorithm is utilized to generate duty cycles for the one switching pair, where its optimal duty cycle should be calculated.

III. Proposed MPC

As analyzed in Section II, the MPC of the multilevel converter with the quasi-PS-PWM/LS-PWM output can be achieved by the combination of the finite-control-set MPC and the multiple-vector MPC. The commercialized available 5L-ANPC converter [1], [29] is utilized as a case study to present the main idea of the proposed MPC.

A. Mathematical Model of the 5L-ANPC Converter

The three-phase 5L-ANPC topology, as shown in Fig. 2, is a combination of an ANPC and an FC topology. Each phase

TABLE I
Switching State of a 5L-ANPC Converter

S_{x1}/S_{x2}	S_{x3}	S_{x4}	u_{xo}	v_x	i_{NPx}	i_{fx}
0	0	0	$-u_{dc}/2$	-2	0	0
0	0	1	$-u_{dc}/4$	-1	0	$-i_x$
0	1	0	$-u_{dc}/4$	-1	i_x	i_x
0	1	1	-0	0	i_x	0
1	0	0	0	0	i_x	0
1	0	1	$u_{dc}/4$	+1	i_x	$-i_x$
1	1	0	$u_{dc}/4$	+1	0	i_x
1	1	1	$u_{dc}/2$	+2	0	0

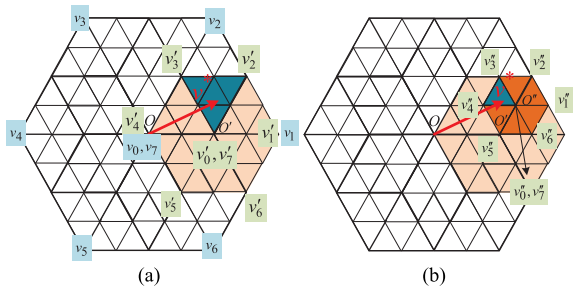

Fig. 3. Space vector diagram for MPC to generate a quasi-PS-PWM/LS-PWM output. (a) Space vector with PS-PWM. (b) Space vector with LS-PWM.

of the 5L-ANPC converter consists of eight switches and an FC. S_{x1}, S'_{x1}, S_{x2}, and S'_{x2} require two switches connected in series or high-voltage switches to bear a higher voltage, which is the double of S_{x3}, S'_{x3}, S_{x4}, and S'_{x4}. S_{x1} and S_{x2} require the same switching signal. The output voltage level and the current direction corresponding to the switching state in the 5L-ANPC are summarized in Table I.

In the 5L-ANPC converter, the number of the voltage vectors in the $\alpha\beta$ frame is $8^3 = 512$. Evaluating all the switching states in the 5L-ANPC converter will lead to a very heavy computational burden. In the proposed method, only the voltage vectors in the vertex and center of the space vector diagram, as plotted out in Fig. 3, are considered. Then, the voltage vector $\boldsymbol{v}$ for the 5L-ANPC converter can be simplified as a two-level converter, and the voltage vector can be listed in Table II.

The output current model can be represented as

$$\boldsymbol{v} = L\frac{d\boldsymbol{i}}{dt} + \boldsymbol{i}R \tag{1}$$

where $\boldsymbol{v} = v_\alpha + jv_\beta$ and $\boldsymbol{i} = i_\alpha + ji_\beta$.

TABLE II
VOLTAGE VECTORS IN THE VERTEX AND CENTER OF THE ORIGINAL HEXAGON

Voltage vector $\boldsymbol{v}$	v_α	v_β	Switching state
$\boldsymbol{v}_0$	0	0	000
$\boldsymbol{v}_1$	$2u_{dc}/3$	0	100
$\boldsymbol{v}_2$	$u_{dc}/3$	$\sqrt{3}u_{dc}/3$	110
$\boldsymbol{v}_3$	$-u_{dc}/3$	$\sqrt{3}u_{dc}/3$	010
$\boldsymbol{v}_4$	$-2u_{dc}/3$	0	011
$\boldsymbol{v}_5$	$u_{dc}/3$	$-\sqrt{3}u_{dc}/3$	001
$\boldsymbol{v}_6$	$-u_{dc}/3$	$-\sqrt{3}u_{dc}/3$	101
$\boldsymbol{v}_7$	0	0	111

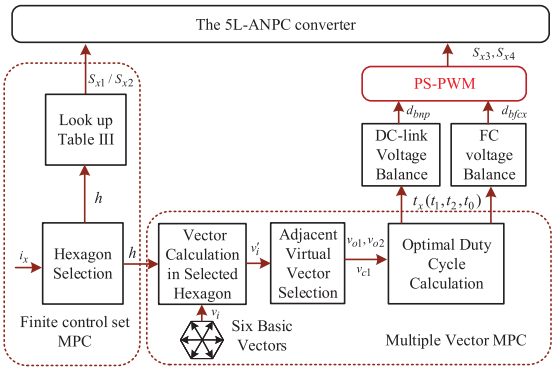

Fig. 4. Control diagram of the proposed MPC with quasi-PS-PWM output.

The FC voltage can be expressed by

$$C_f \frac{du_{fx}}{dt} = i_{fx} \tag{2}$$

where the FC current $i_{fx} = (d_{x3} - d_{x4})i_x$.

The dc-link capacitor voltage difference can be written as

$$C_{\rm dc} \frac{\Delta u_{\rm dc}}{dt} = i_{\rm NP} \tag{3}$$

where $\Delta u_{\rm dc} = u_{\rm dc1} - u_{\rm dc2}$ and $i_{\rm NP} = i_{{\rm NP}a} + i_{{\rm NP}b} + i_{{\rm NP}c}$.

B. MPC With Quasi-PS-PWM Output

In PS-PWM of the 5L-ANPC converter [30], S_{x1}/S_{x2} operates at the fundamental switching frequency. The carriers for S_{x3} and S_{x4} are interleaved with 180° phase shift. Therefore, to achieve a quasi-PS-PWM output, S_{x1}/S_{x2} is the switching state applied during the entire control period. The duty cycle for S_{x3} and S_{x4} will be the same, as shown in Fig. 1(a).

To achieve a comparative output waveform of a PS-PWM using MPC, the switching state of S_{x1}/S_{x2} can be selected and applied during the entire sampling period, while the duty cycles of S_{x3} and S_{x4} are the same and should be calculated using multiple-vector MPC [27], [28]. The full control diagram of the proposed MPC with PS-PWM output is shown in Fig. 4. The basic voltage vectors are the vectors on the vertex of the hexagon, which are listed in Table II.

1) S_{x1}/S_{x2} Selection: When one switching state in a control period is applied, the finite-control-set MPC is inherently equivalent to deadbeat control [31]. As for S_{x1}/S_{x2} selection, only one switching state in a control period should be determined, then the deadbeat approach can be adopted to reduce the computational burden. The desired voltage vector is calculated as

$$\boldsymbol{v}^* = L\frac{\boldsymbol{i}^* - \boldsymbol{i}}{T_s} + \boldsymbol{i}R \tag{4}$$

where $\boldsymbol{v}^* = v_\alpha^* + jv_\beta^*$ and $\boldsymbol{i}^* = i_\alpha^* + ji_\beta^*$.

The desired voltage in the abc stationary frame can be represented as

$$\begin{cases} v_a^* = v_\alpha^* \\ v_b^* = -\dfrac{1}{2}v_\alpha^* + \dfrac{\sqrt{3}}{2}v_\beta^* \\ v_c^* = -\dfrac{1}{2}v_\alpha^* - \dfrac{\sqrt{3}}{2}v_\beta^*. \end{cases} \tag{5}$$

According to Table I, S_{x1}/S_{x2} is 0 when the desired output voltage will be negative, and S_{x1}/S_{x2} is 1 when the desired output voltage will be positive. The switching state of $S_{a1}S_{b1}S_{c1}$ can be determined by looking up Table III. According to Table III, the desired hexagon can be selected, and $\boldsymbol{v}_{c1} = \boldsymbol{v}_h/2$.

2) Adjacent Voltage Vector Selection: After selection of the switching states of S_{x1}/S_{x2}, d_{x3} and d_{x4} should be calculated. As the duty cycles for d_{x3} and d_{x4} are the same, d_{vx} is defined as

$$d_{vx} = d_{x3} = d_{x4}. \tag{6}$$

To simplify the calculation process, S_{x3} and S_{x4} are considered as a whole and represented using virtual switching state S_{vx}. The virtual switching state $S_{vx} = 1$ when $S_{x3} = 1$ and $S_{x4} = 1$, and the virtual switching state $S_{vx} = 0$ when $S_{x3} = 0$ and $S_{x4} = 0$.

If hexagon I is selected, the available hexagon is presented in Fig. 3(a). To be general, the voltage vector $\boldsymbol{v}'$ in the vertex and center of the hexagon in hexagon h can be calculated as

$$\boldsymbol{v}_i' = \boldsymbol{v}_i/2 + \boldsymbol{v}_{c1} \tag{7}$$

where $i \in \{0, 1, \ldots, 7\}$. The correspondent switching states of voltage vector $\boldsymbol{v}'$ are the virtual switching states $S_{va}S_{vb}S_{vc}$. $\boldsymbol{v}_0' = \boldsymbol{v}_7'$.

The proposed method for the optimal duty cycle generation includes three steps: adjacent voltage vector selection, optimal duty cycle calculation for the selected voltage vector, and the duty cycle application to each switching pair in the identical cell.

In the first step, the two adjacent voltage vectors lying in the vertex of the selected hexagon should be selected. Herein,

TABLE III
SWITCHING STATE SELECTION USING HEXAGON SELECTION

Sign			Switching states of $S_{a1}S_{b1}S_{c1}$	Hexagon h
v_a^*	v_b^*	v_c^*		
>0	≤ 0	≤ 0	(100)	1(I)
≥ 0	≥ 0	<0	(110)	2(II)
≤ 0	>0	≤ 0	(010)	3(III)
<0	≥ 0	≥ 0	(011)	4(IV)
≤ 0	≤ 0	>0	(001)	5(V)
≥ 0	<0	≥ 0	(101)	6(VI)

the two adjacent voltage vectors will be selected using a cost function as follows:

$$J_i = (i_\alpha^* - i_\alpha(k+1))^2 + \left(i_\beta^* - i_\beta(k+1)\right)^2 \tag{8}$$

where i_α^* and i_β^* are the reference currents, and $i_\alpha(k+1)$ and $i_\beta(k+1)$ are the predicted current based on the system model.

The currents $i_\alpha(k+1)$ and $i_\beta(k+1)$ can be predicted as

$$\boldsymbol{i}(k+1) = \boldsymbol{i}(k) + \frac{(\boldsymbol{v}(k) - \boldsymbol{i}(k)R)T_s}{L} \tag{9}$$

The current is predicted by substituting $\boldsymbol{v}_i'$ ($i \in \{1, 2, \ldots, 6\}$) into $\boldsymbol{v}$ in (9). The cost function value, when $\boldsymbol{v}_i'$ is substituted, is denoted as J_i.

To selected the two adjacent virtual voltage vectors simultaneously, the cost function can be defined as

$$g_i = J_i + J_{i+1}, \quad i \in \{1, 2, \ldots, 6\} \tag{10}$$

where $J_7 = J_1$. By evaluating (10), two optimal adjacent voltage vectors $\boldsymbol{v}_{o1}$ and $\boldsymbol{v}_{o2}$ with the minimum cost function value will be selected for duty cycle calculation.

3) Optimal Duty Cycle Calculation: The optimal duty cycle is obtained based on the current tracking error minimization. The slopes of the output current of the optimal adjacent vectors can be expressed as

$$\boldsymbol{s}_1 = \frac{1}{L}(\boldsymbol{v}_{o1} - \boldsymbol{i}R) \tag{11}$$

$$\boldsymbol{s}_2 = \frac{1}{L}(\boldsymbol{v}_{o2} - \boldsymbol{i}R) \tag{12}$$

where $\boldsymbol{s}_1 = s_{\alpha1} + js_{\beta1}$ and $\boldsymbol{s}_2 = s_{\alpha2} + js_{\beta2}$.

Moreover, the current slope of the voltage vector lie in the center of the hexagon can be obtained as

$$\boldsymbol{s}_0 = \frac{1}{L}(\boldsymbol{v}_{c1} - \boldsymbol{i}R) \tag{13}$$

where $\boldsymbol{s}_0 = s_{\alpha0} + js_{\beta0}$.

The predicted output currents at the end of the control period can be expressed by

$$i_\alpha(k+1) = i_\alpha(k) + s_{\alpha1}t_1 + s_{\alpha2}t_2 + s_{\alpha0}t_0 \tag{14}$$

$$i_\beta(k+1) = i_\beta(k) + s_{\beta1}t_1 + s_{\beta2}t_2 + s_{\beta0}t_0. \tag{15}$$

Then, the errors between the reference and the predictive current in (8) can be represented using (14) and (15) as

$$\varepsilon_\alpha = \tilde{i}_\alpha + s_{\alpha1}t_1 + s_{\alpha2}t_2 + s_{\alpha0}(T_s - t_1 - t_2) \tag{16}$$

$$\varepsilon_\beta = \tilde{i}_\beta + s_{\beta1}t_1 + s_{\beta2}t_2 + s_{\beta0}(T_s - t_1 - t_2) \tag{17}$$

where $\tilde{i}_\alpha = i_\alpha^* - i_\alpha(k)$ and $\tilde{i}_\beta = i_\beta^* - i_\beta(k)$.

The cost function (8) can be rewritten as

$$J = \varepsilon_\alpha^2 + \varepsilon_\beta^2. \tag{18}$$

To obtain the minimized output current tracking errors, a least-squares optimization problem is formulated to calculate the optimal duty cycles. The optimal values of t_1 and t_2 in (14) and (15) should satisfy the minimum value conditions

$$\frac{\partial J}{\partial t_1} = 0, \quad \frac{\partial J}{\partial t_2} = 0. \tag{19}$$

Therefore, the optimal duty cycles for current tracking can be obtained by solving (19) as

$$t_1 = \frac{(s_{\beta2} - s_{\beta0})\tilde{i}_\alpha + (s_{\alpha0} - s_{\alpha2})\tilde{i}_\beta + (s_{\alpha2}s_{\beta0} - s_{\alpha0}s_{\beta2})T_s}{(s_{\beta2} - s_{\beta0})s_{\alpha1} + (s_{\beta0} - s_{\beta1})s_{\alpha2} + (s_{\beta1} - s_{\beta2})s_{\alpha0}} \tag{20}$$

$$t_2 = \frac{(s_{\beta0} - s_{\beta1})\tilde{i}_\alpha + (s_{\alpha1} - s_{\alpha0})\tilde{i}_\beta + (s_{\beta1}s_{\alpha0} - s_{\beta0}s_{\alpha1})T_s}{(s_{\beta2} - s_{\beta0})s_{\alpha1} + (s_{\beta0} - s_{\beta1})s_{\alpha2} + (s_{\beta1} - s_{\beta2})s_{\alpha0}} \tag{21}$$

$$t_0 = T_s - t_1 - t_2. \tag{22}$$

With the calculated duty cycle and the selected adjacent voltage vector information, d_{vx} can be obtained. According to (6), the duty cycles for S_{x3} and S_{x4} can be obtained. The space vector is directly utilized to calculate the optimal duty cycles. Therefore, the dc voltage utilization of the MPC with quasi-PS-PWM output is the same as that of SVM, however with a much simpler implementation process.

4) DC-Link Capacitor Voltage Balance: As shown in (3), the dc-link voltage balance can be achieved by regulating current i_{NP}. In the center of the selected hexagon h in PS-PWM, two vectors are with the same phase and magnitude, that is, $\boldsymbol{v}_0' = \boldsymbol{v}_7'$. The dc-link capacitor voltage balance can be achieved by adjusting the duty cycles of $\boldsymbol{v}_7'$ and $\boldsymbol{v}_0'$.

The switching states of S_{a1}, S_{b1}, and S_{c1} are (1 0 0) in hexagon I, and $\boldsymbol{v}_7'$ is the vector when S_{x3} and S_{x4} are ON, while $\boldsymbol{v}_0'$ is the vector when S_{x3} and S_{x4} are OFF. In hexagon I, $\boldsymbol{v}_7'$ is the vector when phase "a" is connected to the positive terminal of the dc link and phases "b" and "c" are connected to the neutral point of the dc link. The current will flow from the positive terminal of the dc link to the neutral point of the dc link regardless of the current polarity. In this case, i_{NP} is negative, and Δu_{dc} decreases. In the same way, $\boldsymbol{v}_0'$ is the vector when phase "a" is connected to the neutral point of the dc link and phases "b" and "c" are connected to the negative terminal of the dc link. The current will flow from the neutral point of the dc link to the negative terminal of the dc link regardless of the current polarity. In this case, i_{NP} is positive, and Δu_{dc} increases.

Therefore, these voltage vectors have the same effect on the output current control, but their influences on the neutral point voltage are opposite. Hence, the neutral point capacitor voltage can be balanced by rearranging the time distribution of these voltage vector pairs. The amount of duty cycle for dc-link capacitor voltage balance can be obtained as

$$d_{bnp} = k_{bnp}\frac{\Delta u_{\text{dc}}^* - \Delta u_{\text{dc}}}{u_{\text{dc}}} \tag{23}$$

where $\Delta u_{\text{dc}} = u_{\text{dc2}} - u_{\text{dc1}}$.

Considering the dc-link capacitor voltage, the duty cycle for the center of the hexagon can be rearranged as

$$t_p = t_0/2 - d_{bnp} \tag{24}$$

$$t_n = t_0/2 + d_{bnp}. \tag{25}$$

The range for t_p/t_n is $[0, t_0]$. If k_{bnp} is larger, the dc-link voltage will become balance with shorter time during the dynamic process. However, if k_{bnp} is too large, t_p/t_n is saturated.

In this condition, only a five-segment pulse train will be generated, resulting in even-order harmonics. However, if k_{bnp} is too small, the voltage balance scheme is not effective. Therefore, k_{bnp} is selected using a heuristic searching method.

5) FC Voltage Balance: As the PS-PWM scheme is adopted, the duty cycle for output current control of each part is the same, as presented in (6). Therefore, the FC voltage is naturally balanced in the quasi-PS-PWM output. However, because of the nonlinearity caused by dead time and parameter mismatch in the gate drivers, the FC voltage balance is required.

As S_{x3} and S_{x4} are cascaded cells and the voltage across each cell is the same, the balance of the FC voltage can be achieved by adjusting the duty cycles of S_{x3} and S_{x4}. As long as the sum of the duty cycles of S_{x3} and S_{x4} remains unchanged, the output voltage will not be affected. The duty cycle applied for the FC voltage balance can be denoted as

$$d_{bfcx} = k_{bfc}\text{sgn}(i_x)\frac{u_f^* - u_{fx}}{u_f^*} \tag{26}$$

where $\text{sgn}(*)$ is a sign function that extracts the sign of a real number. If k_{bfc} is larger, the FC voltage will be balanced with shorter time during the dynamic process. However, if k_{bfc} is too large, it will lead to the large oscillation in the FC voltage in the steady state. However, if k_{bfc} is too small, the three FC voltages may be not balanced in the steady state. Therefore, k_{bfc} is also selected using a heuristic searching method. If the FC voltages are around their references, the voltages across S_{x3} and S_{x4} are the same.

The duty cycle for the FC voltage balance can be calculated as

$$d_{x3} = d_{vx} - d_{bfcx} \tag{27}$$

$$d_{x4} = d_{vx} + d_{bfcx}. \tag{28}$$

6) Pulse Train Generation: As analyzed above, the constant-switching-frequency MPC with quasi-PS-PWM output includes two steps during the duty cycle calculation process. In the pulse train generation stage, pulse train generation can also be divided into two steps. First, the switching state S_{x1}/S_{x2} is determined by looking up Table III according to the selected hexagon h. Then, the duty cycles for S_{x3} and S_{x4} are obtained using multiple-vector MPC. As the duty cycle for S_{x3} and S_{x4} is equally distributed, the multiple-vector MPC only need to be implemented for one time. Therefore, the pulse train generation process of the constant-switching-frequency MPC with quasi-PS-PWM output can be illustrated in Fig. 5.

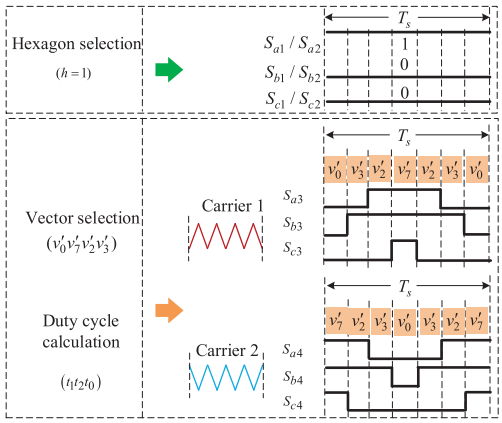

Fig. 5. Illustration of pulse train generation for each switching pairs of the MPC with quasi-PS-PWM output.

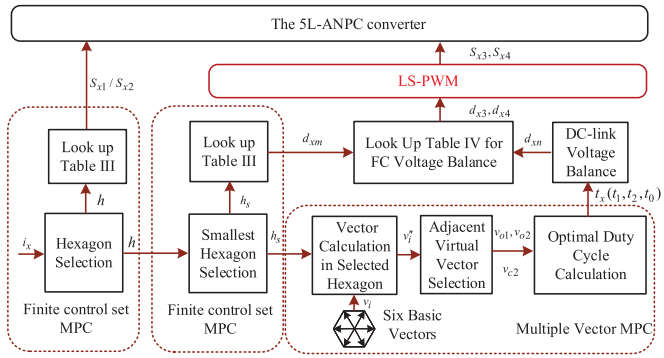

Fig. 6. Control diagram of the proposed MPC with quasi-LS-PWM output.

C. MPC With Quasi-LS-PWM Output

In LS-PWM of the ANPC converter [32], two switching pairs are applied during the entire control period, and the duty cycle will be generated for only one switching pairs, as shown in Fig. 1(b).

1) Output Current Control: Two switching pairs can be selected using the deadbeat approach. The duty cycle calculation for one switching pair is required. S_{x1}/S_{x2} can be calculated using the same method as Sector III-B1. The second switching pair S_{xm}, which will also be applied during the entire period, can be obtained in the same way. The switching state can be determined by selecting the hexagon h_s within the hexagon h, as shown in Fig. 3(b). The full control diagram of the proposed MPC with quasi-LS-PWM output is shown in Fig. 6.

In the middle hexagon, the center of the hexagon has moved from O to O', as shown in Fig. 3. Therefore, the desired voltage vector should also be represented using O' as the beginning of the desired voltage vector. Therefore, the desired voltage vector in the selected hexagon "h" is adjusted as

$$\boldsymbol{v}_s^* = \boldsymbol{v}^* - \boldsymbol{v}_h/2. \tag{29}$$

The desired voltages in the abc frame, i.e., v_{sa}^*, v_{sb}^*, and v_{sc}^*, of $\boldsymbol{v}_s^*$ can be obtained using (5). The switching state of the second switching pair S_{xm} can be selected by looking up Table III. The voltage vector lies in the center of the selected hexagon and is denoted as $\boldsymbol{v}_{c2}$, where $\boldsymbol{v}_{c2} = \boldsymbol{v}_h/2 + \boldsymbol{v}_{hs}/4$.

The last step is to calculate the duty cycle of the third switching pair S_{xn}. After the two-step hexagon selection, the smallest hexagon can be selected, as shown in Fig. 3(b). The voltage vector in the smallest hexagon can be obtained by

$$\boldsymbol{v}_i'' = \boldsymbol{v}_i/4 + \boldsymbol{v}_{c2} \tag{30}$$

where $i \in \{0, 1, \ldots, 7\}$.

The adjacent voltage vector selection from $\boldsymbol{v}_i''$ and optimal duty cycle calculation can be achieved in the same way as those

TABLE IV
d_{x3} AND d_{x4} SELECTION TABLE

		$d_{xm} > d_{xn}$	$d_{xm} < d_{xn}$
$u_{fx} > u_f^*$	$i_x > 0$	$d_{x3} = d_{xn}$	$d_{x4} = d_{xm}$
	$i_x < 0$	$d_{x3} = d_{xm}$	$d_{x4} = d_{xn}$
$u_{fx} < u_f^*$	$i_x > 0$	$d_{x3} = d_{xm}$	$d_{x4} = d_{xn}$
	$i_x < 0$	$d_{x3} = d_{xn}$	$d_{x4} = d_{xm}$

in PS-PWM, which is presented in Sections III-B 2 and III-B 3. In the MPC with quasi-LS-PWM output, the space vector is directly utilized to calculate the optimal duty cycles. Therefore, the dc voltage utilization is also the same as that of SVM, however with a much simpler implementation process.

2) DC-Link Capacitor Voltage Balance: Similar to the dc-link voltage balance method of the MPC with LS-PWM, in the center of the selected hexagon h_s in LS-PWM, two vectors are with the same phase and magnitude, that is, $\boldsymbol{v}_0'' = \boldsymbol{v}_7''$. The dc-link capacitor voltage balance can be achieved by adjusting the duty cycles of $\boldsymbol{v}_0''$ and $\boldsymbol{v}_7''$.

3) FC Voltage Balance: Unlike the PS-PWM-based method, the FC voltage in the MPC with quasi-LS-PWM output is not naturally balanced. To guarantee the stable operation of the 5L-ANPC converter, a proper control scheme must be implemented.

As the voltages across S_{x3} and S_{x4} are the same, the FC voltage balance can be achieved by assigning the duty cycles d_{xm} and d_{xn} to d_{x3} and d_{x4}. The FC voltage value is related to the direction of the phase current and the duty cycle of d_{xm} and d_{xn}. For example, if u_{fx} should increase to reach its reference at the conditions of $i_x > 0$ and $d_{xm} > d_{xn}$, then d_{xm} and d_{xn} should be assigned to d_{x3} and d_{x4}, respectively. Other cases can be analyzed in the same way. Then, the FC voltage balance can be achieved using a simple algorithm, that is, by assigning d_{xm} and d_{xn} to d_{x3} and d_{x4} according to Table IV.

4) Pulse Train Generation: The constant-switching-frequency MPC with quasi-LS-PWM output includes three steps during the duty cycle calculation process. In the pulse train generation stage, it also includes three steps. The switching states of S_{x1}/S_{x2} are determined using the hexagon selection method by looking up Table III. For duty cycles for S_{x3} and S_{x4}, one is obtained using the hexagon selection method and the other is obtained using the multiple-vector MPC. The exact duty cycle for S_{x3} and S_{x4} is determined by considering the FC voltage balance. Therefore, the pulse train generation process of the constant-switching-frequency MPC with quasi-LS-PWM output can be illustrated in Fig. 7.

D. Delay Compensation

In digital implementation of MPC, there is one-step delay between the commanding voltage vector and the applied voltage vector [33] caused by the computation. The two-step prediction should always be implemented to compensate the computational delay to eliminate its adverse effect. Other than the compensation for the output current control, the FC voltage compensation is also required, especially for the MPC with quasi-LS-PWM

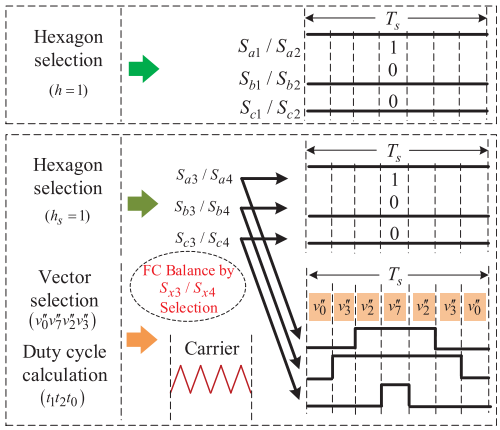

Fig. 7. Illustration of pulse train generation for each switching pairs of the MPC with quasi-LS-PWM output.

TABLE V
SIMULATION AND EXPERIMENTAL PARAMETERS

Simulation	Values	Experiment	Values
DC-link voltage: V_{DC}	1500V	V_{DC}	160V
Load inductance: L	5mH	Load inductance: L	1 mH
Load resistance: R	48.8 Ω	Load resistance: R	9.9 Ω
Output Frequency: f_o	60 Hz	Output Frequency: f_o	60 Hz
DC-link capacitance:C_{dc}	1500μF	DC-link capacitance:C_{dc}	1500μF
Sampling period: T_s	100μs	Sampling period: T_s	100μs
FC capacitance: C_f	50 μF	FC capacitance: C_f	50 μF
		Dead time of IGBTs	1.5μs
		Dead time of GaNs	0.1μs

output. The FC voltage can be compensated as

$$u_{fx}(k+1) = u_{fx}(k) + (d_{x3}(k-1) - d_{x4}(k-1))T_s i_x(k)/C_f. \quad (31)$$

The calculated FC voltage at time instant $k+1$ serves as the initial state of the FC voltage to compensate for the computation delay to reduce the FC voltage ripples.

IV. SIMULATION RESULTS

To validate the effectiveness of the constant-switching-frequency MPC with quasi-PS-PWM/LS-PWM output, simulation studies have been carried out in the MATLAB/Simulink environment. To simplify the presentation, the MPC with quasi-PS-PWM output is denoted as the MPC with PS-PWM, and the MPC with quasi-LS-PWM output is denoted as the MPC with LS-PWM in the following text. The parameters of the simulation and experimental tests are presented in Table V. The equivalent switching frequency of PS-PWM is Nf_c ($N = 2$), while the equivalent switching frequency of LS-PWM is f_c. To achieve a fair comparison of the two MPC methods, the same equivalent switching frequency of the two MPC methods is designed, the carrier period of PS-PWM is set to NT_s, and the sampling point is set to both the top and bottom of each carrier. The carrier period of LS-PWM is set to T_s, and the sampling point is set to the bottom of the carrier. In this way, the sampling frequency and equivalent switching frequency of the MPC with PS-PWM

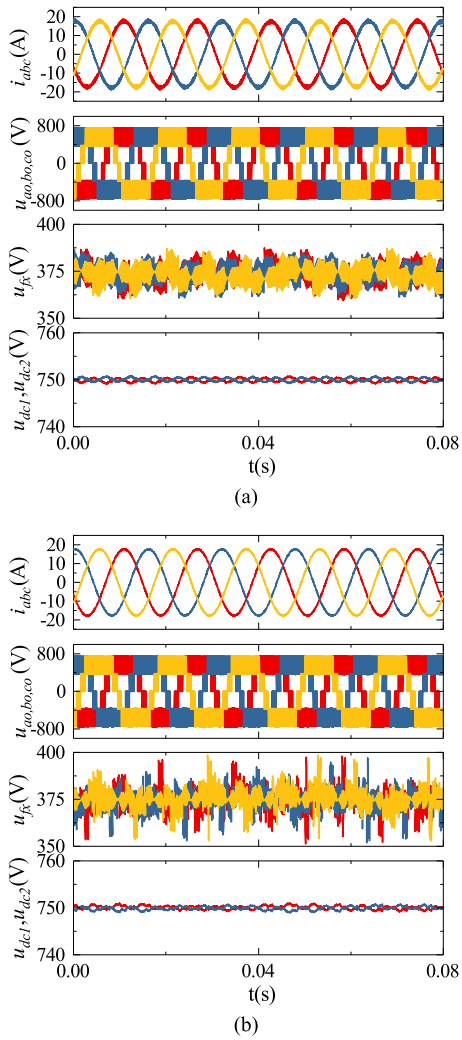

Fig. 8. Steady-state control performance for (a) MPC with PS-PWM and (b) MPC with LS-PWM. For each figure set, from top to bottom are load currents, output voltages, FC voltages, and dc-link capacitor voltages.

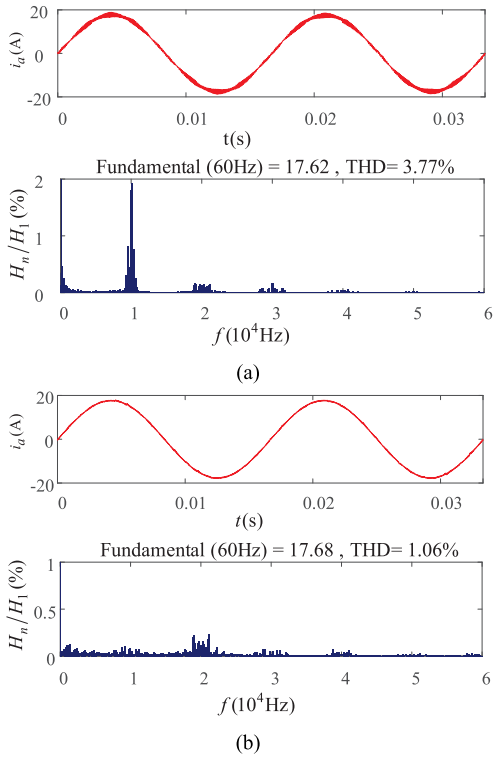

Fig. 9. Steady-state control performance for (a) MPC with PS-PWM and (b) MPC with LS-PWM. From top to bottom, waveforms are the load current and its spectrum.

and LS-PWM are the same, and both are 10 kHz. k_{bnp} is set to 9, and k_{bfc} is set to 0.3.

First, the steady-state performance at an output power of 30 kW is utilized to test the performance of two MPC methods. As shown in Fig. 8, both methods can achieve stable operation of the 5L-ANPC converter with balanced dc-link capacitor voltage, balanced FC voltage, and well-regulated output current. It can be seen that the MPC method with LS-PWM output presents smaller current ripples, while the MPC method with PS-PWM output presents smaller FC voltage ripples. These characteristics are the same with the linear controller with LS-PWM and PS-PWM, indicating that the proposed MPC with LS-PWM/PS-PWM presents the steady-state output waveforms that compared well to LS-PWM/PS-PWM with a linear controller.

In order to further compare the performance of the two MPC methods, the harmonic spectra of the load current are presented in Fig. 9. With the same sampling frequency and switching frequency, the load current total harmonic distortion (THD) of the MPC method with PS-PWM is 3.77%, while that of the MPC method with LS-PWM is 1.06%. It can be seen that the output current quality of the MPC method with LS-PWM presents a much better output current quality. With the proposed MPC method, the constant switching frequency of MPC can be achieved. The current harmonics concentrate on around 10, 20, and 30 kHz, which are in accordance with the times of the equivalent switching frequency.

Other than the steady-state performance evaluation, the dynamic response of proposed MPC methods is also tested. As shown in Fig. 10, the output power is changed from 15 to 30 kW. During the large operation point step changes, the 5L-ANPC converter with both MPC methods operates smoothly. On the other hand, fast dynamic performance is achieved in both cases, indicating that the fast dynamic performance of MPC is maintained. As shown in Fig. 10, the magnitude of the output voltage vector can reach the maximum output voltage magnitude of the SVM, where 863.5 V $\approx U_{\rm dc}/\sqrt{3} = 866$ V. Under this condition, the equivalent duty cycles of each phase $d_x = \frac{S_{x1}}{2} + \frac{d_{x3}}{4} + \frac{d_{x4}}{4}$ are saddle waveforms, which are the same with SVM. Thus, the dc utilization of the proposed methods is comparable with that of SVM.

V. Experimental Results

A 5L-ANPC-converter-based prototype, as shown in Fig. 11, was built in the laboratory to verify the proposed constant-switching-frequency MPC with quasi-PS-PWM/LS-PWM output for multilevel converters. A dSPACE MicroLabBox DS1202

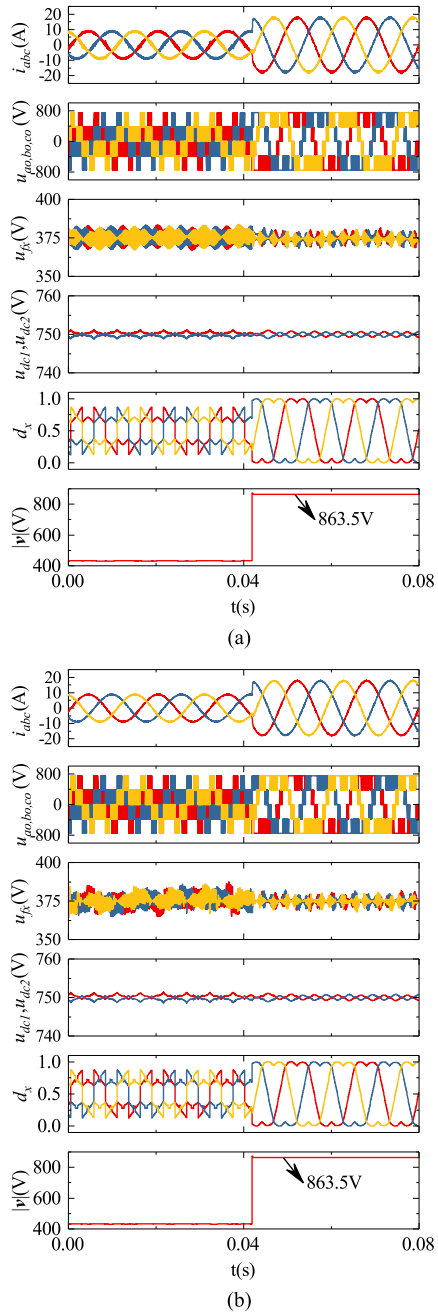

Fig. 10. Transient-state control performance for (a) MPC with PS-PWM and (b) MPC with LS-PWM. From top to bottom, waveforms are load currents, output voltages, FC capacitor voltages, dc-link capacitor voltages, equivalent output duty cycle, and magnitude of the output voltage vector.

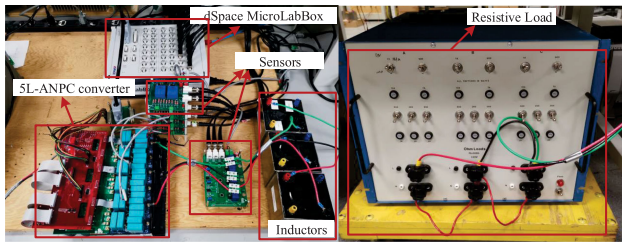

Fig. 11. Experimental setup.

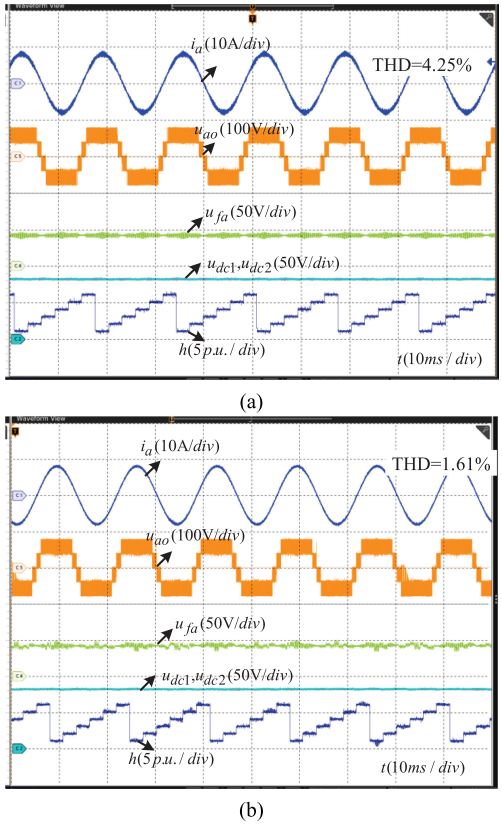

Fig. 12. Steady-state control performance with delay compensation for (a) MPC with PS-PWM and (b) MPC with LS-PWM. For each figure set, from top to bottom are load current, output voltage, FC voltage, dc-link capacitor voltages, and selected hexagon h.

was adopted to implement the digital control, and a slave Xilinx was applied to generate the gate signals for each switch and implement the analog-to-digital conversion. S_{x1}/S_{x2} was implemented by insulated-gate bipolar transistors (IGBTs) (Infineon IKQ50N120CT2), while S_{x3}/S_{x4} was implemented by GaN devices (GaN Systems GS66516). In the following tests, all the variables are directly measured by current and voltage probes. In the experimental verification, the sampling frequency and the switching frequency of the two MPC methods are the same as those designed for the simulation.

One of the major concerns for MPC is the heavy computational burden caused by exhaustive searching of the voltage vector that minimizes the cost functions. As the deadbeat approach is adopted to determine parts of the switching pairs, the cost function evaluation time is reduced to 6. The computation burden of two MPC methods is tested using the dSpace profiler 3.8. It takes 8.84 μs to implement the MPC with LS-PWM, while it takes 9.56 μs to implement the MPC with PS-PWM. The computational burden of both methods only takes less than 10% of the sampling period. The computational burden is acceptable, and the computational burden of the MPC with LS-PWM is 7.5% smaller than that of PS-PWM.

The steady-state control performance with and without delay compensation of the two MPC methods is tested in Figs. 12 and 13. As shown in Fig. 12, both MPC methods can achieve

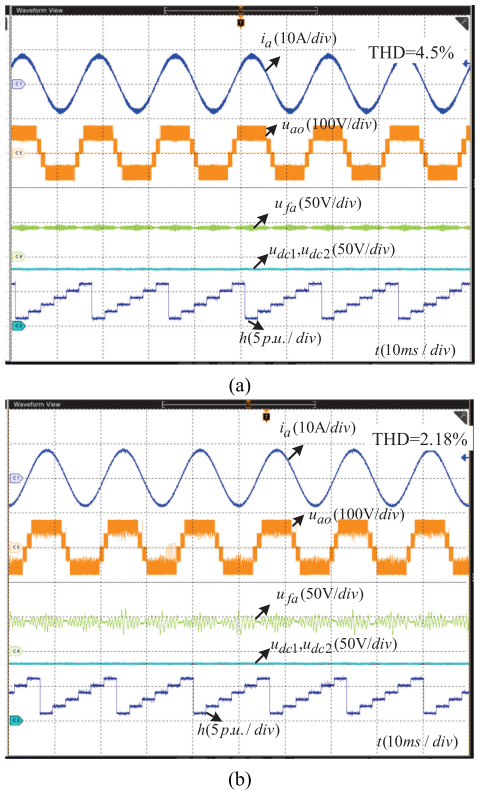

Fig. 13. Steady-state control performance without delay compensation for (a) MPC with PS-PWM and (b) MPC with LS-PWM. For each figure set, from top to bottom are load current, output voltage, FC voltage, dc-link capacitor voltages, and selected hexagon h.

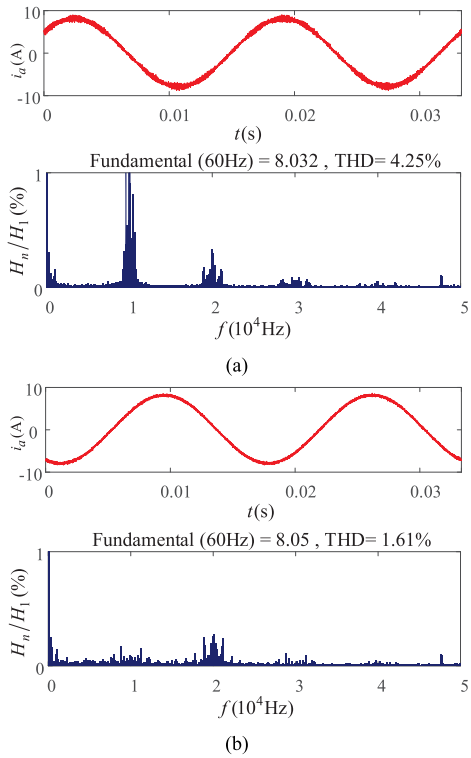

Fig. 14. Fast Fourier transform results of phase "a" current: (a) MPC with PS-PWM; and (b) MPC with LS-PWM. For each figure set, from top to bottom are load current and its spectrum.

a stable operation of the 5L-ANPC converter. The FC voltages are balanced at around $u_{\rm dc}/4$, and dc-link capacitor voltages are balanced at around $u_{\rm dc}/2$. The output voltage u_{ao} is with five stages in both methods. The hexagon switches smoothly in both methods, indicating that the fundamental frequency operation of S_{x1}/S_{x2} is achieved. The current ripples of the MPC with LS-PWM is smaller than that of the MPC with PS-PWM, which agrees with the simulation results. On the other hand, the FC ripples of the MPC with PS-PWM is smaller than that of the MPC with LS-PWM, which also agrees very well with the simulation results. To verify the delay compensation performance, the results of the two methods without delay are presented in Fig. 13. It can be seen that the output current quality of both methods distorted without delay compensation, where the THD of the MPC with PS-PWM increases from 4.25% to 4.50% and that of the MPC with LS-PWM increases from 1.61% to 2.18%. Moreover, the FC ripples of the MPC with LS-PWM increase significantly from ± 5 to ± 15˜V, indicating the necessity of delay compensation for the FC voltage balance in the MPC with LS-PWM.

In order to further validate the steady-state performance of the two MPC methods, the phase "a" current harmonic spectra of the MPC methods are presented in Fig. 14. The data were sampled using an oscilloscope at 1-MHz sampling rate and analyzed using MATLAB. The phase "a" current THD of the MPC with LS-PWM is 1.61%, while the THD of the MPC with PS-PWM is 4.25%. The current harmonics is concentrated at around 10, 20, and 30 kHz, indicating that the constant switching frequency is achieved. The MPC with LS-PWM presents smaller current ripples, which agrees with the simulation results, indicating that the quasi-LS-PWM/PS-PWM output waveforms are achieved using the proposed MPC methods.

Other than the steady-state performance tests, the dynamic performance of the two MPC methods is tested and presented in Fig. 15. During the dynamic performance, the current reference is changed from 4 to 8 A at 0.05 ms. It can be seen that the 5L-ANPC converter is stable during the large operation point step changes in both cases. The FC voltages and dc-link capacitor voltages are balanced during the dynamic. The number of the hexagon switches smoothly even during the dynamic, indicating the fundamental frequency operation even during current reference step changes. The transient response of the MPC with PS-PWM/LS-PWM is very fast, indicating that the advantage of the fast dynamic response in the MPC is maintained. Zoomed waveforms during the load current reference step change from 4 to 8 A are presented in Fig. 16. As shown in the figure, it takes only 0.6 ms to reach its reference in both methods, indicating the fast response in step change of the current reference.

To validate the dc-link voltage and FC voltage balancing capability of the proposed MPC with PS-PWM/LS-PWM, experimental results from unbalanced to balanced capacitor voltage conditions are presented in Figs. 17 and 18. As shown in Fig. 17, the two capacitor voltages are not balanced with a 20-V offset at the beginning, and they become balanced in 30 ms after the

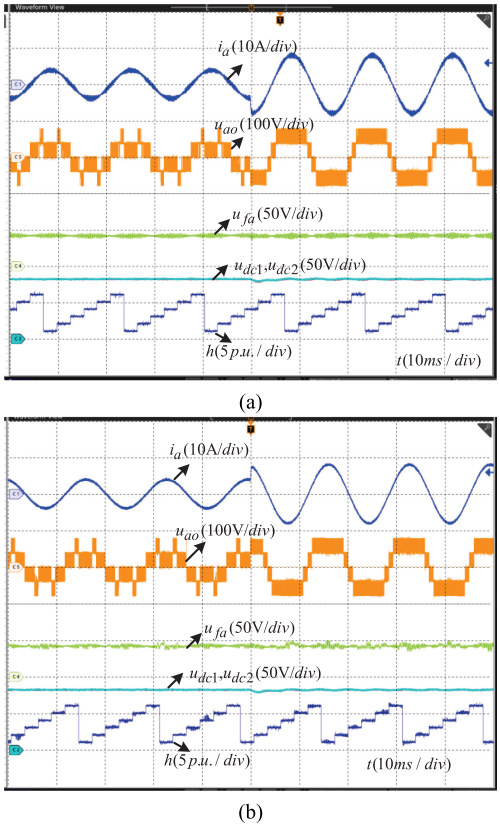

Fig. 15. Dynamic performance for (a) MPC with PS-PWM and (b) MPC with LS-PWM. For each figure set, from top to bottom are load current, output voltage, FC voltage, dc-link capacitor voltages, and selected hexagon h.

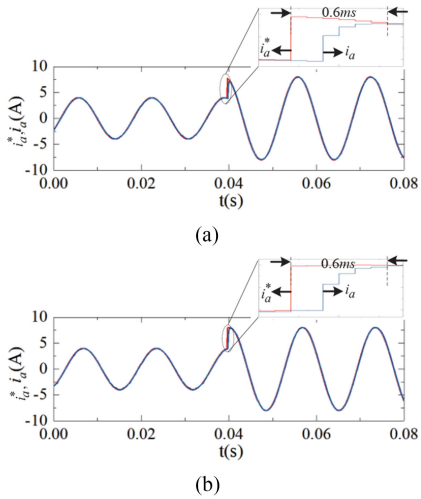

Fig. 16. Zoomed output current tracking performance during transient for (a) MPC with PS-PWM and (b) MPC with LS-PWM.

dc capacitor voltage balancing method is applied, indicating the effectiveness of the dc-link voltage balancing of the proposed MPC methods. The FC voltage balancing capability of the proposed MPC with PS-PWM/LS-PWM is presented in Fig. 18. In the figure, two FC voltages are not balanced with the 10-V offset at the beginning, and they become balanced very quickly

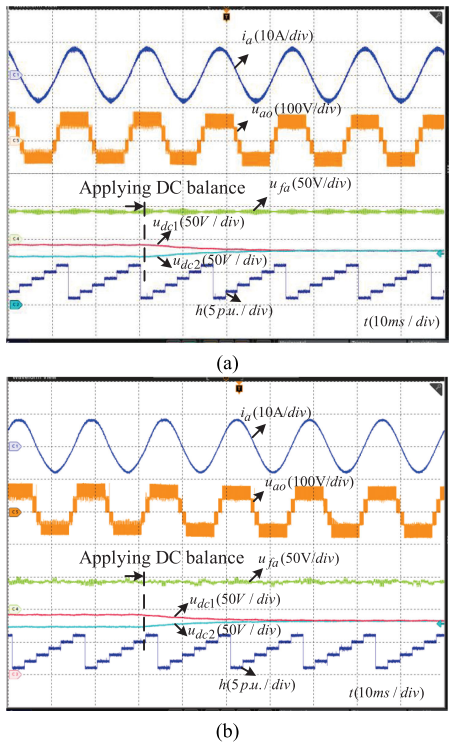

Fig. 17. DC-link capacitor voltage balancing performance for (a) MPC with PS-PWM and (b) MPC with LS-PWM. From top to bottom, waveforms are load currents, output voltages, FC capacitor voltages, dc-link capacitor voltages, and selected hexagon h.

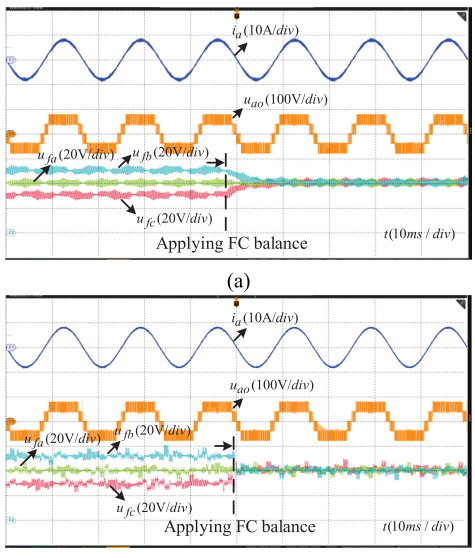

Fig. 18. FC voltage balancing performance for (a) MPC with PS-PWM and (b) MPC with LS-PWM. From top to bottom, waveforms are load currents, output voltages, and three FC capacitor voltages.

after the FC voltage balancing method is applied, indicating the FC voltage balancing capability of the proposed MPC with PS-PWM/LS-PWM method.

VI. Conclusion

In this article, a constant-switching-frequency MPC for the multilevel converter was proposed. By considering the feature of PS-PWM and LS-PWM, the switching pairs of the multilevel converter were categorized into two groups. The switching pairs, which should be applied during the entire control period, were regulated using finite-control-set MPC, while the ones, which should be operated at a constant switching frequency, were regulated by the multiple-vector MPC. The proposed MPC method was easy to implement and had quasi-PS-PWM/LS-PWM output waveforms while retaining the benefit of MPC. Furthermore, the dc voltage utilization of the proposed MPC was comparable to that of the SVM. With the employment of the deadbeat concept, the computation burden could be significantly reduced. The experimental results on a 5L-ANPC converter were presented to validate the effectiveness of the proposed method. The proposed MPC method can be considered as a good candidate for high-performance control of the multilevel converter, where fast dynamic and quasi-PS-PWM/LS-PWM steady-state performance is desired.

References

[1] D. S. Ochs, B. Mirafzal, and P. Sotoodeh, "A method of seamless transitions between grid-tied and stand-alone modes of operation for utility-interactive three-phase inverters," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1934–1941, May/Jun. 2014.

[2] M. Vasiladiotis and A. Rufer, "Analysis and control of modular multilevel converters with integrated battery energy storage," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 163–175, Jan. 2015.

[3] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010.

[4] S. Kouro *et al.*"Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[5] L. Du and J. He, "A simple autonomous phase-shifting PWM approach for series-connected multi-converter harmonic mitigation," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11516–11520, Dec. 2019.

[6] D. Zhou, S. Yang, and Y. Tang, "Model-predictive current control of modular multilevel converters with phase-shifted pulsewidth modulation," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4368–4378, Jun. 2019.

[7] K. Wang, Z. Zheng, Y. Li, K. Liu, and J. Shang, "Neutral-point potential balancing of a five-level active neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1907–1918, May 2013.

[8] Q. A. Le and D. Lee, "Reduction of common-mode voltages for five-level active NPC inverters by the space-vector modulation technique," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 1289–1299, Mar./Apr. 2017.

[9] G. Tan, Q. Deng, and Z. Liu, "An optimized SVPWM strategy for five-level active NPC (5L-ANPC) converter," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 386–395, Jan. 2014.

[10] R. Maheshwari, S. Busquets-Monge, and J. Nicolas-Apruzzese, "A novel approach to generate effective carrier-based pulsewidth modulation strategies for diode-clamped multilevel DC-AC converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7243–7252, Nov. 2016.

[11] S. Busquets-Monge, R. Griñó, J. Nicolas-Apruzzese, and J. Bordonau, "Decoupled DC-link capacitor voltage control of DC-AC multilevel multileg converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 3, pp. 1344–1349, Mar. 2016.

[12] M. Narimani, B. Wu, V. Yaramasu, Z. Cheng, and N. R. Zargari, "Finite control-set model predictive control (FCS-MPC) of nested neutral point-clamped (NNPC) converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7262–7269, Dec. 2015.

[13] V. Monteiro, J. C. Ferreira, A. A. N. Meléndez, and J. L. Afonso, "Model predictive control applied to an improved five-level bidirectional converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5879–5890, Sep. 2016.

[14] T. Geyer and S. Mastellone, "Model predictive direct torque control of a five-level ANPC converter drive system," *IEEE Trans. Ind. Appl.*, vol. 48, no. 5, pp. 1565–1575, Sep./Oct. 2012.

[15] N. Oikonomou, C. Gutscher, P. Karamanakos, F. D. Kieferndorf, and T. Geyer, "Model predictive pulse pattern control for the five-level active neutral-point-clamped inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 6, pp. 2583–2592, Nov./Dec. 2013.

[16] M. Tomlinson, H. D. T. Mouton, R. Kennel, and P. Stolze, "A fixed switching frequency scheme for finite-control-set model predictive control-concept and algorithm," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7662–7670, Dec. 2016.

[17] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model predictive control for power converters and drives: Advances and trends," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 935–947, Feb. 2017.

[18] J. Rodriguez *et al.*"State of the art of finite control set model predictive control in power electronics," *IEEE Trans. Ind. Inform.*, vol. 9, no. 2, pp. 1003–1016, May 2013.

[19] F. Donoso, A. Mora, R. Cárdenas, A. Angulo, D. Sáez, and M. Rivera, "Finite-set model-predictive control strategies for a 3L-NPC inverter operating with fixed switching frequency," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3954–3965, May 2018.

[20] A. Mora, R. Cardenas-Dobson, R. P. Aguilera, A. Angulo, F. Donoso, and J. Rodriguez, "Computationally efficient cascaded optimal switching sequence MPC for grid-connected three-level NPC converters," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12464–12475, Dec. 2019.

[21] Z. Gong, X. Wu, P. Dai, and R. Zhu, "Modulated model predictive control for MMC-based active front-end rectifiers under unbalanced grid conditions," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2398–2409, Mar. 2019.

[22] F. Sebaaly, H. Vahedi, H. Y. Kanaan, and K. Al-Haddad, "Experimental design of fixed switching frequency model predictive control for sensorless five-level packed U-cell inverter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3427–3434, May 2019.

[23] J. Wang, X. Liu, Q. Xiao, D. Zhou, H. Qiu, and Y. Tang, "Modulated model predictive control for modular multilevel converters with easy implementation and enhanced steady-state performance," *IEEE Trans. Power Electron.*, to be published.

[24] F. Sebaaly, H. Vahedi, H. Y. Kanaan, and K. Al-Haddad, "Novel current controller based on MPC with fixed switching frequency operation for a grid-tied inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6198–6205, Aug. 2018.

[25] Y. Yang *et al.*, "Multiple-voltage-vector model predictive control with reduced complexity for multilevel inverters," *IEEE Trans. Transp. Electrific.*, vol. 6, no. 1, pp. 105–117, Mar. 2020.

[26] B. Wu and M. Narimani, *High-Power Converters and AC Drives*, vol. 59. Hoboken, NJ, USA: Wiley, 2017.

[27] Z. Zhang, H. Fang, F. Gao, J. Rodriguez, and R. Kennel, "Multiple-vector model predictive power control for grid-tied wind turbine system with enhanced steady-state control performance," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6287–6298, Aug. 2017.

[28] D. Zhou, P. Tu, and Y. Tang, "Multivector model predictive power control of three-phase rectifiers with reduced power ripples under nonideal grid conditions," *IEEE Trans. Ind. Electron.*, vol. 65, no. 9, pp. 6850–6859, Sep. 2018.

[29] P. Barbosa, P. Steimer, L. Meysenc, M. Winkelnkemper, J. Steinke, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, Jun. 2005, pp. 2296–2301.

[30] K. Wang, L. Xu, Z. Zheng, and Y. Li, "Capacitor voltage balancing of a five-level ANPC converter using phase-shifted PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1147–1156, Mar. 2015.

[31] Y. Zhang, J. Liu, H. Yang, and S. Fan, "New insights into model predictive control for three-phase power converters," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1973–1982, Mar./Apr. 2019.

[32] C. Roncero-Clemente, E. Romero-Cadaval, M. Ruiz-Cortés, and O. Husev, "Carrier level-shifted based control method for the PWM 3L-T-type qZS inverter with capacitor imbalance compensation," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8297–8306, Oct. 2018.

[33] P. Cortes, J. Rodriguez, C. Silva, and A. Flores, "Delay compensation in model predictive current control of a three-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 1323–1325, Feb. 2012.

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