The Influence of the Gate Driver and Common-Source Inductance on the Short-Circuit Behavior of IGBT Modules and Protection

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***Abstract*—In this article, the influence of the gate drive unit on the short-circuit (SC) type II and III behavior of insulated gate bipolar transistor (IGBT) modules was investigated in detail. It is found that the real gate voltage of the IGBT chip contacts cannot be measured across the auxiliary pins of a power module. The difference between applied gate voltage at the sense contacts and the real gate voltage at the IGBT gate contact is shown to be highly dependent on the common-source inductance and hence, the packaging concept. The value of the gate resistance has a significant effect on SC behavior. A gate voltage self-clamping effect during SC was found and verified with the help of circuit simulation. Finally, a gate voltage clamping circuit for improved SC ruggedness of the IGBT modules is introduced. Based on the clamping circuit, a new fast SC type II and III detection method is developed and tested, which can detect and turn-OFF the SC event within 400 ns.**

***Index Terms*—Clamping circuit, gate drive unit (GDU), insulated gate bipolar transistor (IGBT) module, protection, short circuit (SC).**

I. Introduction

AS THE most important component of today's power electronics systems, the insulated gate bipolar transistor (IGBT) is widely used in a variety of power-level applications, from a few hundred volts to several thousand volts [1]. During the lifetime of an IGBT, due to malfunction of the control unit, human error, or other uncontrollable factors, different extreme operating conditions can occur. One of the most common scenarios for IGBTs is the short circuit (SC). In order to avoid damage to the device and even the power system, the SC of IGBTs should be detected and turned OFF within a few microseconds [1]. There are two SC types during the IGBT turn-ON phase. The SC type II, also known as fault under load (FUL) [2], which occurs during the current conducting of the IGBTs. The SC type III describes the occurrence of an SC event during the conduction phase of the antiparallel free-wheeling diode (FWD) [3], [4].

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Both of them have been already investigated in many publications [2]–[7]. A critical situation for the IGBT occurs during an SC type II or III event, caused by the capacitive coupling between the gate-collector capacitance (Miller capacitance). A positive V_{CE} voltage slope during an SC provokes a displacement current through the Miller capacitance, which leads to an overshoot of the gate voltage [1]. Additionally, an accumulation of holes under the gate-oxide takes place, the so-called self-turn-ON effect, causes further rise of the gate voltage dynamically [8]–[10]. Both effects result in a critical SC current peak and thus, more SC energy [1]. Hence, the SC type II and III are considered to be more critical than the direct SC (SC type I). Especially for devices with voltage levels less than 1200 V, the failure mechanism of the SC is usually a thermal failure, which is limited by the critical energy [11], [12].

Considering the protection methods, the well known desaturation monitoring method to detect the collector–emitter voltage V_{CE} under SC faults is widely used [13]. However, this method requires a specific blanking time of a few microseconds to prevent false triggering during the switching process. In [14], a self-adaptive blanking circuit combined with conventional SC protection based on V_{CE} measurement has been introduced. It is suitable for the application of different kinds and working conditions of the IGBTs. Nonetheless, this approach increases the complexity of the driver circuit, and the blanking time remains still above the microsecond level. In [15], a solution with rapid 2-D detection was presented, which can identify SC events and turn OFF IGBTs within a few hundred nanoseconds. The collector current slope $\mathrm{d}i_C/\mathrm{d}t$ and gate emitter voltage V_{GE} are monitored. This SC detection is high speed and can be easily implemented on modules, but it can be triggered unexpectedly by parasitic oscillation in inverter applications when neighboring phases are switched [16]. Another possibility for fast SC detection, as described in [17], uses an internal Rogowski coil as input for fast SC detection of the silicon carbide (SiC) transistors. In this case, the cost of the gate driver would be increased. It should be remarked that the shutdown of an SC should take place after IGBT exits the voltage saturation region to prevent possible dynamic avalanche effects [18], [19]. Second, the IGBT can be turned OFF before reaching an overcurrent two times the rated current [20], which supposes an ultra-fast SC detection.

However, there are only very few publications about the influence of the driver circuit on the SC type II and III behavior, since the gate of the IGBT is already turned ON before SC event,

the transient influence of the gate drive unit (GDU) output stage on an SC can be easily underestimated or neglected. In this article, the influence of the GDU output stage on the SC II and III behavior was investigated. A self-clamping effect caused by the common-source inductance was found during the collector current rise phase, which independently limits the SC current. Moreover, the circuit simulation was utilized to analyze and validate the measurement results. Finally, a clamping circuit consisting of passive components is introduced, aiming to improve the SC ruggedness of IGBT power modules. Based on this clamping circuit, a new fast SC detection method using gate voltage monitoring was developed and tested.

The organization of the article is as follows. Section II presents the experimental setup used; the effect of different gate resistances and reference points on the test results of SCs is shown as well. Section III analyzes the self-clamping effect. Section IV introduces the clamping circuit for improving the SC robustness. Section V introduces the SC detection method based on the clamping circuit. In Section VI, the main conclusion of this article is summarized.

II. Experimental Setup and Results

In this section, the experimental setup for the different SCs is introduced, and the influence of the GDU on the SC behavior is investigated; the measurement results are shown.

A. Testbench Configuration

The IGBT module FS75R17KE3 from Infineon with Econopack was chosen for the investigation. There are six subsystems inside the module (three half-bridge structures). Each subsystem consists of an IGBT chip with antiparallel FWD. The rated current of these modules is 75 A at 15 V gate voltage. The rated blocking voltage is 1.7 kV. The housing of the Econopack package can be removed easily; hence, the influence of the parasitic inductances on the measurements can be minimized in order to realize more precise results. All SC measurements were carried out for only one subsystem (third phase, bottom side). The simplified experimental setup is shown in Fig. 1. The switch S is used to change the position of load inductance L_{load} for SC type II and III investigations, respectively. When performing SC type II test, the load inductor is connected in parallel with the upper IGBT. For SC type III, it is connected in parallel with the lower IGBT.

To achieve a low-inductive experimental setup, the high-side IGBT in the third phase was used as auxiliary switch, which generates the SC event. With respect to the same current rating of both IGBTs, different gate voltage levels are necessary to ensure that the top-side IGBT remains in the voltage saturation area during the SC of the bottom IGBT. In the following SC investigations, the gate voltage of the top-side IGBT and the device under test (DUT) are 30 and 12 V, respectively. The total parasitic inductance L_{par} of the test setup is approximately 55 nH, which can be determined from double-pulse or SC test. This parasitic inductance should be set as small as possible, which corresponds to practical applications. The realized measurement setup is shown in Fig. 2.

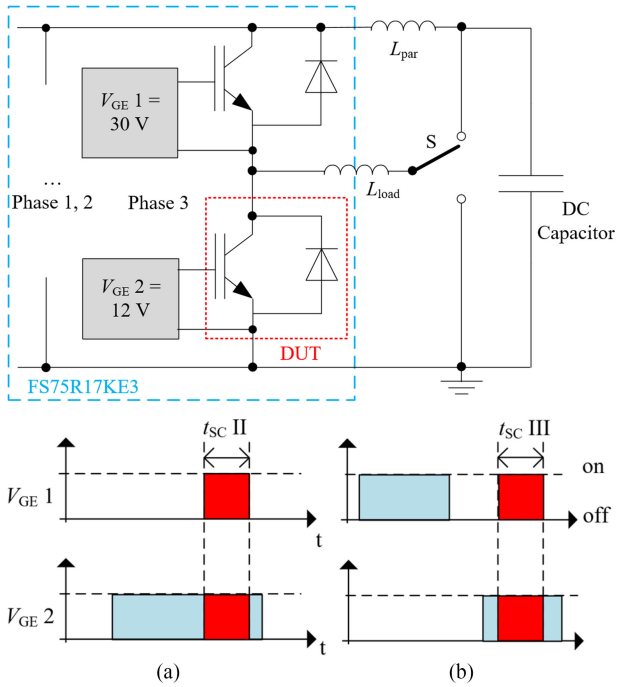

Fig. 1. SC type II and III simplified circuit and the pulse pattern: (a) SC type II, and (b) SC type III.

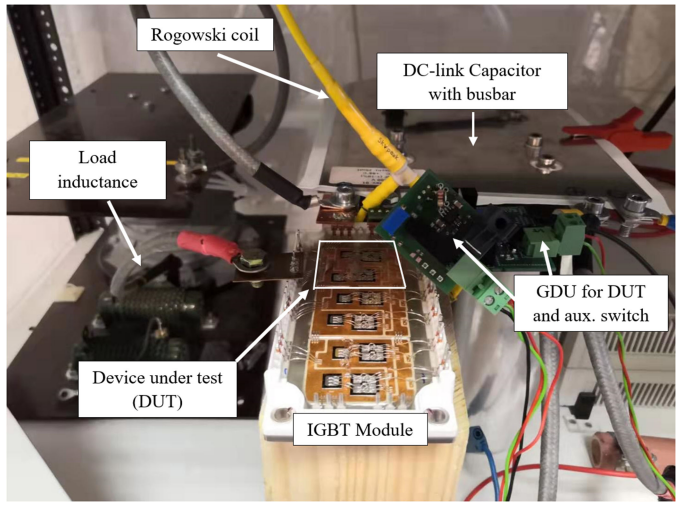

Fig. 2. Measurement setup for SC.

B. GDU Output Stage

The output stage of the GDU is introduced in this subsection, which is essential for analyzing the influence of the gate resistance and the gate self-clamping effect. The widely used GDU output stage is designed with a complementary metal-oxide-semiconductor field-effect transistor (CMOS) push–pull structure [21]. Fig. 3 shows the two types of schematic used and the gate current path during turn-ON and turn-OFF. The buffer capacitances supply the positive and negative gate voltage and provide the gate current to charge and discharge the input capacitance of the IGBT. The gate resistors are placed at the source contacts of the amplification MOS in order to control the

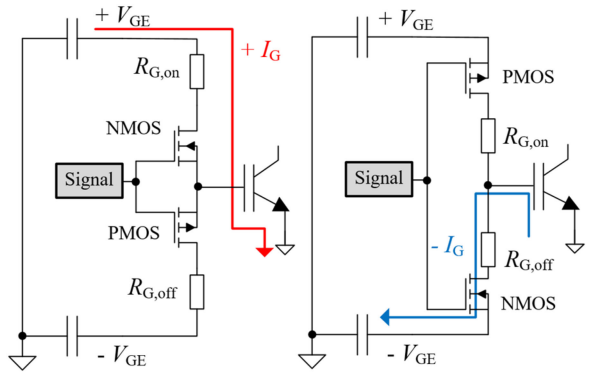

Fig. 3. Two types of CMOS push–pull structure and gate current path during turn-ON (right) and turn-OFF (left).

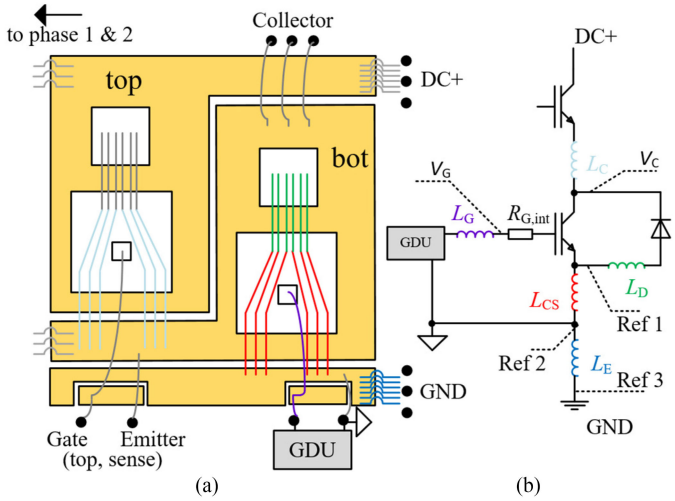

Fig. 4. (a) Module layout of the DUT. (b) Equivalent circuit with parasitic inductances; L_G gate inductance; L_C collector inductance; L_{CS} common-source inductance; L_D FWD inductance; L_E emitter stray inductance; and $R_{G,int}$ gate internal resistance.

switching speed as well as avoid the SC between $+V_{GE}$ and $-V_{GE}$ since the switching speed of the p-type MOS (PMOS) and n-type MOS (NMOS) are usually not identical.

Without any control signal, the bottom MOS is turned ON, and kept so to set the negative gate voltage at the DUTs gate. After the GDU receives the control signal, the bottom MOS is turned OFF at the same time the top MOS is turned ON and the gate current of the DUT flows through the top side MOS, the gate turn-ON resistor $R_{G,on}$ and charges the input capacitance. The topside MOS remains ON until receiving the next turn-OFF signal from the control unit. For turn-OFF of the IGBT, the process is as abovementioned but vice versa.

C. Module Layout of the DUT

For accurate measurements, the housing of the IGBT module has been removed. A sketch of the module layout and the equivalent circuit is shown in Fig. 4.

The bottom IGBT and diode are used for the SC investigations. Different parasitic inductances are highlighted with different colors within Fig. 4. The black dots in Fig. 4(a) symbolize the connection pins of the module, which are accessible from the outside of the module housing. The dotted lines in Fig. 4(b) represent different voltage measurement points and three possible reference points. The gate voltage has been measured using three different reference points aiming to investigate the influence of the gate stray inductance included in the V_{GE} measurement loop. Therefore, the passive probe tip has been connected to the IGBTs gate pad directly, while the position of the probes ground has been varied according to the reference points depicted in Fig. 4. Reference point 1 is the emitter bond wire close to the chip. Reference point 2 contains the common-source inductance and is thus the emitter sense contact of the module. As reference point 3, the emitter load terminal of the module has been chosen. Results comparing the three reference points are shown in the next subsection. The GDU was connected to the gate sense and emitter sense pins of the bottom side IGBT. The common-source inductance L_{CS} is composed of six bond wires [see Fig. 4(a), red] from the chip emitter metallization to the sense emitter connection pad. The tested module's IGBT chips include an 8.5 Ω internal gate resistor [22], which has to be taken into account as well. All other parts of the emitter stray inductance (DCB substrate and wire bonds) are summarized in L_E, which is shown in blue color. The parasitic capacitances of the current path are in the range of picofarad and are not considered in this article.

D. Measurement Results

The SC type II and III measurement results with different external gate turn-ON resistors $R_{G,on}$ and measurement reference points are shown in this subsection.

Fig. 5 shows the influence of $R_{G,on}$ on the SC type II. The reference point Ref 1 was used initially, in order to minimize the measurement error caused by the common-source inductance L_{CS}. For all measurements, the gate turn-OFF resistor was set to 98 Ω, to realize a soft turn-OFF.

As shown in Fig. 5, for $R_{G,on} = 0.3$ Ω, the gate voltage V_{GE} decreases at the beginning of the SC type II event at $t = 0.4$ μs due to the feedback of the common-source inductance (self-clamping effect) caused by di_C/dt. With the increase in $R_{G,on}$, the reduction of the gate voltage becomes smaller, and instead of a gate voltage overshoot, a more extended phase of increased gate voltage phase is distinguished by higher $R_{G,on}$. After the self-clamping took place, the gate is charged due to the positive V_{CE} slope through the Miller capacitance, which finally leads to an increased gate voltage. At higher collector voltages, the Miller -capacitance becomes smaller, and the gate voltage drops to the static applied gate voltage level. The SC current peak using a 0.3 Ω external gate resistor amounts 1136 A, which is more than 15 times the rated current. The reason is that the self-clamping effect of the gate voltage is damped by the 8.5 Ω internal gate resistance. It can also be seen in Fig. 5 that the peak value of the SC current increases with the increase of $R_{G,on}$ due to the weakened gate voltage self-clamping. For SC type III, the same effect is observed as well. The detailed analysis of this process is described in the next section. The self-turn-OFF

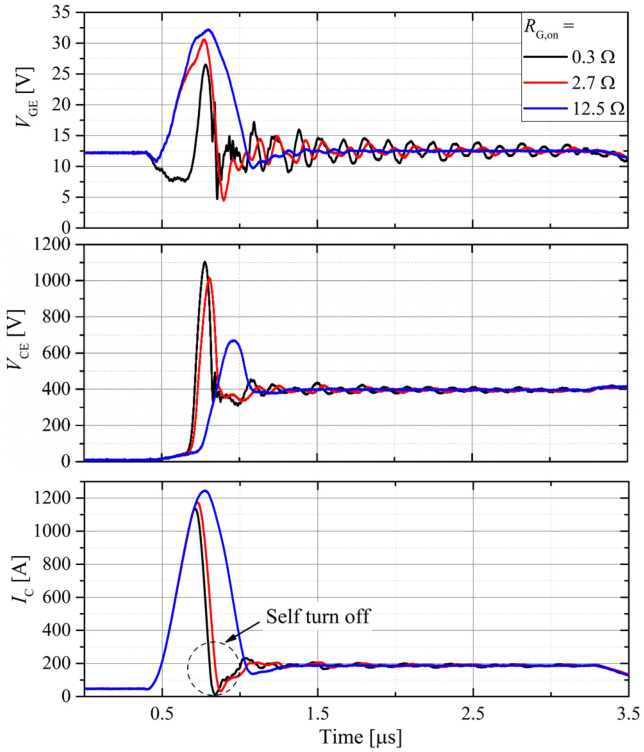

Fig. 5. SC type II measurement with different gate turn-ON resistors. $V_{CE} = 400$ V, $V_{GE} = 12$ V.

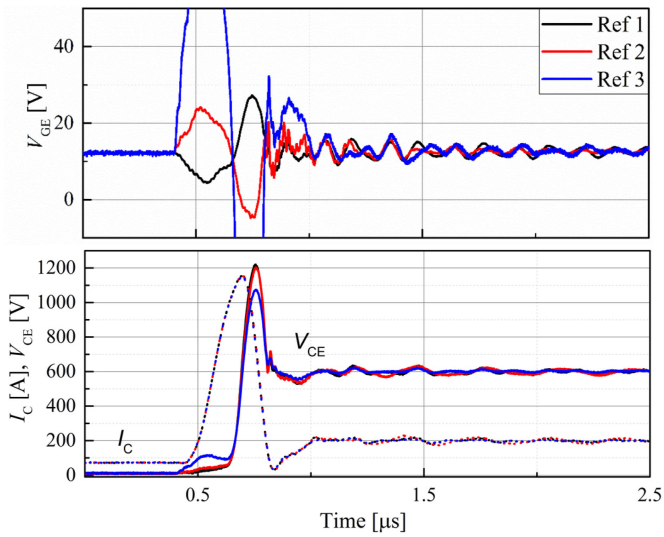

Fig. 6. Impact of the different measurement reference points. $V_{CE} = 600$ V, $V_{GE} = 12$ V, $R_{G,on} = 0.3\ \Omega$.

effect, which is described in [23], can be observed due to the high negative dv_{CE}/dt.

Fig. 6 shows the impact of the different measurement reference points, comparing the gate voltage recorded for different ground lead positions. The deviation of the measured voltage of Ref 1 and Ref 2 is more than 30 V. The voltage curves measured at both reference points are completely opposite, which could lead to erroneous experimental analysis. Without removing the module housing, V_{GE} can be solely measured at the module's auxiliary gate and emitter contacts (reference point 2).

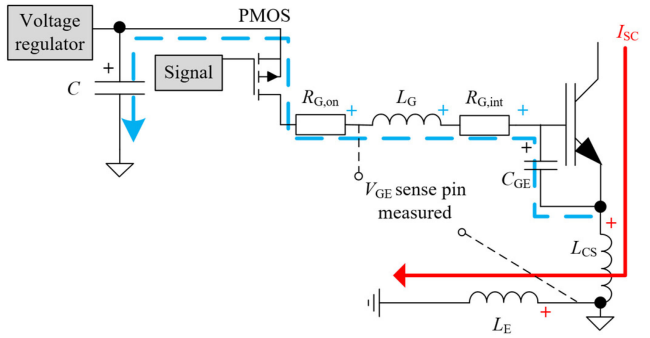

Fig. 7. Equivalent circuit and current flow at the onset of the SC.

III. Analysis of the Gate Self-Clamping and Simulation

In this section, the gate voltage self-clamping effect, which is caused by the common-source inductance, and the influence of the gate turn-ON resistor are analyzed and verified by circuit simulations.

Fig. 7 shows the equivalent circuit of the GDU output stage and the involved DUT during the SC type II and III event. Before the SC, the IGBT is already turned ON; the gate-emitter capacitance C_{GE} is charged and almost equal to the voltage of the buffer capacitance C (black +) of the driver's output stage. During SC, the collector current (red arrow in Fig. 7) flows through the IGBT, the common-source inductance L_{CS}, and the emitter stray inductance L_E, and generates voltages V_{LCS} and V_{LE}, respectively (red +). Thus, a compensating current (dashed arrow) has to flow through the gate inductance L_G and gate turn-ON resistor into the GDU, generating a negative feedback. The MOSFET for negative gate voltage is turned OFF at this moment; therefore, the current cannot flow in this direction.

The ON-state voltage drop of the PMOS can be neglected. The voltage equation of the GDU loop at the beginning of the SC can be expressed as follows:

$$V_C + V_{RG} + V_{LG} \approx V_{GE} + V_{LCS} \tag{1}$$

where V_C is the voltage at the buffer capacitor C of the gate driver and V_{RG} is the sum of the voltage drop across the gate resistor (internal and external). Assume that the internal gate resistance is zero; the measured gate-emitter voltage at the measurement point Ref 2 is higher than the real gate voltage V_{GE}. If the measurement reference point Ref 3 is used, the inductive voltage on the emitter stray inductance V_{LE} is included as well. The inductive voltage on the common-source inductance during the SC can be calculated by

$$V_{LCS} = L_{CS} \cdot \frac{\mathrm{d}i_C}{\mathrm{d}t}. \tag{2}$$

The current slope di_C/dt is defined by the dc-link voltage V_{DC} and the inductance L_{par} in the SC loop. Since the buffer capacitor C (μF range) is much bigger than the internal gate-emitter capacitance C_{GE} (nF range) of the device, the voltage

V_{C} hardly changes during the current rise time. Therefore, due to the induced voltage V_{LCS}, the real gate-emitter voltage is forced to be pulled down. A discussion about the stability of the system of gate driver and semiconductor parasitic components can be found in Section IV.

The influence of $R_{G,\mathrm{on}}$ is further discussed. If $R_{G,\mathrm{on}}$ is very small, e.g., 0 Ω, the voltage drop V_{RG} is also 0 V, and the self-clamping has the maximum impact on the gate voltage of the chip. The larger the resistance, the weaker the self-clamping effect, which matches very well with the measurement results in Fig. 5. After the collector current maximum, $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ becomes negative; a gate voltage peak can be measured (Fig. 5, $R_{G,\mathrm{on}} = 0.3\ \Omega$); this peak is not only caused by the well known capacitive coupling effect through the Miller capacitance. At this time the V_{CE} voltage starts to desaturate, which affects the gate voltage strongly due to the fact that the Miller capacitance is large at low V_{CE} voltages. At the same time, a voltage on L_{CS} is induced during the current falling which also increases the gate voltage. The gate inductance L_{G} has a similar effect on the self-clamping effect as $R_{G,\mathrm{on}}$. For the case of low gate inductance as investigated in this article, the induced voltage on L_{G} may smaller compared with the voltage drop of the gate resistor. If the gate inductance is very high, e.g., a few hundred nH or even a few μH, the self-turn-OFF scenario can happen more probably [23].

A circuit simulation using *LTspice* for the SC was built to provide a detailed analysis. It should be emphasized that this simulation can only analyze the voltage and current on circuit level. The influence caused by internal processes of the semiconductor will not be addressed using this SPICE circuit simulation. Fig. 8 shows the simulation circuit of the GDU output stage. The gate turn-ON/OFF resistors are set to 5 and 98 Ω, respectively. In order to amplify the impact of the common-source inductance L_{CS}, 10 nH was assumed. The positions of the reference points were set according to the measurements. The dc gate voltage supplies were simplified with the voltage source including internal resistance.

Before onset of the SC, a collector current of 75 A is flowing through the IGBT. At about 50 ns, the SC occurs, the collector current increases rapidly, and the inductive voltage across L_{CS} reaches about 20 V. (V_{LCS}). As a consequence, a current, shown in Fig. 8 as I_{LG}, of about 1.5 A flows into the GDU, which causes a 7.5 V voltage drop across the gate turn-ON resistor ($V_{\mathrm{RG\_ON}}$). The voltage across the gate stray inductance is less than 1 V; therefore, it is not shown in the simulation results. The gate voltage V_{GE} is sensed from gate sense to Ref 1, a drop is observed as well, which almost equals the difference between the inductive voltage V_{LCS} and voltage $V_{\mathrm{RG\_ON}}$. The simulation shows good agreement with the measurement results.

IV. Clamping Circuit

Considering that the gate turn-ON resistor has a significant impact on the SC behavior, with the aim of better SC robustness, $R_{G,\mathrm{on}}$ of the IGBT should be set as small as possible. However, one obvious drawback with small $R_{G,\mathrm{on}}$ is the problem of electromagnetic compatibility at highly frequent switching

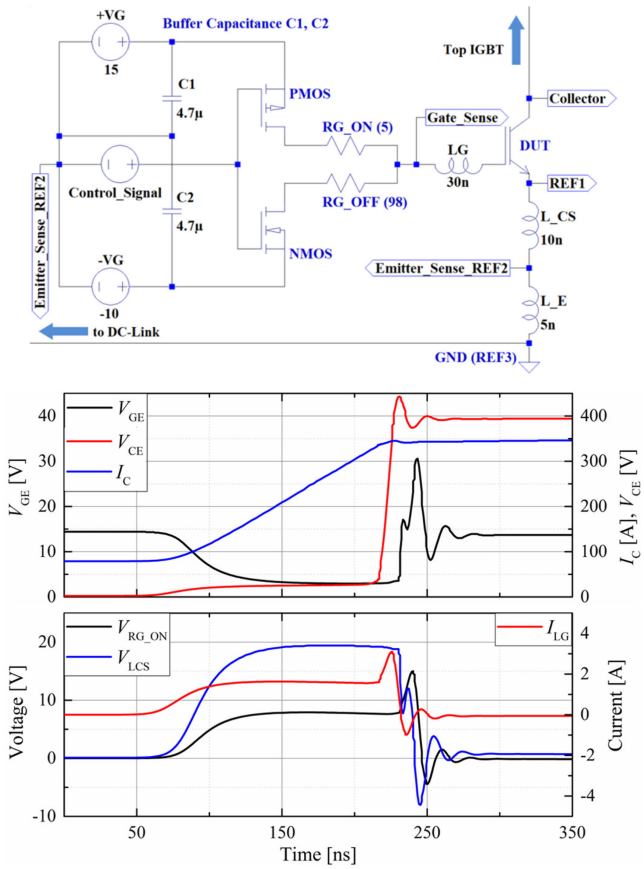

Fig. 8. Simulation circuit of the GDU output stage (top) and simulation results during SC type II (bottom).

operations. A faster reverse-recovery behavior of the FWD has to be taken in to account when using low resistive gate on path, which may result in additional oscillations.

In this section, a clamping circuit is introduced, which can limit the IGBT's gate voltage by using the negative feedback effect of the common-source inductance and emitter stray inductance independently of the used gate resistance.

A. Composition and Working Principle

A minimalistic attempt to achieve the self-clamping effect independent of $R_{G,\mathrm{on}}$ is an antiparallel clamping diode $\mathrm{D_C}$ across $R_{G,\mathrm{on}}$, as depicted by the yellow dashed line in Fig. 9(a). During normal turn-ON, the gate current flows through $R_{G,\mathrm{on}}$. When an SC takes place, the clamping diode $\mathrm{D_C}$ bypasses $R_{G,\mathrm{on}}$ and the reverse gate current due to the induced voltage flows through $\mathrm{D_C}$. However, for some gate driver ICs, (e.g., 1ED020I12FA2 from Infineon) the output for turn-ON and turn-OFF are combined. Hence, it is necessary to include a minimum of one diode into the gate path, to separate the gate ON and OFF resistor to achieve fast turn-ON and soft turn-OFF, as sketched in Fig. 9(b). This layout leads to a more critical SC behavior, since the reverse gate current must pass through a typical big gate turn-OFF resistor, resulting in substantially no clamping effect on the gate voltage. The proposed clamping diode in Fig. 9(a) will not function either.

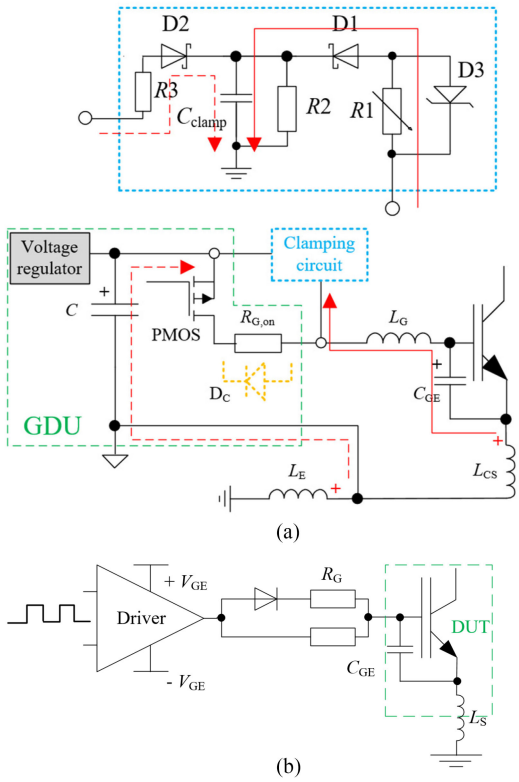

Fig. 9. (a) Schematic of the clamping circuit and current flow (red) at the onset of the SC. (b) Combined GDU output stage with separate gate resistor.

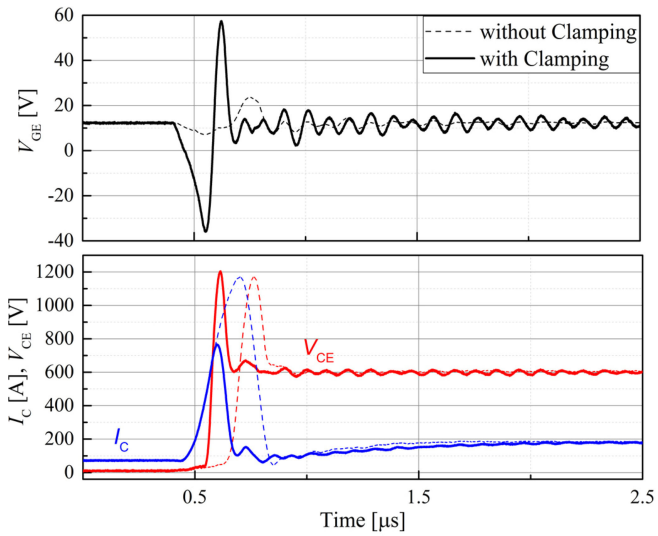

Fig. 10. SC type II measurement: $V_{CE} = 600$ V, $V_{GE} = 12$ V, $R_{G,on} = 0.3\,\Omega$, $R_1 = 0\,\Omega$.

Fig. 9(a) shows the schematic of the clamping circuit. The clamping circuit consists of two fast Schottky diodes D1 and D2, a transient voltage suppressor (TVS) diode D3, a clamp capacitor C_{clamp} with 4.7 μF, a 100-kΩ discharge resistor R2, and a voltage dividing resistor R1. The clamping capacitor C_{clamp} has a similar function as the buffer capacitor in the gate driver's output stage—stabilizing the gate voltage. Thus, the value should be in the order of μF. The adjustable resistor R1 should be set as small as possible to obtain better clamping effect, resistor R3 was set to 100 Ω. R3 has two functions—limit the output current of the voltage regulator and prevent the inductive current caused by the emitter stray inductance L_E to flow back into the driver when an SC occurs, which is shown as red dashed line in Fig. 9(a).

It is worth to note that the extraction of parasitic parameters of the IGBT is important for the configuration of the gate drive and the clamping circuit. The Miller capacitance of the device can be measured by the methods described in [24] and [25] to estimate the intensity of the Miller effect. Apart from that, it can be found in most semiconductor datasheets, although the values of most datasheets are only valid within a limited range of bias voltages. When the voltage increases, the Miller capacitance, however, decreases, so the Miller effect at high voltages is relatively weak.

A knowledge of the values of common-source inductance L_{CS} and emitter stray inductance L_E is essential for the proposed clamping circuit, since it utilizes the negative feedback of the collector current through those inductances to suppress the gate voltage overshoot. L_E can be measured with the voltage drop between the sense emitter and load emitter terminal from switching waveforms. Accurate methods to model extract parasitic inductances are used by software tools, such as *ANSYS Q3D Extractor*.

Under common operation conditions, the voltage V_{clamp} of the clamp capacitor is approximately equal to the output voltage of the linear regulator. It is precharged after turning ON the power supply of the driver board through D2. Only a small influence on the switching behavior could be found, due to the functions of diode D1. While in SC type II or III, the collector current flows via the total emitter stray inductance L_S ($L_S = L_{CS} + L_E$), generates a voltage V_L, and thus, a current into the clamping capacitor through R1. The clamping circuit provides a feedback loop and reduces the gate voltage. Neglecting the voltage on the gate stray inductance, (1) can be modified to

$$V_{Clamp} + V_{R1} = V_{GE} + V_{LCS} + V_{LE} + V_{D1}$$
$$V_{GE} \approx V_{Clamp} + V_{R1} - V_{LS}. \quad (3)$$

The forward voltage drop of D1 is neglected as well; the gate voltage can be described with (3). With the proposed clamping circuit, not only the common-source inductance, but also the emitter stray inductance can be used to limit the gate voltage. This is helpful for the low common-source inductance IGBT packaging configuration, e.g., TO-247 with four pins or IGBT high-power modules (IHM) using the load terminal for connecting the clamping circuit. The resistance R1 is used to adjust the amplitude of the negative feedback, and works as the aforementioned $R_{G,on}$. The TVS diode D3 is applied to limit the maximum voltage on R1, to avoid the disappearance of the feedback (see Fig. 5 with high $R_{G,on}$).

B. SC Measurements With and Without Clamping Circuit

In this subsection, the SC type II and III measurement results are shown with and without the clamping circuit. The voltage dividing resistor R1 was set to 0 Ω in order to obtain the highest impact of the feedback clamping effect.

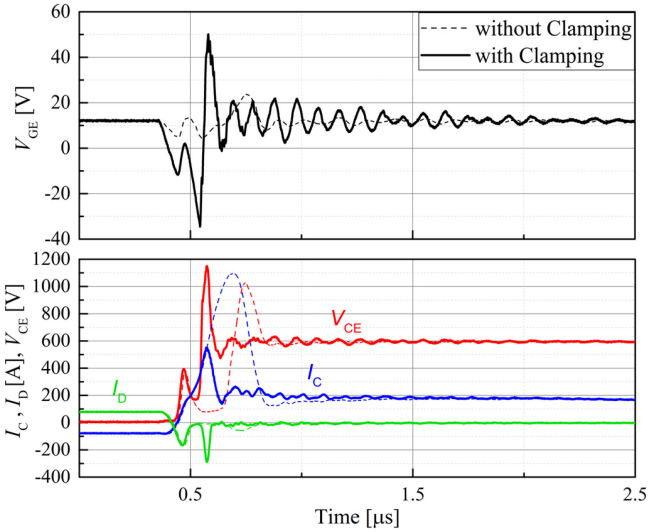

Fig. 11. SC type III measurement: $V_{CE} = 600$ V, $V_{GE} = 12$ V, $R_{G,on} = 0.3\ \Omega$, $R_1 = 0\ \Omega$.

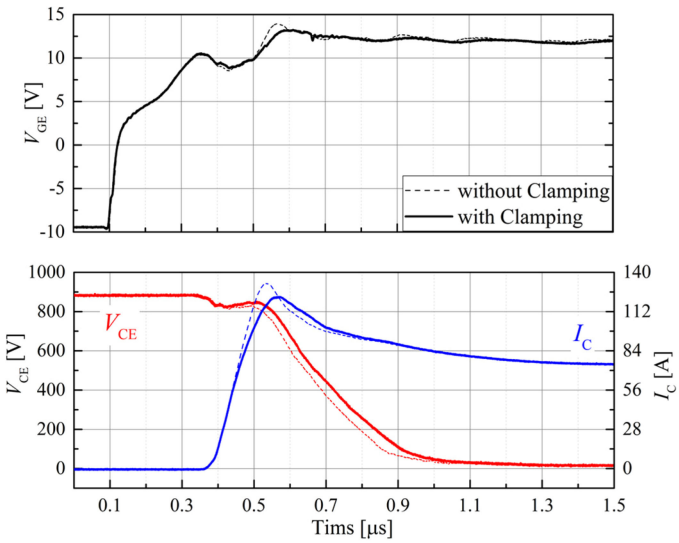

Fig. 12. Double-pulse measurement turn-ON behavior. $V_{CE} = 900$ V, $V_{GE} = 15$ V, $R_{G,on} = R_{G,off} = 6.4\ \Omega$, $R_1 = 0\ \Omega$.

For better analysis, only the first 2.5 μs results are shown. For SC type II, as shown in Fig. 10, before the SC occurrences, a rated current of 75 A flows through the IGBT. During onset of the SC, the gate voltage is pulled down much stronger than without the clamping circuit; a negative gate voltage of -36 V is measured. However, this is due to the measurement error caused by the internal gate resistor; the real gate voltage is still positive. The collector current peak was suppressed to 766 A in comparison to 1172 A without the clamping circuit. The duration of the gate voltage overshoot was found to be approximately 180 ns shorter.

The SC type III measurement is shown in Fig. 11. The current of the FWD I_D was separately measured as well. Before the onset of the SC type III, there was a 75 A flow through the diode. When the SC occurs, the reverse-recovery current of the diode commutates from the FWD to the IGBT and the IGBT is turned ON passively. A collector voltage peak of around 400 V was measured, which is similar to the forward recovery behavior of a similar doped pin-diode of the same voltage class [1]. After the diode's reverse-recovery maximum current peak I_{RRM}, the current slope through the diode changes direction, which can also be seen as a step in the collector current of the IGBT before another steep positive di_C/dt takes place. Each positive di_C/dt slope causes a reduction of the gate voltage. Similar to SC type II, the current with applied clamping circuit is decreased from 1100 to 543 A.

Due to the value of the internal resistance of the DUT, the negative feedback utilized by the clamping circuit cannot avoid the current peak caused by the Miller effect completely. For low-resistive internal gate structure, the effect of the clamping circuit is more pronounced. In multi-chip modules, dynamic current imbalances due to internal gate oscillation have to be taken into account, when reducing the gate resistance. A compromise needs to be found to achieve sufficient efficiency of the clamping circuit and stable dynamic operation in multichip modules. The influence of the clamping circuit on the SC current peak suppression for discrete IGBT devices with low internal gate resistance is shown in [26].

TABLE I
RESULTS OF DOUBLE-PULSE TEST

$V_{CE} = 900$ V, $V_{GE} = 15$ V, $I_C = 75$ A, Room temperature						
Clamping?	R_G [Ω]	t_{rise} [ns]	E_{on} [mJ]	I_{RRM} [A]	t_{fall} [ns]	E_{off} [mJ]
No	6.4	60	22.9	132	248	14.2
Yes	6.4	68	25.2	121	249	14.1
Yes	3.3	61	23	122	248	14.1

A comparison of the SC energy for this laboratory experimental setup does not make much sense. Because the top-side axillary switch, which triggers the SC event, needs to turn ON at this moment, the high dc-link voltage cannot be directly applied to the DUT.

C. Switching Behavior With and Without Clamping Circuit

During regular switching, the IGBT is also subjected by a positive di_C/dt, which is controlled by the dc-link voltage, parasitic inductance in the commutation loop, and the gate resistance. The influence of the presented clamping circuit on the normal switching performance was investigated using the double-pulse test configuration. The turn-ON behavior is shown in Fig. 12, the test results are summarized in Table I. The test conditions were taken from the datasheet; the definitions of the switching parameters are according to [27].

As can be seen in Table I, the clamping circuit slows down the current increasing phase, and produces about 10% more turn-ON loss, even though the reverse-recovery current peak of the diode was decreased by 9.1%. This is due to the induced voltage of the emitter stray inductance L_E during the current rise time, which causes a current flow into the GDU and thereby affects the charging speed for the gate capacitance. This effect can be

compensated to some extent by reducing $R_{G,\mathrm{on}}$ (see Table I). Nevertheless, no influence on turn-OFF behavior was observed. It was also found that the gate resistance does not affect the turn-OFF characteristics, which are intrinsically determined by the IGBT itself [28].

Due to the faster switching transients, the displacement current through the Miller capacitance is stronger owing to the steeper dv/dt. This negative feedback of the Miller capacitance is determined by the voltage dependent Miller capacitance C_{GC} and both voltage slopes dv_{CE}/dt and dv_{GE}/dt, which often makes this feedback highly frequent and a root cause for gate voltage instability. The negative feedback of the collector current slope di_C/dt through the common-source inductance is typically less frequent compared to the feedback of the Miller effect and therefore, leads to rather higher switching losses than to gate oscillation effects. A detailed analysis of the stability in different operation points has to be carried out. However, the impedance of the driver output should be adjusted well to work properly together with the semiconductor over a wide frequency range. A minimized impedance of the driver output and interface allows the driver to compensate the semiconductor feedbacks faster and allows faster switching operations. Damping the resonant circuits of the driver output and the semiconductor parasitic capacitances and inductances with higher ohmic resistors or putting the resonant circuit out of tune by adding additional capacitors, e.g., as external C_{GE}, would slow down the switching slope and therefore, minimize the impact of the displacement feedbacks by the cost of higher switching losses [29]. A crucial design criterion is the inductance L_{G} of the driver output stage and of the whole gate signal interface down to the chip level, since it is a dominating part of the impedance, which can be minimized by an optimized circuit and interface design. The small signal impedance of the power semiconductor device can be experimentally determined according to [24].

V. SC Type II and Type III Detection

Although the clamping circuit described above can enhance the SC type II and III capability of IGBTs, rapid SC detection and shutdown are still beneficial. In this section, a new fast SC detection method, which can detect and turn OFF the SC event within 400 ns, based on the above-mentioned clamping circuit, is introduced and tested.

Fig. 13 shows the schematic of the SC detection circuit. In SC type II or type III with the clamping circuit, the induced voltage on the common-source inductance L_{CS} and emitter stray inductance L_{E} can be used to pull down the gate voltage. This unusual gate voltage drop during ON-state can be identified as an SC event. This circuit can respond very fast on the inductive voltage drop caused by the collector current slope di_C/dt.

The divided gate voltage $V_{\mathrm{GE},(d)}$ is compared with a reference voltage V_{Ref}. If $V_{\mathrm{GE},(d)}$ is smaller than V_{Ref} during ON-state, an SC is detected and the failure state is saved by the RS flip-flop. The failure signal is send via optical isolator to the logic side whereby the GDU shuts down the DUT. The truth table of the GDU detection circuit is shown in Table II.

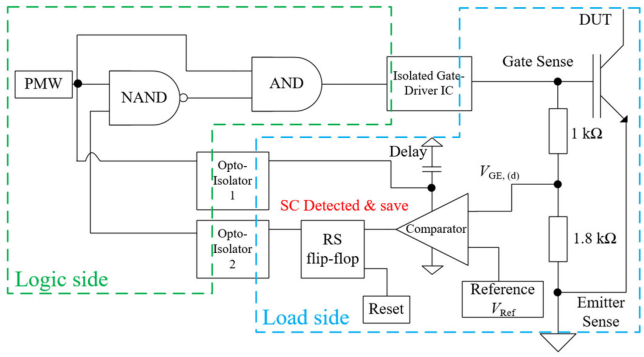

Fig. 13. Schematic of the SC type II and III detection circuit.

TABLE II
Truth Table of GDU and Detection Circuit

NAND	AND	Status
0	0	turn-off
0	1	turn-on
1	0	turn-off
1	1	short circuit

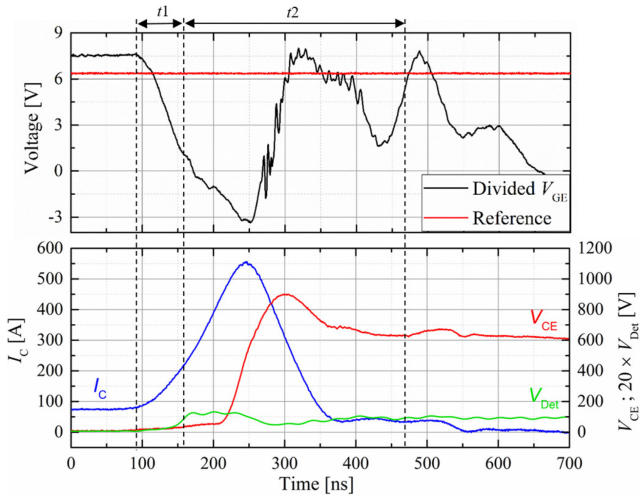

Fig. 14. SC type II with detection: $V_{\mathrm{CE}} = 600$ V, $V_{\mathrm{GE}} = 12$ V, $R_{G,\mathrm{on}} = 6.4\ \Omega$, $R_{G,\mathrm{off}} = 98\ \Omega$, $R_1 = 0\ \Omega$.

During a normal turn-ON progress, the gate voltage rises from 0 V or negative to a positive steady state. As the gate voltage increases, it is lower than the reference voltage, resulting in a malfunction of the detection circuit. Accordingly, a delay is necessary. However, this delay time does not influence the speed of the detection circuit. In the present case, the delay time is set by controlling the power supply of the comparator. When the pulsewidth modulated (PWM) signal is set high, the output of the optical isolator 1 is also set high and therefore, charges the comparator power supply which then starts to monitor the divided gate voltage.

As an example, an SC type II test is shown in Fig. 14. The ratio of the gate voltage divider was set to 1:1.8; the reference voltage is set to 6.9 V. The reference point for measurement

is Ref 2 (see Fig. 1), since this is the reference point for the comparator as well. At about $t = 90$ ns, the SC takes place; the divided gate voltage drops below the reference voltage at about 120 ns. The time interval $t1$ is the detection time, which consists of the propagation delay of the comparator and RS flip-flop.

At the beginning of time interval $t2$, the output of the flip-flop goes high (5 V, V_{Det}). This logic signal is transmitted to the logic side of the driver via optical isolator, thereby turning OFF the gate signal. Approximately at 470 ns, the SC is turned OFF by the gate driver, $t2$ is determined by the propagation delay of the optical isolator 2, the logic gate (NAND and AND), and the gate driver IC. The total reaction time ($t1 + t2$) of the detection circuit is around 380 ns under the given test conditions.

With an optimized reference voltage level and optimization of the logic circuit, the total reaction time can be reduced further more. Another possibility is shorting the gate and emitter by a MOSFET after detecting an SC [15], thereby saving the operating time of the logic circuit ($t2$). However, using this method requires considering the effect of the additional MOSFET on the regular switching, because the junction capacitance of the transistor needs to be charged and discharged during switching as well.

This detection method uses the negative feedback caused by rapid current change during the onset of an SC event. Theoretically, if an SC type II or III takes place, the collector current slope depends on the bus voltage and the parasitic inductance in the SC loop. For specific high-inductive SCs, this method may not be utilized for SC detection. However, this method can adapt the smallest detectable current change by adjusting the reference voltage. Under the above-mentioned experimental conditions, the minimum monitoring current change rate of the proposed method is 1.3 kA/μs. The limitation of this method is that the emitter stray inductance L_{E} must be bigger than the common-source inductance L_{CS}. Otherwise, although the self-clamping effect of the gate voltage still exists, the comparator is not able to detect the gate voltage drop. Instead, a voltage overshoot caused by L_{CS} (see Fig. 6) will be detected. In this case, the level of the reference voltage has to be adjusted to a higher level to identify the SC by monitoring the gate voltage overshoot.

For high-noise operating environments, the immunity of the presented SC detection circuit can be improved by, e.g., integrating the V_{CE} desaturation monitoring.

VI. Conclusion

In this article, the influence of the GDU and the common-source inductance on the SC type II and III were comprehensively investigated. The gate turn ON resistance, internal gate resistor, as well as the topology of the gate driver output can significantly affect the SC characteristics of the device. The gate voltage self-clamping effect due to the common-source inductance during SC II and III was found and verified with measurement and circuit simulations. The measurement reference points should be well defined during the test to avoid significant measurement errors.

A clamping circuit with passive components was introduced. The IGBT is capable of limiting the gate voltage independent of the GDU output stage topology during the SC. The maximum collector current during SC II and III could be decreased successfully by using the presented clamping circuit. The influence of the switching behavior can be compensated to some extent by reducing the gate resistor. Based on the clamping circuit, a new fast SC type II and III detection method was developed and tested, which can turn OFF an SC within 400 ns.

Future work should focus on eliminating the impact of the clamping circuit on the turn-ON process. Moreover, investigations of the implementation of a circuit to improve the SC capability of SiC power MOSFET should be carried out. Compared with silicon IGBTs of the same voltage and current level, due to the smaller chip size and sensitive gate structure, the SC condition is more stressful for SiC power MOSFETs. Suppressing SC current can considerably improve the device's robustness.

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References

[1] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices: Physics, Characteristics, Reliability*, 2nd ed. Berlin, Germany: Springer-Verlag, 2017.

[2] H. G. Eckel and L. Sack, "Experimental investigation on the behavior of IGBT at short-circuit during the on-state," in *Proc. 20th Annu. Conf. IEEE Ind. Electron.*, 1994, vol. 1, pp. 118–123.

[3] J. Lutz, R. Dobler, J. Mari, and M. Menzel, "Short-circuit III in high power IGBTs," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–8.

[4] J. Lutz and T. Basler, "Short-circuit ruggedness of high-voltage IGBTs," in *Proc. 28th Int. Conf. Microelectron.*, 2012, pp. 243–250.

[5] J. Fuhrmann, S. Klauke, and H. G. Eckel, "IGBT and diode behavior during short-circuit type 3," *IEEE Trans. Electron. Devices*, vol. 62, pp. 3786–3791, Nov. 2015.

[6] J. Fuhrmann and H. G. Eckel, "Interaction between IGBT, diode and parasitic inductances during short-circuit type 3," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–8.

[7] J. Fuhrmann and H.-G. Eckel, "Dynamic avalanche in high voltage diodes during short circuit III," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Nuremberg, Germany, 2015, pp. 891–898.

[8] I. Omura, W. Fichtner, and H. Ohashi, "Oscillation effects in IGBT's related to negative capacitance phenomena," *IEEE Trans. Electron. Devices*, vol. 46, no. 1, pp. 237–244, Jan. 1999.

[9] P. Münster, D. Lexow, and H. G. Eckel, "Effect of self turn-on during turn-on of HV-IGBTs," in *Proc. Conf. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2016, pp. 924–931.

[10] P. Münster *et al.*, "Voltage dependence of HV IGBT turn on caused by self turn on," in *Proc. 14th Int. Seminar Power Semicond.*, 2018, pp. 173–178.

[11] T. Rogne, N. A. S. Lefebvre, Z. Khatir, and F. Saint-Eve, "Experimental behavior of single-chip IGBT and COOLMOS devices under repetitive short-circuit conditions," *IEEE Trans. Electron. Devices*, vol. 52, no. 2, pp. 276–283, Feb. 2005.

[12] M. Otsuki, Y. Onozawa, H. Kanemaru, Y. Seki, and T. Matsumoto, "A study on the short-circuit capability of field-stop IGBTs," *IEEE Trans. Electron. Devices*, vol. 50, no. 6, pp. 1525–1531, Jun. 2003.

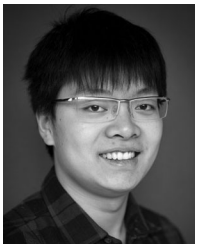
[13] V. John, B. Suh, and T. A. Lipo, "Fast-clamped short-circuit protection of IGBTs," *IEEE Trans. Ind. Appl.*, vol. 35, no. 2, pp. 477–486, Mar./Apr. 1999.

[14] M. Chen, D. Xu, X. Zhang, N. Zhu, J. Wu, and K. Rajashekara, "An improved IGBT short-circuit protection method with self-adaptive blanking circuit based on VCE measurement," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6126–6136, Jul. 2018.

[15] S. Hain and M.-M. Bakran, "New ultra fast short circuit detection method without using the desaturation process of the power semiconductor," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Nuremberg, Germany, 2016, pp. 10–12.

[16] Jan Fuhrmann1 *et al.*, "Enhancing short-circuit capability of high-performance IGBTs by gate-drive unit," in *Proc. Conf. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Nuremberg, Germany, 2019, pp. 515–521.

[17] S. Mocevic *et al.*, "Phase current sensor and short-circuit detection based on rogowski coils integrated on gate driver for 1.2 kV SiC MOSFET half-bridge module," in *Proc. Int. Conf. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 393–400.
[18] R. Baburske *et al.*, "Comparison of critical current filaments in IGBT short circuit and during diode turn-off," in *Proc. 26th Int. Symp. Power Semicond. Devices*, Jun. 2014, pp. 47–50.
[19] R. Baburske *et al.*, "Low-inductive power systems to overcome shortcircuit ruggedness limits," in *Proc. 28th Int. Symp. Power Semicond. Devices*, Jun. 2016, pp. 323–326.
[20] M. Hierholzer, R. Bayerer, A. Porst, and H. Brunner, "Improved characteristics of 3.3kV IGBT modules," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 1997, pp. 201–204.
[21] A. Volke and M. Hornkamp, *IGBT Modules: Technologies, Driver and Application*, 2nd ed. Nuremberg, Germany: Infineon, 2012.
[22] "*FS75R17KE3 IGBT Module Datasheet*," Infineon Technol., Neubiberg, Germany, 2013.
[23] T. Basler, J. Lutz, T. Brückner, and R. Jakob, "IGBT self-turn-off under short-circuit condition," in *Proc. 10th Int. Seminar Power Semicond.*, 2010.
[24] C. Abbate, G. Busatto, A. Sanseverino, F. Velardi, S. Iavarone, and C. Ronsisvalle, "Measurement of IGBT high frequency input impedance in short circuit," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 584–592, Jan. 2017.
[25] T. Funaki, N. Phankong, T. Kimoto, and T. Hikihara, "Measuring terminal capacitance and its voltage dependency for high-voltage power devices," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1486–1493, Jun. 2009.
[26] X. Liu, J. Kowalsky, and J. Lutz, "A clamping circuit for short circuit ruggedness improvement of discrete IGBT devices based on the di/dt Feedback of emitter stray inductance," in *Proc. Int. Symp. Power Electron.*, 2019, pp. 1–6.
[27] *Semiconductor Devices—Part 9: Discrete Devices—IGBTs*, IEC 60747-9:2019, International Electrotechnical Commission, Geneva, Switzerland, 2007.
[28] M. Bohlländer, R. Bayerer, J. Lutz, and T. Raker, "Desaturated switching of trench—Fieldstop IGBTs," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2006.
[29] S. Schuler, "Schwingverhalten von treiber und modul vermeiden," *Elektronpraxis Leistungselektronik Stromversorgung*, pp. 30–33, May 2013.



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