The Current Shaping Modular Multilevel DC–DC Converter

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***Abstract*—The recently proposed modular multilevel dc–dc converter (M2DC) and the HVDC-dc auto transformer (HVDC-AT) enable direct power transfer between dc networks at low-to-moderate step ratios using only a single power electronic conversion stage. In both converter structures, an internal circulating sinusoidal ac current is established to balance the energy within the converter. In practice, however, the frequency of the circulating ac current is limited to a few hundred Hz, requiring significant ripple power to be filtered by large voltage submodule (VSM) capacitors. In this article, a novel energy transfer mechanism for interfacing dc networks is introduced wherein the frequency of the ac currents can be increased by one to two orders of magnitude, thus enabling a commensurate reduction in VSM capacitor size and cost. This is achieved by eliminating the ac chokes within the modular converter structure. Instead, a current source submodule (CSM) is employed to shape the circulating current, leading to a current of nearly square-wave shape with a frequency in the kHz range equal to the switching frequency of the CSM. This article describes one particular topology based on this current shaping mechanism, namely a high step down ratio dc–dc converter. The viability of the mechanism is demonstrated via simulation and experimental results from a laboratory scale implementation.**

***Index Terms*—Current source converter, dc–dc power converters, hybrid converters, multilevel converters, voltage source converter.**

I. Introduction

As SOCIETY becomes further electrified, energy efficiency, reliability as well as the integration of distributed resources will become increasingly important considerations in the design of electrical distribution grids [2]. Compared to ac distribution, dc distribution is particularly advantageous with respect to these considerations given the lower number of power conversion stages required when generators and loads are predominantly dc-based [3]. In order to realize a future of interconnected dc grids, power converter topologies that enable dc grids to exchange power at differing voltage levels are required. In evaluating converter topologies for distribution grid applications, cost is an especially important driver given the relative cost effectiveness of the competing ac transformer for transforming voltages [4]. Of particular relevance to this article are power converter topologies for interfacing high-voltage or medium-voltage dc (HVDC or MVDC) and low-voltage dc (LVDC) networks.

Many converter topologies have been proposed, which can be considered for interfacing a higher-voltage and a lower-voltage dc network, including [4]–[8]. The topologies with galvanic isolation are commonly referred to as solid-state transformers (SSTs) or power electronic transformers. These converters are based on the dual-active bridge (DAB) topology proposed in [9], which features two ac–dc conversion stages coupled through a medium-frequency transformer.

Two SST topologies that are scalable to higher voltages are identified in [10] as the modular multilevel converter structure (MMC) [11]–[13] and the input-series output-parallel structure (ISOP) [4], [14], [15]. In the papers of [11]–[13], the MMC structure of [16] has been considered for the ac–dc conversion stage of the DAB. However, other MMC structures could also have been considered for the ac–dc conversion stage, including [17]–[21]. While both the MMC and the ISOP structures are interesting approaches, power is processed sequentially through two power electronic stages and one magnetic stage, hence the magnetics of the converter must be rated for the full power.

Resonant dc–dc converter structures operating at medium-frequencies have also been proposed for high step down applications including, [22] and [23]. However, compared to hard-switched converters, resonant converters can be subjected to higher peak voltage and/or current stresses that make it difficult to scale these structures for higher power applications.

Addressing the aforementioned drawbacks, two converter structures with a single conversion stage for dc–dc applications have been proposed in literature based on novel energy transfer mechanisms, namely the HVDC-dc autotransformer (HVDC-AT) [24] and the modular multilevel dc–dc converter (M2DC) [25], [26]. The two structures are shown in Fig. 1.

The HVDC-AT and M2DC topologies each feature multiple strings, each string being made up of four arms. Each arm consists of multiple cascaded voltage source submodules (VSMs) and an ac choke. As noted in [27], both approaches offer improved utilization of the power electronics and reduced losses relative to the MMC structure of [11]. However, this advantage reduces for high step ratio applications, as shown in [27], thus these topologies are best suited for low-to-moderate step ratio

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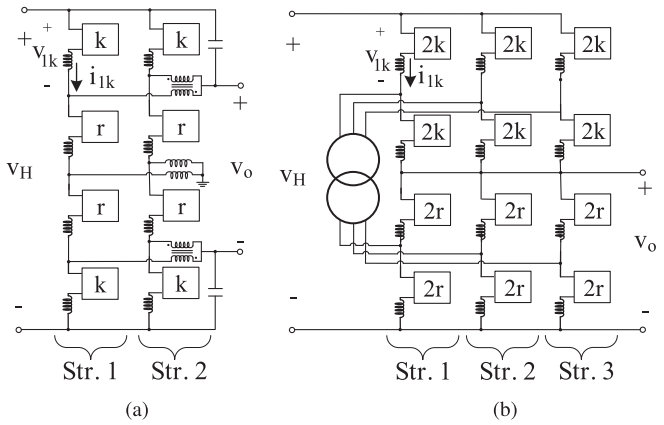


Fig. 1. Single-stage dc–dc converters. (a) M2DC [25]. (b) HVDC-AT [24].

TABLE I
HIGH-LEVEL TOPOLOGY COMPARISON

Parameter	M2DC	HVDC-AT	CS-MMC
Min. String Count	2	3	1
Total Blocking Voltage per String	$\approx 2V_{\mathrm{H}}$	$\approx V_{\mathrm{H}}$	$\approx V_{\mathrm{H}}$
Circulating AC Current Freq., f_{ac}	$\approx$ $60-400$Hz	$\approx$ $60-400$Hz	$\approx$ $5-40$kHz
VSM Capacitor Ripple Freq.	$\approx f_{ac}$	$\approx f_{ac}$	$\approx f_{ac}/2$
Recommended Step Ratio Range	1:1 to 2:1 [28]	1:1 to 4:1 [24]	$>$ 4:1
Recommended Operating Power Range	$10-100$s of MW	$10-100$s of MW	$10-100s$ of kW
Function in a Future DC Grid	Primary Transmission Transformer (XFMR)	Primary Transmission XFMR	Secondary Distribution XFMR

applications. In both topologies, a circulating ac current is established to balance the energy within the converter. The frequency of the ac current is limited to a few hundred Hz due to the presence of the ac choke ac voltage drop as well as the magnetic losses of the coupled inductor [25] and also the transformer in [27].

In this article, a novel energy transfer mechanism for interfacing dc networks is introduced, termed the current shaping modular multilevel converter (CS-MMC). A high-level comparison of the three single-stage modular multilevel dc–dc converter structures is provided in Table I. The advantages of the CS-MMC structure include a significantly reduced VSM count and a one to two orders of magnitude increase in the ac circulating current frequency enabling a commensurate reduction in VSM capacitor size. Given that VSM capacitors consume a majority of VSM volume and represent a major portion of VSM cost, the resulting benefits are an improvement in power density and reduction of cost.

The advantages of the CS-MMC structure are a result of the novel energy transfer mechanism exploited, which uses a current source submodule (CSM) to shape the current within the converter structure. This shaped current is of near square-wave shape, medium frequency, and has a direction that is directly assignable by the control of the converter. This article presents only one topology that demonstrates this energy transfer mechanism, for high step ratio dc–dc conversion applications.

Note, Gray and Lehn [1] provided preliminary insights into the operational concepts of the CS-MMC. In this article, the control and dynamic operation of the CS-MMC are examined.

This article is structured by first introducing the underlying energy transfer mechanism of the CS-MMC. Next, one CS-MMC topology for high step ratio dc–dc conversion applications is presented. This is followed by an overview of the main operating principles of this CS-MMC topology along with a detailed circuit analysis and control design. Finally, simulation and experimental results from a laboratory scale converter system are presented, which demonstrate the viability of the mechanism.

II. ENERGY TRANSFER MECHANISM

Fig. 2(a) presents a circuit diagram of an arm of the HVDC-AT and M2DC topologies. The arm features multiple cascaded VSMs and a series choke. A representative waveform for the arm current, $i_{1\mathrm{k}}$, is also provided in Fig. 2(a). The arm current waveform is a superposition of a dc and an ac current component. The ac current component is typically of sinusoidal waveshape at a select frequency, f_{ac}.

The VSM string is charged when $i_{1\mathrm{k}}$ is positive and discharged when $i_{1\mathrm{k}}$ is negative. These intervals are termed the charge and discharge intervals in this article. It can be observed that the waveform of the string current is not symmetrical about zero leading to a constrained discharge interval duration. The amplitude of the string current is also greater in the charge interval than in the discharge interval due to the dc-offset. The relative duration of the charge and discharge intervals depends on the management of the inductor current trajectory, typically via current control.

The energy transfer mechanism, exploited by the topology of this article, is presented in Fig. 2(b). The mechanism features a string of cascaded VSMs and a CSM. Note, R_L of the CSM represents the load. In the energy transfer mechanism, the CSM defines the shape of the string current. Depending on the states of the CSM switches, the inductor current, i_{L}, is either directed toward the positive or negative terminal of the string. For instance, when switches 1 and 2 conduct, i_{L} is directed toward the negative terminal of the string, i.e., $i_{\mathrm{H}} = i_{\mathrm{L}}$; and conversely, when switches 3 and 4 conduct, i_{L} is directed toward the positive terminal of the string, i.e., $i_{\mathrm{H}} = -i_{\mathrm{L}}$.

The resultant i_{H} waveform has a near square-wave shape with an amplitude equal to i_{L}, in both the charge and discharge intervals. A dc bias in i_{H} is achieved simply by adjusting the ratio of charge and discharge interval durations. In contrast to Fig. 2(a), the duration of the charge and discharge intervals is

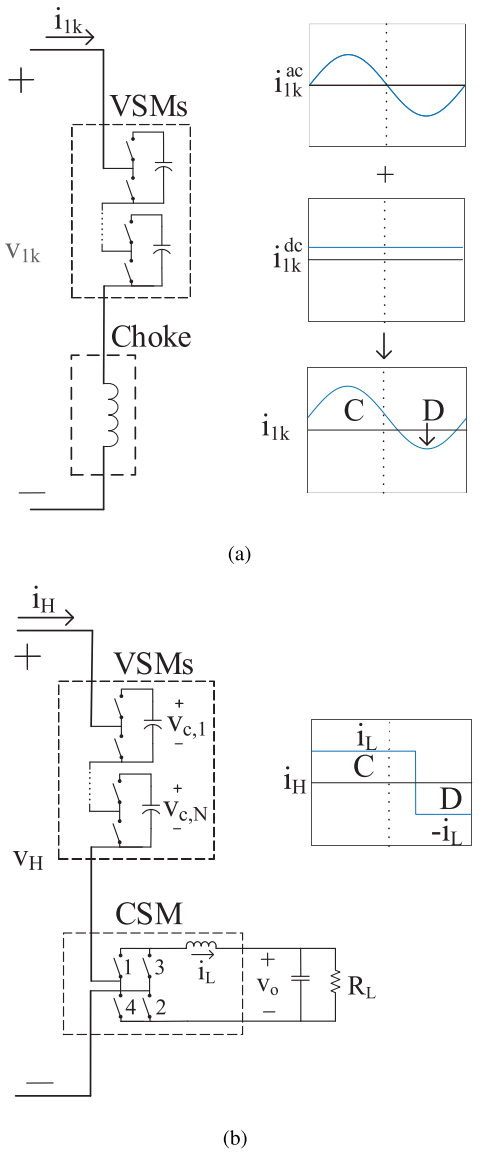


Fig. 2. Conventional and proposed energy transfer mechanisms. (a) One Arm of M2DC and HVDC-AT. (b) CS-MMC.

now directly assigned by the control signals in the proposed mechanism.

The current-shaping feature that is performed by the CSM endows the proposed converter with unique properties. The primary benefit is the ability to reverse the polarity of the string current at high frequency. With this ability, the total energy in the VSM string remains balanced after each CSM switching period enabling a significant reduction in the required VSM capacitor size. In the prior art, such as the HVDC-AT and M2DC, the string current is instead shaped by applying sinusoidal voltage waveforms of hundreds of Hz. This frequency is limited due to the ac voltage drop of the arm ac chokes, which are generally sized in the range of 0.05–0.15 pu for MMCs [29] to limit circulating currents and fault events. In the proposed converter, there is no ac choke in the string, enabling the string current to be of near square-wave shape at the switching frequency of the CSM, which can be in the approximate range of 5–40 kHz (the

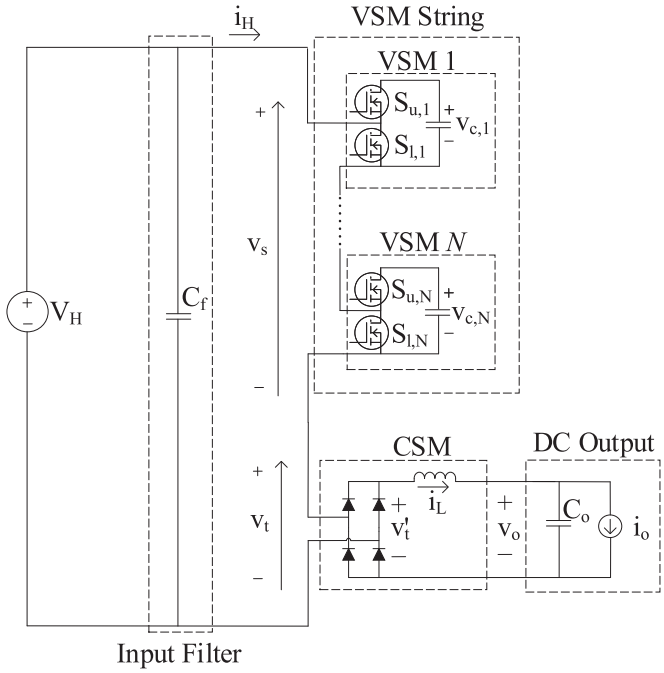


Fig. 3. Proposed CS-MMC topology.

switching frequency range being limited by device switching loss). Accordingly, this property enables the CS-MMC topology to achieve a commensurate reduction in the size and cost of the VSM capacitors compared to the HVDC-AT and M2DC topologies. This also leads to physically smaller VSM size and, thus, higher converter power density.

It should be highlighted that in this mechanism, the near square-wave string current is delivered to the input dc terminals. The delivered current features ac current components at multiples of f_{ac}, which can be significant relative to the dc current component, as can be visually observed in Fig. 2(b). In practice, an input dc-link filter capacitor would need to be included to attenuate these high-frequency harmonics, as shown in Fig. 3.

The next section of this article introduces the proposed converter topology that employs the energy transfer mechanism of Fig. 2(b).

III. Topology Description

One realization of the CS-MMC topology is presented in Fig. 3. The mixed-type string of cascaded VSMs and a CSM is connected across the terminals of the dc input source, denoted V_{H}. The dc output, with a voltage denoted v_{o}, is connected across the dc-side terminals of the CSM. The VSMs are required to insert only positive voltages and, therefore, conventional half-bridge type submodules have been employed. In this topology, the power inductor is separated from the string of series-connected VSMs by the CSM. The CSM consists of a full-bridge rectifier with an inductor. The dc load is represented by a current source, i_{o}, in Fig. 3. The CSM inductor, L, and the dc output capacitor, C_{o}, forms an *LC* filter, which attenuates the VSM capacitor switching ripple from the output voltage, v_o.

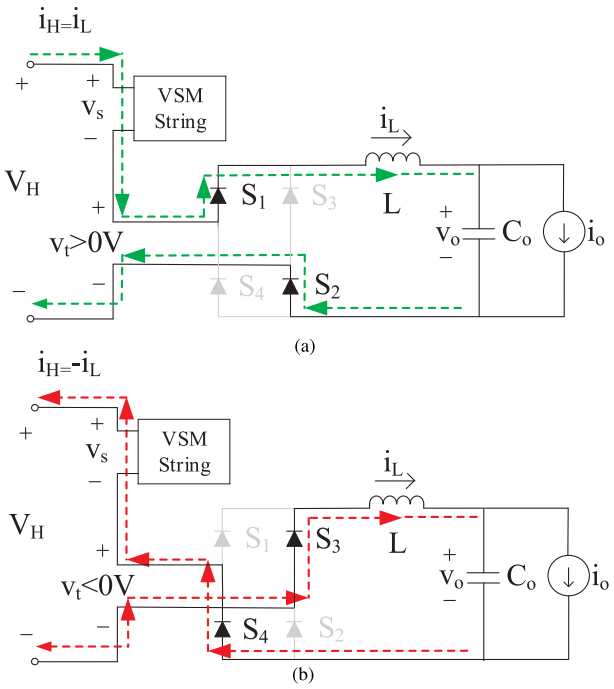


Fig. 4. Charge and discharge operating modes. (a) VSM charge mode: $v_t > 0$ and $i_H = i_L$. (b) VSM discharge mode: $v_t < 0$ and $i_H = -i_L$.

Since a passive rectifier is used here as the CSM, converter operation is dictated by the VSM capacitor voltages and gating signals. The CSM is accordingly not controlled in this topology and it is instead control of the VSM string that determines, which CSM diodes conduct. VSM string operation imposes a voltage v_t on the CSM rectifier, which, in turn, commutates the rectifier and changes the polarity of the string current.

A. Operating Principles

Referring to Fig. 3, the voltage across the ac-side terminals of the CSM, v_t, can be expressed as follows:

$$v_t(t) = V_H - v_s(t) \tag{1}$$

where $v_s(t)$ is the net voltage of the VSM string and is equal to the following:

$$v_s(t) = \sum_{k=1}^{N} v_{c,k}(t) n_k(t) \tag{2}$$

where N is the total number of VSMs in the string; $v_{c,k}$ is the cell capacitor voltage associated with VSM cell k; n_k is the insertion index of VSM cell k, which is equal to 0 if the VSM cell is bypassed and 1 if inserted. Referring to Fig. 3, VSM cell 1 is inserted when $S_{u,1} = 1$ and $S_{l,1} = 0$. Conversely, VSM cell 1 is bypassed when $S_{u,1} = 0$ and $S_{l,1} = 1$.

By varying the number of inserted VSMs, the voltage across the ac-side terminals of the CSM can be modified, as per (1).

Fig. 4 presents the two operating modes of the converter: VSM charge and VSM discharge mode. The operating modes are set by the polarity of v_t. Referring to Fig. 3, the instantaneous power delivered to the CSM, denoted p_t, and to the VSM string, denoted p_s, can be expressed as follows:

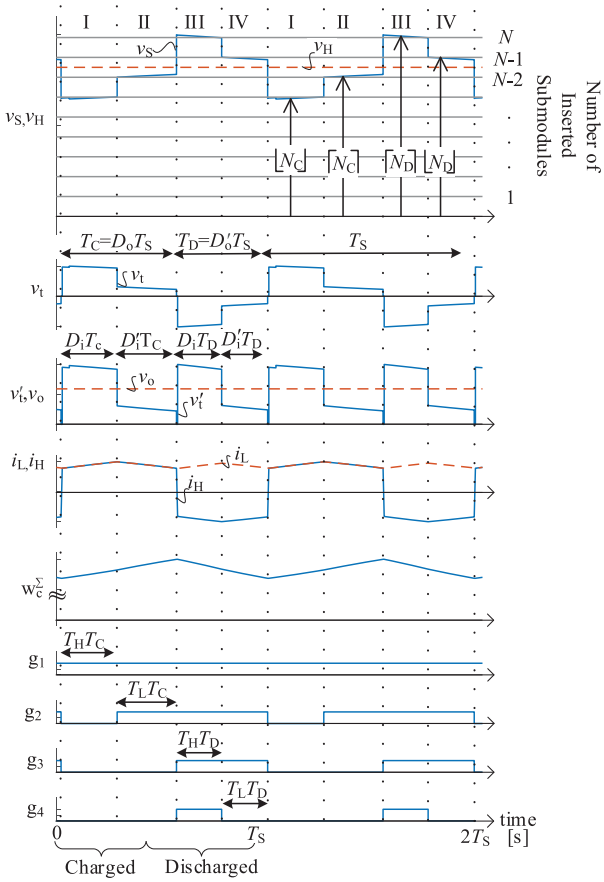


Fig. 5. Representative operating waveforms.

$$p_t(t) = v_t(t) i_H(t) \tag{3a}$$

$$p_s(t) = v_s(t) i_H(t) \tag{3b}$$

where $i_H(t)$ is the string current.

As can be observed in Fig. 4, when $v_t > 0$, the diodes S_1 and S_2 are forward-biased leading to a string current, $i_H = i_L$. Conversely, when $v_t < 0$, diodes S_3 and S_4 are forward-biased leading to a string current, $i_H = -i_L$. Therefore, when $v_t > 0$, the dc input source delivers power to both the VSM string and to the CSM; and when $v_t < 0$, the VSM string delivers power to the dc input source and to the CSM. Power is, therefore, delivered to the CSM irrespective of the direction of i_H. Accordingly, (3a) can be alternately expressed as follows:

$$p_t(t) = |v_t(t)| i_L(t). \tag{4}$$

An equivalent representation of (4) is the following:

$$p_t(t) = v'_t(t) i_L(t) \tag{5}$$

where v'_t, labeled in Fig. 3, is the rectified voltage appearing at the output of the CSM full-bridge rectifier.

Representative operating waveforms of the converter are provided in Fig. 5. There are four distinct intervals in each switching period, which are labeled in Fig. 5 as intervals I, II, III, and IV. In order to realize the 4-level waveform of v_s, four unique gating signals are generated. The gating signals are presented in Fig. 5 as g_1, g_2, g_3, and g_4. Each gating signal corresponds to one of the

four intervals, i.e., g_1 corresponds to interval I. These signals are distributed to the N VSM cells according to a sorting algorithm described in Section III-E. The functionality of the four intervals can be summarized as follows:

1) Interval I: Charge mode at high v_t';
2) Interval II: Charge mode at low v_t';
3) Interval III: Discharge mode at high v_t';
4) Interval IV: Discharge mode at low v_t'.

Intervals I and II correspond to the VSM charge mode of Fig. 4(a); and Intervals III and IV correspond to the VSM discharge mode of Fig. 4(b). As can be observed in Fig. 5, $i_H = i_L$ during charge mode; and $i_H = -i_L$ during discharge mode. In Intervals I and III, v_t' is of a high voltage level; and conversely, in intervals II and IV, v_t', is of a low voltage level.

B. Regulating the Energy of the VSM String

By varying the relative duration of the charge and discharge modes, the VSM string energy, W_c^{Σ}, can be controlled. The relative duration between the VSM charge and discharge modes is represented with an assignable duty ratio, D_o, termed the outer duty ratio. The total duration of the charge and discharge intervals (denoted T_C and T_D, respectively) can be expressed as follows:

$$T_C = D_o T_s \tag{6a}$$

$$T_D = D_o' T_s \tag{6b}$$

where $D_o \in [0.5, 1]$ is a duty ratio term; and T_s is the switching period.

The waveform of the total instantaneous energy in the VSM string, $W_c^{\Sigma}(t)$, is also included in Fig. 5. As can be observed, the VSM string energy increases during VSM charge mode and decreases during VSM discharge mode. The VSM string energy is calculated by the following expression:

$$W_c^{\Sigma}(t) = \frac{C}{2}\sum_{k=1}^{N} v_{c,k}^2(t) \tag{7}$$

where C is the capacitance of a VSM cell capacitor.

The net voltage of the VSM string, v_s, is a 4-level waveform as can be observed in Fig. 5. Of the four voltage levels, two correspond to $v_s \geq V_H$ and the other two to $v_s \leq V_H$.

The number of inserted VSM cells corresponding to intervals I, II, III, and IV is as follows:

1) Interval I: $N_1 = \lfloor N_C \rfloor$;
2) Interval II: $N_2 = \lceil N_C \rceil$;
3) Interval III: $N_3 = \lceil N_D \rceil$;
4) Interval IV: $N_4 = \lfloor N_D \rfloor$;

where $\lfloor \cdot \rfloor$ represents the floor function; and $\lceil \cdot \rceil$ represents the ceiling function; and N_C and N_D represent the average number of VSM cells inserted during the charge and discharge operating modes, respectively. They are defined as follows:

$$N_C = \frac{1}{D_o T_s}\int_{t=0}^{D_o T_s}\sum_{k=1}^{N} n_k(t)dt \tag{8a}$$

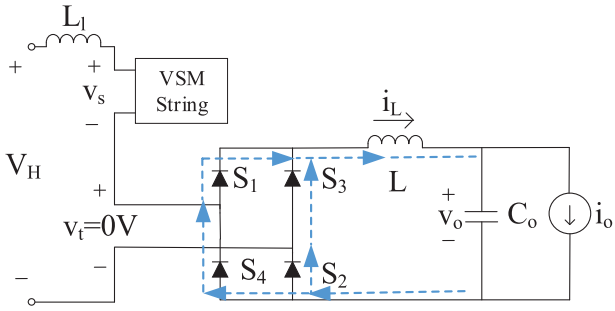


Fig. 6. Circuit operation during commutation intervals.

$$N_D = \frac{1}{D_o' T_s}\int_{t=D_o T_s}^{T_s}\sum_{k=1}^{N} n_k(t)dt. \tag{8b}$$

It can be shown that the following are the averaged expressions for N_C and N_D

$$N_C = \frac{V_H - V_o}{V_c} \tag{9a}$$

$$N_D = \frac{V_H + V_o}{V_c} \tag{9b}$$

where V_o is the average output voltage; and V_c is the nominal VSM cell capacitor voltage.

An important observation can be made by comparing the expressions of N_C and N_D in (9): the average number of cells inserted during the charge and discharge operating modes is not equal, i.e., $N_C < N_D$. In addition, as noted earlier and observed in Fig. 4, the magnitude of the string current is equal to the inductor current, i_L, in both the VSM charge and discharge modes, i.e., $|i_H(t)| = i_L(t)$. Therefore, to ensure that the VSM string energy is balanced over a full switching period, the relative duration of the charge and discharge modes is made unequal, i.e., $T_C \geq T_D$. Referring to (6), this implies that the duty ratio term, $D_o \geq 0.5$.

It is instructive here to derive an expression for the total number of VSM cells in the string, N. It can be observed in Fig. 5, that the maximum number of inserted VSM cells occurs in Interval III and is equal to $\lceil N_D \rceil$ cells. Accordingly, an expression for the total number of VSM cells in the string can be derived from (9b), resulting in the following:

$$N = \left\lceil \frac{V_H + V_o}{V_c} \right\rceil. \tag{10}$$

C. Commutation Interval

When transitioning between VSM charge and discharge operating modes, a natural commutation interval occurs. During this commutation interval, the ac-side and dc-side of the CSM are decoupled. The circuit operation during this commutation interval is presented in Fig. 6. The loops formed on either side of the full-bridge rectifier are defined as the ac-side and dc-side loop. This decoupling is highly advantageous as commutation of the string current occurs at a *di/dt* rate limited only by the leakage inductance of the ac-side loop, L_l. As a result, commutation occurs within a fraction of a switching period and the string

current, i_{H}, is of nearly square-wave shape, as can be observed in Fig. 5. Over the commutation interval, the change in the string current is equal to $2i_{\mathrm{L}}$, i.e., $\Delta i_{\mathrm{H}} = 2i_{\mathrm{L}}$.

D. Regulating the Output Voltage

It is by synthesizing two voltage levels on either side of V_{H} that the VSM string regulates the output voltage, v_{o}. As can be observed in Fig. 5, the voltage across the ac-side terminals of the CSM, v_{t}, is reflected as a positive voltage, v'_{t}, in both VSM charge and VSM discharge modes. During Interval I and Interval III, this reflected voltage is equal and corresponds to a high v'_{t} denoted $v'_{\mathrm{t,H}}$. During Interval II and Interval IV, the reflected voltage is equal and corresponds to a low v'_{t} denoted $v'_{\mathrm{t,L}}$. The high and low v'_{t} values can be expressed as follows:

$$v'_{\mathrm{t,L}} = V_{\mathrm{H}} - \frac{\lceil N_{\mathrm{C}} \rceil}{N} v_{\mathrm{c}}^{\Sigma} \tag{11a}$$

$$v'_{\mathrm{t,H}} = V_{\mathrm{H}} - \frac{\lfloor N_{\mathrm{C}} \rfloor}{N} v_{\mathrm{c}}^{\Sigma} \tag{11b}$$

$$\equiv V_{\mathrm{H}} - \frac{\lceil N_{\mathrm{C}} \rceil - 1}{N} v_{\mathrm{c}}^{\Sigma} \tag{11c}$$

where v_{c}^{Σ} represents the total sum of the VSM cell capacitor voltages and is defined by the following expression:

$$v_{\mathrm{c}}^{\Sigma} = \sum_{k=1}^{N} v_{\mathrm{c,k}}. \tag{12}$$

Note the reflected voltages are equal in Intervals I and III and in Intervals II and IV due to the symmetry of the voltage levels of v_{s} on either side of V_{H}. While symmetrical voltage levels have been assumed to simplify the analysis in this article, asymmetrical voltage levels are also possible.

By varying the relative duration of the high and low v'_{t} voltage levels, an average output voltage V_{o} between the high and low v'_{t} values can be controlled for. Accordingly, this converter is able to achieve noninteger step voltage conversion ratios. The relative duration between the high and low v'_{t} voltage levels is represented with an assignable duty ratio D_{i}, termed the inner duty ratio. The total duration of the high and low v'_{t} voltage intervals (denoted T_{H} and T_{L}, respectively) can be expressed as follows:

$$T_{\mathrm{H}} = D_{\mathrm{i}} T_{\mathrm{s}} \tag{13a}$$

$$T_{\mathrm{L}} = D'_{\mathrm{i}} T_{\mathrm{s}}. \tag{13b}$$

Using both (6) and (13), the durations of each of the four intervals can be calculated. The durations of the four intervals are as follows:

$$T_1 = D_{\mathrm{o}} D_{\mathrm{i}} T_{\mathrm{s}} \tag{14a}$$

$$T_2 = D_{\mathrm{o}} D'_{\mathrm{i}} T_{\mathrm{s}} \tag{14b}$$

$$T_3 = D'_{\mathrm{o}} D_{\mathrm{i}} T_{\mathrm{s}} \tag{14c}$$

$$T_4 = D'_{\mathrm{o}} D'_{\mathrm{i}} T_{\mathrm{s}} \tag{14d}$$

where T_x is the duration of interval $x \in [1, 2, 3, 4]$.

Note that to regulate the output voltage as described in this section, a maximum bound on the dc input voltage, V_{H}, can be established for a given V_{c} and N as follows:

$$V_{\mathrm{H}} \leq N V_{\mathrm{c}} - V_{\mathrm{o}} \tag{15}$$

where NV_{c} is the maximum instantaneous voltage that the VSM string can insert (i.e., all N VSM cells are inserted).

E. Internal Balancing of VSM String

The four gating signals, g_1 to g_4, are distributed to the N VSM cells once per switching period according to the relative states of charge of the VSM cells. As an example, in Fig. 5, there are nine VSM cells; and g_1 is distributed to six of the VSM cells; and g_2, g_3, and g_4 are distributed to one VSM cell each. The distribution of the gating signals to the nine VSMs differs from one switching period to the next.

While the total VSM string energy is balanced over a switching period, the individual VSM cell voltages will not necessarily be balanced. However, over a sufficient number of switching periods, the VSM cells will become balanced as is illustrated in the simulation and experimental results presented later in this article.

F. Switching Frequency Considerations

To develop a deeper understanding of the operation of the converter during commutation intervals, it is instructive to derive a constraint equation for the maximum switching frequency of the converter.

Referring to Fig. 6, the following expression can be obtained for the net change in the string current, i_{H}, over a commutation interval

$$\Delta i_{\mathrm{H}} = \frac{1}{L_{\mathrm{l}}} \int_0^{T_{\mathrm{T}}} v_{\mathrm{l}}(t) dt \tag{16}$$

where T_{T} is the duration of the commutation interval, L_{l} is the leakage inductance of the ac-side loop, and v_{l} is the voltage across inductor L_{l}.

For each commutation interval, $\Delta I_{\mathrm{H}} = 2I_{\mathrm{L}}$ and $V_{\mathrm{l}} = V'_{\mathrm{t,H}}$. Therefore, (16) can be simplified and rearranged to solve for T_{T} as follows:

$$T_{\mathrm{T}} = \frac{2 I_{\mathrm{L}} L_{\mathrm{l}}}{V'_{\mathrm{t,H}}}. \tag{17}$$

Since there are two commutation intervals in each switching period, the following constraint can be imposed on the switching period, T_{s}

$$T_{\mathrm{s}} > 2T_{\mathrm{T}}. \tag{18}$$

A more restricted form of (18) can be expressed as follows:

$$T_{\mathrm{s}} > \frac{2T_{\mathrm{T}}}{T_{\mathrm{T\%}}} \tag{19}$$

where $T_{\mathrm{T\%}}$ represents the percentage of a switching period, which is a commutation interval. From a converter rating perspective, it is desired to minimize $T_{\mathrm{T\%}}$. Therefore, in practice, $T_{\mathrm{T\%}}$ is likely to be limited to a small value, such as $T_{\mathrm{T\%}} < 5\%$.

If (19) and (17) are combined, the following expression for the maximum switching frequency is derived:

$$f_{\mathrm{s}} < \frac{V'_{\mathrm{t,H}} T_{\mathrm{T\%}}}{4 I_{\mathrm{L}} L_{\mathrm{l}}} \tag{20}$$

where $f_{\mathrm{s}} = 1/T_{\mathrm{s}}$.

From (20), it can be observed that the limit for the maximum switching frequency of the converter can be increased by minimizing the leakage inductance term. Additionally, if typical values are plugged into (20), it can be shown that medium-switching frequencies are readily obtainable with this topology even though low voltages ($V'_{\mathrm{t,H}}$) are being applied across the leakage inductance during commutation intervals.

It should also be highlighted that f_{s} in (20) is the effective switching frequency of the converter. This switching frequency sets the frequency of the circulating ac current (i.e., f_{ac} in Table I is equal to f_s); however, the actual switching frequency of the VSM cells is lower, given that only a fraction of the VSM cells are being switched in each switching period.

The average number of VSM cells that are switched per switching period, N_{s}, is equal to the following:

$$N_{\mathrm{s}} = 1 + \lceil N_{\mathrm{D}} \rceil - \lceil N_{\mathrm{C}} \rceil \tag{21}$$

where, for example, if $N_{\mathrm{s}} = 6$, then there are on average six cell insertion and six cell bypass operations per switching period. Note, to create a four-level net VSM string voltage, it is required that $N_{\mathrm{s}} \geq 3$.

If the equations of (9) are substituted into (21), the following simplified expression results:

$$N_{\mathrm{s}} = 1 + \left\lceil \frac{V_{\mathrm{H}} + V_{\mathrm{o}}}{V_{\mathrm{c}}} \right\rceil - \left\lceil \frac{V_{\mathrm{H}} - V_{\mathrm{o}}}{V_{\mathrm{c}}} \right\rceil. \tag{22}$$

By employing (21), the average VSM cell switching frequency can be calculated as follows:

$$f_{\mathrm{s,cell}} = \frac{N_{\mathrm{s}}}{N} f_{\mathrm{s}}. \tag{23}$$

As an example, the cell switching frequency corresponding to Fig. 5 can be calculated to be $f_{s,\mathrm{cell}} = 3/9 f_{\mathrm{s}}$ by applying (23).

In the next section, the state-space model of the converter is derived along with expressions for the average inner and outer duty ratio terms, D_{i} and D_{o}, respectively.

IV. Circuit Analysis

A. Dynamic State Equations

The following state equations can be derived by applying Kirchoff's Voltage and Current Law to Fig. 3, where loss terms and leakage inductances have been neglected

$$C \frac{dv_{\mathrm{c,i}}}{dt} = (1 - 2g_3) i_{\mathrm{L}}(t) n_{\mathrm{i}}(t) \tag{24a}$$

$$L \frac{di_{\mathrm{L}}}{dt} = v'_{\mathrm{t}}(t) - v_{\mathrm{o}}(t) \tag{24b}$$

$$C_{\mathrm{o}} \frac{dv_{\mathrm{o}}}{dt} = i_{\mathrm{L}}(t) - \frac{v_{\mathrm{o}}(t)}{R} \qquad \forall i \in [1, N] \tag{24c}$$

where C_{o} is the output capacitor; R is the equivalent resistance of the dc load (i.e., $i_{\mathrm{o}} = v_{\mathrm{o}}/R$ in Fig. 3); and g_3 is the gating signal corresponding to Interval III (described previously in Section III-A), which can be represented by the following piecewise function:

$$g_3 = \begin{cases} 0 & 0 < t < d_{\mathrm{o}} T_{\mathrm{s}} \\ 1 & d_{\mathrm{o}} T_{\mathrm{s}} < t < T_{\mathrm{s}}. \end{cases} \tag{25}$$

It can be observed that

$$\langle g_3 \rangle_{T_{\mathrm{s}}} = \langle d'_{\mathrm{o}} \rangle_{T_{\mathrm{s}}} \tag{26a}$$

$$= D'_{\mathrm{o}} - \hat{d}_{\mathrm{o}} \tag{26b}$$

where $\langle \cdot \rangle_{T_{\mathrm{s}}}$ represents the average over a switching period, $(\hat{\cdot})$ designates a small-signal ac quantity, and d_{o} is the time varying outer duty cycle whose steady-state value is D_{o}.

For the development of the steady-state analysis and the state-space model, it is desired to find simplified expressions of (24a) and (24b), which is the focus of the following two sections.

1) Simplifying (24a): The total sum of the VSM cell voltages, v_{c}^{Σ}, is a proxy for the total energy contained in the VSM string. For the control of the converter, it is v_{c}^{Σ} that is regulated, which indirectly ensures that the total energy of the VSM string is balanced. This is similar to that proposed in [29]. A state equation for v_{c}^{Σ} can be obtained by summing (24a) over all VSM cells 1 to N, resulting in the following expression:

$$C \frac{dv_{\mathrm{c}}^{\Sigma}}{dt} = (1 - 2g_3) i_{\mathrm{L}} \sum_{k=1}^{N} n_{\mathrm{k}} \tag{27}$$

where

$$\sum_{k=1}^{N} n_{\mathrm{k}} = \begin{cases} \lfloor N_{\mathrm{C}} \rfloor & 0 < t < d_{\mathrm{o}} d_{\mathrm{i}} T_{\mathrm{s}} \\ \lceil N_{\mathrm{C}} \rceil & d_{\mathrm{o}} d_{\mathrm{i}} T_{\mathrm{s}} < t < d_{\mathrm{o}} T_{\mathrm{s}} \\ \lceil N_{\mathrm{D}} \rceil & d_{\mathrm{o}} T_{\mathrm{s}} < t < (d_{\mathrm{o}} + d_{\mathrm{o}} d'_{\mathrm{i}}) T_{\mathrm{s}} \\ \lfloor N_{\mathrm{D}} \rfloor & (d_{\mathrm{o}} + d_{\mathrm{o}} d'_{\mathrm{i}}) T_{\mathrm{s}} < t < T_{\mathrm{s}} \end{cases} \tag{28}$$

where d_{i} is the time varying inner duty cycle whose steady-state value is D_{i}.

Equation (27) can be simplified by assuming that the number of cells inserted in the charge and discharge modes is simply equal to the average values, N_{C} and N_{D}, respectively, which were defined earlier in (8). Accordingly, by employing (8), (28) can be approximated by the following function:

$$\sum_{k=1}^{N} n_{\mathrm{k}} \approx \begin{cases} N_{\mathrm{C}} & 0 < t < d_{\mathrm{o}} T_{\mathrm{s}} \\ N_{\mathrm{D}} & d_{\mathrm{o}} T_{\mathrm{s}} < t < T_{\mathrm{s}}. \end{cases} \tag{29}$$

Substituting (29) into (27) and noting (25), the following simplified expression can be obtained:

$$C \frac{dv_{\mathrm{c}}^{\Sigma}}{dt} = i_{\mathrm{L}} \left(N_{\mathrm{C}} g'_3 - N_{\mathrm{D}} g_3 \right) \tag{30}$$

where $(')$ denotes the complement of the signal.

2) Simplifying (24b): It is convenient to first expand (24b) as follows:

$$L\frac{di_{\mathrm{L}}}{dt}=\begin{cases}v'_{\mathrm{t,H}}(t)-v_{\mathrm{o}}(t) & 0<t<d_{\mathrm{o}}d_{\mathrm{i}}T_{\mathrm{s}}\\ v'_{\mathrm{t,L}}(t)-v_{\mathrm{o}}(t) & d_{\mathrm{o}}d_{\mathrm{i}}T_{\mathrm{s}}<t<d_{\mathrm{o}}T_{\mathrm{s}}\\ v'_{\mathrm{t,H}}(t)-v_{\mathrm{o}}(t) & d_{\mathrm{o}}T_{\mathrm{s}}<t<(d_{\mathrm{o}}+d'_{\mathrm{o}}d_{\mathrm{i}})T_{\mathrm{s}}\\ v'_{\mathrm{t,L}}(t)-v_{\mathrm{o}}(t) & (d_{\mathrm{o}}+d'_{\mathrm{o}}d_{\mathrm{i}})T_{\mathrm{s}}<t<T_{\mathrm{s}}.\end{cases}\tag{31}$$

If the expressions of $v'_{\mathrm{t,L}}$ and $v'_{\mathrm{t,H}}$ from (11a) and (11c), respectively, are substituted into (31), the following simplified expression for the time derivative of i_{L} is obtained:

$$L\frac{di_{\mathrm{L}}}{dt}=V_H-\tfrac{v_{\mathrm{c}}^{\Sigma}(t)}{N}\lceil N_{\mathrm{C}}\rceil+(g'_2+g_4)\tfrac{v_{\mathrm{c}}^{\Sigma}(t)}{N}-v_{\mathrm{o}}(t)\tag{32}$$

where g'_2+g_4 is a combination of the g_2 and g_4 gating signals (described previously in Section III-A). This combination can be represented by the following piecewise function:

$$g'_2+g_4=\begin{cases}1 & 0<t<d_{\mathrm{o}}d_{\mathrm{i}}T_{\mathrm{s}}\\ 0 & d_{\mathrm{o}}d_{\mathrm{i}}T_{\mathrm{s}}<t<d_{\mathrm{o}}T_{\mathrm{s}}\\ 1 & d_{\mathrm{o}}T_{\mathrm{s}}<t<(d_{\mathrm{o}}+d'_{\mathrm{o}}d_{\mathrm{i}})T_{\mathrm{s}}\\ 0 & (d_{\mathrm{o}}+d'_{\mathrm{o}}d_{\mathrm{i}})T_{\mathrm{s}}<t<T_{\mathrm{s}}.\end{cases}\tag{33a}$$

From inspection, it can be observed that

$$\langle g'_2+g_4\rangle_{T_{\mathrm{s}}}=\langle d_{\mathrm{i}}\rangle_{T_{\mathrm{s}}}\tag{34a}$$

$$=D_{\mathrm{i}}+\hat{d}_{\mathrm{i}}.\tag{34b}$$

In the next section, a steady-state analysis is performed to derive expressions for the time average outer and inner duty ratio terms, D_{o} and D_{i}, respectively.

B. Steady-State Analysis

1) Average Inner Duty Ratio Term, D_i: To derive an expression for D_{i}, volt-second balance is applied to (32).

If (9a) and (34) are, then, substituted into the resulting expression, the following equation for D_{i} is obtained:

$$D_{\mathrm{i}}=\left\lceil\frac{V_{\mathrm{H}}-V_{\mathrm{o}}}{V_{\mathrm{c}}}\right\rceil-\left(\frac{V_{\mathrm{H}}-V_{\mathrm{o}}}{V_{\mathrm{c}}}\right).\tag{35}$$

2) Average Outer Duty Ratio Term, D_o: To derive an expression for D_{o}, charge balance is applied to (30). By substituting in (26), (9a), and (9b), the following equation for D_{o} is obtained:

$$D_{\mathrm{o}}=\frac{1}{2}+\frac{1}{2}\frac{V_{\mathrm{o}}}{V_{\mathrm{H}}}.\tag{36}$$

Since the term $V_{\mathrm{o}}/V_{\mathrm{H}}\geq 0$, $D_{\mathrm{o}}\geq 0.5$.

C. Verification of Energy Balance

The purpose of this section is to prove that energy balance in the VSM string is achieved in each switching period.

An expression for the net energy accumulation in the VSM string over a switching period is equal to the following:

$$\Delta W_{\mathrm{c}}^{\Sigma}=\int_0^{T_{\mathrm{s}}}i_{\mathrm{H}}(t)v_{\mathrm{s}}(t)dt.\tag{37}$$

Equation (37) can be expanded out for the VSM charge and discharge modes as follows:

$$\Delta W_{\mathrm{c}}^{\Sigma}=\overbrace{\frac{N_{\mathrm{C}}}{N}\int_0^{D_{\mathrm{o}}T_{\mathrm{s}}}i_{\mathrm{L}}(t)v_{\mathrm{c}}^{\Sigma}(t)dt}^{\text{Charge mode}}-\overbrace{\frac{N_{\mathrm{D}}}{N}\int_{D_{\mathrm{o}}T_{\mathrm{s}}}^{T_{\mathrm{s}}}i_{\mathrm{L}}(t)v_{\mathrm{c}}^{\Sigma}(t)dt}^{\text{Discharge mode}}\tag{38}$$

which can be simplified to the following averaged expression:

$$\Delta W_{\mathrm{c}}^{\Sigma}=\frac{D_{\mathrm{o}}T_{\mathrm{s}}I_{\mathrm{L}}N_{\mathrm{C}}V_{\mathrm{c}}^{\Sigma}}{N}-\frac{D'_{\mathrm{o}}T_{\mathrm{s}}I_{\mathrm{L}}N_{\mathrm{D}}V_{\mathrm{c}}^{\Sigma}}{N}.\tag{39}$$

Note that $V_{\mathrm{c}}^{\Sigma}=NV_{\mathrm{c}}$.

If the expressions of (36) and (9) are inserted into (39), the following results:

$$\Delta W_{\mathrm{c}}^{\Sigma}=0.\tag{40}$$

Therefore, there is no net energy accumulation in the VSM string over a switching period. Accordingly, energy balance of the VSM string is achieved.

D. Linearized State-Space Model

To design the control for this converter, it is desired to derive a state-space model of the following form:

$$\dot{\mathbf{x}}=\mathbf{A}\mathbf{x}+\mathbf{B}\mathbf{u}\tag{41}$$

where $\mathbf{x}$ is the state vector and $\mathbf{u}$ is the input vector. Both vectors can be expanded out as follows:

$$\mathbf{x}=\begin{bmatrix}v_{\mathrm{c}}^{\Sigma}\\ i_{\mathrm{L}}\\ v_{\mathrm{o}}\end{bmatrix},\mathbf{u}=\begin{bmatrix}d_{\mathrm{i}}\\ d_{\mathrm{o}}\end{bmatrix}.$$

It can be recognized that the state equations of (30) and (32) are nonlinear differential equations. Accordingly, a linearization of the state equations is considered.

The linearized state vector and input vector are defined as follows:

$$\langle\mathbf{x}\rangle_{T_{\mathrm{s}}}=X+\hat{x}\tag{42a}$$

$$\langle\mathbf{u}\rangle_{T_{\mathrm{s}}}=U+\hat{u}.\tag{42b}$$

By applying (42) to the state equations and neglecting the nonfirst-order terms, the following small-signal ac state-space model of the converter is obtained:

$$\dot{\hat{\mathbf{x}}}=\mathbf{A}\hat{\mathbf{x}}+\mathbf{B}\hat{\mathbf{u}}\tag{43a}$$

$$\hat{\mathbf{y}}=\mathbf{C}\hat{\mathbf{x}}+\mathbf{D}\hat{\mathbf{u}}\tag{43b}$$

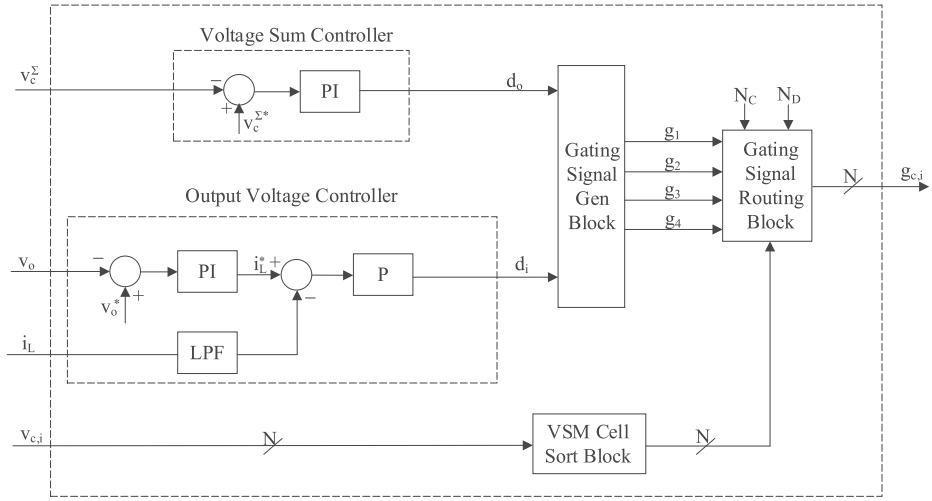


Fig. 7. Dynamic controller.

where

$$\hat{\mathbf{x}} = \begin{bmatrix} \hat{v}_{\mathrm{c}}^{\Sigma} \\ \hat{i}_{\mathrm{L}} \\ \hat{v}_{\mathrm{o}} \end{bmatrix}, \hat{\mathbf{u}} = \begin{bmatrix} \hat{d}_{\mathrm{i}} \\ \hat{d}_{\mathrm{o}} \end{bmatrix}$$

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 \\ \frac{D_{\mathrm{i}} - \lceil N_{\mathrm{C}} \rceil}{LN} & 0 & -\frac{1}{L} \\ 0 & \frac{1}{C_{\mathrm{o}}} & -\frac{1}{RC_{\mathrm{o}}} \end{bmatrix} \mathbf{B} = \begin{bmatrix} 0 & \frac{I_{\mathrm{L}}(N_{\mathrm{C}}+N_{\mathrm{D}})}{C} \\ \frac{V_{\mathrm{c}}^{\Sigma}}{LN} & 0 \\ 0 & 0 \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}, \mathbf{D} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

where the output vector is $\hat{\mathbf{y}} = [\hat{v}_{\mathrm{c}}^{\Sigma}, \hat{i}_{\mathrm{L}}, \hat{v}_{\mathrm{o}}]^T$.

The closed-loop control of the converter, presented in Section V, is based on the small-signal ac state-space model of (43).

V. Control Design

The dynamic controller for the converter is provided in Fig. 7. The main elements of the controller are the following: voltage sum controller, output voltage controller, VSM sort block, gating signal generation block, and the gating signal routing block. These control blocks are briefly described in the following sections.

1) Voltage Sum Controller: This controller regulates the total sum of all VSM cell capacitor voltages, v_{c}^{Σ}, with respect to the reference $v_{\mathrm{c}}^{\Sigma *}$ by adjusting the outer duty ratio term, d_{o}.

2) Output Voltage Control Block: This controller regulates the output voltage, v_{o}, with respect to the reference v_{o}^{*} by adjusting the inner duty ratio term d_{i}. This controller consists of an outer control loop and inner control loop. The outer control loop generates an inductor current reference, i_{L}^{*}. The difference between the reference and the inductor current is fed through a gain block to generate the inner duty ratio term, d_{i}.

3) Gating Signal Generation Block: The role of this block is to generate the gating signals g_1, g_2, g_3, g_4 corresponding to the four intervals of Fig. 5. The two inputs to the block are the duty ratio terms, d_{o} and d_{i}. To generate the pulsewidth modulation gating signals, sawtooth carrier waveforms are employed.

4) VSM Sort Block: The block sorts the VSM cell capacitors by voltage level. This sorted sequence is, then, provided as an input to the gating signal routing block.

5) Gating Signal Routing Block: The role of the routing block is to ensure that the individual VSM cells are balanced. The four gating signals, g_1–g_4, are distributed to the N VSM cells according to the sequence provided by the VSM sort block. The gating signals are distributed in such a way that the cells of lowest charge are charged more over the switching period and those of greatest charge are discharged more over the switching period. The distribution of the gating signals to the N VSM cells is provided in Table II. As an example, g_1 is distributed to the $\lfloor N_{\mathrm{C}} \rfloor$ VSM cells of lowest charge and g_3 is routed to the $\lfloor N_{\mathrm{D}} \rfloor - \lceil N_{\mathrm{C}} \rceil$ VSM cells of greatest charge.

TABLE II
Gating Signal Routing

Gating Signal Sequence	Number of Cells
g_1 (Lowest)	$\lfloor N_{\mathrm{C}} \rfloor$
g_2	1
g_4	1
g_3 (Greatest)	$\lfloor N_{\mathrm{D}} \rfloor - \lceil N_{\mathrm{C}} \rceil$

VI. Simulation Results

In this section, steady-state and transient simulation case results are provided for the converter of Fig. 3. The main circuit parameters for the simulation are provided in Table III. The

TABLE III
SIMULATION PARAMETERS

Parameter	Value	Unit
DC Input Voltage, V_H	3	kV
DC Output Voltage, V_o	380	V
Rated Power, P_r	10	kW
Switching Frequency, f_s	10	kHz
Nominal Cell Voltage, V_c	400	V
Number of VSM Cells, N	9	-
Cell Capacitor, C	72	μF
Leakage Inductance, L_l	10	uH
CSM Inductor, L	1.3	mH
Output Capacitor, C_o	200	μF

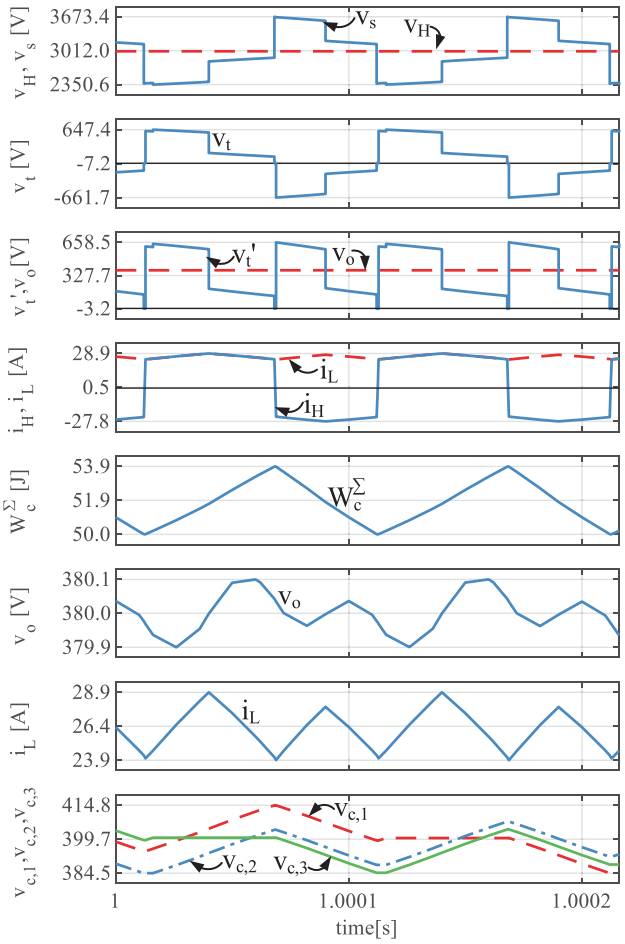


Fig. 8. Steady-state simulation results.

dc input voltage is 3 kV and the dc output voltage is 380 V representing a step ratio of 7.9:1. An example application may be interfacing a future dc distribution grid to a dc load such as a household, for instance. The switching devices for the VSMs have been considered to be 650 V SiC MOSFETs. The steady-state and transient simulation results are provided in Figs. 8 and 9, respectively.

A. Steady-State Case Results

Fig. 8 presents two switching periods of steady-state operation where the full rated power of 10 kW is delivered to the load. The waveforms provided in Fig. 8 are similar to those provided earlier in Fig. 5 but with additional waveforms for three of the nine individual VSM cell capacitor voltages, $v_{c,1}$, $v_{c,2}$ and $v_{c,3}$. As can be observed, the output voltage, v_o, is regulated to the reference value of 380 V. The VSM cell capacitor voltages are also shown to be balanced and regulated to the reference value of 400 V with a maximum voltage ripple of approximately 4% peak. The inductor current, i_L, has an average value of 26.3 A with 10% peak ripple. The nearly square-wave shape of i_H can be directly observed.

It can be observed in the waveform of i_L and v_o that a form interleaving on the dc-side of the CSM occurs. This is due to the rectified voltage, v_t', being a positive voltage value in both the charge and discharge operating modes. If, for example, $D_o \approx 1/2$, the effective switching frequency on the dc-side of the CSM is $\approx 2f_s$. This interleaving reduces the inductor ripple current by nearly 1/2 in this simulation case. Note that the ripple current during VSM charge mode is greater than in VSM discharge mode since $D_o \geq 1/2$.

B. Transient Case Results

Fig. 9 presents the transient simulation results where step changes in the load have been simulated. At $t = 1.001$ s, a step-change in load from 2.5 to 10 kW occurs and at $t = 1.007$ s, a step-change in load from 10 to 2.5 kW occurs. In addition to the waveforms of Fig. 8, additional plots have been provided for d_o, d_i, and the dc load current, i_o. Note that only one VSM cell capacitor voltage waveform has been provided in Fig. 9.

It can be observed in Fig. 9 that the total energy in the VSM string is balanced. Therefore, the sum of the VSM cell voltages is being well regulated. In addition, the average inductor current settles to i_o within approximately 1 ms after the step changes in load. The output voltage, v_o, has an overshoot of 5% when the load steps from 10 to 2.5 kW. The output voltage settles within approximately 6 ms. The maximum voltage ripple for VSM cell 1 is approximately four times greater for the 10 kW load compared to the 2.5 kW load.

Additionally, it can be observed that the voltage levels of v_t are the same irrespective of the load current value. It is, therefore, through adjusting d_i that the converter is able to regulate the power delivered to the CSM. Recall, by varying d_i, the relative duration of $v'_{t,H}$–$v'_{t,L}$ is adjusted. During load changes, the inner duty ratio term, d_i, adjusts to decrease or increase the inductor current depending on the direction of the load change. To decrease the inductor current, the power delivered to the CSM must be less than the power delivered to the load. Conversely, to increase the inductor current, the power delivered to the CSM must be greater than the power delivered to the load. An increase in power is accompanied by an increase in d_i and, conversely, a decrease in power is accompanied by a decrease in d_i as observed in Fig. 9. However, the steady-state value of D_i is not significantly impacted by the load as illustrated in Fig. 9 as well as in the analytically derived equation of (35). Also important to

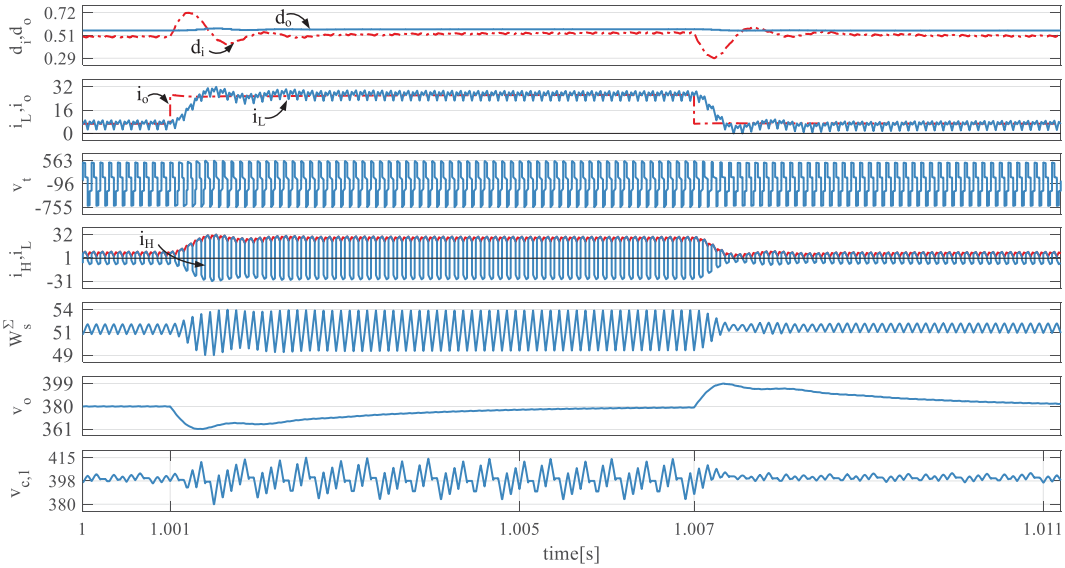


Fig. 9. Transient simulation results.

TABLE IV
EXPERIMENTAL PARAMETERS

Parameter	Value	Unit
DC Input Voltage, V_{H}	750	V
DC Output Voltage, V_{o}	95	V
Rated Power, P_{r}	1.2	kW
Switching Frequency, f_{s}	5.0	kHz
Nominal Cell Voltage, V_{c}	167	V
Number of VSMs, N	6	-
Cell Capacitor, C	4.72	mF
CSM Inductor, L	5	mH
Output Capacitor, C_{o}	2.5	mF

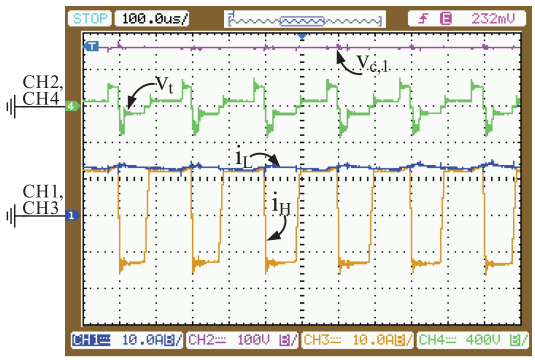
highlight is that the outer duty ratio term, d_{o}, is not significantly impacted by load changes. This is shown in both Fig. 9 and (36).

VII. EXPERIMENTAL RESULTS

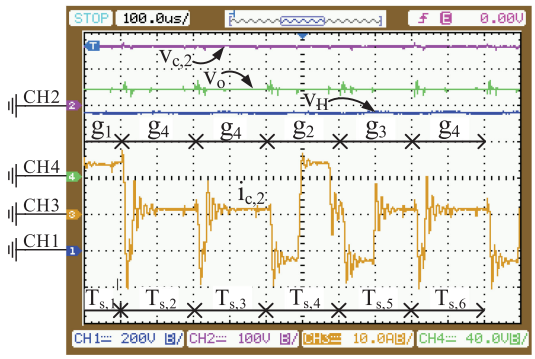
In this section, experimental results from a laboratory scale converter are presented. The experimental results are for a 750–95 V converter with a rated power of 1.2 kW. The main circuit parameters for this experimental system are provided in Table IV.

A. Steady-State Experimental Results

Fig. 10 presents five full switching periods of steady-state operation with 1.2 kW of power being delivered to a resistive load. Fig. 10(a) provides the waveforms of the capacitor voltage for VSM cell 1, $v_{\mathrm{c,1}}$, the voltage across the ac-side terminals of the CSM, v_{t}, the inductor current, i_{L}, and the string current, i_{H}. Fig. 10(b) provides waveforms for the capacitor voltage of VSM cell 2 and the current into the capacitor of VSM cell 2, $v_{\mathrm{c,2}}$ and $i_{\mathrm{c,2}}$, respectively, the dc input voltage, V_{H}, and the output voltage, v_{o}.



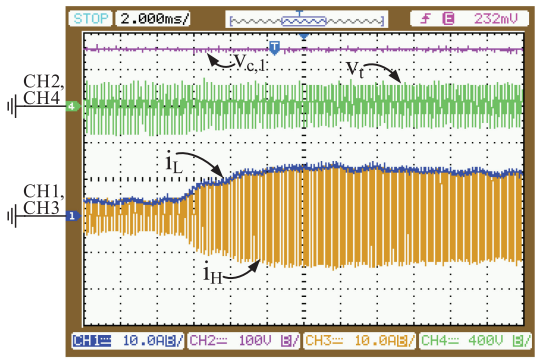
(a)



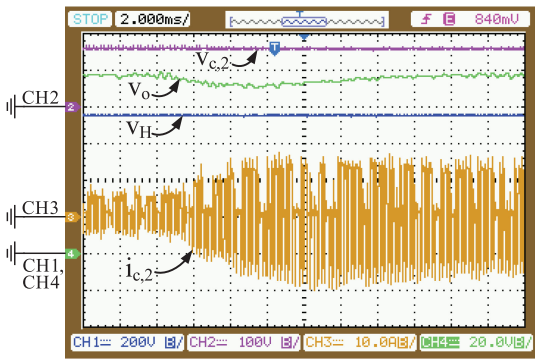
(b)

Fig. 10. Steady-state experimental waveforms. (a) $v_{\mathrm{c,1}}, v_{\mathrm{t}}, i_{\mathrm{L}}, i_{\mathrm{H}}$. (b) $v_{\mathrm{c,2}}, V_{\mathrm{H}}, v_{\mathrm{o}}, i_{\mathrm{c,2}}$.

The dc input voltage can be observed to be 750 V and the output voltage is shown to be tightly regulated to the reference value of 95 V. The average inductor current is 13.2 A corresponding to approximately 1.2 kW of power being delivered to the load. The



(a)



(b)

Fig. 11. Transient experimental waveforms. (a) $v_{c,1}, v_t, i_L, i_H$. (b) $v_{c,2}, V_H, v_o, i_{c,2}$.

VSM cell capacitor voltages are also shown to be balanced and tightly regulated to the reference value of 167 V. The magnitude of the string current, i_H, can also be seen to be equal to the inductor current, i_L, during VSM charge and discharge modes.

It can also be observed in the experimental waveforms that the sequence of the four intervals is different from that presented in Fig. 5. The sequence of the intervals is instead III, IV, II, and I. This is done simply for ease of experimental implementation.

The *di/dt* of the string current, i_H, during commutation intervals is slower for the transition to charge mode compared to the transition to discharge mode. This difference is a result of the alternate sequence of the four intervals employed in the experimental system.

Some additional insights can be made by comparing the string current waveform, i_H, with the waveform of the current into VSM cell capacitor 2, $i_{c,2}$. In Fig. 10(b), six switching periods are labeled as $T_{s,1}$–$T_{s,6}$. For each switching period, one of the four unique gating signals, g_1–g_4, is distributed to the VSM cell 2. The gating signal corresponding to VSM cell 2 in each interval can be obtained directly by inspection. For instance, in switching period $T_{s,2}$, VSM cell 2 is inserted during interval III and bypassed for intervals I, II, and IV. Therefore, referring back to Fig. 5, it can be deduced that g_4 is being distributed to VSM cell 2 during this switching period. It can be observed that over the total duration of the six switching periods, all four gating signals are distributed to VSM cell 2.

B. Transient Experimental Results

The transient experimental results are presented in Fig. 11. In this transient case, the load undergoes a step change from 4 to 12 A. As can be observed, the waveforms are similar to those observed in the simulated waveforms of Fig. 9. In Fig. 11, the VSM cell capacitor voltages are well regulated and balanced. As expected, a depression in the output voltage, v_o, is observed for the step-change in load. The system settles to the new steady-state operating point in approximately 10 ms.

VIII. Conclusion

In this article, a novel energy transfer mechanism is proposed, which enables a single-stage modular multilevel dc–dc converter topology to be realized with a reduced number of VSMs and a significantly reduced VSM capacitor size compared to other approaches.

The proposed topology features a cascade connection of current and voltage-source submodules in a single string. The power inductor of this topology is separated from the string of submodules by the CSM. The placement of the power inductor on the output of the CSM allows rapid commutation of the string current with a *di/dt* limited only by the leakage inductance of the commutation loop formed on the ac-side of the CSM. This is highly advantageous as it enables the CSM to shape a string current of nearly square-wave shape at the switching frequency of the CSM.

In the M2DC and the HVDC-AT topologies, the circulating ac current component in the string is limited to approximately 60–400 Hz due to ac choke ac voltage drop and magnetic loss considerations. Comparatively, for the CS-MMC, which does not feature an ac choke, the circulating ac current components are in the medium frequency range (approximately 5–40 kHz) enabling a commensurate reduction in VSM capacitor size over these other topologies. Additionally, the CS-MMC can realize a high step down ratio dc–dc converter, with a reduced number of installed voltage source submodules due to the single string structure together with a low string total blocking voltage requirement.

This article presents the operating principles, control design, and circuit analysis for one particular architecture of the CS-MMC along with supporting simulation and experimental results from a laboratory scale converter system.

Appendix

In this section, analytical equations are developed for sizing the VSM cell capacitors, C, the CSM inductor, L, and the output capacitor, C_o.

A. VSM Cell Capacitor Sizing

The VSM cell capacitor is sized based on the maximum voltage ripple. The VSM cell voltage ripple, Δv_c, can be approximated by the following empirically derived expression:

$$\Delta v_c = \frac{1}{C}\int_0^{T_D = D_o' T_s} i_H dt \tag{44}$$

where v_c is equal to the capacitor ripple voltage.

If the small-ripple assumption is considered, $I_{\mathrm{H}} = I_{\mathrm{L}}$, and, therefore, (44) can be rearranged to solve for the following expression for C:

$$C = \frac{I_{\mathrm{L}} D_{\mathrm{o}}'}{V_{\mathrm{c}\%} V_{\mathrm{c}} f_{\mathrm{s}}} \tag{45}$$

where $V_{\mathrm{C}\%}$ represents the voltage ripple peak as a percentage of the nominal value.

B. CSM Inductor Sizing

The CSM inductor can be sized based on the maximum allowable current ripple. In deriving an expression for the maximum inductor current ripple, only VSM charge mode is considered, given the interleaving nature of the charge and discharge modes.

The current ripple, Δi_{L}, can be approximated by the following expression:

$$\Delta i_{\mathrm{L}} = \frac{1}{2L} \int_0^{T_{\mathrm{i}} = D_{\mathrm{i}}' D_{\mathrm{o}} T_{\mathrm{s}}} \left(v_{\mathrm{t}}'(t) - v_{\mathrm{o}}(t) \right) dt. \tag{46}$$

By applying the small-ripple approximation and noting from Section III-D that $V_{\mathrm{t}}' = V_{\mathrm{t,L}}'$ during interval II, the following expression for L results:

$$L = \frac{D_{\mathrm{i}}' D_{\mathrm{o}}}{2 I_{\mathrm{L}} I_{\mathrm{L}\%} f_{\mathrm{s}}} \left(V_{\mathrm{o}} - V_{\mathrm{t,L}}' \right) \tag{47}$$

where $I_{\mathrm{L}\%}$ represents the current ripple peak as a percentage of the nominal value.

C. Output Capacitor Sizing

In this article, the output capacitor, C_{o}, is sized to limit output voltage overshoot for load rejections. While the overshoot is highly dependent on the control design, a minimum capacitance value can be established based on the stored energy in the inductor L. The inductor will fully discharge into the output capacitor when there is a load rejection. An expression for the minimum capacitance value can, therefore, be derived as follows:

$$C_{\mathrm{o}} = \frac{L I_{\mathrm{L}}^2}{(V_{\mathrm{o}} * (1 + V_{\mathrm{o}\%}))^2 - V_{\mathrm{o}}^2} \tag{48}$$

where $V_{\mathrm{o}\%}$ represents the maximum overshoot as a percentage of the nominal value.

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