Letters

Passive Damping Optimization of the Integrated-Magnetics-Based Differential-Mode Ćuk Rectifier

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***Abstract*—Interaction of the ac-link capacitor with ac- and dc-side inductors in the Ćuk converter topology introduces resonant frequency oscillations that affect the dynamic response and performance of the converter. To mitigate these effects, in this letter, a simple passive damping-based solution is employed, which is optimized both from control perspective and power loss for an integrated-magnetics-based differential-mode Ćuk rectifier. An experimental prototype is developed to validate the effect of no damping versus optimized damping and its effects on the rectifier performance parameters are provided.**

***Index Terms*—Control, Cuk converter, damping, differential mode, passive, rectifier, stability.**

I. Introduction

THE differential-mode Ćuk rectifier (DMCR), as shown in Fig. 1, provides benefits in terms of reduced device count, modularity, and continuous-input and continuous-output currents. The lack of transformer and symmetry of the DMCR leads ideally to identical applied voltage across the ac- and dc-side inductors, thereby making them a suitable candidate for magnetic integration [1], [2]. Integrated magnetics (IM) provides various advantages in terms of enhancing the power density and specific power of the DMCR, reduced total harmonic distortion (THD) via ripple cancellation, and improved magnetics efficiency by lowering the core loss. This is typically achieved by coupling the winding of the ac- and dc-side inductors to achieve maximum flux cancellation.

However, the absence of damping in the ac-link path of the DMCR yields complex conjugate zeroes and poles in close neighborhood. If the locations of these poles and zeros reside within the control bandwidth of the loop gain, they yield uncontrollable *LC* oscillations that may deteriorate the performance of the converter [3], [4].

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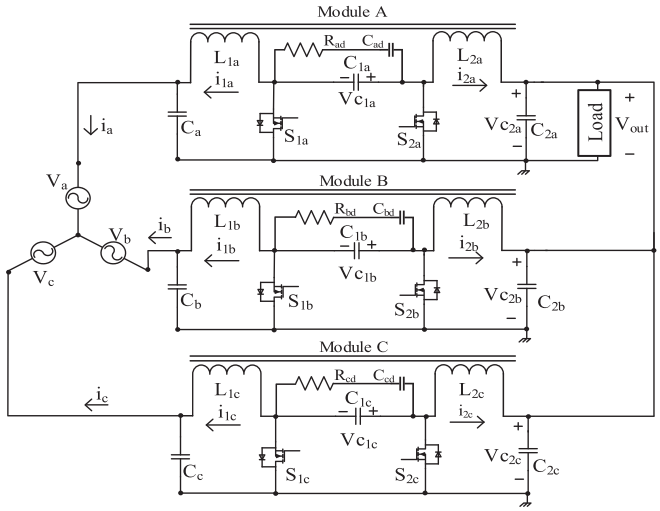

Fig. 1. Schematic of a three-phase IM-based nonisolated DMCR.

In this letter, in order to dampen the oscillations in the ac-link voltage and current of the DMCR, a *RC* damper, determined using a systematic analysis and optimized approach, is used across the ac-link capacitor, as shown in Fig. 1. Furthermore, to validate the effect of the *RC* damper, an experimental prototype of the IM-based DMCR is developed. In a prior work, [5] by our group, a *RC* damper is introduced for a single-phase inverter; however, the approach to determine the *RC*-damper values is based solely on a trial and error. Unlike the present manuscript, [5] does not outline any mechanism for tuning the *RC* damping for optimizing THD and efficiency. Finally, it is noted that, even though controlled virtual damping approach (as exhibited in [6] for a full-bridge inverter) is a possibility, the higher dimensionality and nonlinearity of the DMCR necessitate complex state estimation and enhanced computation [7] due to control complexity and/or added cost of high-bandwidth sensors.

II. DMCR Analysis

A. Effect of RC Damper on Converter Response

The input of the DMCR is connected differentially to the three-phase three-wire utility grid, while the output is connected in parallel configuration to the load. The ac- and dc-side

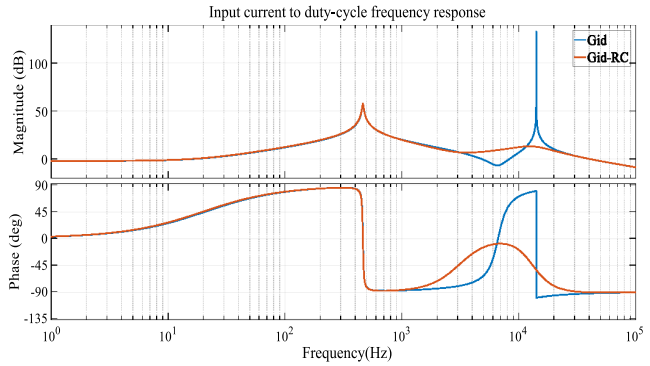

Fig. 2. Frequency response of G_{id} and G_{id-RC}.

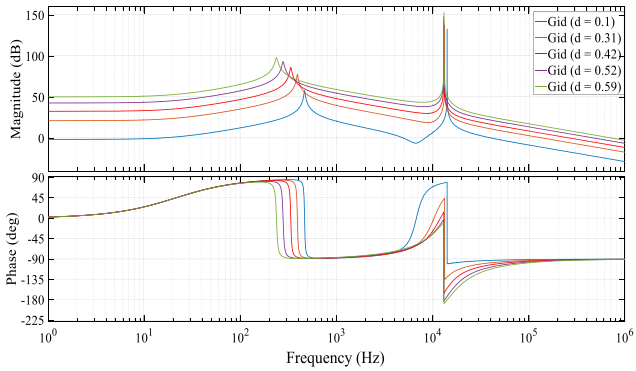

Fig. 3. Frequency response of G_{id} with varying input voltage and duty cycle.

inductors represented by L_{1a} (L_{1b}, L_{1c}) and L_{2a} (L_{2b}, L_{2c}) in Module A, (B, C), are coupled together to form an IM.

Effect of the *RC* damper on the open-loop response of the DMCR is analyzed by constructing its small-signal model. For simplicity, parameters L_{1a} and L_{2a} are considered to be the same. Symbol M represents the coupled inductance and is expressed in terms of coupling factor (k) as follows:

$$M = k\sqrt{L_1 L_2}. \tag{1}$$

The duty-cycle to input-current transfer function for the DMCR without and with the *RC* damper are as follows:

$$G_{id} = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0}$$
$$G_{id-RC} = \frac{x_4 s^4 + x_3 s^3 + x_2 s^2 + x_1 s + x_0}{y_5 s^5 + y_4 s^4 + y_3 s^3 + y_2 s^2 + y_1 s + y_0} \tag{2}$$

where the parameters are defined in Appendix A.

The Bode plot in Fig. 2 displays the frequency response of G_{id} and G_{id-RC}. The first peak corresponds to the interaction between the output capacitor and the dc-side inductor. The second peak corresponds to the interaction of ac-link capacitor with the ac- and dc-side inductors and varies with duty cycle and operating conditions. Addition of the *RC* damper in the DMCR introduces one zero and one pole near the second peak of the G_{id}. In contrast to the dc–dc operation, for the DMCR, continuously varying operating conditions introduce duty-cycle dependent oscillations.

As shown in Fig. 3, as the duty cycle is increased, the response becomes more prone to oscillations due to complex conjugate zeroes and poles being in close vicinity.

In order to suppress these duty-cycle dependent oscillations, the R_d and C_d values of the *RC* damper for the DMCR are so selected such that the damper provides a lower-impedance path to the ac-link capacitor up to the maximum resonance frequency of the DMCR. Based on the power-stage parameters displayed in Table 1 and taking the input-voltage and duty-cycle variations into account, the maximum resonance frequency is determined to be 14.8 kHz, as evident from Fig. 3.

To determine the values of R_d and C_d that provide equal or lower impedance up to 15 kHz, a parametric plot of the impedance of the ac-link capacitor (Z_1), and the *RC* damper

TABLE I
POWER STAGE PARAMETERS OF A DMCR MODULE

Input voltage (line to line)	208 V (RMS)
Output voltage (V_{out})	Up to 200 V dc
Ac-and dc-side inductance (L_{1a}, L_{2a})	100 μH
Ac-side capacitance (C_a)	4.4 μF
Dc-side capacitance (C_{2a})	3 mF
Blocking capacitance (C_{1a})	1.5 μF
Switching frequency (f_s)	100 kHz

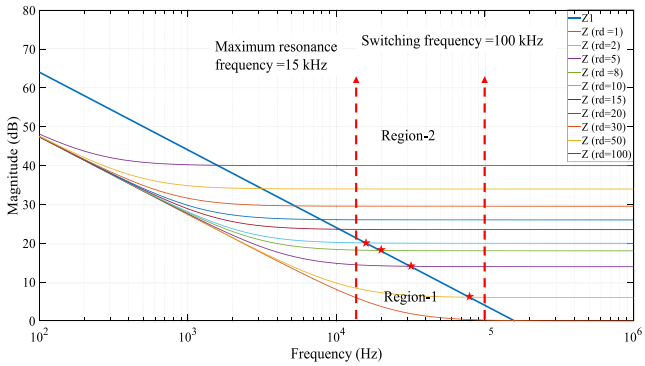

Fig. 4. Impedance plot of the ac-link capacitor and the RC damper. The lower and upper bounds on the value of R_d and C_d are found to be (10 Ω, 6.8 μF) and (2 Ω, 6.8 μF), respectively.

at different values of R_d is shown in Fig. 4. The intersection of impedance Z_1 in blue with two red dotted markers sets the upper and lower bound on the value of R_d for a given C_d. It is inferred from Fig. 4 that, a higher value of C_d provides enhanced damping by reducing the overall impedance. Using Fig. 4, any value of R_d between 1 and 10 Ω can be chosen to dampen the oscillations. It is inferred from Fig. 4, that the lowest R_d provides overall better damping from the control-performance viewpoint but will also allow the energy transfer at switching frequency thereby bypassing the ac-link capacitor C_1.

B. Power Loss in the RC Damper

Although the *RC* damper improves the DMCR frequency response by snubbing the intramodular interactions, it incurs a

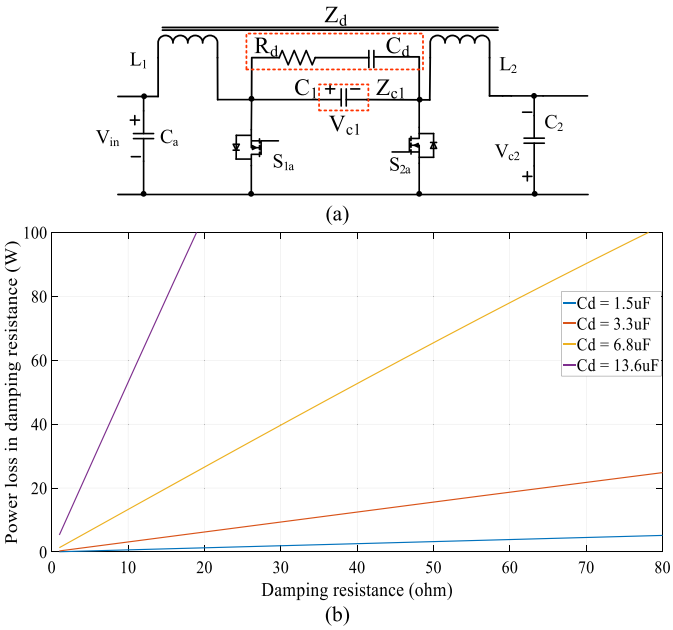

Fig. 5. (a) *RC* damper placed in parallel to the ac-link capacitor. (b) Parametric plot of power loss in in R_d with variation in C_d.

modest power loss. Fig. 5(a) displays the *RC* damping network across the ac-link capacitance. By using

$$i_{cd,\mathrm{rms}}|_{60\mathrm{Hz}} = \frac{V_{c1,\mathrm{rms}}|_{60\mathrm{Hz}}}{Z_d} = \frac{jV_{c1,\mathrm{rms}}\left(\omega C_d\right)}{1+j\omega R_d C_d} \tag{3}$$

where $Z_d = \frac{1+j\omega R_d C_d}{j\omega C_d}$, the total loss in R_d is found to be

$$P_{Rd} = \mathrm{Real}\left(i_{cd,\mathrm{rms}}^2 R_d\right). \tag{4}$$

Fig. 5(b) displays P_{Rd} with variation in R_d and C_d. It is noted that, P_{Rd} increases with higher C_d compared to R_d. Thus, from an efficiency standpoint, higher value of C_d should be avoided. This tradeoff between the control performance and efficiency leads to the optimization of the R_d and C_d. To achieve satisfactory PFC operation with input current THD $<5\%$ a higher value of R_d is used.

III. Experimental Results

To validate the performance with/without using the *RC* damper in the ac-link path, an experimental prototype of the DMCR is designed, as shown in Fig. 6. The power-stage parameters for the DMCR are provide in Table I. The DMCR comprises SiC MOSFET (C2M0040120D: 1200 V, 36 A). The duty cycles generated by the DSP are used to drive the SiC-MOSFET's operating at a switching frequency ($f_s = 1/T_s$) of 100 kHz. A conventional dual-loop control comprising an inner current loop and an outer voltage control is used.

A. Without RC Damping

Fig. 7(a) displays the steady-state waveform of the three-phase input currents and phase-A input voltage. The DMCR

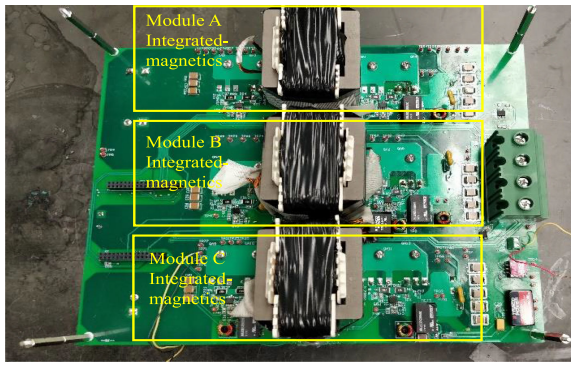

Fig. 6. Experimental prototype of the IM-based DMCR.

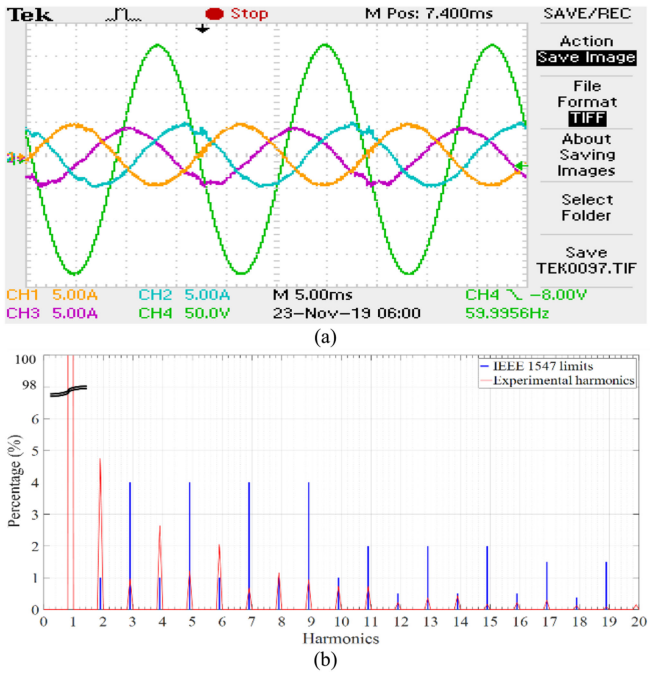

Fig. 7. (a) Three-phase input-current waveforms without the *RC* damper. Signals in orange, blue, and purple represent input currents (5 A/div) of phases A, B, and C, respectively. Signal in green represent phase-A line-to-neutral voltage (50 V/div). (b) Comparison of the phase-A input-current harmonic spectrum with the IEEE-519-2014 standard.

is operated at an input voltage of 208-V rms and the current reference is set at 4-A peak. The control ensures that the current reference is in phase with the input voltage. The THD and power factor of the DMCR for an output power of 1 kW is found to be 6.68% and 0.998, respectively. The efficiency of the DMCR is found to be 92%.

Fig. 7(b) displays a comparison of the harmonic spectrum of phase-A current and limits on the allowable harmonics in ac-grid. The odd harmonics that arise due to the intermodular interaction among the DMCR modules are below the limits specified by IEEE-519-2014 standard. However, the even harmonics that arise due to the nonlinearity of the DMCR are higher than that specified in the standard. As evident from Fig. 7(a), the THD of the input current waveform at rated voltage is observed to be

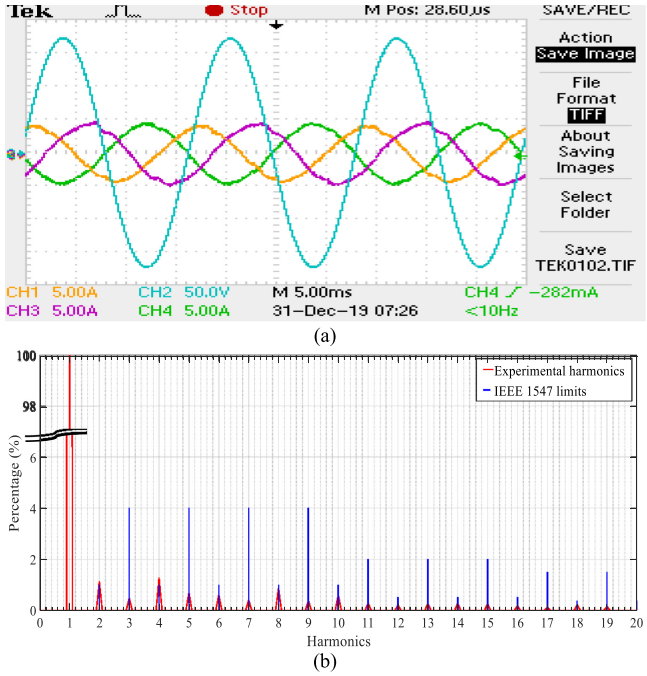

Fig. 8. Three-phase input current waveforms with the *RC* damper. Signals in orange, blue, and purple represent input currents (5 A/div) of phases A, B, and C, respectively. Signal in green represent phase-A line-to-neutral voltage (50 V/div). (b) Comparison of the phase-A input-current harmonic spectrum with the IEEE 519-2014 standard.

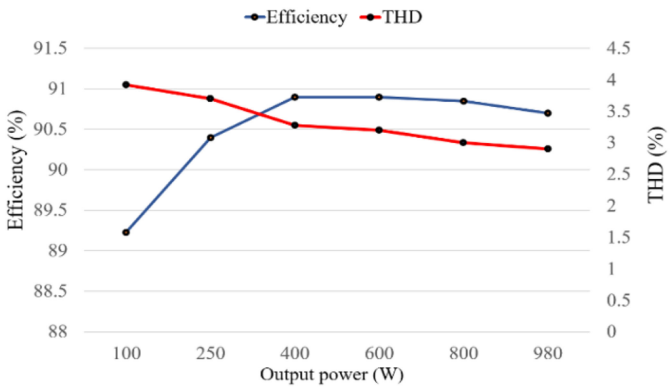

Fig. 9. Variation in efficiency and THD of DMCR with varying output power ranging from 100 to 1000 W.

6.68%, which is higher than the set value of 5% based on the IEEE-519-2014 standard [8].

B. With RC Damping

For the same operating conditions as abovementioned, Fig. 8(a) displays the steady-state input current waveforms of the DMCR at a power level of 1 kW. The values of R_d and C_d are selected to be 5 Ω and 6.8 μF, respectively. The THD and the power factor are found to be 3% and 0.997, respectively.

Fig. 8(b) displays the amplitude of the harmonic components present in the input current of phase A. It is seen that, the amplitude of each harmonic component complies with the maximum

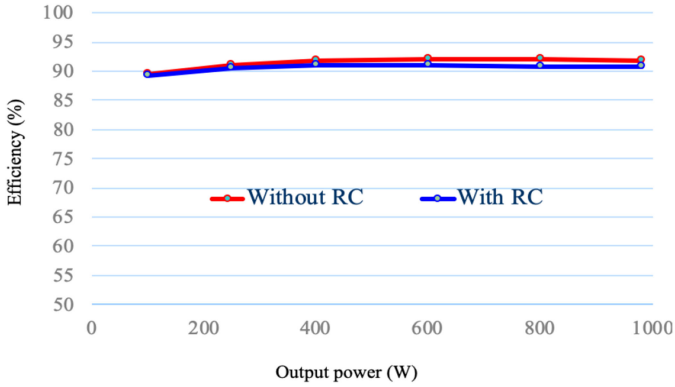

Fig. 10. Efficiency vs output power of the DMCR with/without RC damping.

allowable limits on drawable harmonic current as specified by the IEEE-519-2014 standard.

Fig. 9 displays efficiency and THD with varying output power for the DMCR operating with the *RC* damper. The THD is found to be acceptably below 5% for the operating regime.

In Fig. 10, the efficiencies of the DMCR operating with and without the *RC* damper are plotted. For the former, a modest reduction in efficiency for the DMCR is observed for a rated power of 1 kW, while at 10% of the rated power the difference is found to be negligibly small.

IV. Conclusion

Lack of damping in the ac-link path of the DMCR results in frequency-dependent *LC* oscillations. To snub these oscillations, without enhanced control complexity and sensing/estimation needs, a *RC* damping is introduced in the ac-link path. Inclusion of the *RC* damper in the DMCR requires a tradeoff between the performance and efficiency of the DMCR. A systematic mechanism is provided to tune the *RC* damper to realize this tradeoff and an acceptable control performance.

Appendix A
Coefficients of G_{id} and G_{id-RC}

G_{id} *Numerator Coefficients*

$$a_3 = C_1C_2R^2V_{in}\left(L-M\right)\left(1-d\right)$$

$$a_2 = V_{in}\left[Ld + C_1R^2 - d^2\left(L + C_2R^2\right) + Md^2 + R^2d(C_2 - C_1\right]$$

$$a_1 = V_{in}R\left[\left(L-M\right)\left(C_1 - C_2d^2\right) + Ld\left(C_2 - C_1\right) + C_1Md\right]$$

$$a_0 = 2RV_{in}d\left(1-d\right).$$

G_{id} *Denominator Coefficients*

$$b_4 = C_1C_2R^2\left(L^2 - M^2\right)\left(1-d\right)^2$$

$$b_3 = C_1R\left(L^2 - M^2\right)\left(1-d\right)^2$$

$$b_2 = R^2(1-d)^2\left(L\left(C_1 + C_2\right) - 2\left(L-M\right)\left(C_2d - C_2d^2\right)\right)$$

$$b_1 = R(1-d)^2\left(L - 2\left(L-M\right)\left(d-d^2\right)\right)$$
$$b_0 = R^2(1-d)^4.$$

G_{id-RC} *Numerator Coefficients*

$$\begin{aligned}
x_4 =\ & C_1C_2C_dR^2R_dV_{in}\left(L - M\right)\left(1 - d\right)\\
x_3 =\ & RV_{in}\left(C_1C_2LR + C_2C_dLR + C_1C_dLR_d\right.\\
& - C_1C_2MR - C_2C_dMR - C_1C_dMR_d\\
& - C_2C_dLR_dd^2\\
& + C_2C_dMR_dd^2 - C_1C_2LRd - C_2C_dLRd\\
& - C_1C_dLR_dd + C_2C_dLR_dd + C_1C_2MRd\\
& \left. + C_2C_dMRd + C_1C_dMR_dd\right)\\
x_2 =\ & V_{in}\left(C_1LR + C_dLR - C_1MR - C_dMR\right.\\
& - C_2LRd^2 - C_dLR_dd^2 + C_2MRd^2\\
& + C_dMR_dd^2 - C_1LRd + C_2LRd - C_dLRd\\
& + C_dLR_dd + C_1MRd + C_dMRd\\
& + C_1C_dR^2R_d - C_1C_dR^2R_dd\\
& \left. + C_2C_dR^2R_dd - C_2C_dR^2R_dd^2\right)\\
x_1 =\ & V_{in}\left(Ld + C_1R^2 + C_dR^2 - Ld^2 + Md^2\right.\\
& - C_2R^2d^2 - C_1R^2d + C_2R^2d - C_dR^2d\\
& \left. - 2C_dRR_dd^2 + 2C_dRR_dd\right)\\
x_0 =\ & 2RV_{in}d\left(1 - d\right)\left(R + R_dd\right).
\end{aligned}$$

G_{id-RC} *Denominator Coefficients*

$$\begin{aligned}
y_5 =\ & C_1C_2C_dR^2R_d\left(L^2 - M^2\right)\left(1 - d\right)^2\\
y_4 =\ & R\left(L^2 - M^2\right)\left(1 - d\right)^2\left(C_1C_2R + C_2C_dR\right.\\
& \left. + C_1C_dR_d\right)\\
y_3 =\ & R(1 - d)^2\left(C_1L^2 + C_dL^2 - C_1M^2 - C_dM^2\right.\\
& + C_1C_dLRR_d + C_2C_dLRR_d\\
& - 2C_2C_dLRR_dd + 2C_2C_dMRR_dd\\
& \left. + 2C_2C_dLRR_dd^2 - 2C_2C_dMRR_dd^2\right)\\
y_2 =\ & R(1 - d)^2\left(C_1LR + C_2LR + C_dLR + C_dLR_d\right.\\
& + 2C_2LRd^2 + 2C_dLR_dd^2 - 2C_2MRd^2\\
& - 2C_dMR_dd^2 - 2C_2LRd - 2C_dLR_dd\\
& \left. + 2C_2MRd + 2C_dMR_dd\right)\\
y_1 =\ & R(1 - d)^2\left(L - 2Ld + 2Md + 2Ld^2 - 2Md^2\right.\\
& \left. + C_dRR_d + C_dRR_dd^2 - 2C_dRR_dd\right)\\
y_0 =\ & R^2(1 - d)^4.
\end{aligned}$$

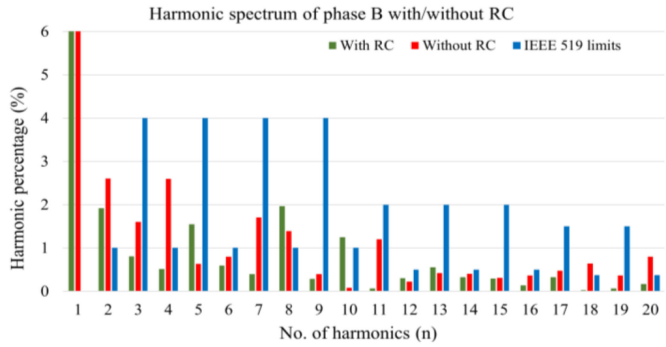

Fig. 11. Comparison of harmonic spectrum for the DMCR, operating with/without the *RC* damper, against IEEE-519-2014 harmonic limits.

Appendix B
Harmonic Spectrum of Phase B With/Without *RC* Damping

Fig. 11 displays a comparison of phase B harmonic spectrum with/without employing *RC* damping against IEEE-519-2014 limits. It is seen that the addition of *RC* damping reduces the majority of input current harmonics to bring down the THD under 5% limit.

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