Modified Single-Edge SVPWM Technique to Reduce the Switching Losses and Increase PWM Harmonics Frequency for Three-Phase VSIs

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***Abstract*—This article proposed a modified single-edge space vector pulsewidth modulation (MS-SVPWM) technique by adjusting the zero vectors of saw-tooth carrier SVPWM technique for three-phase voltage source inverters to reduce the switching losses and increase the PWM noises frequency. Mathematical analysis and implementation of the proposed MS-SVPWM are demonstrated in detail. The differences in PWM noises reduction between MS-SVPWM and modified SVPWM technique are compared by time-varying PWM noises analysis, computer simulation, and experimental results. With the same average switching frequency of conventional SVPWM, MS-SVPWM could increase the PWM harmonics frequency by 50%. Employing the same carrier frequency, MS-SVPWM could reduce average switching frequency by 33% compared with conventional SVPWM technique, and the switching losses could be reduced by more than 25% when the phase angle is less than 60°. Reduction of switching losses could ease the cooling requirements and result in greater compactness of the system, especially vital concern in high-power applications and limited-space environments. The detailed experimental results confirm the effectiveness of the proposed MS-SVPWM at last.**

***Index Terms*—Harmonic suppression, low-order harmonics, space vector pulsewidth modulation (SVPWM), switching losses, three-phase voltage source inverter (VSI).**

I. Introduction

SPACE vector pulsewidth modulation (SVPWM) technique is widely employed to achieve excellent static and dynamic performances in three-phase voltage source inverters (VSIs) [1]–[6]. However, undesirable sideband voltage harmonics will generate during the intrinsic switching process. The high-frequency harmonics mainly concentrate nearby the carrier frequency and its multiples [4], [7], which brings iron core losses, copper resistive losses, unpleased acoustic noise, and electromagnetic interference in motor drive system or grid-connected inverter [8], [9]. Thus, the high-frequency harmonics caused by PWM technique are quite common issues in three-phase VSIs and should be addressed properly [10], [11].

To eliminate the PWM harmonics and reduce the intensity of noise, random PWM-based (RPWM) methods have been developed, in which switching frequency, pulse position, or pulsewidth vary randomly from one switching cycle to another [12], [14]. For common random PWM frequency technique, the switching frequency values are normally picked randomly within a predefined switching frequency range typically ±25% around a nominal switching frequency [12], [13]. Compared with the fixed switching frequency PWM technique, RPWM-based methods could spread power of noise over a wide frequency range and reduce the peaky PWM noise about 9–10 dB [15]. A hybrid RPWM technique based on modified SVPWM (MSVPWM) is proposed in [16], which could reduce the PWM noise more effectively. However, for RPWM-based methods, the power of noise is distributed in a wide frequency domain, which may overlap with the system resonant frequencies, resulting in additional vibration and acoustic noise. In addition, the random switching cycles will weaken the performance of the closed-loop system.

Employing output filters after VSIs is another particularly effective approach to reduce the switching ripple and make the output voltage sinusoidal [20], [22], [24]. In order to achieve an almost sinusoidal voltage and avoid additional resonance suppressing control, the resonance frequency of filter has to be well below the lowest frequency of the output voltage harmonic resulting from PWM and above the fundamental frequency for output filters, such as the *LC* or *LCL* filter [17]–[24]. To avoid inductors saturation caused by fundamental component, the filters are large in size, which brings additional negative effects on control performance. These characteristics limit applications of output filters [20]. By using smaller size magnetically coupled inductors and interleaved technique, a novel approach is proposed in [21] to remove high-frequency PWM harmonics for parallel inverters without additional negative effect on control performance. However, this technique could only be employed in parallel inverters and not in the common three-phase inverters.

In fact, with the increase of switching frequency, inductance and capacitance would be smaller and the negative effects of PWM noises are weakened for power filter [23], [27]. At the same time, the higher switching frequency would increase the switching losses significantly, tighten the cooling requirements,

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and result in greater size of the system, especially vital concern in high-power applications and limited-space environments for conventional PWM techniques. Thus, we try to propose new optimized approaches for SVPWM technique, which move the low-frequency PWM harmonics to high-frequency area with unchanged switching frequency. By changing the original switching state functions of regular center-aligned SVPWM, MSVPWM method is proposed to shift the carrier frequency harmonics to double of that in [3]. Compared with the RPWM technique, the primary benefits of the new optimized approaches include the following.

1) The new optimized approach focuses on eliminating the negative effect caused by carrier frequency PWM harmonics, which could remove the PWM harmonics more effectively.
2) By preventing PWM harmonics from spreading to low-frequency zone, the system resonant frequencies acoustic noise caused by time-varying carrier frequency could be removed and smaller output filter could be employed in VSIs system.

However, MSVPWM could not eliminate the carrier frequency harmonics completely and its PWM harmonics levels are still unacceptable in some applications. Therefore, this article proposed an optimized SVPWM strategy based on single-edge SVPWM, called MS-SVPWM, which could shift the whole carrier frequency noises to double or reduce the average switching frequency by 33% with the same PWM harmonics frequency.

II. Proposed MS-SVPWM Strategy

A. Introduction of the Proposed MS-SVPWM Strategy

There are two common SVPWM algorithms: double-edge SVPWM (triangular carrier) and single-edge SVPWM (sawtooth carrier) including trailing-edge SVPWM and leading-edge SVPWM, as shown in Fig. 1(a) and (c), respectively. $f_a(t)$, $f_b(t)$, and $f_c(t)$ are three-phase reference waves, s_a, s_b, and s_c are three-phase switching states, $V_a(t)$ is phase-A voltage, and T_c is the carrier period. Usually, all switches would be operated once in each carrier cycle. Therefore, the switching times are equal to 6 for conventional SVPWM techniques in a carrier cycle. The proposed MS-SVPWM tries to adjust the order of zero vectors based on single-edge SVPWM to reduce switching times.

For regularly sampled single-edge SVPWM in Fig. 1(c), the switching states of three-phase are 000→100→110→111→000→100→110→111 in two adjacent carrier cycles. Since switching state 000 is equivalent to 111 for the two-level three-phase VSIs, the MS-SVPWM is proposed by adjusting the zero vectors, resulting in three-phase switching states being 000→100→110→111→111→100→110→000, as shown in Fig. 1(d). Its switching states are different in two adjacent carrier cycles, and the average switching times are 4 in a carrier cycle, which is 67% of conventional SVPWM techniques'. In other words, the proposed MS-SVPWM could reduce the average switching frequency by 33% with the same carrier frequency. If the average switching frequency is the same, MS-SVPWM could increase the PWM harmonics frequency by 50%, which could be employed in VSIs to reduce the size of output filters and cancel PWM harmonics.

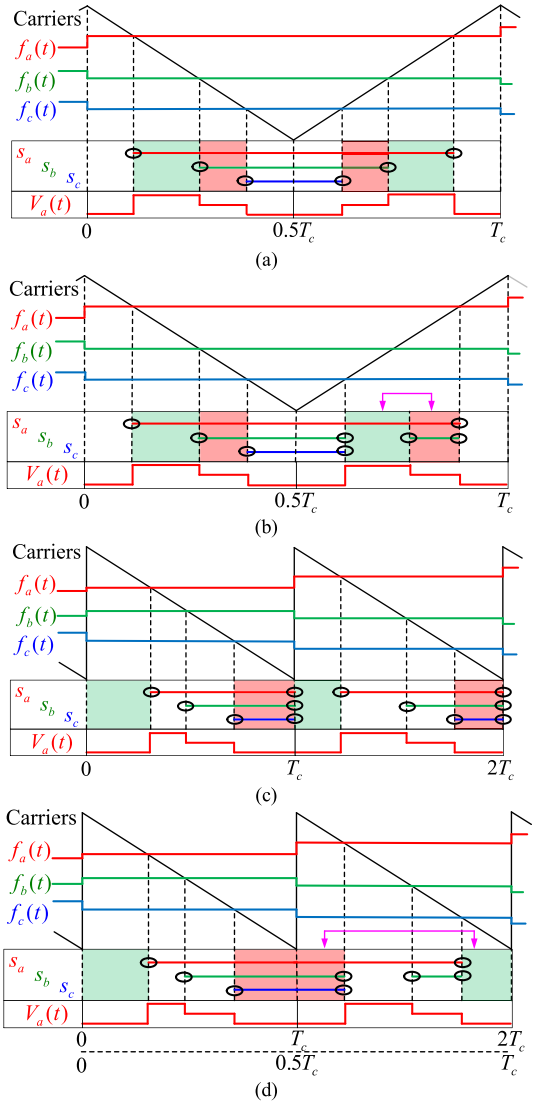

Fig. 1. Three-phase switching states and phase-A voltages of (a) center-aligned SVPWM, (b) MSVPWM, (c) single-edge SVPWM, and (d) MS-SVPWM.

The MSVPWM has been proposed in other paper, as shown in Fig. 1(b). The switching states and phase voltage of MSVPWM and MS-SVPWM are similar by comparing Fig. 1(b) and (d), which makes the innovation of MS-SVPWM confusing. However, MS-SVPWM is different from MSVPWM in aspects of implementation and PWM harmonics distribution. For the sake of comparing MS-SVPWM with MSVPWM, this article regards two adjacent carrier cycles as a new carrier cycle.

The MSVPWM is achieved from center-aligned SVPWM by exchanging the active vectors to shift the carrier frequency PWM harmonics to double at the price of increasing 33% average switching frequency. MS-SVPWM is proposed from single-edge SVPWM by adjusting the active vectors. For MSVPWM, there are still some carrier frequency harmonics remaining.

With the same conditions, MS-SVPWM could remove the carrier frequency harmonics completely. The following PWM harmonics analysis, computer simulation, and experimental results demonstrate these differences clearly.

B. PWM Harmonics Analysis of MS-SVPWM and MSVPWM

Due to the adjustment of zero vectors, three-phase switching states of MS-SVPWM are different compared with the single-edge SVPWM technique in two adjacent carrier cycles. Thus, it is necessary to analyze voltage harmonics components of MS-SVPWM by double Fourier integral and show its advantages in PWM harmonics cancellation compared with that of MSVPWM. The PWM voltage waveform can be alternatively expressed in time-varying form as follows:

$$f(t) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty}(A_{0n}\cos n\omega_0 t + B_{0n}\sin n\omega_0 t) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}[A_{mn}\cos(m\omega_c t + n\omega_0 t) + B_{mn}\sin(m\omega_c t + n\omega_0 t)] \quad (1)$$

where m is the carrier index variable, n is the baseband index variable, ω_c is the carrier angular frequency, ω_0 is the target fundamental angular frequency, A_{mn} and B_{mn} are the amplitudes of the harmonic components coefficients. The first term of (1) corresponds to dc offset component. The second term defines the fundamental waveform and its baseband harmonics. The third term represents the sideband harmonics, which exists as the groups around carrier harmonics frequencies [5]. For MS-SVPWM and MSVPWM technique, the reference wave consists of the sine wave and its third-harmonic [3], all defined as follows:

$$y(t) = M\cos\omega_0 t - p\cos 3\omega_0 t \quad (2)$$

where $M = \frac{2a}{\sqrt{3}}$, $p = \frac{3a}{4\pi}$ and a is the modulation ratio.

By comparing carriers with reference wave, the PWM voltage is produced as a set of square waves with fixed period and varying pulsewidth. The pulsewidth of PWM voltage represents the reference wave value in corresponding carrier cycle. The PWM voltages also could be obtained using the unit cells, as shown in Fig. 2. The naturally sampled single-edge SVPWM samples the reference wave in each cell by the straight line with slope ω_0/ω_c, which is stair-step for the regularly sampled SVPWM.

1) PWM Harmonics of MS-SVPWM: The unit cells and PWM voltages of MS-SVPWM are shown in Fig. 2(a). The amplitude of the harmonic components coefficients with MS-SVPWM $A1_{mn}$ and $B1_{mn}$ are defined as follows:

$$A1_{mn} + jB1_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\frac{\pi}{2}(M\cos y - p\cos 3y - 1)} V_{dc}e^{j(mx+ny+n\gamma x)}dxdy + \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{0}^{\frac{\pi}{2}(M\cos y - p\cos 3y + 1)} V_{\rm dc}e^{j(mx+ny+n\gamma x)}dxdy \quad (3)$$

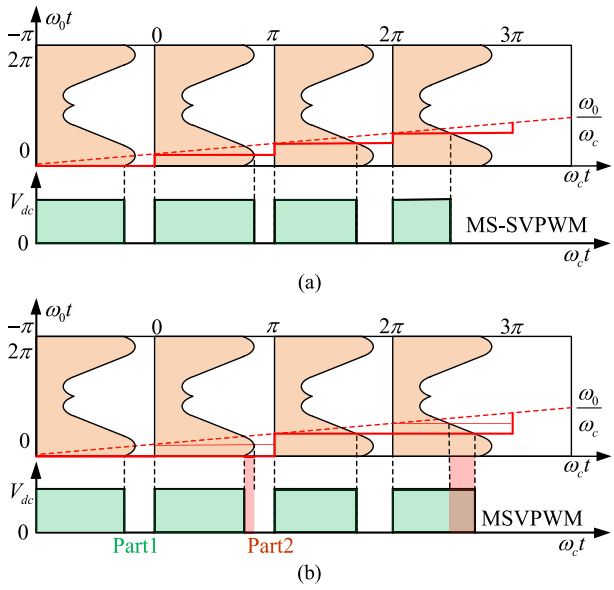

Fig. 2. Unit cells and PWM voltages of (a) the proposed MS-SVPWM and (b) MSVPWM for PWM harmonics analysis.

where $\gamma = \omega_0/\omega_c$. The dc offset in (1) is $A1_{00} = V_{\rm dc}$, when $m = 0$ and $n = 0$. For the baseband harmonics in (1), $A1_{01} = 0.5MV_{\rm dc}$, $A1_{03} = -0.5pV_{\rm dc}$. The harmonic components coefficients of sideband harmonics are as follows:

$$A1_{mn} = \frac{2V_{\rm dc}}{q\pi}\cos m\frac{\pi}{2}\begin{bmatrix} -J_0(q\frac{\pi}{2}M)J_h(q\frac{\pi}{2}p)\sin h\frac{\pi}{2}|_{3h=|n|} + \\ J_0(q\frac{\pi}{2}p)J_k(q\frac{\pi}{2}M)\sin k\frac{\pi}{2}|_{k=|n|} + \\ \sum J_k(q\frac{\pi}{2}M)J_h(q\frac{\pi}{2}p)\sin(k-h) \\ \quad \times\frac{\pi}{2}|_{3h+k=|n|} + \\ \sum J_k(q\frac{\pi}{2}M)J_h(q\frac{\pi}{2}p)\sin(k-h) \\ \quad \times\frac{\pi}{2}|_{|3h-k|=|n|} \end{bmatrix} \quad (4)$$

$$B1_{mn} = -\frac{2V_{\rm dc}}{q\pi}\cos m\frac{\pi}{2}\begin{bmatrix} J_0(q\frac{\pi}{2}M)J_h(q\frac{\pi}{2}p)\cos h\frac{\pi}{2}|_{3h=|n|} + \\ J_0(q\frac{\pi}{2}p)J_k(q\frac{\pi}{2}M)\cos k\frac{\pi}{2}|_{k=|n|} + \\ \sum J_k(q\frac{\pi}{2}M)J_h(q\frac{\pi}{2}p)\cos(k-h) \\ \quad \times\frac{\pi}{2}|_{3h+k=|n|} + \\ \sum J_k(q\frac{\pi}{2}M)J_h(q\frac{\pi}{2}p)\cos(k-h) \\ \quad \times\frac{\pi}{2}|_{|3h-k|=|n|} \end{bmatrix} \quad (5)$$

where $q = m + n\gamma$, function form as $J_h(0.5q\pi p)$ is Bessel function, and h and k are positive integers. For single-edge SVPWM or MS-SVPWM, m is an odd number, then $\cos(0.5m\pi) = 0$ and $A1_{mn} + jB1_{mn} = 0$. Thus, there is no carrier frequency PWM voltage harmonic components in (4) and (5). By substituting the harmonic components coefficients back into (1),

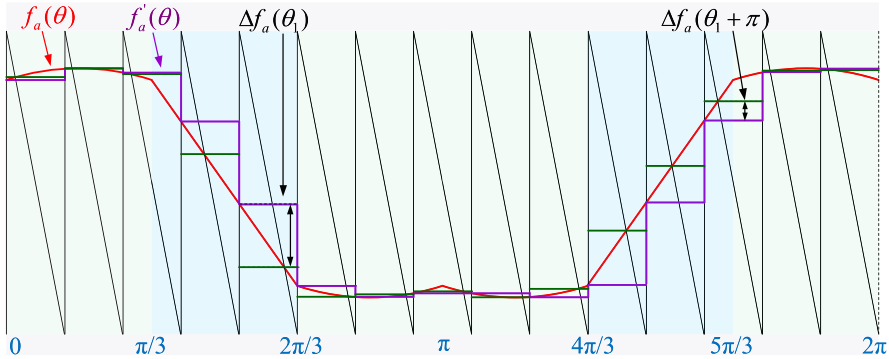

Fig. 3. Ideal reference wave, stair-step reference wave, and carriers of regularly sampled single-edge SVPWM.

the time-varying PWM voltage can be expressed in terms of its harmonic components as follows:

$$u_{an}(t) = \frac{A1_{00}}{2} + A1_{01}\cos\omega_0 t + A1_{03}\cos 3\omega_0 t + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left[A1_{mn}\cos(m\omega_c t + n\omega_0 t) + B1_{mn}\sin(m\omega_c t + n\omega_0 t)\right]. \quad (6)$$

The line voltage u_{ab} is given by

$$u_{ab}(t) = \sqrt{3}A1_{01}\cos(\omega_0 t + \frac{\pi}{6}) - 2\sin\frac{n\pi}{3}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left\{\begin{matrix} A1_{mn}\sin\left[m\omega_c t + n\left(\omega_0 t - \frac{\pi}{3}\right)\right] \\ -B1_{mn}\cos\left[m\omega_c t + n\left(\omega_0 t - \frac{\pi}{3}\right)\right]\end{matrix}\right\}. \quad (7)$$

There are only the second-order carrier frequency harmonics and no carrier frequency harmonics with MS-SVPWM.

2) PWM Harmonics of MSVPWM: The PWM voltage of MSVPWM contains two parts, as shown in Fig. 2(b). Part1 is the same as PWM voltage of MS-SVPWM and part2 is defined by

$$A2_{mn} + jB2_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{\frac{\pi}{2}[M\cos(y-\gamma\pi)-p\cos 3(y-\gamma\pi)+1]}^{\frac{\pi}{2}(M\cos y - p\cos 3y+1)} V_{dc}e^{j(mx+ny+n\gamma x)}dxdy. \quad (8)$$

The coefficients of sideband harmonic components $A2_{mn}$, $B2_{mn}$ are complicated. However, the period of part2 is equal to MSVPWM's carrier period. Thus, there are only carrier frequency harmonics and its multiple harmonics in part2. If carrier ratio is large enough ($\gamma \approx 0$), the coefficients of sideband harmonics components $A2_{mn}$, $B2_{mn}$ are equal to 0 and the part2 will be absent. In this situation, the MSVPWM is the same as MS-SVPWM. In practical applications, MSVPWM could not remove the carrier frequency harmonics completely.

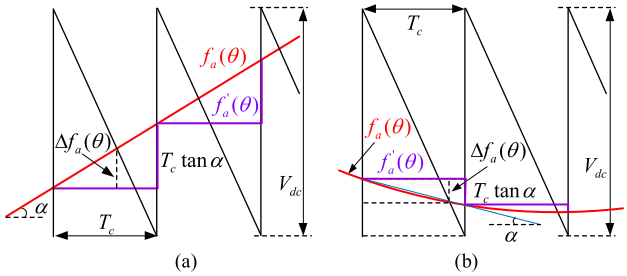

Fig. 4. Diagram of error compensation for MS-SVPWM when θ in (a) [4π/3, 5π/3] and (b) [2π/3, π].

C. Error Compensation to Cancel the Low-Frequency Harmonics

The low-order harmonics components was caused by the unbalanced (not cosine) error between ideal reference wave and stair-step reference wave for regularly sampled single-edge SVPWM. As seen in Fig. 3, the error is $\Delta f_a(\theta) = f_a(\theta) - f'_a(\theta)$, where $f_a(\theta)$ is the ideal reference wave and $f'_a(\theta)$ is the actual reference wave for regularly sampled single-edge SVPWM. Because the stair-step reference wave lacks cosine symmetry, the second and fourth low-order fundamental frequency harmonics are produced by unsymmetrical sampled errors for regularly sampled single-edge SVPWM and MS-SVPWM.

A creative V-carrier PWM method is proposed in [25] to eliminate the low-order harmonics with single-edge PWM for VSIs. Due to the conflict between V-carrier and adjustment of zero vector, the V-carrier PWM is not suitable for the proposed MS-SVPWM. Therefore, an error compensation method is proposed in this section to cancel the low-order harmonics in MS-SVPWM caused by regularly sampled error.

There is no low-order harmonics for naturally sampled single-edge SVPWM technique. Thus, the key point of the error compensation is letting $\Delta f_a(\theta) = 0$ in each carrier cycle. When θ is in [4π/3, 5π/3], the relationships of ideal reference wave $f_a(\theta)$, stair-step reference wave $f'_a(\theta)$ and their difference $\Delta f_a(\theta)$ are shown in Fig. 4(a), where the amplitude of carrier is $V_{\rm dc}$. According to the relationship in Fig. 4(a), the errors satisfy

$$\Delta f_a(\theta) = \frac{3\sqrt{3}a\gamma(V_{\rm dc} - f_a(\theta))}{1 + 3\sqrt{3}a\gamma}. \quad (9)$$

TABLE I
THREE-PHASE REFERENCES ERROR COMPENSATION FOR REGULARLY SAMPLED SINGLE-EDGE SVPWM

Angle	Phase A	Phase B	Phase C
$0 \le \theta \le \frac{\pi}{3}$	$\pi a\gamma \sin(\theta - \frac{\pi}{6})(V_{dc} - f_a(\theta))$	$\frac{3\sqrt{3}a\gamma(V_{dc} - f_b(\theta))}{1+3\sqrt{3}a\gamma}$	$-\pi a\gamma \sin(\theta + \frac{5\pi}{6})(V_{dc} - f_c(\theta))$
$\frac{\pi}{3} \le \theta \le \frac{2\pi}{3}$	$-\frac{3\sqrt{3}a\gamma(V_{dc} - f_a(\theta))}{1-3\sqrt{3}a\gamma}$	$\pi a\gamma \sin(\theta - \frac{\pi}{2})(V_{dc} - f_b(\theta))$	$-\pi a\gamma \sin(\theta + \frac{\pi}{2})(V_{dc} - f_c(\theta))$
$\frac{2\pi}{3} \le \theta \le \pi$	$-\pi a\gamma \sin(\theta + \frac{\pi}{6})(V_{dc} - f_a(\theta))$	$\pi a\gamma \sin(\theta - \frac{5\pi}{6})(V_{dc} - f_b(\theta))$	$\frac{3\sqrt{3}a\gamma(V_{dc} - f_c(\theta))}{1+3\sqrt{3}a\gamma}$
$\pi \le \theta \le \frac{4\pi}{3}$	$-\pi a\gamma \sin(\theta - \frac{\pi}{6})(V_{dc} - f_a(\theta))$	$-\frac{3\sqrt{3}a\gamma(V_{dc} - f_b(\theta))}{1-3\sqrt{3}a\gamma}$	$\pi a\gamma \sin(\theta + \frac{5\pi}{6})(V_{dc} - f_c(\theta))$
$\frac{4\pi}{3} \le \theta \le \frac{5\pi}{3}$	$\frac{3\sqrt{3}a\gamma(V_{dc} - f_a(\theta))}{1+3\sqrt{3}a\gamma}$	$-\pi a\gamma \sin(\theta - \frac{\pi}{2})(V_{dc} - f_b(\theta))$	$\pi a\gamma \sin(\theta + \frac{\pi}{2})(V_{dc} - f_c(\theta))$
$\frac{5\pi}{3} \le \theta \le 2\pi$	$\pi a\gamma \sin(\theta + \frac{\pi}{6})(V_{dc} - f_a(\theta))$	$-\pi a\gamma \sin(\theta - \frac{5\pi}{6})(V_{dc} - f_b(\theta))$	$-\frac{3\sqrt{3}a\gamma(V_{dc} - f_c(\theta))}{1-3\sqrt{3}a\gamma}$

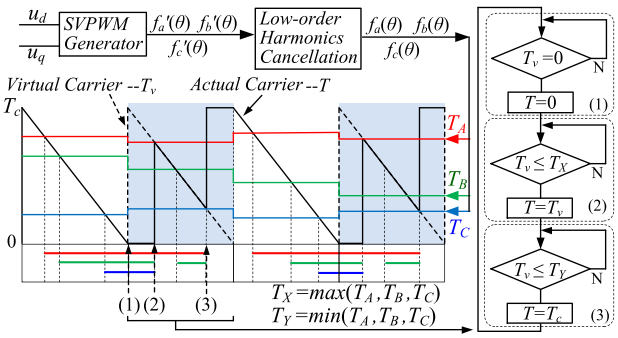

Fig. 5. Diagram of the proposed MS-SVPWM implementation.

When θ is in [2π/3, π], the relationship of ideal reference wave $f_a(\theta)$, stair-step reference wave $f_a'(\theta)$ and their difference $\Delta f_a(\theta)$ are shown in Fig. 4(b). The error $\Delta f_a(\theta)$ is defined as follows:

$$\Delta f_a(\theta) = \pi\gamma a \sin\left(\theta + \frac{\pi}{6}\right)(V_{\rm dc} - f_a(\theta)). \qquad (10)$$

The error compensation of three-phase reference waves are shown in Table I. Thanks to the improvement of MCU's computation speed, the multiplication and trigonometry in Table I only cost small amount of computation and the whole compensated program is less than 150 instruction cycles in each PWM cycle. The second- and fourth-order fundamental frequency harmonics could be equivalent to third-order harmonics in *D–Q* axis system, where error could be compensated with modulation parameters simply.

D. Implementation of MS-SVPWM

The proposed MS-SVPWM could be implemented easily in MCU according to the diagram in Fig. 5. The stair-step reference waves $f_a'(\theta)$ $f_b'(\theta)$ $f_c'(\theta)$ are produced by *SVPWM generator*. The module *low-order harmonics cancellation* is employed to eliminate the errors between ideal reference waves $f_a(\theta)$ $f_b(\theta)$ $f_c(\theta)$ and stair-step reference waves, where $f_a(\theta)$ $f_b(\theta)$ $f_c(\theta)$ also could be expressed as PWM duties T_A T_B T_C. The carrier period is T_c, actual carrier value is T, and virtual carrier value used to aid the process is T_v. Each other actual carrier is adjusted to implement the MS-SVPWM based on the following rules, which are shown as the flowchart in Fig. 5.

1) If the period register of virtual carrier T_v is equal to zero, the period register of actual carrier T is set to zero.
2) If the period register of virtual carrier T_v is less than the maximum value in three reference waves, the period register of actual carrier T is equal to T_v.
3) When the period register of virtual carrier T_v is less than the minimum value in three-phase reference waves, the actual carrier T is equal to carrier period T_c.

PWM signals are generated by comparing of three-phase reference waves and the actual carriers. The topology of VSI is the same as the conventional VSI employing SVPWM and there is no additional circuit in driving system.

TABLE II
MAIN PARAMETERS OF SVPWM, MSVPWM AND MS-SVPWM

Techniques	Carrier Fre	Switching Fre	Lowest PWM Fre
SVPWM	4.0 kHz	4.0 kHz	4.0 kHz
MSVPWM	3.0 kHz	4.0 kHz	3.0 kHz
MS-SVPWM	3.0 kHz	4.0 kHz	6.0 kHz

III. COMPARISON OF SVPWM, MSVPWM, AND THE PROPOSED MS-SVPWM

In this section, the switching losses and PWM harmonics of SVPWM, MSVPWM, and the proposed MS-SVPWM are compared. The dc-link voltage is equal to 100 V, average switching frequency is 4.0 kHz, and the fundamental frequency is 100 Hz, as shown in Table II.

A. PWM Voltage Harmonics

Fig. 6 shows the line voltage harmonics spectrum of center-aligned SVPWM, MSVPWM, and the proposed MS-SVPWM, when modulation ratio is equal to 0.9. The switching frequency of center-aligned SVPWM is constant 4.0 kHz. Thus, its lowest

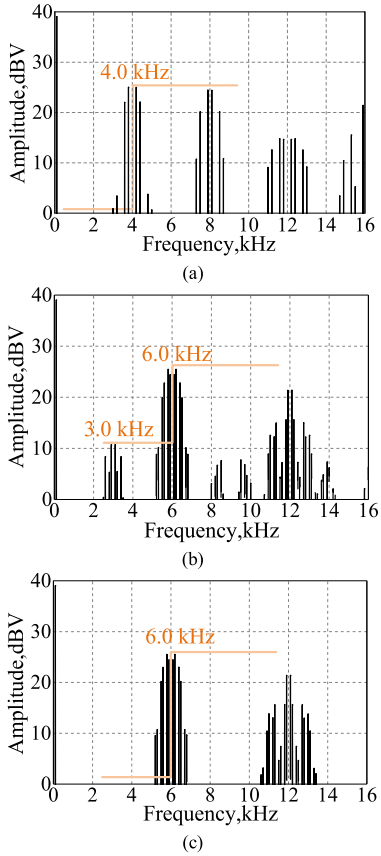

Fig. 6. Line voltage harmonics spectrum with (a) center-aligned SVPWM, (b) MSVPWM, and (c) MS-SVPWM strategy when modulation ratio is 0.9, and average switching frequency is 4.0 kHz.

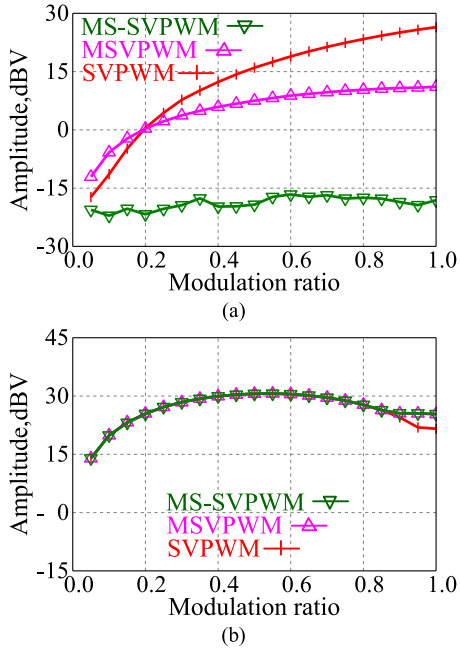

Fig. 7. Comparison of (a) first and (b) second-order carrier frequency PWM harmonics amplitudes in line voltage with center-aligned SVPWM, MSVPWM, and MS-SVPWM.

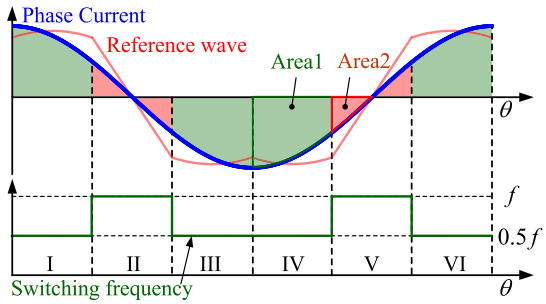

Fig. 8. Switching frequency and phase current when phase angle is 0°.

frequencies of PWM harmonics are around 4.0 kHz, as illustrated in Fig. 6(a). Varying switching frequency of MSVPWM and MS-SVPWM is equal to the carrier frequency or double, and the average switching frequency is also 4.0 kHz. As seen in Fig. 6(b), MSVPWM could remove the most PWM harmonics around 3.0 kHz significantly, which depends largely on carrier ratio. However, the left carrier frequency PWM harmonics may be still unacceptable in some applications.

For results of MS-SVPWM in Fig. 6(c), there is no PWM harmonics around 3.0 kHz. The lowest frequencies of PWM harmonics are about 6.0 kHz, which is 150% of that employing the center-aligned SVPWM.

The first- and second-order carrier frequency PWM harmonics varying with modulation ratio employing center-aligned SVPWM, MSVPWM, and MS-SVPWM techniques are shown in Fig. 7(a) and (b). For these three approaches, the trends and levels of second-order carrier frequency PWM harmonics are almost the same. As seen in Fig. 7(a), in order of SVPWM, MSVPWM, and MS-SVPWM technique, the amplitudes of carrier frequency harmonics gradually decrease. For MS-SVPWM, the levels of carrier frequency PWM harmonics are below –15 dBV.

B. Switching Losses and Phase Angle

The instantaneous switching energy losses are dependent on the amplitude of the load current through the switches at the switching moments [27], [28]. The switching losses in one arm are proportional to the area defined by sine wave and angle axis with constant switching frequency. Fig. 8 shows the switching frequency and reference wave of the same phase for the proposed MS-SVPWM technique when phase angle is equal to 0. The switching frequency is half of conventional SVPWM technique in sectors I, III, IV, and VI, where the phase current is around its maximum value. Thus, the switching losses in Area1 of Fig. 8 are half of conventional SVPWM technique and that in Area2 is the same as conventional SVPWM technique. In this situation, MS-SVPWM technique could reduce about 43.3% switching losses compared with conventional SVPWM by calculation.

Because the phase current peak is gradually moving away from the half switching frequency zone varying with the increase of phase angle, the switching losses reduction of MS-SVPWM technique also decreases until phase angle is equal to 90°, as shown in Fig. 9. The reduction of switching losses is equal to 25% when phase angle is equal to 90°.

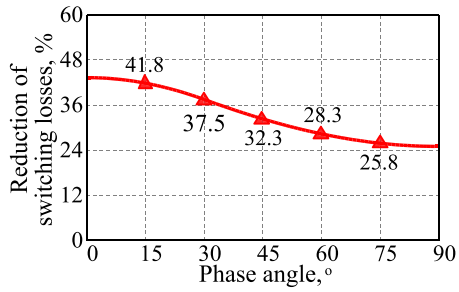

Fig. 9. Reduction of switching losses varying with phase angle from 0° to 90°.

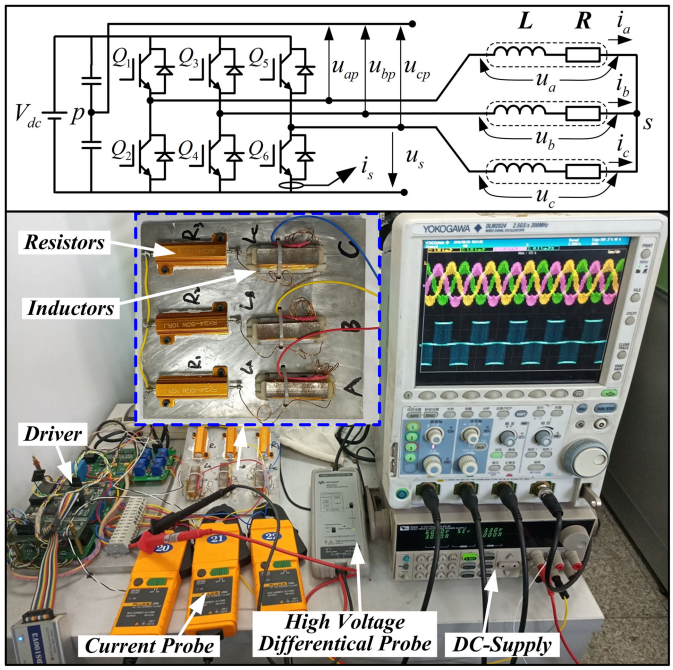

Fig. 10. Diagram and photograph of experimental platform.

TABLE III
SPECIFICATION AND PARAMETER OF SYSTEM

Specification and Parameter	Value
DC-link Voltage	60 V
Fundamental Frequency	100 Hz
Phase Resistance	10.0 Ω
Phase Inductance	0.48 mH
Switching Frequency	4.0 kHz
Modulation ratio	0.9

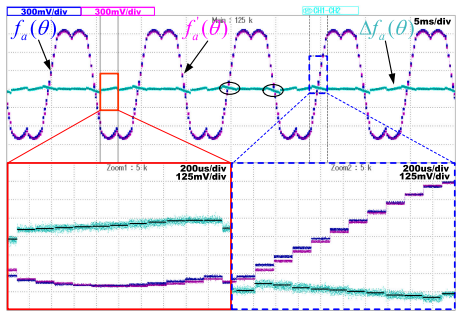

Fig. 11. Phase-A reference wave without and with error compensation.

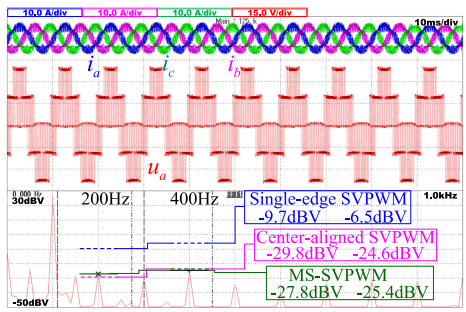

Fig. 12. Comparison of low-order harmonics levels with single-edge SVPWM, center-aligned SVPWM and MS-SVPWM.

IV. Experimental Validations and Analysis

In this section, the *RL* load driven by the two-level VSI experimental system has been implemented to verify the capability of MS-SVPWM in reducing switching frequency and increasing the PWM harmonics frequency practically.

The photograph and diagram of experimental platform is shown in Fig. 10. The voltage u_s and current i_s of insulated gate bipolar transistor (IGBT) in phase-C low-arm are measured to demonstrate the switching process with different PWM techniques. The phase voltage and phase currents are measured by high voltage differential probe and currents probes, respectively.

The specification and parameters of experimental system are shown in Table III. The average switching frequency of SVPWM, MSVPWM, and MS-SVPWM is 4.0 kHz. The carrier frequency of SVPWM is 4.0 kHz and 3.0 kHz for MSVPWM and MS-SVPWM. The following results of fast Fourier transform show the power spectrum amplitude of phase voltage and phase current. The sampling frequency in oscilloscope is 125 kHz.

A. Low-Order Harmonics Cancellation

As analyzed in the previous section, there are low-order harmonics components with the regularly sampled single-edge SVPWM-based techniques. An error compensation method is proposed with MS-SVPWM to eliminate the low-order harmonics, which compensates the error between ideal reference wave and stair-step reference wave.

The stair-step reference wave, compensated reference wave, and the errors are demonstrated in Fig. 11. Obviously, the errors lack cosine symmetry and the second, fourth-order fundamental frequency harmonics are produced in phase voltage. The reference wave after compensation is the same as that of naturally sampled single-edge SVPWM, which would not generate the low-order harmonics.

The levels of low-order harmonics employing regularly sampled single-edge SVPWM, center-aligned SVPWM and MS-SVPWM are shown in Fig. 12. Their average switching frequency is 6.0, 4.0, and 4.0 kHz, respectively. For regularly sampled single-edge SVPWM, the level of the second- and fourth low-order harmonics is –9.7 and –6.5 dBV. With error compensation in three-phase reference waves, the level of the

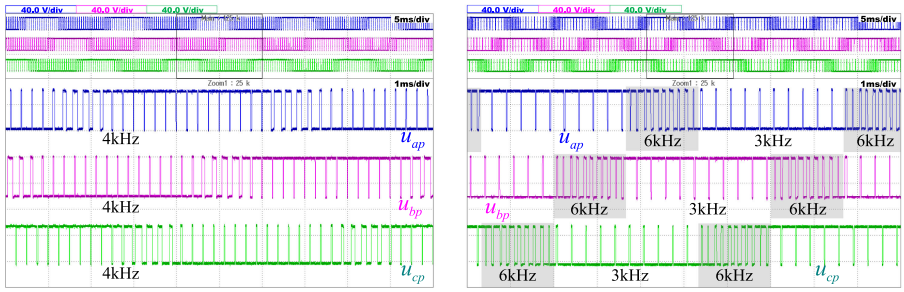

Fig. 13. Pole voltages with (a) center-aligned SVPWM, and (b) MSVPWM and MS-SVPWM.

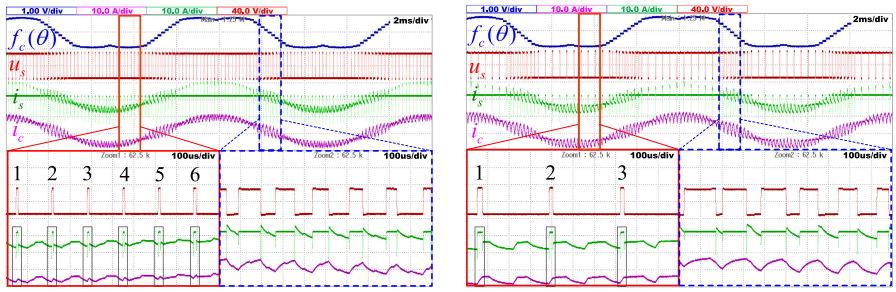

Fig. 14. Reference wave, phase current, collector current, and collector-to-emitter voltage of IGBT in phase-C lower arm with (a) center-aligned SVPWM and (b) MS-SVPWM.

second- and fourth low-order harmonics is –27.8 and –25.4 dBV, reduced by more than 18 dBV, whose levels are similar with that of center-aligned SVPWM technique.

B. Comparison of Switching Frequency

Three-phase pole voltages of SVPWM, MSVPWM, and MS-SVPWM are shown in Fig. 13. For center-aligned SVPWM in Fig. 13(a), the switching frequency is evenly distributed in a fundamental cycle. Due to the adjustment of switching states for MSVPWM and MS-SVPWM, the switching frequency in one phase arm is 6.0 kHz, in other two phase arms is 3.0 kHz and the average switching frequency is $(1 \times 6\ \text{kHz} + 2 \times 3\ \text{kHz})/3 = 4\ \text{kHz}$, as shown in Fig. 13(b).

In order to compare the details of switching process with center-aligned SVPWM and MS-SVPWM, the collector current i_s and collector-to-emitter voltage u_s of IGBT in phase-C, phase current, and reference wave are shown in Fig. 14, when phase angle of load is equal to 1.8°. These figures are zoomed at the position where phase current is around maximum value and zero-crossing. As seen in Fig. 14(a), for the center-aligned SVPWM, the switching frequency is always 6 kHz. For MS-SVPWM in Fig. 14(b), when phase current is around maximum value, where the switching loss is maximum in the switching action, the switching frequency is 3 kHz. The switching frequency is 6 kHz when phase current is around zero-crossing. Thus, the switching losses reduction for MS-SVPWM is more than 33% with the same PWM harmonics until phase angle is larger than 30°.

C. Comparison of PWM Harmonics

The phase voltage, phase current, and their harmonics MS-SVPWM are shown in Figs. 15 and 16. The levels of first- and second-order carrier frequency harmonics in phase voltage, phase current are compared in Table IV. The average switching frequency of all techniques is equal to 4.0 kHz.

The MSVPWM could reduce the amplitude of carrier frequency harmonics by 14.1 dBV in phase voltage and 12.6 dBA in phase current compared with center-aligned SVPWM. The results of MS-SVPWM are shown in Figs. 15(c) and 16(c). The level of carrier frequency PWM harmonics is decreased by 33.7 dBV and 32.8 dBA in phase voltage and phase current, respectively, compared with that of center-aligned SVPWM, which is similar to the background harmonics. The levels of second-order carrier frequency harmonics employing MSVPWM and MS-SVPWM are almost equal to that of center-aligned SVPWM.

As seen in Figs. 15 and 16, MSVPWM could reduce the carrier frequency harmonics significantly. However, some are still left. There is no carrier frequency harmonics with the proposed MS-SVPWM. These experimental results confirm that the lowest frequencies of PWM harmonics employing MS-SVPWM (6.0 kHz) increase 50% compared with that of center-aligned SVPWM (4.0 kHz) with the same average switching frequency.

Phase-A current and voltage using center-aligned SVPWM, MSVPWM, and MS-SVPWM are enlarged in Fig. 17(a), (b), and (c), respectively. As seen in Fig. 17(a), the period of main harmonics in phase-A current is 250 μs, and their frequency is around 4.0 kHz. For MSVPWM and MS-SVPWM technique, the frequency of main harmonics in phase voltage and phase current is around 6.0 kHz, which is double of the carrier frequency.

There are two similar phase voltage waveforms, whose frequency is equal to double carrier frequency, in a carrier cycle for

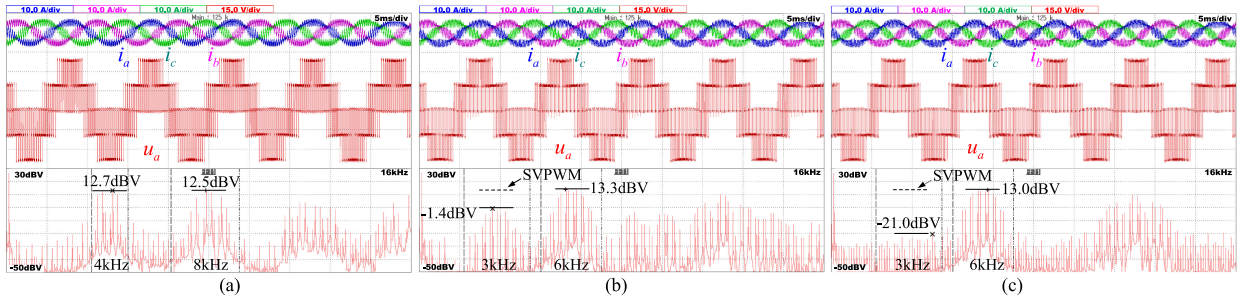

Fig. 15. Phase voltage harmonics spectrum with (a) center-aligned SVPWM, and (b) MSVPWM, and (c) MS-SVPWM.

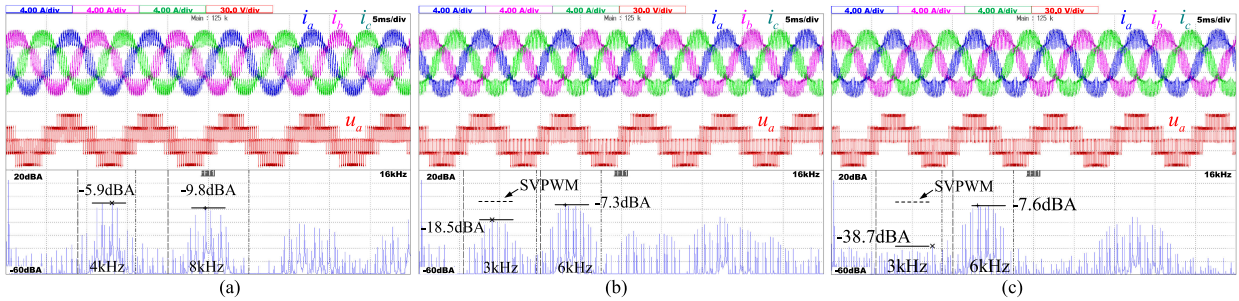

Fig. 16. Phase current harmonics spectrum with (a) center-aligned SVPWM, (b) MSVPWM, and (c) MS-SVPWM.

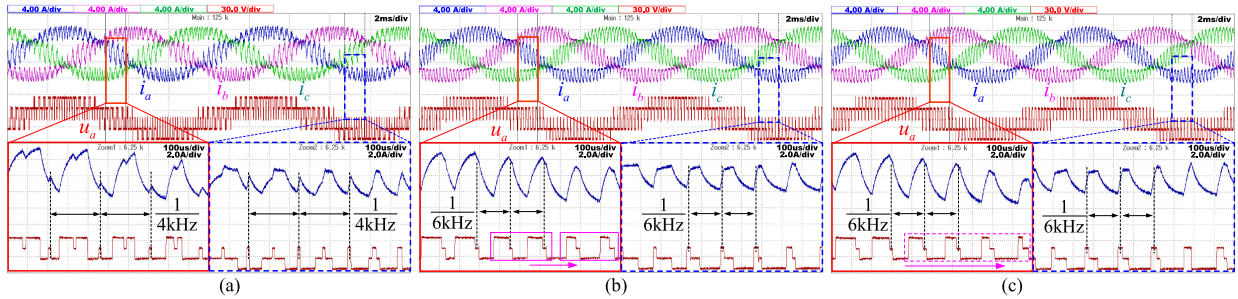

Fig. 17. Enlarged figure of phase voltage and phase current with (a) center-aligned SVPWM, (b) MSVPWM, and (c) MS-SVPWM.

TABLE IV
COMPARISON OF LEVELS OF PWM HARMONICS WITH SVPWM, MSVPWM, AND MS-SVPWM

Techniques		SVPWM	MSVPWM	MS-SVPWM
Phase voltage	1st order	12.7 dBV	-1.4 dBV	-21 dBV
	2nd order	12.5 dBV	13.3 dBV	13.0dBV
Phase current	1st order	-5.9 dBA	-18.5 dBA	-38.7 dBA
	2nd order	-9.8 dBA	-7.3 dBA	-7.6 dBA

and (c). Each phase voltage waveform of MS-SVPWM varies with the modulation ratio and electrical angle. However, two phase voltage waveforms of MSVPWM in a carrier cycle are identical. The two correlated phase voltage waveforms contain the carrier frequency harmonics. Thus, MSVPWM could not eliminate the carrier frequency harmonics completely. Compared with MSVPWM, MS-SVPWM could almost eliminate the carrier frequency harmonics with the same switching losses.

D. Analysis of MS-SVPWM With the Experimental Results

The proposed MS-SVPWM could reduce the switching losses and increase the PWM harmonics frequency. However, the relationship between reducing switching losses and increasing PWM harmonics frequency is confusing. Thus, some experiments have been done to further analyze and demonstrate MS-SVPWM strategy.

1) Same Average Switching Frequency: The PWM harmonics in phase voltage employing SVPWM and MS-SVPWM with the same average switching frequency are compared in Fig. 18(a). The PWM harmonics frequencies with MS-SVPWM are all above 6.0 kHz, which increases by 33% compared with that of SVPWM technique. For applications with inductive loads, the higher frequency of PWM voltage harmonics means lower level of noises in current or smaller size of output filters.

2) Same PWM harmonics frequencies distribution: In Fig. 18(b), the average switching frequency of MS-SVPWM (4.0 kHz) is 67% of that of SVPWM (6.0 kHz) when their PWM harmonics frequencies are the same. Compared with

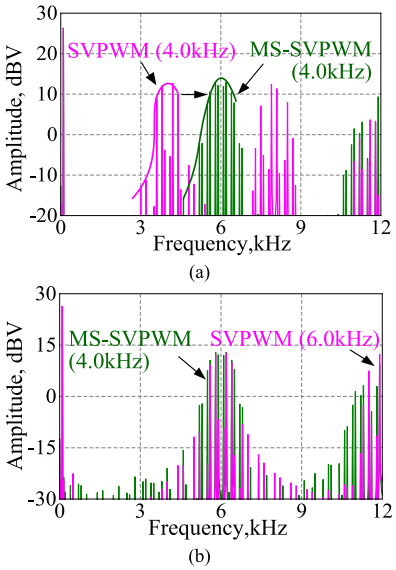

Fig. 18. PWM harmonics in phase voltage of center-aligned SVPWM and MS-SVPWM with (a) the same average switching frequency, and (b) the same PWM harmonics frequencies distribution.

SVPWM, the MS-SVPWM could remain the same levels of PWM harmonics and reduce switching frequency by 33%.

V. Conclusion

This article proposed the MS-SVPWM technique by adjusting the zero vectors for three-phase VSIs to reduce the switching losses and increase the PWM harmonics frequency. The PWM voltage harmonics of MS-SVPWM and MSVPWM are analyzed and compared by double Fourier integral, which verifies MS-SVPWM could eliminate the carrier frequency PWM harmonics completely but not for MSVPWM.

When the average switching frequency of MS-SVPWM is equal to SVPWM's, the MS-SVPWM could increase the PWM harmonics frequency by 50%. With the same PWM harmonics frequency distribution of SVPWM technique, the MS-SVPWM would reduce average switching frequency by 33%, and the switching losses could be reduced by more than 33% or 25% when phase angle is less than 30° or 60°, respectively. The suitable switching frequency of MS-SVPWM could be selected based on the requirement in practical applications to balance the reduction of switching losses and the increment of PWM harmonics frequency. The idea may be applicable in multilevel and multiphase VSIs.

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