Limit-Cycle-Free Digitally Controlled DC–DC Converters Based on Dyadic Digital PWM

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***Abstract*—Quantization-induced limit cycle oscillations (LCOs) in digitally controlled dc–dc converters are addressed in this article. The novel dyadic digital pulsewidth modulator is proposed to increase the effective pulsewidth modulator resolution, as required for LCO-free operation, at low cost, without sacrificing dc accuracy and with no detrimental effects on the ripple voltage. Experimental results on a synchronous buck validate the approach highlighting effective LCOs' suppression and dc accuracy enhancement at 5× reduced peak output voltage ripple and up to 16-dB lower frequency harmonic component reduction compared to thermometric dithering for the same resolution increase.**

***Index Terms*—Digital control of power converters, dithering, dyadic digital pulse modulation (DDPM), dyadic digital pulsewidth modulation (DDPWM), high-resolution pulsewidth modulation, limit cycle oscillations (LCOs).**

I. Introduction

DIGITAL control of electronic power converters presents several key advantages compared to traditional analog control [1], [2], since it enables much simpler implementation of advanced algorithms, low sensitivity to component tolerances, full hardware reconfigurability, high flexibility/design reuse, and reduced time to market [3]–[8], which ultimately reduce costs and make digital control the preferred choice in most application domains.

In spite of the above unquestionable advantages, the accuracy and the transient response of digital power converters can be impaired by their inherent quantization [9], which may also lead to unwanted low-frequency limit cycle oscillations (LCOs) [10], [11], not found in analog controlled converters. These issues are in great part related to the limited resolution of the digital pulsewidth modulator (DPWM), which is, therefore, very critical. Unfortunately, in a standard counter-comparator DPWM, the duty cycle resolution is proportional to the system clock cycle and inversely proportional to the switching frequency. As a consequence, high DPWM resolution is traded off with the counter clock frequency and, hence, with power consumption [2], and the problem is exacerbated at high switching frequencies, which are enabled by advanced semiconductors (SiC and GaN) and are highly desirable to reduce the size of passive elements and, hence, to increase power density [12], [13].

In this scenario, specific techniques for DPWM resolution enhancement have been proposed at the hardware level, and alternative approaches for high-resolution LCO-free DPWMs have been the subject of extensive research [9]–[11], [14], [15]. Most of the proposed solutions, however, result either in a degraded dc accuracy and/or in an increased cost and complexity.

Ring oscillators and delay-line-based high-resolution DPWMs, in particular, achieve subclock cycle resolution by employing a set of delay elements and require a large silicon area, and their performance is strongly dependent on supply, temperature, and manufacturing process variations [16]–[21]. Hybrid architectures, which combine together the counter and the delay line approaches, result in a reduced occupied area even though they have the same sensitivity from environmental and implementation parameters of previous solutions [22], [23]. The DPWM resolution, in addition, can also be enhanced with other hardware-based techniques, among which the multiphase pulsewidth modulators and interleaved converters should be cited [24], [25].

In order to enhance the DPWM resolution without increasing the digital clock rate, digital techniques consisting of the variation of the duty cycle of one least significant bit (LSB) over predefined dithering patterns have been proposed so as to control the average duty cycle with a sub-LSB resolution [10], [26], [27]. Dithering is inexpensive and amenable of a simple digital implementation, but, unfortunately, it may introduce noise at switching frequency subharmonics, which cannot be properly rejected by the converter output filter and generally leads to relevant subswitching frequency output ripple.

Among dithering methods, the sigma–delta ($\Sigma\Delta$) DPWM techniques have proven to be effective to increase resolution, but they operate at slow conversion speed, and the feedback loop nonlinearity is responsible for the generation of low-frequency idle tones inducing additional ripple in the output voltage [28]–[32].

More recently, the dyadic digital pulsewidth modulation (DDPWM) technique, based on the dyadic digital pulse modulation (DDPM) [33]–[35], has been proposed in [36] as a

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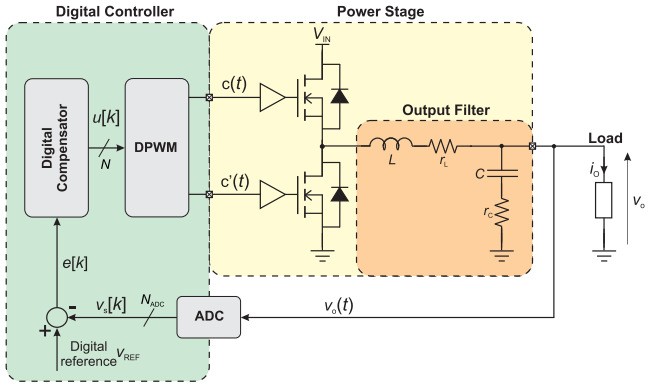

Fig. 1. Digitally controlled synchronous buck dc–dc converter with the PID compensator.

systematic approach to achieve accurate LCO-free operation in a digital power converter at negligible cost and design effort. In this article, more insight into the frequency- and time-domain characteristics of the new DDPWM technique in open-loop and closed-loop power converters is provided both analytically and by extensive experimental validation, which reveal increased digital power converter resolution with reduced output voltage ripple and no transient response degradation.

The rest of this article is organized as follows. In Section II, the role played by the DPWM resolution in the onset of LCOs in digitally controlled power converters is revised, and the conventional thermometric dithering technique is introduced. In Section III, the high-resolution DDPWM technique is proposed starting from the DDPM technique in [33], and the advantages in terms of spectral and time-domain characteristics compared to the thermometric dithering are highlighted in Section IV. The results presented in Sections III and IV are experimentally validated in Section V with reference to a synchronous buck converter digitally controlled by a specifically designed field-programmable gate array (FPGA)-based test setup. Experimental results highlight effective LCO suppression and dc accuracy enhancement at $5\times$ reduced output voltage ripple compared to thermometric dithering at the same resolution and with no transient performance degradation. Finally, Section VI concludes this article.

II. Onset of LCOs

A synchronous buck dc–dc converter operated at $f_\mathrm{s} = 1/T_\mathrm{s}$ switching frequency with a digital proportional–integral–derivative (PID) compensator, whose block diagram is reported in Fig. 1, is considered in the following to discuss the onset of quantization-induced LCOs and then to introduce the proposed LCO-free operation technique.

With reference to Fig. 1, the output voltage $v_\mathrm{O}(t)$ of the buck is converted into a digital stream $v_\mathrm{s}[k] = v_\mathrm{O}(kT_\mathrm{s})$ by an analog-to-digital converter (ADC) at $1/T_\mathrm{s}$ sample rate with a resolution

$$q_\mathrm{ADC} = \frac{V_\mathrm{FS}}{2^{N_\mathrm{ADC}}} \tag{1}$$

where $[0, V_\mathrm{FS}]$ is the ADC input range, and N_ADC is the number of bits of the converter. The digital error signal, $e[k] = v_\mathrm{REF} - v_\mathrm{s}[k]$, where v_REF is the constant digital reference, is fed to the PID compensator, which drives a DPWM clocked at $f_\mathrm{clk} = 1/T_\mathrm{clk}$. Since both the switching period $T_\mathrm{s} = KT_\mathrm{clk}$ and the active period $T_\mathrm{ON} = HT_\mathrm{clk}$ $(H, K \in \mathbb{N})$ are constrained to be integer multiples of T_clk, the duty cycle turns out to be quantized over $K = T_\mathrm{s}/T_\mathrm{clk}$ levels, resulting in a dc output voltage resolution

$$q_\mathrm{DPWM} = V_\mathrm{IN}\frac{T_\mathrm{clk}}{T_\mathrm{s}} = \frac{V_\mathrm{IN}}{K} \tag{2}$$

with V_IN being the input voltage.

Based on [10], a sufficient condition for the LCO-free operation is achieved when the following requirements are met at the same time.

1) The Nyquist stability criterion under large-signal conditions is respected.
2) The integral control coefficient is not zero.
3) The ADC quantization bin is larger than the LSB of the DPWM, so that at least one of the quantized dc output voltages $n/K \cdot V_\mathrm{IN}$ at a fixed duty cycle n/K falls in the zero-error bin of the controller, i.e.,

$$q_\mathrm{ADC} > q_\mathrm{DPWM}. \tag{3}$$

Such conditions are, therefore, normally taken as LCO-free design criteria.

While the first two requirements can be met by design with convenient PID coefficients, (3) is related just to the resolution of the ADC (q_ADC) and of the DPWM (q_DPWM) [8]. Assuming, for the sake of simplicity, that V_IN matches the input swing of the ADC and replacing the expressions of q_DPWM and q_ADC from (2) and (1) in (3), the last condition for the LCO-free operation requires that

$$2^{-N_\mathrm{ADC}} = \frac{q_\mathrm{ADC}}{V_\mathrm{IN}} > \frac{1}{K} = \frac{f_\mathrm{s}}{f_\mathrm{clk}}. \tag{4}$$

Meeting (4) results in a stringent tradeoff between f_s, f_clk, and N_ADC, which limits the dc accuracy of the buck converter at high switching frequency f_s for a given digital clock frequency f_clk and/or imposes operation at inconveniently high clock frequency f_clk to achieve a target static accuracy at high switching frequency f_s.

For example, for an $f_\mathrm{clk} = 5\,\mathrm{MHz}$ system clock and an $f_\mathrm{s} = 100\,\mathrm{kHz}$ switching frequency, the resolution of the ADC, and, hence, the dc accuracy of the converter, is limited by (4) to 5 bits or less, which is not acceptable for most practical purposes. Conversely, operating at switching frequencies in the 10-MHz range, which are enabled by emerging GaN and SiC power semiconductors, a dc accuracy equivalent to $N_\mathrm{ADC} = 8$ bit or more requires impractically high digital clock frequencies exceeding 2 GHz.

A. High-Resolution PWM Techniques

Adopting the thermometric dithering approach illustrated in Fig. 2 to increase the DPWM resolution, the digitally quantized duty cycle is $(n+1)/2^N$ in the first m switching periods of a 2^M dithering pattern and $n/2^N$ in the remaining periods, so that an average duty cycle $(n \cdot 2^M + m)/2^{N+M}$ quantized over

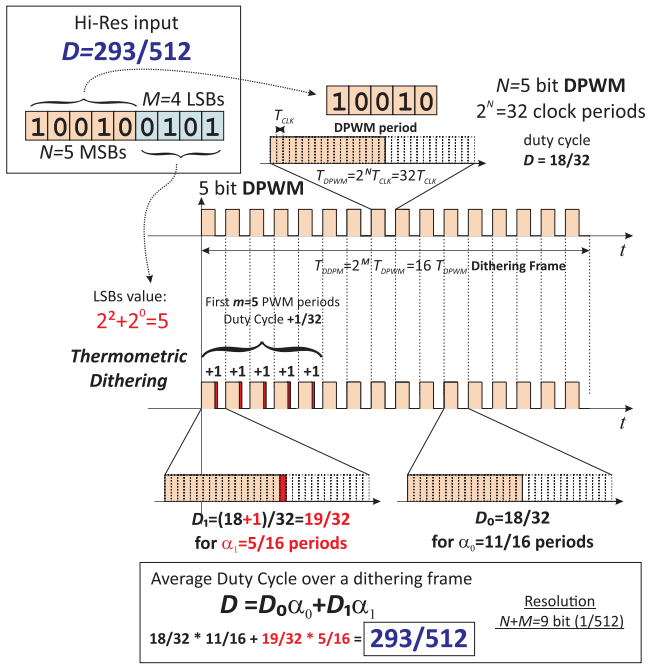

Fig. 2. High-resolution DPWM by thermometric duty cycle dithering over 2^M switching periods.

$N + M$ bits can be achieved, thus increasing the effective DPWM resolution by M bits. As mentioned in Section I, this technique may introduce noise at switching frequency subharmonics.

While empirically optimized dithering patterns [10] and $\Sigma\Delta$ modulation can be adopted to mitigate these issues, the new, deterministic, DDPWM approach is proposed in this article to achieve resolution enhancement at lower ripple and dynamic performance degradation compared to thermometric dithering.

III. High-Resolution Dyadic Digital Pulsewidth Modulation

The DDPWM adopted in this article to overcome the limitations of previous dithering techniques is based on the DDPM introduced in [33] and illustrated in the following with reference to Fig. 3.

A. Dyadic Digital Pulse Modulation

The DDPM modulation associates to any binary number m, represented on M bits in terms of its binary digits $b_i \in \{0, 1\}, i = 0 \dots M-1$, as

$$m = \sum_{i=0}^{M-1} b_i 2^i$$

the 2^M bit long digital stream

$$\Sigma_m(t) = \sum_{i=0}^{M-1} b_i S_i(t), \quad 0 < t < T_0 \tag{5}$$

obtained by superposition of the dyadic basis signals $S_i(t)$ for $i = 0 \dots M-1$, which include exactly 2^i digital "ones" separated by $2^{M-i} - 1$ digital "zeros," arranged so that to be orthogonal (i.e., $S_i(t) \cdot S_j(t) = 0 \; \forall i \neq j$), as illustrated in Fig. 3(a). Since "one" pulses in a dyadic basis signal $S_i(t)$ are exactly 2^i and are nonoverlapping, it follows that $\Sigma_m(t)$ includes a number of "one" pulses equal to m and has a mean value of $(m/2^M)V_{\text{IN}}$.

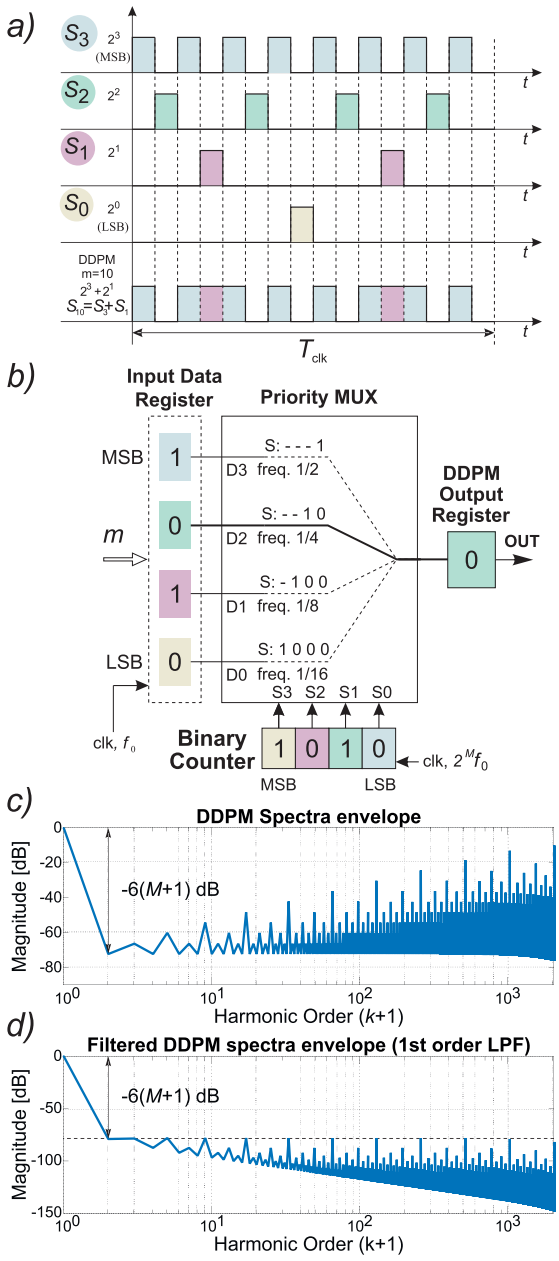

Fig. 3. DDPM [33]. (a) DDPM pattern. (b) DDPM modulator hardware. (c) Envelope of the spectra of the different 4096 DDPM patterns at 12-bit resolution. (d) Spectral envelope as in (c) after first-order filtering.

Moreover, following [33], the spectrum of the DDPM signal in (5) can be expressed as

$$X_m^{\text{DDPM}}(f) = \sum_{k=-\infty}^{+\infty} a_k c_{k,m} \delta(f - k f_0) \tag{6}$$

where $f_0 = 1/T_0$

$$a_k = \frac{1}{2^M}\text{sinc}\left(\frac{k}{2^M}\right)\text{e}^{-\frac{jk\pi}{2^M}} \tag{7}$$

and

$$c_{k,m} = \sum_{i=0}^{M-1} b_{i,m}2^i \sum_{p=0}^{2^{M-i}-1}(-1)^p\delta\left[k-2^i p\right] \tag{8}$$

$\delta[\cdot]$ is the Kronecker function defined as

$$\delta[n] = \begin{cases} 1, & n = 0 \\ 0, & n \neq 0. \end{cases} \tag{9}$$

Looking at the envelope of the spectra of DDPM signals in (6) for different m, i.e.,

$$S(kf_0) = \max_m \left|X_m^{\text{DDPM}}(kf_0)\right| \tag{10}$$

which is reported in Fig. 3(c) for $M = 12$ bit, it can be observed that the ac spectral components of DDPM streams are concentrated at high frequencies and can be easily filtered out. In detail, looking at (8), the dominant spectral components of a DDPM stream are found to be at $k = 2^h$, $h = 0\ldots(M-1)$ harmonics, increase with k with a slope of 20 dB/dec, and can be kept $-6(M+1)$dB below the dc by a first-order filter with a cutoff frequency $f_c = f_0/\sqrt{3}$, as illustrated in Fig. 3(d).

B. Dyadic Digital Pulse Modulator

The DDPM streams discussed above can be generated by simple digital hardware, i.e., a priority multiplexer (PMUX) driven by a binary counter, as shown in Fig. 3(b).

The PMUX is a combinational network with $2 \cdot M$ inputs, i.e., M data inputs $D_{M-1}\cdots D_0$ and M selection inputs $S_{M-1}\cdots S_0$, and one output OUT, and it implements the Boolean function

$$OUT = \sum_{i=0}^{M-1} D_{M-i-1}\cdot S_i \cdot \prod_{k=0}^{i-1}\overline{S_k} \tag{11}$$

where sums and products are intended as Boolean OR and AND operators, respectively. In other words, in the PMUX, the digital output OUT takes the value of the bit D_{M-k} of the data input, with k being the index of the first "one" in the selection inputs starting from the LSB (i.e., bits $k-1\ldots0$ are all zeros). It is assumed that $OUT = 0$ if all selection inputs are zero.

The data inputs of the PMUX are fed by the input data register, which samples the input codes m at frequency f_0, while the selection inputs are connected to a free-running M-bit binary counter operated at the clock frequency $2^M f_0$.

Every other clock period (i.e., 2^{M-1} times in a full count), $S_0 = 1$ and the output OUT takes the value of D_{M-1}. In the other counting periods, i.e., when $S_0 = 0$, in one half of the cases (i.e., 2^{M-2} times in a full count), $S_1 = 1$ and the output OUT is forced to the logic value of D_{M-2}. By similar arguments, the output OUT is driven in a full counting period to the value of D_i exactly 2^i times according with the DDPM pattern in Fig. 3(a).

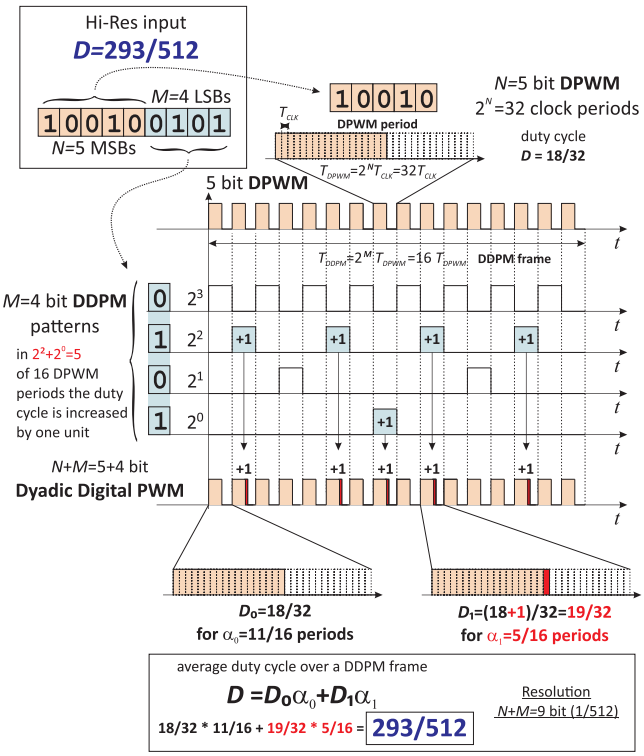

Fig. 4. $N+M$ bit DDPWM technique to increase the effective resolution of N bit DPWM to $N+M$ bits by M-bit DDPM dithering over 2^M periods.

C. Dyadic Digital Pulsewidth Modulation

In this article, the DDPWM technique is adopted to increase the effective resolution of an N-bit DPWM to $N+M$ bits, so as to achieve LCO-free operation without trading off switching frequency and dc accuracy in a dc–dc converter.

According to the proposed technique, the duty cycle of a DPWM signal is modulated between two adjacent quantization levels, i.e.,

$$D_0 = \frac{n}{2^N}$$

and

$$D_1 = D_0 + 1\text{LSB}_{\text{DPWM}} = \frac{n+1}{2^N}$$

where n is the value represented in the first N MSBs of the input, according to the M-bit DDPM pattern, which corresponds to the integer m represented by the last M LSBs of the digital input, as shown in Fig. 4. Since a duty cycle D_0 is applied $2^M - m$ times and a duty cycle D_1 is applied m times over a pattern of 2^M switching periods, the average duty cycle over 2^M periods is

$$D = \frac{n}{2^N}\frac{2^M-m}{2^M} + \frac{n+1}{2^N}\frac{m}{2^M} = \frac{n\cdot 2^M + m}{2^{N+M}} \tag{12}$$

and corresponds to the value of the digital input $n\cdot 2^M + m$ quantized over 2^{N+M} levels.

In practice, the proposed DDPWM technique can be implemented replacing the DPWM module in the digitally controlled dc–dc converter in Fig. 1 by the DDPWM in Fig. 5, which is

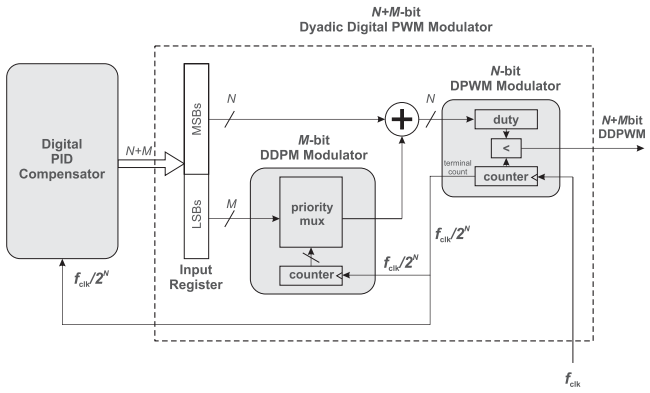

Fig. 5. Architecture of the proposed DDPWM.

operated at the same clock frequency $f_{\rm clk}$ and includes an N-bit DPWM and an M-bit DDPM modulator as in Fig. 3. Thanks to DDPWM, the output voltage can be quantized at $N+M$ bit resolution, making it possible to meet the LCO-free operation condition (3) with $+M$-bit ADC resolution and increase the overall output accuracy with respect to plain DPWM.

IV. Frequency- and Time-Domain Analysis

Compared to conventional dithering techniques, such as thermometric dithering, the increased resolution is achieved by DDPWM at minimum output ripple and dynamic performance degradation due to the spectral characteristics of DDPWM signals, which will be analyzed and discussed in what follows in both frequency and time domains.

A. Spectrum of an $N+M$ DDPWM Signal

An $N+M$ bit DDPWM signal $x_{n,m}^{\rm DDPWM}(t)$ can be expressed as

$$x_{n,m}^{\rm DDPWM}(t) = x_n^{\rm DPWM}(t) + \hat{x}_{m,n}^{\rm DDPM}(t) \tag{13}$$

where

$$\hat{x}_{m,n}^{\rm DDPM}(t) = x_m^{\rm DDPM}(t)\left[x_{n+1}^{\rm DPWM}(t) - x_n^{\rm DPWM}(t)\right] \tag{14}$$

in which $x_{n+1}^{\rm PWM}(t) - x_n^{\rm PWM}(t)$ is the difference between the DPWM waveforms with $(n-1)/2^N$ and $n/2^N$ duty cycles, i.e., a stream of one-clock-period pulses at frequency $f_{\rm s}$ delayed of $nT_{\rm s}/2^N$ and $x_m^{\rm DDPM}(t)$ is a DDPM signal with unit-time slot $T_{\rm S}$ and period $T_0 = 2^M \cdot T_{\rm S}$, as shown in Fig. 4. The same signal $\hat{x}_{m,n}^{\rm DDPM}(t)$ can also be conveniently described as a DDPM signal with unit-time slot $T_{\rm S}$, where unit pulses $\Pi_{T_{\rm s}}(t)$ are replaced with time-scaled and delayed pulses $\Pi_{\frac{T_{\rm S}}{2^N}}(t - \frac{n}{2^N}T_{\rm s})$.

Based on (13), the spectrum of $x_{n,m}^{\rm DDPWM}(t)$ can be expressed as

$$X_{n,m}^{\rm DDPWM}(f) = X_n^{\rm DPWM}(f) + \hat{X}_{m,n}^{\rm DDPM}(f) \tag{15}$$

where the first term

$$X_n^{\rm DPWM}(f) = \frac{n}{2^N}\sum_{k=-\infty}^{+\infty} \operatorname{sinc}\left(\frac{kn}{2^N}\right) {\rm e}^{-\frac{\jmath\pi kn}{2^N}}\delta\left(f - kf_{\rm s}\right) \tag{16}$$

is the spectrum of an N-bit DPWM signal at frequency $f_{\rm S}$ with constant duty cycle $n/2^N$ and

$$\hat{X}_{n,m}^{\rm DDPM}(f) = \sum_{k=-\infty}^{+\infty} b_{k,n}c_{k,m}\delta\left(f - k\frac{f_{\rm s}}{2^M}\right) \tag{17}$$

where $c_{k,m}$ are the coefficients of the DDPM sequence spectrum defined in (8), and

$$b_{k,n} = \frac{1}{2^{N+M}}\operatorname{sinc}\left(\frac{k}{2^{N+M}}\right){\rm e}^{-\frac{\jmath\pi k\left(2^N+n\right)}{2^{M+N}}} \tag{18}$$

describes period-by-period duty cycle variations and is closely related to the spectrum of a DDPM signal in Fig. 3(c).

B. Spectrum of an $N+M$ Thermometric Dithering Signal

By the same approach adopted in (13), a thermometric dithering signal can be expressed as

$$x_{n,m}^{\rm TH}(t) = x_n^{\rm DPWM}(t) + \hat{x}_{m,n}^{\rm TH,DITH}(t) \tag{19}$$

where

$$\hat{x}_{m,n}^{\rm TH,DITH}(t) = x_m^{\rm DPWM,T_0}(t)\left[x_{n+1}^{\rm DPWM}(t) - x_n^{\rm DPWM}(t)\right] \tag{20}$$

where $x_m^{\rm DPWM,T_0}(t)$ is a DPWM signal with period $T_0 = 2^M T_{\rm s}$ and duty cycle $m/2^M$.

The spectrum of $x_{n,m}^{\rm TH}(t)$ can be, therefore, written as

$$X_{n,m}^{\rm TH}(f) = X_n^{\rm DPWM}(f) + \hat{X}_{n,m}^{\rm TH,DITH}(f) \tag{21}$$

where $X_n^{\rm DPWM}(f)$ is expressed as in (16) and

$$\hat{X}_{n,m}^{\rm TH,DITH}(f) = \sum_{k=-\infty}^{+\infty} b_{k,n}d_{k,m}\delta\left(f - k\frac{f_{\rm s}}{2^M}\right) \tag{22}$$

in which $b_{k,n}$ has the same expression as in (18), and

$$d_{k,m} = \frac{m}{2^M}\operatorname{sinc}\left(\frac{km}{2^M}\right){\rm e}^{-\frac{\jmath\pi km}{2^M}}. \tag{23}$$

C. Comparison of Spectral Characteristics

Based on the above analysis, the dc component of $\hat{X}_{n,m}^{\rm DDPM}(f)$ in (15) and of $\hat{X}_{n,m}^{\rm TH,DITH}(f)$ in (21) corrects the dc value of $X_n^{\rm DPWM}(f)$ as demanded to achieve an increased $(N+M)$-bit resolution. At the same time, the other spectral components result in tones at subharmonics $kf_{\rm s}/2^M$ for $k = 0\ldots 2^M-1$ of the switching frequency, whose fundamental frequency $f_{\rm s}/2^M$ decreases exponentially with the resolution enhancement M so as to approach the passband of the output filter and cause output voltage ripple.

While, in thermometric dithering, the amplitude of subharmonic tones is maximum at lower order harmonics and is a monotonically decreasing function of k, as dictated by $d_{k,m}$ in (23), the amplitude of the same tones in DDPWM increases with k, as dictated by the behavior of $c_{k,m}$ in (8), and shown in Fig. 3(c) and (d). As a consequence, DDPWM provides better distribution of the baseband subswitching frequency spectral energy toward high frequencies, where the attenuation of the output filter is higher.

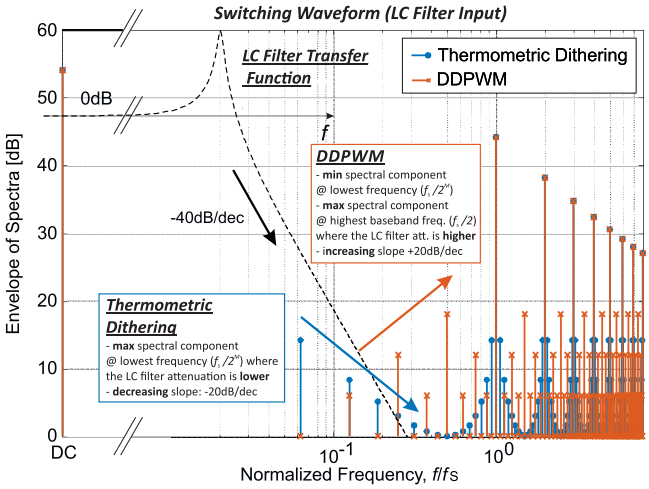

Fig. 6. Envelope of the spectra of $N = 4$-bit DPWM with $M = 5$ bit thermometric dithering over 2^M periods as in Fig. 2 and of $N + M$ DDPWM patterns.

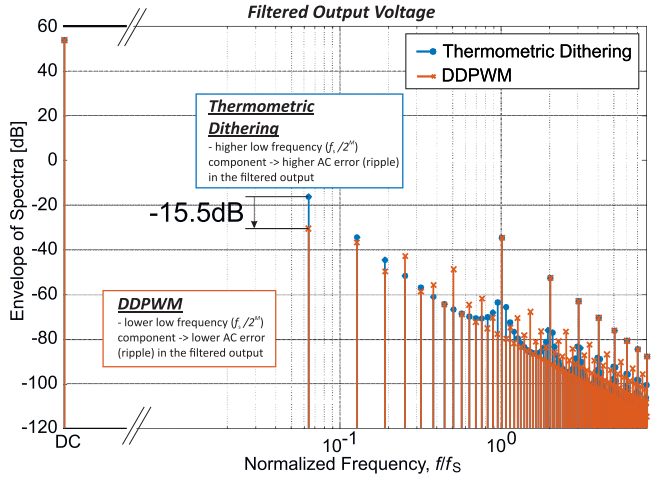

Fig. 7. Envelope of the spectra of $N = 4$-bit DPWM with $M = 5$ bit thermometric dithering over 2^M periods as in Fig. 2 and of $N + M$ DDPWM patterns, filtered by a second-order LC filter, as in the buck converter in Fig. 1, with corner frequency $2 \times 10^{-2} f_s$.

The favorable spectral properties of DDPWM streams can be observed in Fig. 6, where the envelope of the spectra of DDPWM and thermometric dithering patterns for the same $M = 5$ bit increased resolution are compared. In particular, it can be observed that DDPWM shows minimum energy at lowest frequency harmonic components, which are closer to the passband of the LC filter and give a particularly critical contribution to the output voltage ripple. From the same figures, it can be observed that DDPWM effectively results in improved output accuracy as far as the lowest frequency spurious component at frequency $f_s/2^M$ is above the cutoff frequency f_c of the output filter. In other words, DDPWM can be adopted to achieve an output resolution enhancement, expressed in bits, up to

$$M_{\max} = \left\lfloor \log_2 \left(\frac{f_s}{f_c} \right) \right\rfloor \tag{24}$$

where $\lfloor \cdot \rfloor$ is the floor rounding operator.

As a consequence, for the same LC filter, adopting DDPWM results in significantly lower baseband spurious, as shown in Fig. 7, and, hence, in a lower ripple under all possible quantized duty cycle values, as shown by the simulation results in Fig. 8, where a reduction of 6× in the worst-case peak ripple, which corresponds to a 15.5-dB reduction in the lowest spectral component of Fig. 7, is observed.

D. Time-Domain Analysis and Transient

Since the PID compensator output in a power converter featuring DDPWM is updated every switching period as in a plain N-bit DPWM, and not once over dithering patterns when adopting thermometric or $\Sigma\Delta$ dithering, the adoption of DDPWM is expected not to affect the transient performance compared to plain N-bit DPWM.

Moreover, comparing the open-loop step response of a true high-resolution DPWM converter and of a DDPWM converter with sub-DPWM LSB duty cycle step change at time $t = 0$,

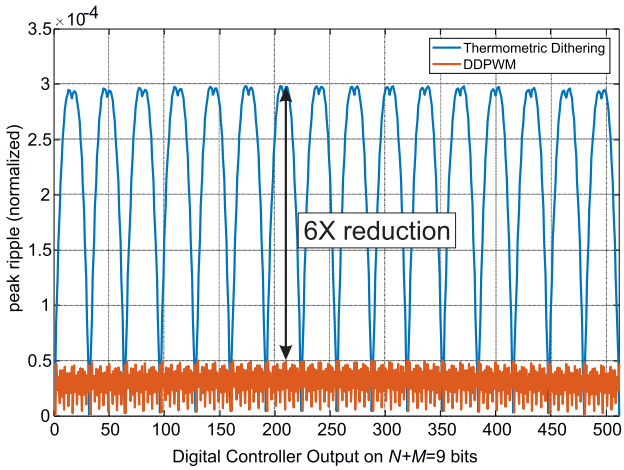

Fig. 8. Simulated dithering-induced ripple voltage in the open-loop configuration (normalized with respect to the dc output voltage) versus high-resolution duty cycle by $M = 5$ bit thermometric dithering (see Fig. 2) and by $N = 4$-bit and $M = 5$ bit DDPWM (see Fig. 4).

which are reported in Fig. 9, it can be observed that the amount of additional delay introduced in DDPWM depends on the phase of the DDPM counter in correspondence of the step transition and is, in any case, higher for smaller step changes (up to 16 switching cycles in the worst case for 1/16 DPWM LSB output change) and lower for more relevant output changes (one switching period worst-case delay for 1/2 DPWM LSB output change). This peculiar characteristic of DDPWM gives rise to lower relative transient errors for relevant output changes, as observed in Fig. 10, and an optimal response time–accuracy tradeoff under transient conditions.

Based on frequency- and time-domain analysis, the unique features of DDPWM make it possible to achieve increased output resolution and LCO-free operation without output ripple and dynamic performance degradation, thus resulting in a net improvement at negligible hardware and software cost.

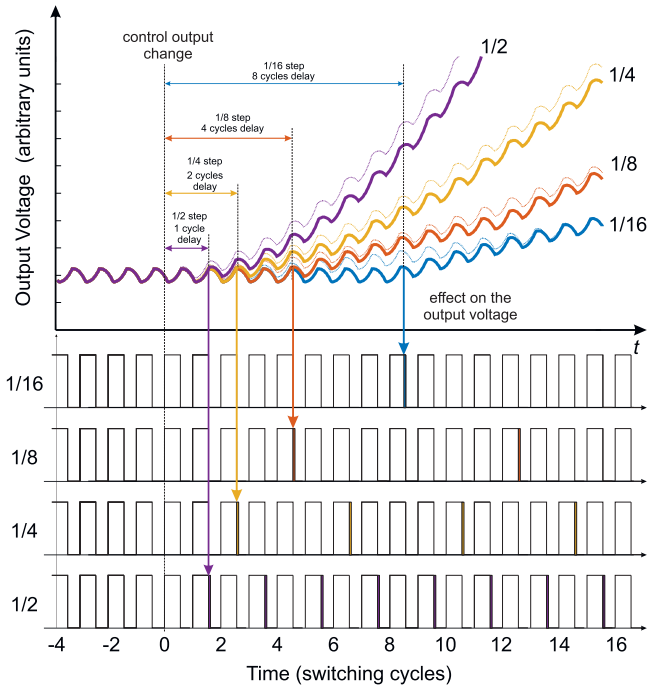

Fig. 9. Simulated open-loop transient response of the output voltage of the buck converter featuring $N = 5$ and $M = 4$ DDPWM compared to ideal transient under fractional duty cycle step changes corresponding to the different LSBs (1/2, 1/4, 1/8, and 1/16).

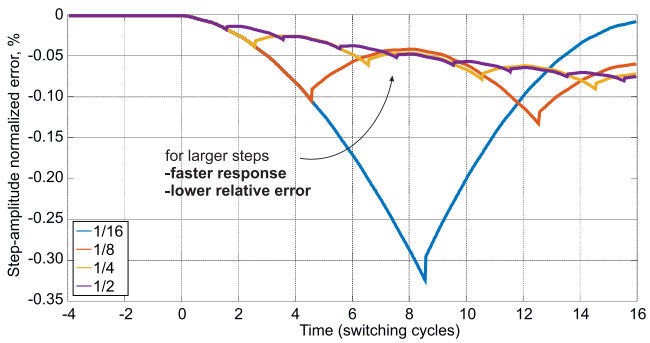

Fig. 10. Step amplitude normalized error between the DDPWM and the ideal transient waveforms considered in Fig. 9.

V. Experimental Results

To validate the proposed approach, a two-layer printed circuit board has been specifically designed to accommodate the power stage in Fig. 1 with the parameters listed in Table I, while the digital control algorithm has been implemented on an Altera prototyping board [37] by referring to the parallel implementation form of the PID compensator [8]. Compensator gains are also reported in Table I and have been computed to get a crossover frequency of 5 kHz with a phase margin of $\varphi = 55^\circ$.

The testbench for the experimental verification of the algorithm has been designed using a system-on-chip (SOC) approach, which, in the same integrated circuits, combines an embedded high-performance general processor and a large amount of programmable logic. Such an SOC-based testbench has been adopted to easily experiment with different ADC and DPWM

TABLE I
Synchronous Buck: Power Stage and PID Controller Parameters

Quantity	Symbol	Unit	Value
Input Voltage	V_{IN}	V	10
Output Voltage	V_{O}	V	5.12
Switching Frequency	f_{s}	kHz	100
Filter Inductance	L	μH	100
Inductace Series Resistance	r_{L}	mΩ	56
Filter Capacitance	C	μF	220
Capacitor Equivalent Series Resitance	r_{C}	mΩ	90
PID Proportional Gain	k_{P}	–	2.6781
PID Integral Gain	k_{I}	–	0.0408
PID Derivative Gain	k_{D}	–	6.5019

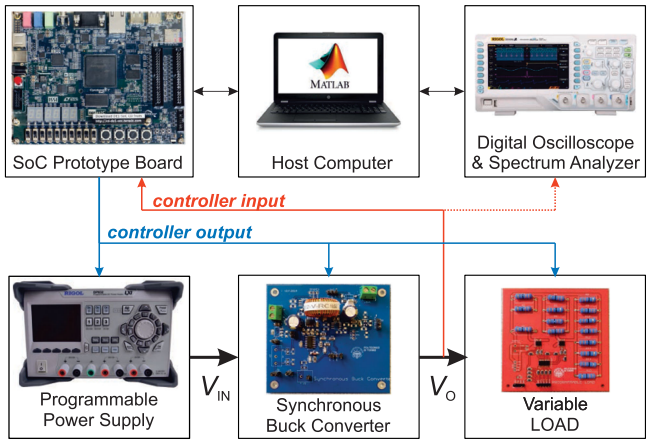

Fig. 11. Block diagram of the experimental testbench.

settings without major hardware changes and by a user-friendly interface. It is worth to be observed, however, that the DDPWM technique introduced in this article can be conveniently implemented in low-cost microcontrollers in software or takes advantage of a custom DDPM modulator hardware peripheral, which could possibly be available in future microcontrollers at negligible area overhead [34].

A. Experimental Test Setup

The block diagram of the testbench is reported in Fig. 11 and includes the synchronous buck power converter introduced before and an Altera DE1-SOC prototyping board [37], which operates as a programmable digital controller. The board contains a dual-core hard processor ARM-based system and an FPGA in a single chip and a 12-bit ADC. The testbench also includes a digitally programmable power supply, a digitally programmable resistive load, and a four-channel digital oscilloscope. The FPGA configuration and the embedded processor code are downloaded from a host computer in a configuration phase. The FPGA comprises an interface to the ADC, which acquires the input and output voltages of the synchronous buck, a PID controller (or compensator), whose gain coefficients may be externally programmed, and a DPWM, which can be configured by a multiplexer (MUX) so that to implement plain N-bit DPWM, $N + M$-bit DDPWM (architecture in Fig. 5) or thermometric dithering over 2^M switching cycles.

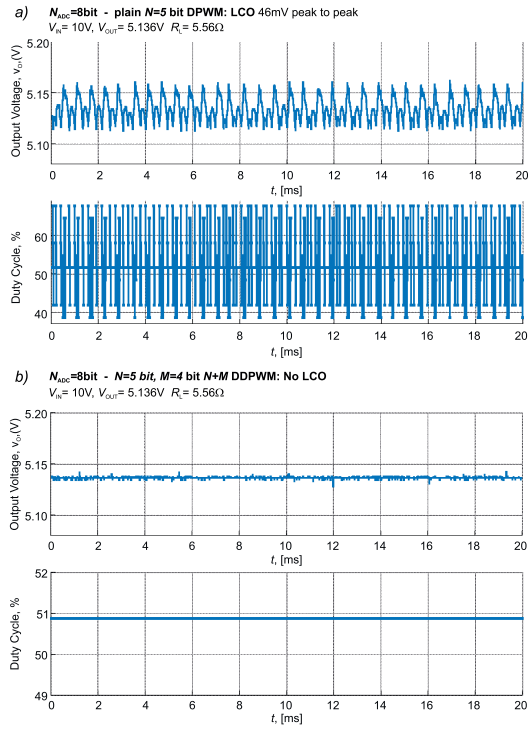

Fig. 12. Output voltage waveforms and duty cycle waveforms of the synchronous buck at $f_s = 100\,\text{kHz}$ switching frequency and $f_{clk} = 3.2\,\text{MHz}$ digital clock frequency for $N_{ADC} = 8$ (a) using plain DPWM at $N = 5$ bit resolution and resulting in LCOs, and (b) using $N + M$ bit DDPWM with $N = 5$ and $M = 4$, revealing LCO suppression.

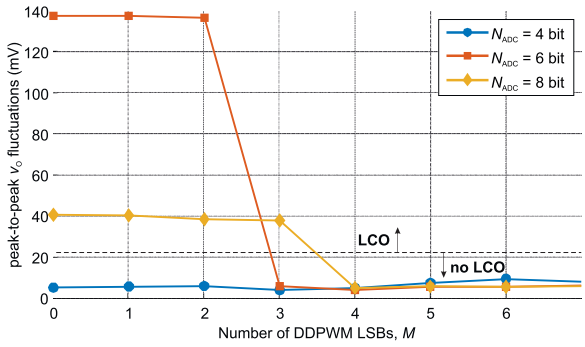

Fig. 13. Amplitude of LCOs for $N + M$-DDPWM with $N = 5$ under different values of M for $N_{ADC} = 4$, $N_{ADC} = 6$, and $N_{ADC} = 8$, open-circuit load.

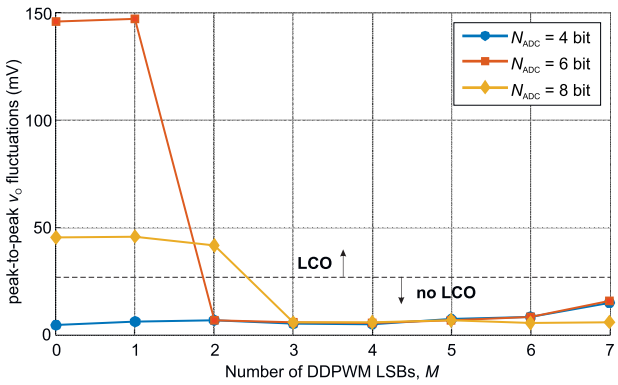

Fig. 14. Amplitude of LCOs for $N + M$-DDPWM with $N = 5$ under different values of M for $N_{ADC} = 4$, $N_{ADC} = 6$, and $N_{ADC} = 8$, $I_O = 1\,\text{A}$ load current.

The PID coefficients, the MUX, and the DPWM control signals are provided by the embedded processor through a digital interface. The application software on the embedded processor runs on the Linux operating system, which provides access to all the system peripherals of the board and can be interfaced to a host computer running MATLAB through a dedicated data server. A MATLAB script may be used to run a sequence of experiments with different converter parameters, to acquire the corresponding data, to process them, and to display parametrically the results.

B. Experimental Results

The synchronous buck converter has been extensively tested to validate the results on the DDPWM technique. In particular, its effectiveness in suppressing LCOs and in increasing the effective output resolution is first considered. Then, the measured output ripple is compared with thermometric dithering in both time and frequency domains. Finally, the measured load transient response of the converter is discussed.

1) LCO Suppression and DC Accuracy: The effectiveness of DDPWM in suppressing LCOs is experimentally verified in Fig. 12. In Fig. 12(a), in particular, the output voltage of the buck converter with an $N_{ADC} = 8$ bit ADC operated at $f_s = 100\,\text{kHz}$ switching frequency by a plain DPWM clocked at $f_{clk} = 3.2\,\text{MHz}$, resulting in an $N = 5$ bit DPWM resolution, not meeting the LCO-free operation condition (3), is reported. Significantly, 46-mV peak-to-peak amplitude LCOs can be observed consistently with the theory [10]. By contrast, in Fig. 12(b), an LCO-free operation is observed under the same $N_{ADC} = 8$ bit ADC resolution, switching frequency, and digital clock rate by using $N + M$ DDPWM with $N = 5$ and $M = 4$.

The same tests have been performed for an ADC resolution $N_{ADC} = 4$, $N_{ADC} = 6$, and $N_{ADC} = 8$ under different number of bits of the dyadic modulator M ($M = 0$ being plain DPWM). The corresponding experimental results are summarized in Figs. 13 and 14 for an open-circuit load and for a 1-A output current, respectively.

The results reveal a reduced LCO amplitude for $N_{ADC} = 8$ while increasing M, up to a complete LCO suppression from $M = 4$ for open-circuit load and from $M = 3$ for 1-A load current. For $N_{ADC} = 6$, the complete LCO suppression is achieved starting from $M = 3$ ($M = 2$) for open-circuit load (1-A load current) as expected from (4) in view of the reduced ADC resolution. From the same figures, it can also be observed that increasing M above 6 results in higher output ripple due to the lowest DDPWM ripple component below the output LC filter cutoff frequency, consistently with (24) that yields $M_{max} = 6$ for a switching frequency of 100 kHz and an LC filter cutoff frequency of 1 kHz.

Finally, for $N_{ADC} = 4$, the LCO-free operation is achieved also for plain DPWM (i.e., $M = 0$), but at the cost of a coarse output voltage regulation, as shown in Fig. 15. Looking at Fig. 15, by contrast, it can be observed that the LCO-free

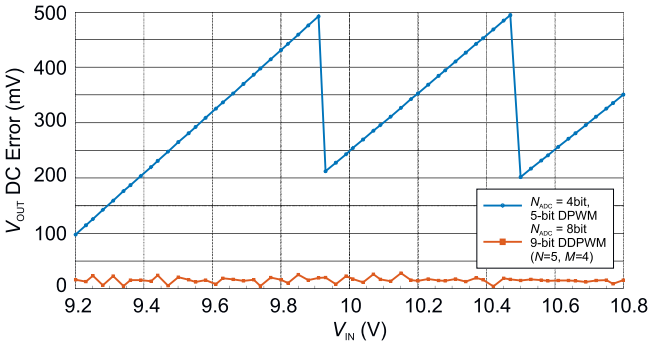

Fig. 15. Static error in the output voltage under different input voltages.

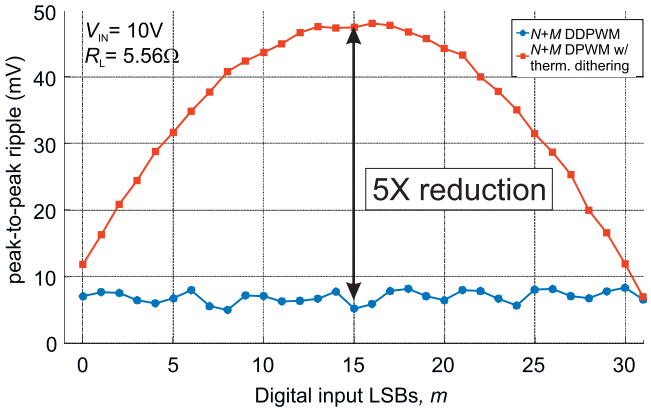

Fig. 16. Measured dithering-induced ripple voltage (open-loop configuration) versus high-resolution duty cycle by the thermometric dithering (see Fig. 2) and by DDPWM (see Fig. 4) under the same $M = 5$ resolution enhancement.

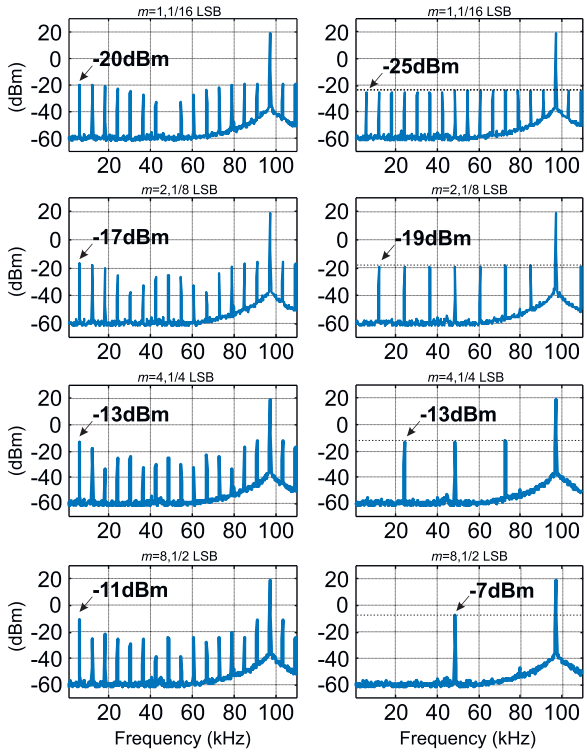

Fig. 17. Measured spectra of the switching node A in Fig. 1 in open-loop conditions with $M = 4$ bit increased resolution by thermometric dithering (left column) and DDPWM (right column) for 50% duty cycle and $m = 1$ (first row), $m = 2$ (second row), $m = 4$ (third row), and $m = 8$ (fourth row).

operation and the dc accuracy can be obtained at the same time by adopting DDPWM.

2) Output Ripple: The low-frequency output ripple resulting from $N = 5$, $M = 5$ DDPWM is then compared in Fig. 16 with thermometric dithering. To avoid possible confusion of ripple and LCOs related to the closed-loop operation, the ripple test has been performed under open-loop conditions, by sweeping the M LSBs of the modulator output from 0 to 31, for a value $n = 16$ of the N MSBs, which corresponds (for $m = 0$) to a 50% duty cycle. The experimental results presented in Fig. 16 are consistent with Figs. 7 and 8 and reveal negligible low-frequency ripple (not distinguishable from the equivalent-series-resistance-related ripple voltage) for DDPWM, when compared with the significant ripple up to about 50 mV of the thermometric dithering, for all possible values of m.

3) Measured Spectra: The spectra of the switching node voltage of the buck converter (i.e., the LC filter input voltage) in open-loop conditions are plotted in Fig. 17 for thermometric dithering (left column) and for DDPWM (right column) for $N = 5$ and $M = 4$, with DPWM duty cycle 50% and different fractional duty cycle values of 1/16 LSB (i.e., $m = 1$), 1/8 LSB (i.e., $m = 2$), 1/4 LSB (i.e., $m = 4$), and 1/2 LSB (i.e., $m = 8$) and validate the analysis presented in Section III. In particular, it can be observed that the critical spectral component at the lowest frequency $f_s/16$ is increasing in amplitude with the fractional duty cycle for thermometric dithering, while such a component appears (and with 5 dB lower amplitude than with thermometric dithering) only for 1/16 LSB fractional duty cycle, since the fundamental frequency of DDPWM for 1/8 LSB, 1/4 LSB, and 1/2 LSB fractional duty cycle is $f_s/8$, $f_s/4$, and $f_s/2$, respectively.

The spectra of the buck output voltage, reported in Fig. 18 under the same test conditions, reveal that with thermometric dithering, the output ripple is dominated by the low-frequency component at $f_s/16$, which is either very low (-52 dBm for $m = 1$) or not present (for $m = 2, 4, 8$) in DDPWM. As a consequence, an improvement in the dominant ripple component ranging from 6 up to 16 dB is achieved by DDPWM.

In Fig. 19, the output spectra of the converter in closed-loop conditions is reported for $N_{\mathrm{ADC}} = 8$ bit and for a DPWM resolution of $N = 5$. In Fig. 19(a), in particular, no dithering technique is adopted, and the very high noise floor reveals the presence of LCOs; in Fig. 19(b), thermometric dithering with $M = 4$ proves effective to suppress LCOs, but gives rise to -40 dBm output ripple; and, finally, Fig. 19(c) reveals that DDPWM with $M = 4$ also leads to the LCO-free operation with a reduction of 12 dB in the dominant ripple component, thus confirming the advantage of DDPWM previously highlighted in Fig. 18 under open-loop conditions.

4) Load Transient: The load transient response for an output current step from 330 mA to 1 A of the buck converter in closed-loop conditions for plain DPWM at 9-bit resolution without dithering [i.e., $N = 9$ and $M = 0$; see Fig. 20(a)] for

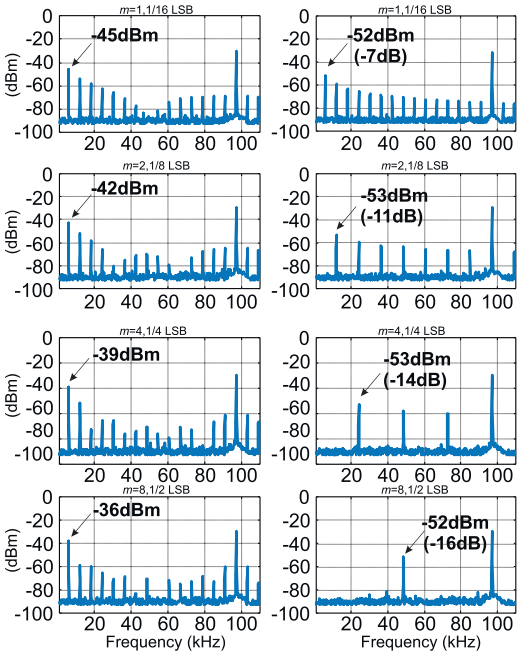

Fig. 18. Measured spectra of the ac component of the buck converter output voltage in Fig. 1 in open-loop conditions with $M = 4$ bit increased resolution by thermometric dithering (left column) and DDPWM (right column) for 50% duty cycle and $m = 1$ (first row), $m = 2$ (second row), $m = 4$ (third row), and $m = 8$ (fourth row). The dominant subharmonic reduction achieved by DDPWM compared to thermometric dithering is reported in braces in the right plots.

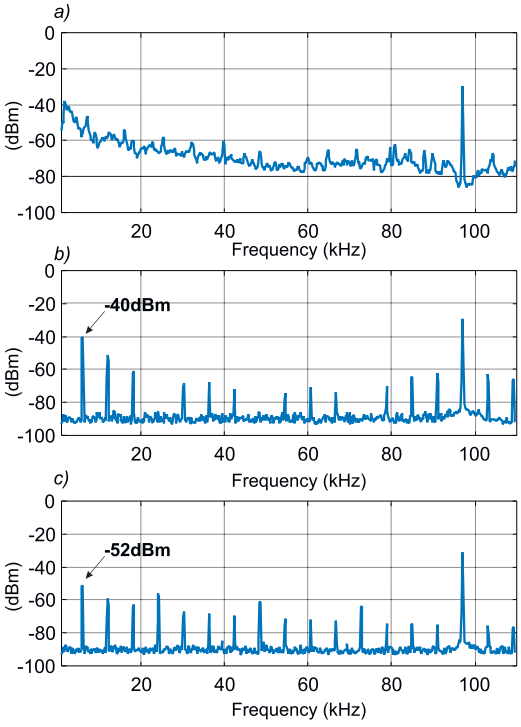

Fig. 19. Measured spectra of the ac component of the buck converter output voltage in Fig. 1 in closed-loop conditions for $N_{\mathrm{ADC}} = 8$ (a) using plain DPWM at $N = 5$ bit resolution and resulting in LCOs, (b) using $N + M$ bit thermometric dithering with $N = 5$ and $M = 4$, revealing LCO suppression and -40 dBm highest ripple component @$f_{\mathrm{s}}/16$, and (c) using $N + M$ bit DDPWM with $N = 5$ and $M = 4$, revealing LCO suppression and -52 dBm highest ripple component @$f_{\mathrm{s}}/16$.

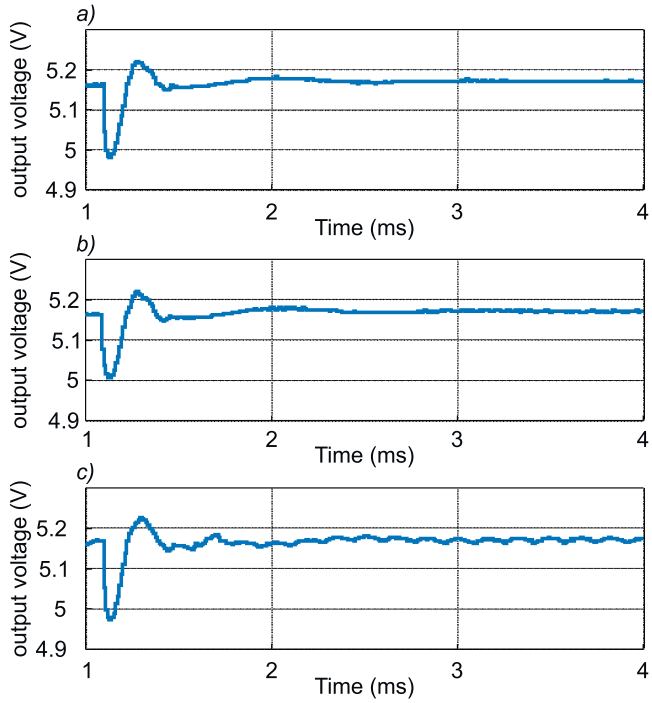

Fig. 20. Measured output voltage of the synchronous buck converter under 330-mA–1 A load transient for $N_{\mathrm{ADC}} = 8$ bit: (a) plain DPWM with $N = 9$ bit resolution ($f_{\mathrm{s}} = 100$ kHz and $f_{\mathrm{clk}} = 51$ MHz), (b) DDPWM with $N = 5$ bit $M = 4$ bit ($f_{\mathrm{s}} = 100$ kHz and $f_{\mathrm{clk}} = 3.2$ MHz), and (c) thermometric dithering with $N = 5$ bit and $M = 4$ bit ($f_{\mathrm{s}} = 100$ kHz and $f_{\mathrm{clk}} = 3.2$ MHz).

DDPWM with $N = 5$ and $M = 4$ [see Fig. 20(b)] and for thermometric dithering with $N = 5$ and $M = 4$ are compared [see Fig. 20(c)] and reveal no detrimental impact of DDPWM on the load transient.

VI. Conclusion

The DDPWM modulation technique has been proposed as a systematic approach to increase the effective resolution of DPWM so as to suppress quantization-induced LCOs in digitally controlled power converters at reduced hardware complexity and minimum performance degradation.

Measurements on a synchronous buck converter confirm the effectiveness of the technique, enabling an LCO-free operation at higher switching frequency and/or dc accuracy than in plain DPWM at the same digital clock frequency. Compared to thermometric dithering, a lower frequency ripple (up to 5× measured peak ripple reduction and up to 16 dB lower frequency harmonic component reduction) has been observed with the proposed technique for the same 4-bit DPWM resolution enhancement.

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