High-Efficiency High-Power-Density *CLLC* Resonant Converter With Low-Stray-Capacitance and Well-Heat-Dissipated Planar Transformer for EV On-Board Charger

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***Abstract*—In this article, a high-efficiency high-power-density wide-bandgap-based *CLLC* resonant converter with a low-stray-capacitance and well-heat-dissipated planar transformer is presented, which is used as the isolated dc–dc stage for an electric vehicle on-board charger. A generalized planar transformer design methodology is proposed and validated by practical designs and experimental tests. A novel and simple transformer configuration is proposed to reduce the winding stray capacitance and enhance the winding thermal dissipation. The proposed transformer configuration is compared with different planar transformer designs, and the tradeoffs of employing the proposed design are well analyzed. Moreover, the system design and optimization of the high-efficiency high-power-density *CLLC* resonant converter is studied. The proposed transformer design and the system optimization approach are employed in a 6.6-kW/500-kHz *CLLC* resonant converter prototype. The prototype achieves a peak efficiency of 97.85% and a power density of 114 W/in^3.**

***Index Terms*—Electric vehicle (EV) on-board charger, high efficiency, high power density, planar transformers, resonant converters, thermal dissipation, wide-bandgap (WBG) devices, winding stray capacitance.**

I. Introduction

ELECTRIC vehicle (EV) and hybrid plug-in EV are gaining more and more attention because of their reduced fuel usage and greenhouse emissions [1]. A battery charger located inside a vehicle is classified as an on-board charger (OBC), which allows EV owners to charge their vehicles wherever a suitable power source is available. For the OBC, the power density demand is high due to the limited space on a vehicle. However, the state-of-the-art Si-based level 2 OBC products have low power density of 3–12 W/in^3, as well as low efficiency of 92–94% [2].

With the emergence of wide-bandgap (WBG) power semiconductor devices, it is possible to upgrade the switching frequency to several 100 kHz or even megahertz. The size of passive components will shrink a lot at very high switching frequency. Meanwhile, with the employment of soft-switching topologies, the excessive switching loss can be avoided. The size for the cooling system can be kept small. System power density can be significantly improved.

A typical two-stage isolated OBC includes a power factor correction (PFC) stage and an isolated dc–dc stage. The normal strategy is to use the PFC only to do power factor correction and use the isolated dc–dc stage to implement the voltage regulation as well as provide the galvanic isolation. In this case, the PFC dc-link voltage is usually a fixed value. Common candidates for the isolated dc–dc stage include a series-resonant converter (SRC), a phase-shifted full-bridge converter (FSFB), and an *LLC*/*CLLC* resonant converter [3]. Both the SRC and the FSFB have difficulties in terms of efficiency and voltage regulation for light-load conditions [4]–[7]. The *LLC*/*CLLC* resonant converters are able to obtain zero-voltage switching (ZVS) and good voltage regulation for full-load range [8]–[13]. In particular, the *CLLC* resonant converter acquires a symmetrical gain curve, which guarantees similar operating frequency and power losses at both power flow directions. The major drawback for the *LLC*/*CLLC* resonant converter is the drop of efficiency when the operating frequency is far away from the resonant frequency. To improve the system efficiency and the density of passive components, the variable PFC dc-link solution is adopted to maintain a narrow switching frequency range at wide battery voltage [2], [14]–[17]. Instead of selecting 250–450 V as the dc-link voltage, it is more reasonable to select 500–900 V (twice of the battery voltage), since the PFC can only boost the voltage. However, there are concerns for increasing the dc-link voltage. First, higher voltage rating switches need to be selected, and those switches typically have higher Rdson. Since the device conduction loss is proportional to the square of the device current, the device conduction loss is still significantly reduced. Another concern for increasing the dc-link voltage is the increased volt–second for

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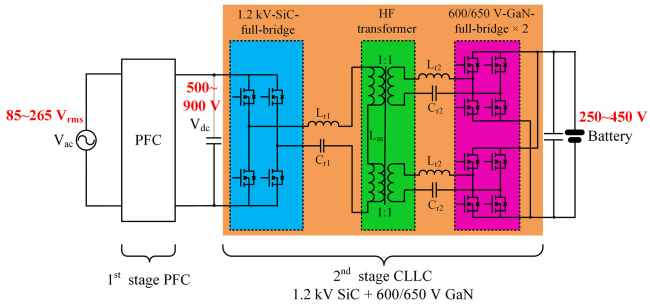

Fig. 1. Selected structure of the WBG-based variable dc-link EV OBC.

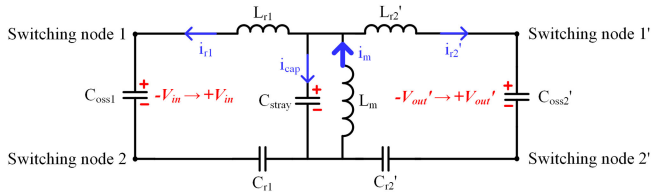

Fig. 2. Equivalent circuit of the *CLLC* resonant converter during the dead time.

the transformer, which may lead to higher core loss. This issue can be easily solved by increasing the number of turns of the transformer. The maximum flux density in the core can be kept the same, and the core loss will not be increased. Moreover, the winding loss is proportional to the square of the winding current, so it can be significantly reduced as well. In [18], the system efficiency of different solutions is compared; it is found that higher dc-link voltage solution improves the system efficiency.

From the PFC dc link to the battery side, the 2:1 voltage conversion ratio can be easily achieved by an integer-turn step-down transformer. The dc-link voltage will vary with the battery voltage to maintain the nearly 2:1 voltage ratio. In this case, the PFC undertakes the tasks of both power factor correction and voltage regulation. The efficiency of the PFC may be affected. However, the isolated dc–dc stage has more weight on the loss in the total loss chart, which is mainly due to the high-frequency transformer loss and the high conduction loss on the secondary-side device. The loss reduction on the *LLC*/*CLLC* stage is higher than the loss increase on the PFC stage, so the overall efficiency is still enhanced [18].

An adequate topology (see Fig. 1) needs to be selected to adapt to the variable dc-link operation. First, a single H-bridge is selected on the primary side instead of two series-connected H-bridges. For the off-the-shelf WBG power devices, either two series-connected 600/650-V GaN full bridges or one 1.2-kV SiC full bridge [17] can be selected to sustain the 500–900-V dc-link voltage. The latter one is chosen here, since the single 1.2-kV SiC device has smaller Rdson than that of two 600/650-V GaN devices at similar current rating. Second, *CLLC* is selected instead of *LLC*, since it acquires a symmetrical gain curve, which guarantees similar operating frequency and efficiency at both power flow directions. Third, two paralleled 600/650-V GaN-based full-bridge converters are employed on the battery side to reduce the conduction loss.

For the *CLLC* resonant converter, the transformer design is very critical. High switching frequency introduces high core loss and winding loss. A planar transformer stands out for very high frequency applications ($\geq$500 kHz) because of the following benefits [2], [19]–[23]. First, the printed circuit board (PCB) trace windings are extremely thin, and the number of turns is very few. Skin and proximity effects are significantly diminished for the planar transformer; hence, transformer ac winding loss is greatly reduced. Second, better coupling in geometry minimizes the leakage inductance and the ac winding loss. Third, the low-profile characteristics and the high filling factor make the power density of the planar transformer very high. Fourth, the better insulation property of the FR4 brings space saving for the high-voltage operation. Fifth, PCB winding has better thermal dissipation, which enables PCB winding to sustain higher current density. Last but not the least, the fixed and reliable winding structure makes the parasitic parameters controllable. The fabrication and assembly process is much easier compared with the Litz-wire wound transformer. It is good for mass production.

Despite the advantages, there are still several challenges for the successful appliance of the planar transformer, especially for the high-power-density applications.

First, the intrawinding capacitance (the stray capacitance between turns of each winding) is high compared to that of the wire-wound transformer, because of the large overlapping area and small distance between the adjacent turns. This will affect soft switching, transformer and converter efficiency, and the waveform quality, which will be explained as follows. ZVS will be harder to achieve because the magnetizing current (i_{m}) will, thus, flow not only to charge and discharge the device junction capacitance (C_{oss1}, C'_{oss2}), but also be distributed into the intrawinding capacitance (C_{stray}) during the dead time, as shown in Fig. 2. C_{stray} represents the total winding stray capacitance referred to the primary side, and it can be seen as an equivalent intrawinding capacitor. Although a higher magnetizing current can be applied, but more conduction loss will be produced and the system efficiency drops. The voltage regulation will be affected as well [24], which results in a wider operating frequency range. The transformer current quality and utilization will be degraded due to the dv/dt-introduced resonance between the intrawinding capacitance and the resonant inductor. To address this challenge, Saket *et al.* [24] proposed the strategy of placing the turns in a specific fashion to minimize the electric field intensity. Meanwhile, the permittivity is reduced by inserting the Kapton tape between the adjacent turns of each winding. However, complicated interboard connections are required, and it is labor intensive to insert the Kapton tapes between different boards, which makes this approach not cost-effective.

The second challenge for the planar transformer is the high interwinding capacitance (the stray capacitance between different windings). Usually, interleaving of primary and secondary windings is adopted for a multiwinding configuration [21] to reduce the leakage flux and the corresponding ac winding loss. But this will result in large overlapping area and small distance between primary and secondary windings, which is the root

TABLE I
VOLT–SECOND AND OUTPUT CURRENT COMPARISON BETWEEN 6.6-kW/500-kHz EV OBC AND 1-kW/1-MHz 380-V–12-V *LLC*

Parameters	6.6 kW/500 kHz EV OBC	1 kW/1 MHz 380 V-12 V LLC
Maximum volt-second	4.5×10^{-4} V·s	4.75×10^{-5} V·s
Maximum output dc current	22 A	83.33 A

cause of the high interwinding capacitance. The interwinding capacitance is usually a major path for the common-mode (CM) current [25]–[27]. The dv/dt-induced CM current will flow into the secondary side and then enter the earth ground and will be seen by the line impedance stabilization network (LISN) eventually. In order to meet the conducted electromagnetic interference (EMI) standard, a larger EMI filter is required to bypass the CM current flowing into the LISN, which greatly impacts the system power density [4]. The common approaches to suppress the CM current due to the high interwinding capacitance can be grouped into two categories. The first one is to use a passive cancellation and balance technique [28]–[30]. Basically, the principle is to create an additional 180°-phase-shifted CM current with the same magnitude to cancel the original CM current through the interwinding capacitance. However, this method requires additional passive components, and it is sensitive to the tolerance. The second category is to employ shielding layers between primary and secondary windings [31], [32]. The shielding layer is connected to the primary-side ground and has the same layout as that with the secondary winding. The CM current from the primary side will flow into the shielding layer and then circulate back to the primary-side ground. The CM current from the secondary side will circulate back as well, because there is no voltage potential difference between the secondary winding and the shielding layer. The major drawback of this method is the additional eddy current losses in the shielding layer. Actually, the above two mechanisms do not cut down the physical interwinding capacitance between primary and secondary windings. They either compensate or bypass the CM current. In this article, the physical interwinding capacitance is significantly reduced by increasing the instance between primary and secondary windings.

The third challenge for the high-power-density planar transformer is the thermal management. Planar transformer winding usually sustains higher current density compared with the Litz-wire wound transformer [21], [23]. In particular, for the EV OBC, the transformer has the characteristics of high volt–second and low current. The maximum volt–second and the maximum output dc are compared with the 1-kW/1-MHz 380-V–12-V *LLC* [33], which is shown in Table I.

The volt–second of the EV OBC is 9.5 times of the volt–second of the 380-V–12-V *LLC*, while the output dc is only 1/4 of the 380-V–12-V *LLC*. In general, the winding loss is not a dominate factor; hence, the winding width is not necessarily to be overdesigned to reduce the dc resistance (DCR) of the winding. To save the footprint, the winding can be designed close to its thermal limited width. The FR-4 material has much lower thermal conductivity compared with copper. The thermal dissipation capability for PCB inner layers is much worse than the outer layers because the heat generated in the inner layers needs to go through the low-thermal-conductive FR-4 material to reach the air. Researchers in [20], [34], and [35] propose different methods of integrating resonant inductors into the transformer. Those methods can be grouped into two categories. The first mechanism is to use the air to conduct the leakage flux. The main drawbacks are the greatly magnified ac winding loss and the EMI issue caused by unconstrained magnetic fields. The second mechanism is to use the magnetic material to conduct the leakage flux. In this method, the low-permeability magnetic shunt suffers from high core loss. In [2], the leakage flux is diverted into a third leg of the ferrite core. The extra loss is reduced to 15–17% of transformer total losses. To sum, the magnetic integration is a good approach to reduce magnetic component counts and improve the system power density, but it also makes the thermal management of the transformer even harder. Therefore, an alternative approach is proposed here to utilize external resonant inductors. The corresponding power losses are produced outside the transformer, so the thermal stress of the transformer is released. Moreover, by putting the windings only on the outer layers of the PCB through magnetic core reconfiguration, the thermal stress can be further released.

An adequate core and winding configuration is proposed to address the three challenges, which is the major contribution of this article. To reduce the intrawinding capacitance, a matrix transformer concept is adopted. The overlapping area within each winding, which is the dominate cause of the intrawinding capacitance, can be reduced significantly by splitting the core into several units and routing the turns horizontally. The core area by the footprint area ratio can be kept high as well by keeping very few turns for each unit core due to the matrix transformer structure. To reduce the interwinding capacitance, the primary and secondary windings are placed on the top and bottom layers, which have larger distance from each other. This layout can also address the third challenge, since the PCB outer layers have much better thermal dissipation capability than the inner layers. The system can finally achieve high power density and high efficiency with the proposed methods.

The rest of this article is organized as follows. Section II introduces the proposed generalized design methodology for planar transformers. Section III presents the novel low-stray-capacitance and well-heat-dissipated planar matrix transformer design. The comparison with different planar transformer designs and the tradeoff analysis are also studied in this section. Section IV discusses the system design and optimization of the high-efficiency high-power-density *CLLC* resonant converter. The experimental verification is conducted in Section V. Finally, Section VI concludes this article.

II. PROPOSED GENERALIZED DESIGN METHODOLOGY FOR PLANAR TRANSFORMERS

The design of the planar transformer is discussed in a number of literature works [2], [19], [21], [24], [33], [36], but a generalized design methodology is lacked. Compared with

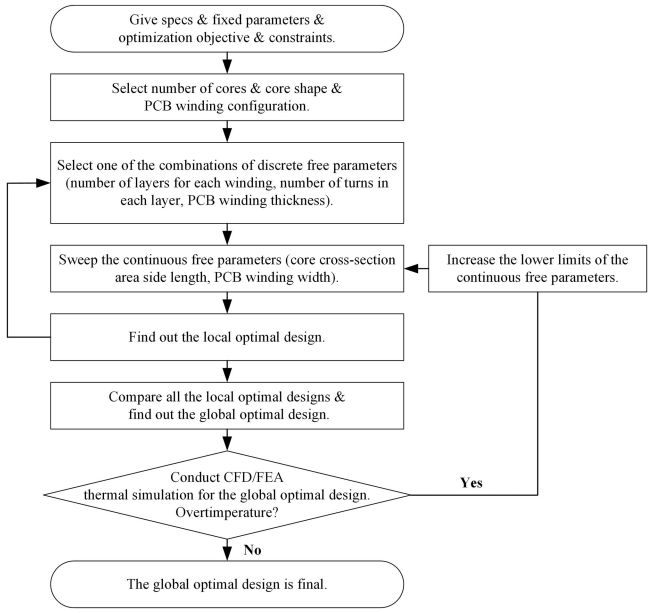

Fig. 3. Proposed generalized design methodology for high-power-density planar transformers.

conventional transformers, the PCB winding structure is fixed to some degree, which makes the planar transformer easier to be parameterized. In terms of optimization, some advanced optimization algorithms are conducted for the conventional wire-wound transformer [37], [38]. Although the optimal design can be found out, it is hard to find relations and tradeoffs between different parameters and objectives due to too many free variables. This article proposes a generalized design methodology for high-power-density planar transformers. By analyzing the core and winding geometries, only a few free parameters are needed for the optimization. By sweeping the free parameters, the trends of the objectives are easy to observe. The optimal design can be found for the given objectives and constraints.

The proposed design methodology for high-power-density planar transformers is shown in Fig. 3. This methodology is generalized for the design and optimization of nonintegrated planar transformers. As mentioned before, transformer core loss or winding loss has to be compromised if the resonant inductor is integrated. The integrated design will have more challenges in thermal management, especially when a large leakage inductance value is required. Moreover, to achieve a certain leakage inductance value, the transformer winding structure is confined to some degree, which will hinder the optimization process in terms of efficiency or power density. The proposed design methodology is explained as follows.

A. Specifications, Fixed Parameters, Objective, and Constraints

Specifications for a planar transformer include the operating frequency (f), excitation voltage waveform ($v(t)$), winding current waveform ($i(t)$), turns ratio (n), and required magnetizing inductance (L_{m}) value. It should be mentioned that the winding current waveforms can be obtained from the circuit simulation to get more accurate result.

The fixed parameters include the magnetic core Steinmetz parameters (α, β, and k), the insulation distance between different turns in the primary windings (δ_{pp}), the insulation distance between different turns in the secondary windings (δ_{ss}), the insulation distance between the primary windings and secondary windings (δ_{ps}), the insulation distance between the core and the primary windings (δ_{cp}), the insulation distance between the core and the secondary windings (δ_{cs}), thickness of each PCB (t_{pcb}), and the distance between different layers in the PCB (t_{ll}).

The optimization objective can be expressed as a weighing function of transformer total losses (P_{total}) and the box volume (V):

$$f = \min\left\{W_1 \cdot P_{\mathrm{total}} + W_2 \cdot V\right\} \tag{1}$$

where f is the objective function; and W_1 and W_2 are weighting factors, which can be defined according to the requirements.

The constraints for planar transformer design can be summarized as follows. It should be noticed that not all the constraints are required for each design.

1) $B_{\mathrm{max}} < B_{\mathrm{sat}}$. The maximum flux density in the core (B_{max}) is normally much less than the saturation flux density (B_{sat}) of the core material.
2) $J < J_{\mathrm{max}}$. The current density (J) in the winding should be smaller than the maximum allowable current density (J_{max}). J_{max} is limited by the winding temperature rise.
3) $P_{\mathrm{total}} < P_{\mathrm{total(required)}}$ or $\eta > \eta_{\mathrm{required}}$. The total losses ($P_{\mathrm{total}}$) or the efficiency ($\eta$) of the planar transformer can be restricted according to the requirement.
4) $V < V_{\mathrm{max}}$. The box volume of the planar transformer (V) can be confined according to the required maximum box volume or the required minimum power density. Compared to conventional transformers, the footprint of planar transformer is increased; hence, it is more meaningful to consider the box volume rather than consider just the core volume.
5) $g < g_{\mathrm{max}}$. The air-gap length (g) should be confined as well. If g is too large, the fringing flux will cause more winding loss.
6) Minimize L_{lk}. The leakage inductance value (L_{lk}) is not a design target for this methodology because an external inductor is assumed to be employed. However, for a certain space, a larger leakage inductance indicates stronger leakage magnetic field intensity, which can cause more ac winding loss. Therefore, the leakage inductance value should be minimized.
7) Minimize C_{intra} and C_{inter}. This is usually not considered in the conventional transformer design. However, this factor cannot be ignored, since the planar transformer normally has much higher winding stray capacitance. The drawbacks of high intrawinding capacitance (C_{intra}) and high interwinding capacitance (C_{inter}) have already been discussed in Section I. Since the winding stray capacitance is closely related to the winding structure, an optimized winding configuration should be selected.

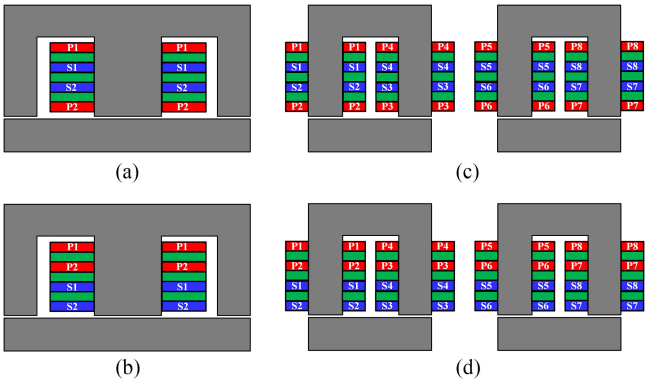

Fig. 4. Typical core and winding configurations of planar transformers. (a) Single-core (E-I core) interleaved winding. (b) Single-core (E-I core) noninterleaved winding. (c) Multiple-core (U-I core) interleaved winding. (d) Multiple-core (U-I core) noninterleaved winding.

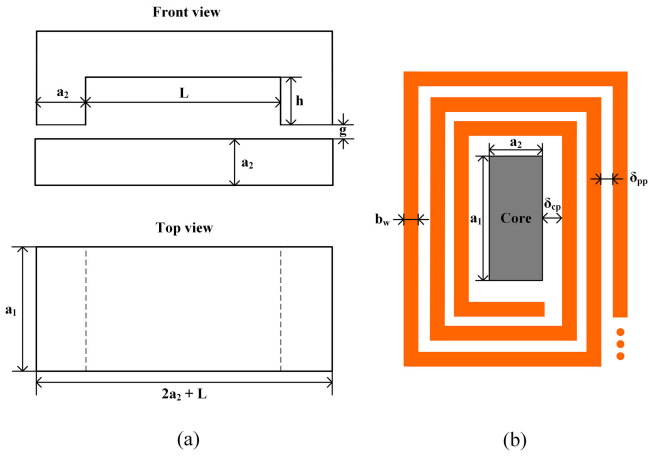

Fig. 5. (a) U-I core sets geometry. (b) Cross-sectional view and winding geometry for each pillar.

8) $T_{\text{core}} < T_{\text{curie}}$ and $T_{\text{winding}} < T_{\text{pcb(max)}}$. The core temperature ($T_{\text{core}}$) should be much less than the Curie temperature (T_{curie}), and the winding temperature (T_{winding}) should be less than the PCB maximum allowable temperature ($T_{\text{pcb(max)}}$). It is hard to analytically calculate the temperature rise for planar transformers. For this constraint, it should be checked after the optimal design is obtained. Computational fluid dynamics (CFD) or finite-element analysis (FEA) thermal simulation can be employed. If the temperature rise is out of the desired range, the design should be discarded.

B. Selection of the Number of Cores, Core Shape, and Winding Configuration

For the high-power-density applications, the conventional single-core transformer is not the only option. The series-connected multiple-core solution needs to be considered as well, since it can distribute the total power into multiple cores and ease the voltage and thermal stress on each single core.

The magnetic core shape and the PCB winding configuration are closely related. For the E-I or E-E core, windings are wound around the center pillar. For the U-I or U-U core, windings can be wound around both side pillars. There are other core shapes, such as pot core. For the winding structure, an alternating placement (interleaving) of primary and secondary windings in the vertical direction along the same core pillar is commonly used to achieve the most flux cancellation, which can reduce the leakage inductance and ac winding loss. However, this structure will boost the interwinding capacitance. The typical core and winding configurations are shown in Fig. 4. Advanced winding structures should be considered to cut down the interwinding capacitance without sacrificing a lot of the ac winding loss.

Meanwhile, the windings can be wound on a single PCB or multiple PCBs. For each PCB, windings can be placed in a single layer or in multiple layers. Different winding configurations greatly impact the leakage inductance, ac winding loss, winding stray capacitance, as well as the winding thermal dissipation. One of the core and winding configurations should be selected for this step, and the following optimization is based on the selected core shape and winding structure.

C. Selection of Combination of Discrete Free Parameters

In planar transformers, the number of layers for each winding (m), the number of turns in each layer (N_0), and the PCB winding thickness (t_{w}, typically $=$ 1 oz, 2 oz, 3 oz...) can be seen as discrete free parameters. The three parameters are all free design parameters, but their values are discrete. Meanwhile, all three parameters are small integers. The number of layers for each winding is constrained by the cost of the PCB, and the number of turns in each layer is restricted by the footprint area or the box volume. The winding thickness should be confined as well due to the high-frequency operation. For the operating frequency $\geq$500 kHz, the winding thickness should be no more than 3 oz. Therefore, the combinations of the three parameters are very limited. For this step, one of the combinations should be chosen.

D. Sweeping the Continuous Free Parameters

The cross-sectional area of the core (A_{e}) and the winding width (b_{w}) are continuous free parameters. They can be chosen as any value within certain range. Here, the core shape is selected as U-I core as an instance (see Fig. 5). The two sides of the cross-sectional surface are a_1 and a_2, respectively. To employ fewer variables, k_0 is defined as the ratio of a_1 by a_2 as

$$k_0 = \frac{a_1}{a_2}. \tag{2}$$

k_0 is actually the length-by-width ratio of the cross-sectional surface, and its value can be manipulated to improve the system power density, which will be discussed later in this article. When the ratio of a_1 by a_2 is a constant, it can be defined that $a_2 = a$ and $a_1 = k_0 a$. Then, only two variables (a and b_{w}) are free continuous parameters. The other geometry-related parameters, loss-related parameters, and the leakage inductance value can be expressed by a, b_{w}, fixed parameters, and the selected discrete free parameters.

First, the geometry-related parameters are derived as follows. The derivations are based on a single-U-I-core single multilayer PCB planar transformer:

$$L = 2\delta_{\text{cp}} + (N_0 - 1)\cdot\delta_{\text{pp}} + N_0 \cdot b_{\text{w}} \tag{3}$$

$$h = t_{\text{pcb}} + 2\delta_{\text{cp}} \tag{4}$$

$$g = \frac{\mu_0 \cdot k_0 a^2 \cdot (m \cdot N_0)^2}{2L_{\text{m}}} \tag{5}$$

$$V_{\text{core}} = 2k_0 a^2 \cdot (h + L + 2a) \tag{6}$$

$$V = [k_0 a + N_0 b_{\text{w}} + (N_0 - 1)\delta_{\text{pp}} + 2\delta_{\text{cp}}]\cdot [L + 2a + N_0 b_{\text{w}} + (N_0 - 1)\delta_{\text{pp}} + 2\delta_{\text{cp}}]\cdot (2a + g + h) \tag{7}$$

$$l_{\text{w0}} = 2{N_0}^2 \cdot b_{\text{w}} + 2(k_0 + 1)\cdot N_0 \cdot a + 4N_0 \cdot \delta_{\text{cp}} + 4N_0 \cdot \left(\frac{N_0}{2} - 1\right)\cdot \delta_{\text{pp}} \tag{8}$$

where L is the length of the window, h is the height of the window, g is the length of the air-gap, V_{core} is the core volume, V is the transformer box volume, and l_{w0} is the total length of each winding in one layer.

According to (5), the air-gap length is inversely proportional to the required magnetizing inductance value. The total reluctance in the transformer magnetic circuit is dominated by the reluctance of the air-gap, so the magnetizing inductance value can be tuned by adjusting the air-gap length in practical designs.

Second, the loss-related equations are derived as follows:

$$B_{\text{max}} = \frac{\int_0^{\frac{T}{4}} v(t)dt}{m \cdot N_0 \cdot k_0 a^2} \tag{9}$$

$$P_{\text{core}} = K_{\text{waveform}} \cdot k \cdot f^{\alpha} \cdot {B_{\text{max}}}^{\beta} \cdot V_{\text{core}} \tag{10}$$

$$R_{\text{dc}} = m \cdot \rho_{\text{Cu}} \cdot \frac{l_{\text{w0}}}{b_{\text{w}} \cdot t_{\text{w}}} \tag{11}$$

$$P_{\text{winding}} = \sum_{h=1}^{\infty} F_{\text{ac(h)}} \cdot {I_{\text{h}}}^2 \cdot R_{\text{dc}} \tag{12}$$

$$P_{\text{total}} = P_{\text{core}} + P_{\text{winding}} \tag{13}$$

where B_{max} is the maximum flux density in the core, P_{core} is the core loss, K_{waveform} represents the core loss density under different excitation voltage waveforms [39], [40], R_{dc} is the winding DCR value, ρ_{Cu} is the resistivity of copper, P_{winding} is the winding loss, $F_{\text{ac(h)}}$ is the winding ac factor for the hth harmonic component, which can be estimated by Dowell's model [41] or by FEA simulation, and P_{total} is the transformer total loss.

According to (9), the maximum flux density in the core is proportional to the volt–second of the excitation source. The high operating frequency can reduce the volt–second and avoid the saturation of the core, but the side effect is the increased core loss and ac winding loss.

Third, the leakage inductance value (L_{lk}) can be calculated by

$$L_{\text{lk}} = \frac{\mu_0 \cdot l_{\text{w0}} \cdot b_{\text{w}}}{I_{\text{p}}^2} \cdot \int_0^{t_{\text{pcb}}} H(x)^2 dx \tag{14}$$

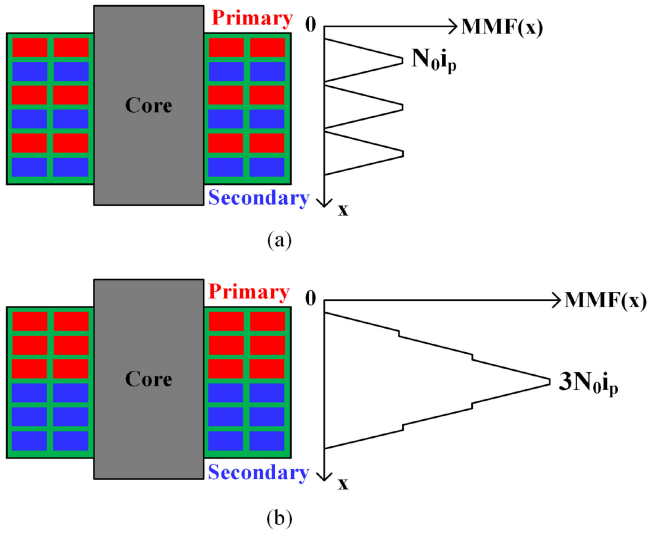

Fig. 6. (a) MMF distribution of the interleaved winding structure. (b) MMF distribution of the noninterleaved winding structure.

where I_{p} is the rms value of the primary winding current, t_{pcb} is the thickness of the PCB, and $H(x)$ is the magnetic field strength along the vertical direction, which is related to the winding configuration. The MMF distribution of the interleaved and noninterleaved winding structures are shown in Fig. 6.

From (14), it is clear that the leakage inductance value reflects the energy stored in the space among the windings. Any method of increasing the leakage inductance is to either enhance the magnetic field intensity or enlarge the space for the leakage flux. Usually, the increased magnetic field intensity will magnify the proximity effect, and more ac winding loss will be produced.

Last but not least, the winding stray capacitance can be calculated.

To calculate the intrawinding capacitance, it is reasonable to make two assumptions. First, the stray capacitance between the turns in the same layer can be ignored because the overlapping area is much smaller than the overlapping area for the turns in different layers [21]. Second, the stray capacitance between nonadjacent turns can be neglected as well because the distance between nonadjacent turns is usually much larger than the distance between adjacent turns. Then, the key is to calculate the stray capacitance between the adjacent turns in different layers. According to the principle of conservation of energy, the intrawinding capacitance between the two adjacent turns can be derived as

$$C_{\text{turn-to-turn}} = \frac{\varepsilon_0 \varepsilon_{\text{r}} \cdot \int_V E^2 dV}{U^2} \tag{15}$$

where ε_0 is the vacuum permittivity, ε_{r} is the relative permittivity of the medium, E is the electric field intensity between the two turns, V represents the space/volume between the two turns, and U is the voltage different between the two terminals.

It is clear that the intrawinding capacitance between the adjacent turns is closely related to the electric field intensity distribution [42]. Since the distance between the two layers is fixed, the electric field intensity distribution is proportional to the voltage distribution. For analysis purpose, the turns are

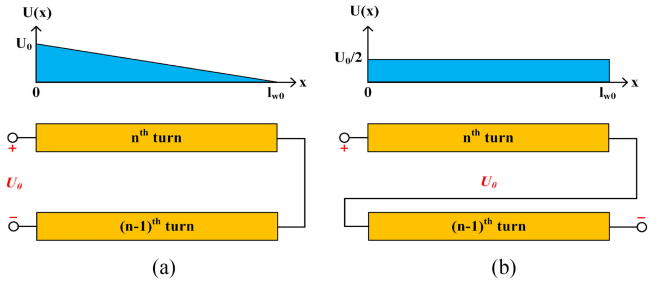

Fig. 7. (a) Voltage distribution between adjacent turns in different layers (connection method 1). (b) Voltage distribution between adjacent turns in different layers (connection method 2).

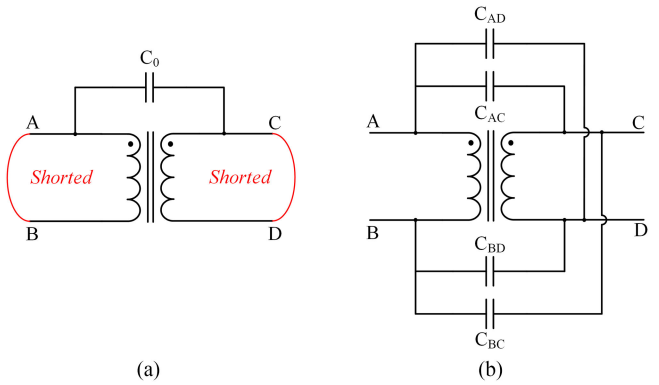

Fig. 8. (a) Single-lumped-capacitor model of the interwinding capacitance. (b) Four-lumped-capacitor model of the interwinding capacitance.

straightened, as shown in Fig. 7. The voltage distribution between the turns changes for different connections of the adjacent turns, which will result in different turn-to-turn intrawinding capacitance values. Since the voltage distribution only varies along the winding (x-axis), (15) can be expressed as

$$C_{\text{turn-to-turn}} = \frac{\varepsilon_0 \varepsilon_{\text{r}} \cdot b_{\text{w}} \cdot t_{\text{ll}} \cdot \int_0^{l_{\text{w0}}} E(x)^2 dx}{{U_0}^2} \tag{16}$$

where b_{w} is the winding/turn width and t_{ll} is the distance between two layers.

Once the turn-to-turn intrawinding capacitance value is obtained, the lumped intrawinding capacitance for each winding can be derived as

$$C_{\text{intra(lumped)}} = \frac{1}{\frac{1}{C_{\text{1-to-2}}} + \frac{1}{C_{\text{2-to-3}}} + \frac{1}{C_{\text{3-to-4}}} + \cdots + \frac{1}{C_{\text{(m-1)-to-m}}}} \tag{17}$$

where m is the number of layers for each winding.

For the calculation of the interwinding capacitance, the single-lumped-capacitor model and the four-lumped-capacitor model can be employed, as shown in Fig. 8. The two models here are suited for the two-winding transformer, and they can be extended for the multiwinding transformer as well.

For the single-lumped-capacitor model, the transformer can be seen as a two-terminal device. The primary-side winding is shorted, and the secondary-side winding is shorted as well. If an *RLC* meter is utilized to measure the parameter across the primary and secondary sides, the measured capacitance value is the lumped capacitor value (C_0). This capacitor can also be regarded as the total value of the distributed capacitance between the primary winding and the secondary winding. If the primary and secondary windings have the same length of l_{w}, the interwinding capacitance value for the unit length can be seen as C_0/l_{w}. Moreover, the single lumped capacitor can be calculated according to the winding geometry as

$$C_0 = \frac{\varepsilon_0 \varepsilon_{\text{r}} \cdot b_{\text{w}} \cdot l_{\text{w}}}{t_{\text{ll}}}. \tag{18}$$

In reality, the transformer is a four-terminal device, so the four-lumped-capacitor model is more practical to represent its terminal characteristics. Again, if we assume that the primary and secondary windings have the same length, which is the case for the matrix transformer, the total displacement current can be calculated as [32]

$$i_{\text{dis}} = \frac{C_0}{2}\dot{V}_{\text{A}} + \frac{C_0}{2}\dot{V}_{\text{B}} - \frac{C_0}{2}\dot{V}_{\text{C}} - \frac{C_0}{2}\dot{V}_{\text{D}}. \tag{19}$$

The total displacement current can also be derived as

$$\begin{aligned} i_{\text{dis}} = {} & (C_{\text{AC}} + C_{\text{AD}})\dot{V}_{\text{A}} + (C_{\text{BC}} + C_{\text{BD}})\dot{V}_{\text{B}} \\ & - (C_{\text{AC}} + C_{\text{BC}})\dot{V}_{\text{C}} - (C_{\text{AD}} + C_{\text{BD}})\dot{V}_{\text{D}}. \end{aligned} \tag{20}$$

According to the principle of conservation of the displacement current, we have

$$C_{\text{AC}} = C_{\text{BD}} = C_{\text{BC}} = C_{\text{AD}} = \frac{C_0}{4}. \tag{21}$$

Since all the interested parameters are expressed by a, b_{w}, and the fixed parameters, the local optimization objective can be written as a function of a and b_{w} as well

$$f(a, b_{\text{w}}) = \min\{W_1 \cdot P_{\text{total}}(a, b_{\text{w}}) + W_2 \cdot V(a, b_{\text{w}})\}. \tag{22}$$

By sweeping a and b_{w}, the plot of $W_1 \cdot P_{\text{total}}(a, b_{\text{w}}) + W_2 \cdot V(a, b_{\text{w}})$ can be obtained. The constraints will work as the boundary conditions and shape the plot. The minimum value of the plot is the local optimal design for the selected set of discrete free parameters.

E. Global Optimization and Validation

The same optimization process should be conducted for each combination of discrete free parameters. After all the combinations are evaluated and compared, the global optimal design is found out. Next, the thermal performance of this design should be validated by CFD or FEA thermal simulation. If the temperature rise is too much, the lower limits for the side length of core cross-sectional area (a) or the PCB winding width (b_{w}) should be elevated, and the optimization process should be conducted once again until the temperature rise of the global optimal design meets the requirement. Then, the global optimal design is considered as the final design.

For the implementation of the proposed design methodology, only numerical calculations are required except for the thermal simulation, which makes the optimization process simple and fast.

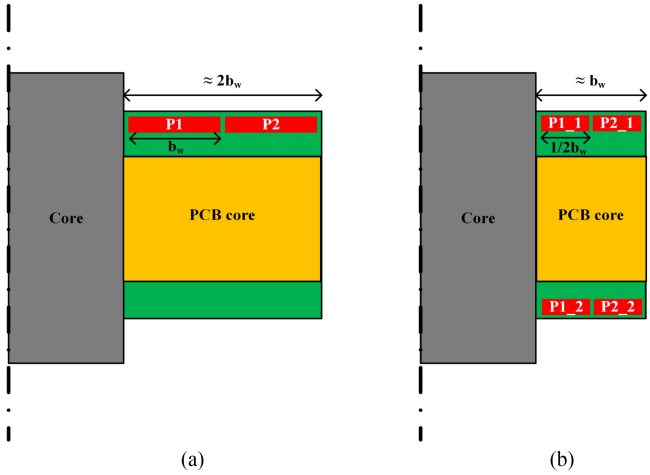

Fig. 9. (a) Parallel routing strategy to reduce the intrawinding capacitance. (b) Split-turn routing strategy to reduce the intrawinding capacitance.

III. Proposed Planar Transformer Design for the *CLLC* Resonant Converter

A. Investigation of Low-Stray-Capacitance and Well-Heat-Dissipated Transformer Configuration and Tradeoff Analysis

1) Reduction of Intrawinding Capacitance: When the number of turns for each winding is determined, the key is to cut down the turn-to-turn intrawinding capacitance. According to (16), two practical approaches can be taken. One is to reduce the physical stray capacitance between adjacent turns. The other approach is to minimize the electric field intensity between turns.

To reduce the physical stray capacitance, either cutting down the overlapping area or increasing the distance between adjacent turns can be employed. The parallel routing (horizontal routing) of adjacent turns is an effective way to reduce the overlapping area, as shown in Fig. 9(a). The overlapping area is decreased from the winding length by width to the winding length by thickness, and the thickness of PCB windings is typically much smaller than the width of PCB windings. However, this approach increases the winding footprint area because the vertical space in the PCB has not been utilized.

To minimize the electric field intensity between turns, the split-turn strategy can be applied. As shown in Fig. 9(b), one turn is split into two parts, and the two paralleled half-turns are aligned with each other vertically (P1_1 and P1_2; P2_1 and P2_2). Since there is no voltage difference along the winding between the two half-turns, the equivalent stray capacitance between them is zero. Then, the intrawinding capacitance is determined by the stray capacitance between paralleled adjacent half-turns, which has been significantly reduced. If the insulation distance between adjacent turns is assumed to be negligible compared with the winding width, the winding footprint area is half of the footprint area of the configuration in Fig. 9(a). However, multiple layers are required for each winding in this structure.

2) Reduction of Interwinding Capacitance: Similarly, the interwinding capacitance can be cut down by either reducing the physical stray capacitance or minimizing the electric field intensity between the primary winding and the secondary winding. The principle of the shielding layer approach [31], [32] is actually minimizing the voltage difference between the shielding layer and the secondary winding, so the equivalent interwinding capacitance between the shielding layer and the secondary winding is zero. As mentioned before, the major drawback of employing a shielding layer is the increased eddy current loss, which lowers the system efficiency. Therefore, reducing the physical stray capacitance between the primary winding and the secondary winding is investigated in this article. Combined with the methods of reducing the intrawinding capacitance, four different winding configurations are shown in Fig. 10 to cut down both the intrawinding capacitance and the interwinding capacitance. A four-layer PCB is utilized, and the primary and secondary windings are both assumed to have two turns, which is for the case of a 1:1 transformer or a unit core for a matrix transformer. The reference case is shown in Fig. 10(a), which has the commonly used interleaved winding structure [33]. The configuration in Fig. 10(b) reduces the interwinding capacitance by halving the overlapping area and increasing the distance between the primary and secondary windings. According to a standard 1.6-mm four-layer PCB stack-up, the distance between the two middle layers (PCB core) is 1200 μm, while the distance between the top two layers and the distance between the bottom two layers are only 140 μm. The configuration in Fig. 10(c) reduces the interwinding capacitance by halving the overlapping area.

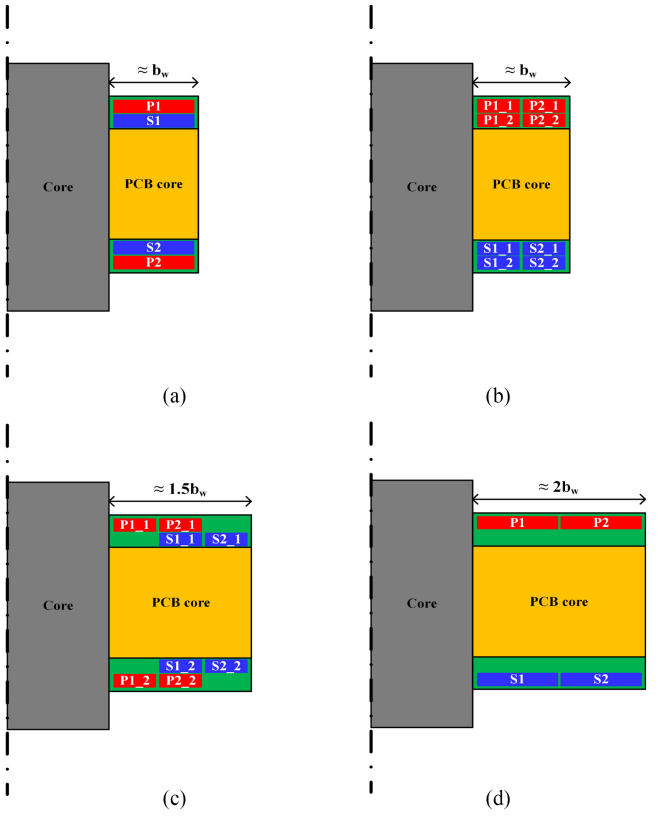

Fig. 10. (a) Conventional interleaved winding structure (reference). (b) Split-turn noninterleaved winding structure. (c) Split-turn interleaved and partially misaligned winding structure. (d) Paralleled routing winding structure.

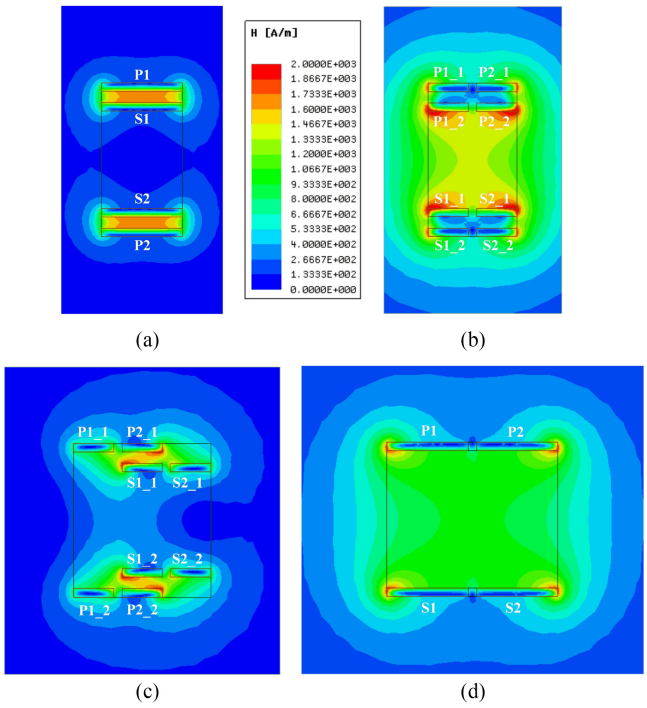

Fig. 11. Magnetic field intensity distributions for different winding configurations. (a) Conventional interleaved winding structure (reference). (b) Split-turn noninterleaved winding structure. (c) Split-turn interleaved and partially misaligned winding structure. (d) Paralleled routing winding structure.

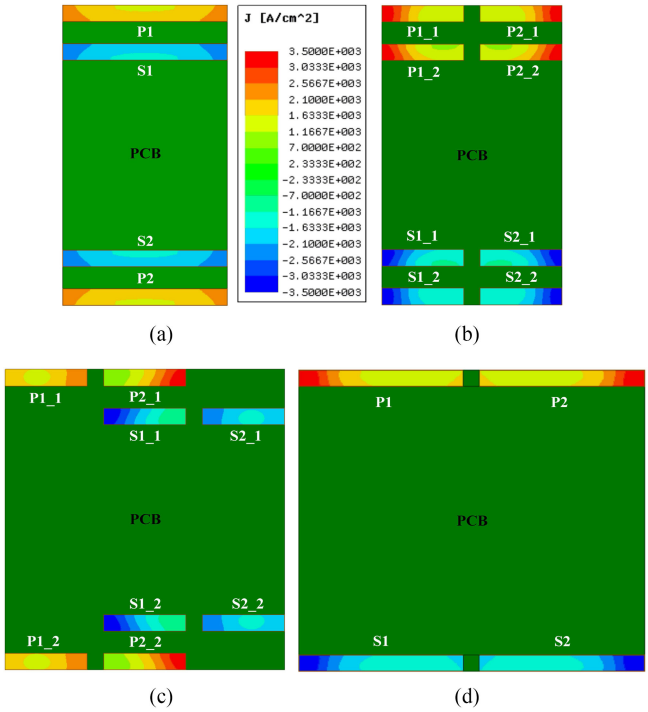

Fig. 12. Current intensity distributions for different winding configurations. (a) Conventional interleaved winding structure (reference). (b) Split-turn noninterleaved winding structure. (c) Split-turn interleaved and partially misaligned winding structure. (d) Paralleled routing winding structure.

TABLE II
PER-UNIT VALUE OF INTERESTED PARAMETERS FOR DIFFERENT WINDING CONFIGURATIONS

Parameters	Case (a)	Case (b)	Case (c)	Case (d)
Intra-winding capacitance	1	1.57	1.42	0.24
Inter-winding capacitance	1	0.065	0.187	0.082
Leakage inductance	1	3.99	1.66	4.81
AC winding loss	1	1.22	1.17	1.13
Winding footprint area	1	1	1.5	2

The interleaved winding structure is still maintained. Finally, the configuration in Fig. 10(d) reduces the interwinding capacitance by increasing the distance between the primary winding and the secondary winding.

To compare the above winding configurations, FEA simulations are employed. The magnetic field intensity distributions for different scenarios are shown in Fig. 11. The current density distributions for different scenarios are shown in Fig. 12. The total intrawinding capacitance (the sum of primary and secondary sides), interwinding capacitance, leakage inductance value, ac winding loss, and the winding footprint area are evaluated for all configurations and summarized in Table II. It should be noticed that the corresponding parameters for the reference case [case (a)] are regarded as the per unit for each row in the table, and the insulation distance between the adjacent turns is assumed to be negligible compared with the winding width.

For the intrawinding capacitance, case (d) exhibits the minimum value. For case (b), there is no voltage difference between the two paralleled half turns (P1_1 and P1_2; P2_1 and P2_2), but the voltage difference between the two diagonal half turns (P1_1 and P2_2; P2_1 and P1_2) is not zero. This is the reason why the intrawinding capacitance of case (b) is higher than the reference case [case (a)]. The same reason applies for case (c). To cut down the intrawinding capacitance, the winding configuration in case (d) is the best option.

In terms of the interwinding capacitance, both cases (b) and (d) present less than 10% of the interwinding capacitance value for the reference case. Since case (b) has much higher intrawinding capacitance compared with case (d), case (d) is the best choice by taking consideration of both the intrawinding capacitance and the interwinding capacitance.

However, case (d) displays the largest leakage inductance among all the cases due to the increased space between the primary winding and the secondary winding. Based on the FEA simulation in Fig. 11(d), the overall magnetic field intensity is still kept low, which will not magnify the ac winding effect significantly. The quantitative analysis of ac winding loss is conducted in the next paragraph. For the leakage inductance value in a single PCB, it is normally no more than several 100 nH [18]. If the *LLC*/*CLLC* resonant converter is designed for variable-frequency operation (device-to-device (D2D) operation), the required resonant inductance value is usually in the microhertz range. The increased leakage inductance in the PCB can be used as part of the resonant inductor. If the *LLC*/*CLLC* resonant converter is designed for fixed-frequency operation

(DCX operation), the required resonant inductance value can be very small. The increased leakage inductance in the PCB can be used as the entire resonant inductor. For both scenarios, the increased leakage inductance in the PCB will not affect the system operation.

Another crucial concern of employing a novel winding structure is the increased ac winding loss. From the FEA simulation results, the ac winding loss for cases (b), (c), and (d) is all higher than the reference case. Case (d) produces the minimum additional ac winding loss, which is 13% higher than the reference case. Suppose that the transformer efficiency is 99%, and the core and winding losses are nearly equal. The additional ac winding loss will only cause 0.065% drop of the transformer efficiency. Moreover, according to the current density distribution in Fig. 12(d), only the edge of the turns has significantly higher current density (edge effect). When the width of the turns is extended, the ratio of the high-current-density portion will be reduced. Hence, the extra ac winding loss will be diminished as well. Based on the FEA simulation result, when the winding width by thickness ratio is 40:1, the extra ac winding loss compared with the reference case becomes less than 5%. For cases (b) and (c), since the winding width is half of that in case (d), the ratio of the high-current-density portion is larger than that in case (d), which leads to the smaller effective conduction area. Therefore, more ac winding loss will be produced by cases (b) and (c).

The increase of the DCR of the winding should be considered as well. For cases (b), (c), and (d), since the paralleled routing strategy is employed in one layer, the equivalent winding length of the outer turn is larger than that of the inner turn, which causes the increase of the DCR of the winding. This issue can be released by utilizing the matrix transformer structure. The matrix transformer is defined as an array of elemental transformers interwired to form a single transformer [43]. It has been successfully used for high-turn-ratio applications [13], [19], [33], [36]. The key is to split a single core into multiple identical cores or pillars and employ very few number of turns for each unit. The matrix transformer boosts the space utilization rate and reduces the footprint, because of the high core area by the winding–area ratio. Since very few turns (normally one to two turns) are wound for each unit core or unit pillar in one layer, the increase of the equivalent winding length is insignificant. Meanwhile, as mentioned earlier, the EV OBC belongs to high volt–second and low-current applications. The core cross-sectional area dominates the transformer footprint, and the winding width is significantly smaller compared with the core dimension. Therefore, the percentage for equivalent winding length increase is minor.

The reduction of the transformer winding stray capacitance will benefit the system efficiency. During the dead time, the magnetizing current will charge and discharge both the device junction capacitances and the transformer winding stray capacitance, as shown in Fig. 2. The junction capacitance of the discrete WBG device is normally in the range of tens of picofarads to 200 pF. It is in the same range or even smaller than the planar transformer winding stray capacitance. If the *CLLC* converter operates at fixed frequency (DCX operation), the magnetizing inductance is designed only for the sake of achieving ZVS. If the transformer winding stray capacitance dominates in the paralleled capacitive branch shown in Fig. 2, the reduction of the winding stray capacitance will diminish the required magnetizing current significantly. Then, the primary-side device conduction loss and the winding loss will be reduced because of the diminished total current. The percentage of the loss reduction depends on the ratio of the magnetizing current to the load current. This loss reduction will be very obvious for light-load conditions. If the *CLLC* converter operates at variable frequency (D2D operation), the magnetizing inductance value is normally designed to satisfy the desired voltage regulation capability. For this scenario, although the magnetizing current is not reduced, the dv/dt of the switch will be increased for the case with smaller winding stray capacitance, which cuts down the device switching loss. Moreover, since the transformer stray capacitance draws less current, the magnetizing current is large enough to charge and discharge higher junction capacitance value. Therefore, higher current rating device can be utilized without the worry of losing ZVS. For the same voltage rating, the device Rdson is almost reversely proportional to device current rating. The device conduction loss will be significantly reduced. Based on the above discussion, the reduction of the winding stray capacitance can boost the system efficiency significantly; hence, a little compromise of the transformer winding loss is reasonable.

The winding footprint area is doubled for case (d). However, as mentioned before, the EV OBC belongs to high volt–second and low-current applications. The core cross-sectional area dominates the transformer footprint, so the increased winding footprint area will not increase the transformer footprint significantly. Meanwhile, since all the conductors are in the outer layers of the PCB, the thermal dissipation capability is improved. The winding width can be diminished to save the winding footprint area. Moreover, the EMI filter size can be cut down because of the significantly reduced interwinding capacitance (91.8% reduction). If the interwinding capacitance is the dominate path for the CM current in the circuit, the magnitude of the CM noise will be reduced by 21.7 dB, which is almost as good as the shielding layer technique claimed in [44]. The system power density can be improved. Therefore, the paralleled routing structure [case (d)] can significantly cut down both the intrawinding capacitance and the interwinding capacitance with little compromise or even boost of the system efficiency and power density. This winding structure is selected as the proposed low-stray-capacitance winding configuration.

Another observation from the FEA simulation results is the magnified leakage inductance and the ac winding loss in case (c), though the interleaved structure is employed. It is because the vertical misalignment between the primary winding and the secondary winding weakens the magnetic field canceling. The uncanceled magnetic flux will enhance the ac winding effect and lead to higher winding loss. Therefore, the primary winding and the secondary winding should be vertically overlapped as much as possible to maintain the good magnetic flux canceling.

3) Enhancement of Winding Thermal Dissipation: By placing the windings on the outer layers of the PCB, the thermal

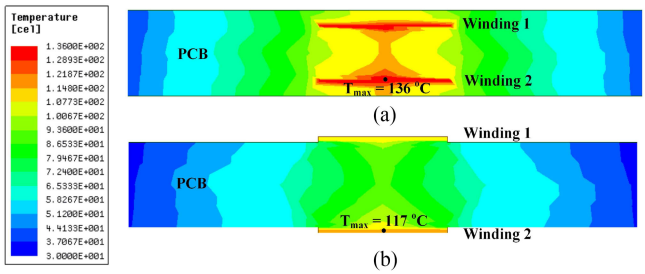

Fig. 13. (a) CFD thermal simulation of inner-layer PCB windings. (b) CFD thermal simulation of outer-layer PCB windings.

TABLE III
SPECIFICATIONS AND FIXED PARAMETERS OF THE DESIRED PLANAR TRANSFORMER

Parameters	Values
Operating frequency	500 kHz
Primary side voltage	±900 V (square wave)
Primary side current	11.3 Arms
Secondary side current	8.7 Arms
Turns ratio	2:1:1
Desired magnetizing inductance	31 μH
Selected core material	Hitachi ML27D
Insulation space	$\delta_{pp} = \delta_{ss} = 20$ mil; $\delta_{ps} = \delta_{cp} = \delta_{cs} = 80$ mil
PCB thickness	1.6 mm

dissipation capability of the windings will be improved, because the heat transfer coefficient is elevated. CFD thermal simulations are conducted for inner-layer PCB windings and outer-layer PCB windings, respectively (see Fig. 13). Each winding is set to generate the same power loss, and the PCBs receive 20-ft^3/min top-side forced-air cooling. The ambient is set to be 20 °C. It is shown that the maximum temperature for the outer-layer PCB winding is around 20 °C lower than that for the inner-layer PCB winding at the same condition.

To sum, the keys for constructing a low-stray-capacitance and well-heat-dissipated planar transformer are listed as follows.

1) Each winding should only be routed in one layer. There should not be any vertical overlapping between different turns of the same winding.
2) Primary and secondary windings should be vertically overlapped as much as possible.
3) Primary and secondary windings should be placed in the two outer layers of the PCB.

B. Optimization of the Proposed Planar Transformer

A high-efficiency high-power-density planar transformer is required to be designed for the 6.6-kW/500-kHz *CLLC* resonant converter in Fig. 1. The design and optimization process follows the methodology proposed in Section II.

First, the specifications and fixed parameters of the desired planar transformer are listed in Table III. The objective is to design a high-power-density transformer with efficiency higher than 98.9%. According to (1), the objective function is a weighting function of the transformer total loss and the box volume, which is a multiobjective function. In order to simplify the optimization process, it is proposed here to simplify it into a single-objective function about the box volume. The total loss (or efficiency) becomes a constraint in the optimization. Therefore, the local objective function can be written as

$$f(a, b_w) = \min\{V(a, b_w)\}$$
$$\text{Efficiency constraint: } P_{total}(a, b_w) < 1.1\% \times 6.6\,\text{kW}. \quad (23)$$

Except for the efficiency constraint, other applied constraints include core maximum flux density and winding maximum current density

$$B_{max} < 0.52\ \text{T}(B_{sat})$$
$$J_{max} < 3300\ \text{A/cm}^2. \quad (24)$$

Second, the number of cores, core shapes, and PCB winding configurations need to be established. Since the required turns ratio is 2:1:1, the primary number of turns is not equal to the secondary number of turns. It is not practical to use a single core to achieve the proposed winding configuration. Two cores with 1:1 turns ratio can be series connected in the primary side to construct a 2:1:1 matrix transformer. For each unit core or pillar, it is easy to implement the 1:1 turns ratio. The primary winding and secondary winding can be routed in exact the same fashion. The perfect vertical overlapping between the primary and secondary windings will minimize the leakage inductance and ac winding loss. By series-connecting the core units, it is easy to achieve high turns ratio without losing the benefit of almost perfect magnetic flux canceling.

In this design, two U-I cores are interwired as a matrix transformer to utilize the proposed winding structure. The core and winding configuration is shown in Fig. 14; the primary windings are placed on the top layer and the secondary windings are placed on the bottom layer. The primary windings of the two cores are both on the top layers. They are series connected by a PCB trace in a middle layer or by a jumper wire. The secondary windings are independent for each core. The arrows in Fig. 14 represent the corresponding current direction. It is clear that the secondary-induced current direction is opposite to that of the primary current, which achieves the flux canceling between the primary and secondary windings.

Next, one combination of the discrete parameters (m, N_0, and t_w) needs to be selected. Obviously, for the proposed winding structure, there is no vertical overlapping for primary winding or secondary winding itself, so the number of layers for each winding (m) is equal to 1. Since the operating frequency is 500 kHz, the winding thickness (t_w) should not exceed 3 oz, in order to avoid excessive ac winding loss due to skin and proximity effects. Meanwhile, the optimization objective is to find the minimum box volume of the planar transformer; hence, it is reasonable to use a thicker PCB winding for saving the footprint area. The number of turns for each layer (N_0) should not be a large integer because it will increase the footprint area, as well as the transformer box volume. Moreover, for the proposed split-core winding structure, N_0 should be an integer multiple of 4, which means at least one turn of winding is wound on each pillar of each unit core. To sum, the combinations of the discrete

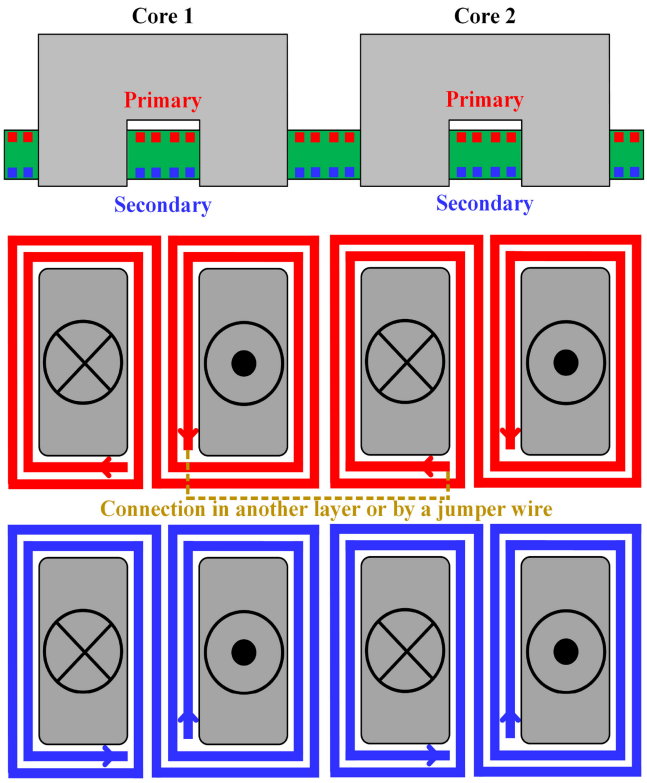

Fig. 14. Core and winding configuration of the proposed planar matrix transformer.

free parameters are listed as follows:

$$m = 1,\ t_{\mathrm{w}} = 3,\ N_0 = 4, 8, 12, 16, 20, 24, 28\ldots. \tag{25}$$

Then, local optimization can be conducted by sweeping the core cross-sectional area side length (a) and the winding width (b_{w}). Here, the length-by-width ratio of the cross-sectional surface (k_0) is selected as 6 to match the dimension of other components in the power converter and boost the system power density. The plot of $V(a, b_{\mathrm{w}})$ for one of the local optimizations ($m = 1$, $t_{\mathrm{w}} = 3$, and $N_0 = 8$) is shown in Fig. 15. The edge in this plot is shaped by the constraints. The lower limit of a is restricted by the B_{sat} and the efficiency constraints, and the lower limit of b_{w} is confined by the $J_{\max}$ and the efficiency constraints. The efficiency constraint also removes points from the plane, which causes the serrated edge. The local optimal design is found out with the transformer box volume of 127.7 cm^3. Meanwhile, since the core loss, winding loss, and total loss are all functions of the cross-sectional area side length (a) and the winding width (b_{w}), the 3-D plot of the core and winding losses for different design points can be obtained, as shown in Fig. 16. From the 3-D plot, it is clear that our optimal design (minimum box volume) does not present the minimum total loss, but the total loss of our optimal design point satisfies the efficiency constraint (98.9%). It is reasonable to sacrifice a little bit of efficiency to achieve much higher power density.

The same process is conducted for other N_0 values, which is to place different number of turns on each layer. Table IV presents the minimum transformer box volume for different N_0.

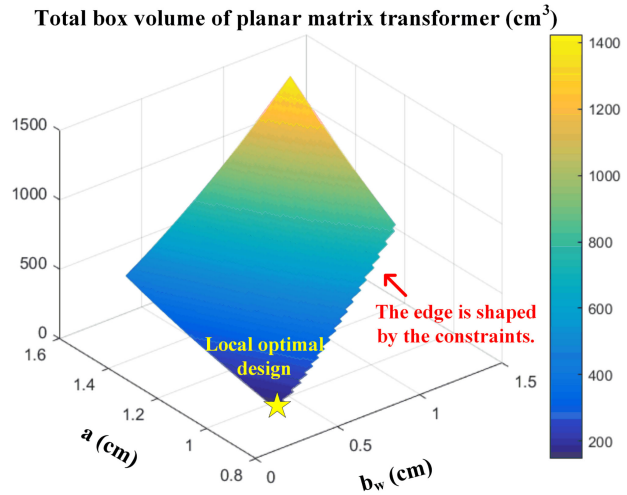

Fig. 15. Local optimization (minimum box volume) at $m = 1$, $t_{\mathrm{w}} = 3$, and $N_0 = 8$.

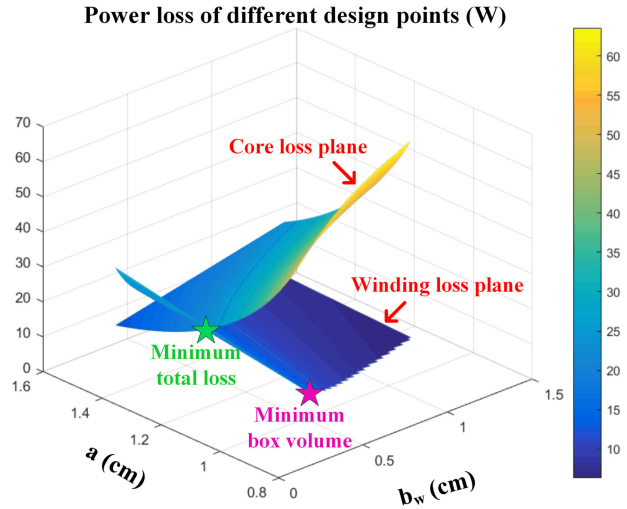

Fig. 16. Power loss for different design points of the planar matrix transformer at $m = 1$, $t_{\mathrm{w}} = 3$, and $N_0 = 8$.

TABLE IV
MINIMUM TRANSFORMER BOX VOLUME AND MINIMUM TRANSFORMER FOOTPRINT AREA FOR DIFFERENT N_0

N_0	Minimum transformer box volume (cm^3)	Minimum transformer footprint area (cm^2)
4	No solution	No solution
8	127.7	70.3
12	122.1	73.6
16	127	87
20	149	108
24	183.7	135
28	190.3	196.8

Meanwhile, in terms of system power density, a smaller footprint area of the planar transformer is preferred. The system height is decided by the tallest component in the system. Due to the low-profile characteristics of the planar transformer, it is usually not the tallest component in the system. The minimum footprint area for different N_0 is listed in Table IV as well.

TABLE V
KEY PARAMETERS FOR THE GLOBAL OPTIMAL DESIGN

Parameters	Values
Power rating	6.6 kW
Operating frequency	500 kHz
Number of cores	2
Core material	Hitachi ML27D
Core side length a_1, a_2	5.34 cm, 0.89 cm
Core cross-section area	4.75 cm^2
Maximum flux density	118 mT
Turns ratio	2:1:1
Number of turns	8 (pri.); 4 (sec.); 4 (sec.)
Winding thickness t_w	3 oz (105 μm)
Winding width b_w	100 mil (2.54 mm)
Core loss	50.6 W
Winding loss	18.9 W
Total loss	69.5 W
Efficiency	98.9%

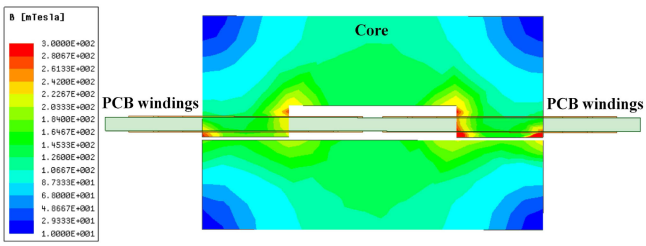

Fig. 17. Electromagnetic FEA simulation (Maxwell 3-D transient) for the global optimal design.

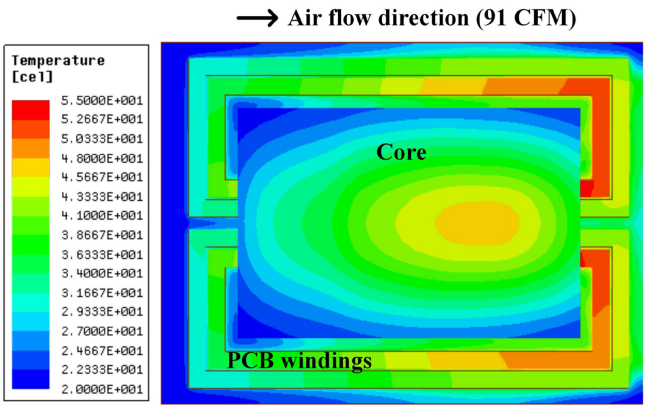

Fig. 18. Thermal CFD simulation (Icepak steady state) for the global optimal design.

To consider both the minimum box volume and the minimum footprint area, $N_0 = 8$ is selected as the global optimal design, which has exactly the same core and winding structure shown in Fig. 14. The key parameters of the global optimal design are listed in Table V.

To validate the global optimal design, electromagnetic FEA simulation and thermal CFD simulation are conducted for each unit U-I core. The results are shown in Figs. 17 and 18, respectively. From the electromagnetic simulation, the average B_{max} for the cross-sectional area is 114 mT, which basically coincides with the designed value. Then, the generated core loss and winding loss are imported into the thermal model. The ambient temperature is set to be 20 °C, and the planar transformer receives 91-ft^3/min forced-air cooling, which is the air flow of the selected fan blower. The simulated temperature rise is acceptable for this design, so the global optimal design is considered as final.

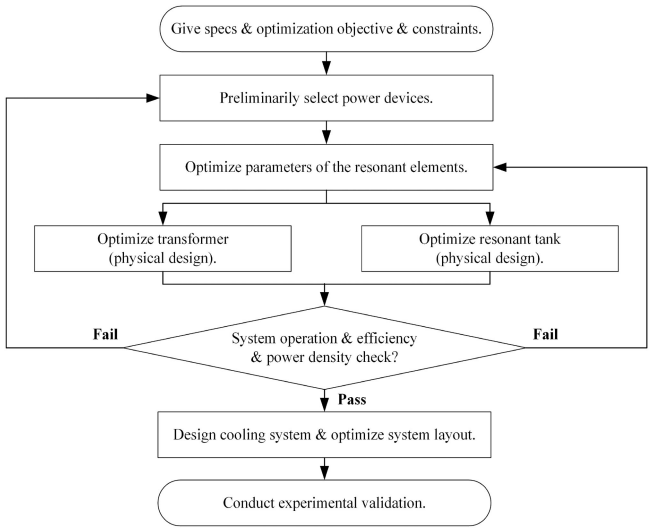

Fig. 19. System design and optimization of the *CLLC* resonant converter.

IV. SYSTEM DESIGN AND OPTIMIZATION OF THE *CLLC* RESONANT CONVERTER

The flowchart of system design and optimization for the high-efficiency and high-power-density *CLLC* resonant converter is demonstrated in Fig. 19. The system design and optimization process is illustrated as follows.

A. System Specifications, Constraints, and Optimization Objectives

The system specifications include the selected circuit topology, input voltage range, output voltage range, the load range, and the resonant frequency. The system constraints include the efficiency and the box volume (power density). The optimization objective can also be the system efficiency or system power density or a weighting function of the efficiency and the power density for general cases.

B. Power Device Preliminary Selection

According to the system input and output voltage range requirements, the 1.2-kV SiC power MOSFET should be selected for the primary-side converter, while the 600/650-V GaN HEMT should be selected for the secondary-side converter. In terms of the current rating, a higher current rating device will have a smaller Rdson, which can reduce the conduction loss and improve system efficiency. However, a higher current rating device has a larger junction capacitance, which requires more magnetizing current to achieve ZVS. The increased magnetizing current may backfire the system efficiency. For this step, the power devices can be initially chosen. If the designed system efficiency does not meet the requirement, the power devices can be reselected. In this article, Wolfspeed 1200-V/30-A SiC

MOSFET (C3M0075120J) is selected for the primary-side switch and GaN System 650-V/30-A GaN HEMT (GS66508B) is selected for the secondary-side switch.

C. Optimization of Parameters for Resonant Elements

The resonant elements consist of the resonant inductor (L_r), the resonant capacitor (C_r), and the transformer magnetizing inductance (L_m). The resonant elements and the load range directly determines the operating frequency range and the voltage regulation capability of the *CLLC* converter. The optimization of resonant element parameters is illustrated as follows.

1) Specify Fixed Parameters: The fixed parameters include the resonant frequency (f_r), the dead-time (t_d), the load range (R_{load}), and the required voltage regulation range for the *CLLC* converter. The fixed parameters can also be seen as system specifications. Although the variable dc-link solution significantly reduces the required voltage regulation range, the *CLLC* converter needs to compensate the double-line frequency voltage ripple (100 or 120 Hz) from the PFC output. Otherwise, the battery will endure a large ripple current [2]. If the peak-to-peak voltage ripple from the PFC dc link is 5%, the required voltage regulation range for *CLLC* is 0.975–1.025.

2) Determine the Constraints: The first constraint is the efficiency requirement. To achieve the requirement, first, ZVS needs to be guaranteed at any operating points to avoid the excessive switching loss. The ZVS constraint defines the upper limit of the magnetizing inductance (L_m)

$$L_m \le \frac{t_d}{8(C_{oss1} + C'_{oss2} + C_{stray}) \cdot f_{max}} \tag{26}$$

where C_{oss1} is the primary device junction capacitance, C'_{oss2} is the secondary device junction capacitance referred to the primary side, C_{stray} is the transformer total stray capacitance referred to the primary side, and f_{max} is the maximum operating frequency.

Second, the operating frequency range should be restricted as well, since the efficiency drops significantly if the operating frequency is far away from the resonant frequency. Usually, the resonant frequency (f_r) is selected as the center of the operating frequency. The minimum operating frequency (f_{min}) and the maximum operating frequency (f_{max}) can be initialized at certain range. The operating frequency range should be narrowed if the efficiency constraint is not fulfilled.

The next constraint is the monotonicity of the gain curve. For the *CLLC* resonant converter, the gain curve can be nonmonotonic during the desired operating frequency range (shown in Fig. 20). This characteristic brings trouble for linear control [45]. The gain curves are different for different load conditions or quality factors (Q), which is defined as the ratio of the resonant inductor impedance to the equivalent load resistance. To guarantee the monotonicity of the gain curve, the partial derivative of the gain with respect to the frequency should be negative for all operating frequency ($[f_{min}, f_{max}]$). The complete analytical expression of the gain with respect to the operating frequency can be referred to [45].

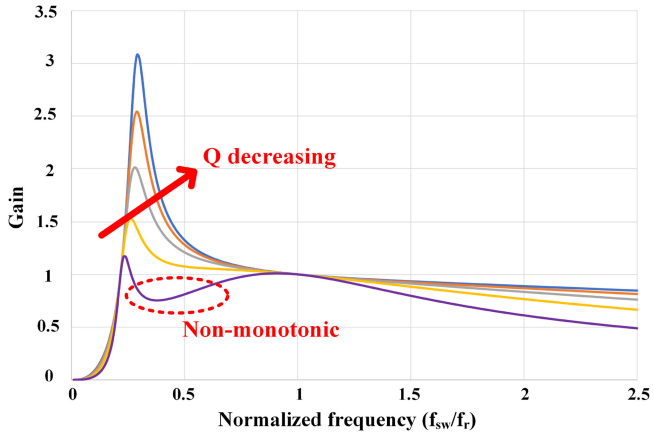

Fig. 20. *CLLC* family gain curves for different Q.

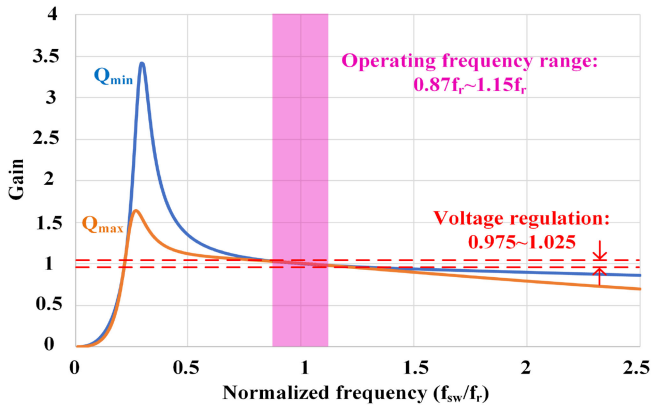

Fig. 21. Gain curves for optimized resonant element parameters.

The last constraint is that the required voltage regulation range needs to be achieved for any load conditions (Q).

3) Optimize System Efficiency and Power Density: The optimization target can be the system efficiency or power density or a weighting function of the efficiency and power density. In this article, the value of the resonant elements is optimized to improve system efficiency. A larger magnetizing inductance is preferred to reduce device conduction loss. The resonant inductance (L_r) and the ratio of the resonant inductance to the magnetizing inductance (L_r/L_m) are two free variables. The resonant capacitance is determined by L_r and the resonant frequency f_r. By sweeping the two free variables (L_r, L_r/L_m) within the constraints, the maximum magnetizing inductance can be found out. The calculation is based on the first harmonic approximation model [45]. The corresponding values are the optimal parameters for resonant elements.

By following the above procedure, the parameters of the resonant elements are optimized for the 6.6-kW/500-kHz *CLLC* resonant converter shown in Fig. 1. The optimized resonant element parameters are $L_r = L_{r1} = 2L_{r2} = 3.07$ μH, $C_r = C_{r1} = \frac{1}{2}C_{r2} = 33$ nF, and $L_m = 31$ μH. The corresponding gain curves for the heaviest load condition (Q_{max}) and the lightest load condition (Q_{min}) are demonstrated in Fig. 21. The operating frequency range of the *CLLC* converter is from 435 to 575 kHz

($0.87f_r$–$1.15f_r$). The voltage regulation range of the *CLLC* converter is 0.975–1.025 to compensate the 5% peak-to-peak voltage ripple from the PFC dc link.

D. Physical Design and Optimization of Transformer and Resonant Tank

After the resonant element parameters are determined, the physical design and optimization of transformer and resonant tank (L_r, C_r) can be conducted. The transformer design and optimization has already been thoroughly discussed in this article. For the design of the resonant inductor, as mentioned before, external inductors are employed in this article to alleviate the thermal stress of the high-power-density planar transformer. For the design of separate resonant inductors, both the planar inductor and the Litz-wire wound inductor can be utilized. The low-profile less-labor-intense planar inductor is selected in this article. The design and optimization of the planar inductor is very similar to the design of the planar transformer. Most of the design methodology proposed in Section II is applicable to the planar inductor design and optimization as well. There are only two crucial differences. First, the maximum flux density (B_{max}) in a planar inductor is determined by the peak current rather than the volt–second, since the resonant inductor voltage is not clamped by the source. Second, there is no flux canceling between the adjacent turns in an inductor because the current directions are all the same. Therefore, the number of turns for a planar inductor should be as few as possible to avoid the excessive ac winding loss.

For the resonant capacitor, film capacitors and ceramic capacitors can be taken into consideration. The ceramic capacitors usually exhibit smaller size, lower equivalent series resistance, and higher corner frequency. However, the voltage rating of ceramic capacitors is limited compared to film capacitors. For the selected full-bridge topology, the capacitor does not need to block any dc voltage, so the voltage rating requirement of the capacitor is significantly lowered. Meanwhile, multiple capacitors can be paralleled to reduce the thermal stress for each capacitor. Moreover, the capacitance value should be consistent under the operating temperature range. Eventually, the C0G/NP0 ceramic capacitors are employed in this article.

E. System Operation, Efficiency, and Power Density Check

After the power devices are selected and the magnetic components are designed and optimized, the system operation, efficiency, and power density can be checked. If any of the system requirements are not met, either reselecting the power devices or redesigning the resonant elements can be conducted.

F. Cooling System Design and System Layout Optimization

The cooling system usually takes a large portion of the system box volume. By the employment of forced-air cooling, the thermal resistance of the heat sinks can be significantly cut down; hence, a smaller heat sink can reach the desired thermal resistance. To achieve a high-power-density design, the system-level layout optimization is necessary. The key is to improve the space utilization rate or achieve a high space filling factor for the system box volume. To boost the space filling factor, the constrained dimension (the maximum dimension) in the system needs to be determined. For this design, the system length is determined by the length of the secondary-side GaN-based power converter due to the eight power devices and eight corresponding gate driver circuits. Therefore, the primary-side SiC-based converter, the transformer, the resonant tank, and the heat sinks can be extended to the same length. This is the reason why the transformer core cross-sectional length by width ratio is selected as 6. The system height is determined by PFC dc-link electrolytic capacitors. Although the PFC stage is not in the scope of this article, the *CLLC* resonant converter will be eventually combined with the PFC stage. Due to the low-profile characteristic of the planar transformer, its height is much lower than the system height. The resonant tank can be placed on the top or on the bottom of the planar transformer to construct the double-layer structure. In this way, the space filling factor is much increased, and the system power density is boosted. Moreover, the resonant inductors can be designed much larger to coordinate the length and width of the transformer. Therefore, the resonant inductor loss is much reduced. Although the total volume of the external inductor and the transformer may be bigger than that of a single integrated transformer, the system can still achieve high power density by optimizing the system layout.

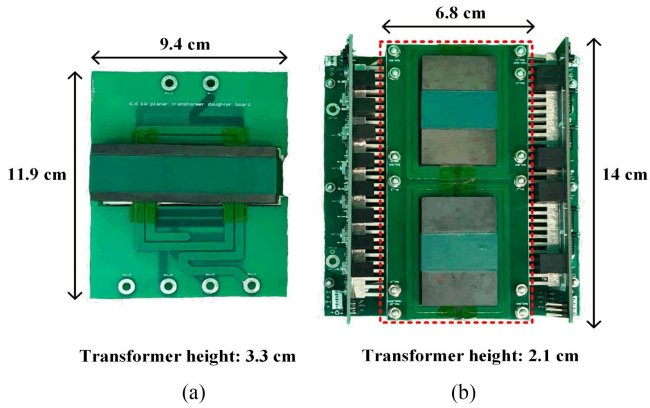

Fig. 22. Pictures of the two planar transformers. (a) Transformer 1. (b) Transformer 2.

V. Experimental Verification

To validate the proposed transformer design, two planar transformers are designed for the 6.6-kW/500-kHz *CLLC* resonant converter by following the methodology proposed in Section II. The first transformer prototype utilizes the conventional single E-I core with interleaved windings [see Fig. 4(a)], while the second transformer employs the proposed core and winding configuration (see Fig. 14). The two transformers are shown in Fig. 22. The key parameters are summarized in Table VI. To evaluate the circuit performance, two 6.6-kW/500-kHz *CLLC* resonant converter prototypes are built employing the two different transformer designs, respectively. The 6.6-kW full-load

TABLE VI
KEY PARAMETERS OF TWO PLANAR TRANSFORMER PROTOTYPES

Parameters	Transformer 1	Transformer 2
Core and winding configuration	Single E-I core with interleaved winding (Fig. 4(a))	Proposed configuration (Fig. 14)
Power rating	6.6 kW	6.6 kW
Operating frequency	500 kHz	500 kHz
Number of cores	1	2
Core material	Hitachi ML27D	Hitachi ML27D
Core cross-section area	8.07 cm^2	4.75 cm^2
Maximum flux density	93 mT	118 mT
Number of turns	6 (pri.); 3 (sec.); 3 (sec.)	8 (pri.); 4 (sec.); 4 (sec.)
Winding thickness	3 oz (105 μm)	3 oz (105 μm)
Winding width	160 mil (4.06 mm)	100 mil (2.54 mm)
Magnetizing inductance	31 μH	31 μH

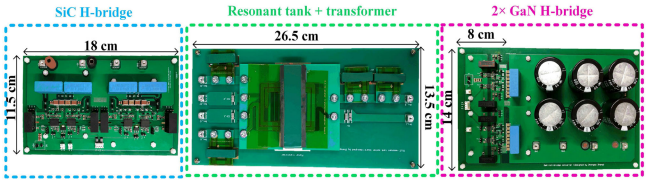

Fig. 23. Modular-designed 6.6-kW/500-kHz *CLLC* resonant converter prototype (prototype 1).

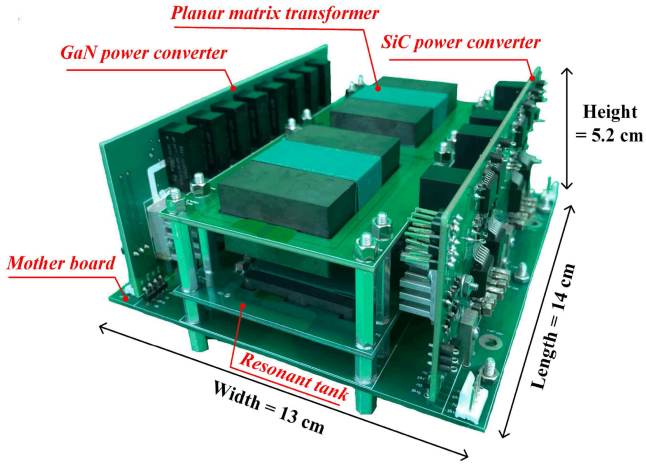

Fig. 24. Integrated-designed high-power-density 6.6-kW/500-kHz *CLLC* resonant converter (prototype 2).

tests are conducted for both prototypes. The battery charging profile is: when the battery voltage is below 300 V, the circuit output is controlled in the constant current mode (22 A); when the battery voltage is above 300 V, the circuit output is controlled in the constant power mode (6.6 kW). Prototype 1 is a modular-designed *CLLC* resonant converter with transformer 1, as shown in Fig. 23. Prototype 2 is an integrated-designed high-power-density *CLLC* with transformer 2, as shown in Fig. 24. The CREE C2M SiC MOSFET (C2M0080120D) is utilized in prototype 1 as the primary-side switch, and the CREE C3M SiC MOSFET (C3M0075120J) is utilized in the high-power-density

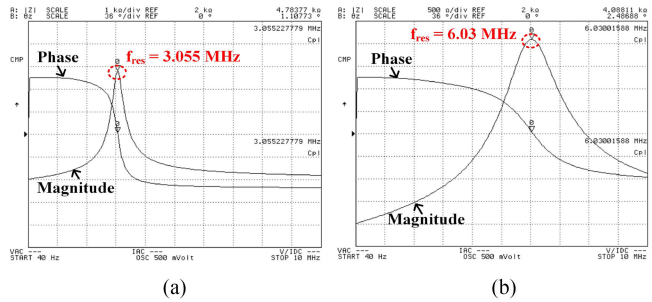

Fig. 25. (a) Measured open-circuit impedance curve of transformer 1. (b) Measured open-circuit impedance curve of transformer 2.

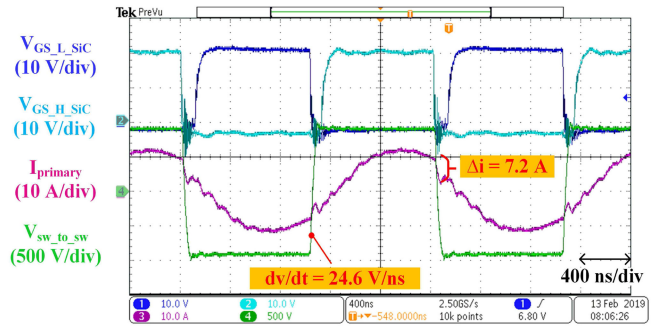

Fig. 26. Measured full-load primary-side waveforms of the *CLLC* resonant converter prototype 1 (450-V battery voltage and charging mode).

CLLC converter (prototype 2). The two devices have similar Rdson, which presents the similar per unit current conduction loss. The only difference is that the latter device has 27.5% smaller junction capacitance, which presents 27.5% higher dv/dt under the same magnetizing current in the switching transient. The secondary-side device is the same for the two *CLLC* resonant converters (GaN System GS66508B).

For the first challenge mentioned in the introduction section, the high intrawinding capacitance introduced soft-switching, transformer and converter efficiency, as well as waveform quality problems; the proposed design addresses them very well, which can be verified from the impedance curves in Fig. 25 and experimental waveforms in Figs. 26–29.

First of all, the winding stray capacitance of the two transformers can be obtained through measuring the input impedance on the primary side (by Agilent 4294A Impedance Analyzer), while keeping the secondary side open-circuited. The measured impedance curves for the two transformers are shown in Fig. 25. Since the secondary side of the transformer is open-circuited, the resonance occurs between the transformer magnetizing inductance and the total winding stray capacitance referred to the primary side. Based on the resonance frequency of the impedance curve and the magnetizing inductance value (31 μH for both designs), the total stray capacitance for transformers 1 and 2 can be calculated as 87.5 and 22.5 pF, respectively. Therefore, the total winding stray capacitance is almost cut down by four times compared with the conventional design (transformer 1).

Second, soft switching is fully achieved on both primary- and secondary-side switches at full operating range for prototype 2.

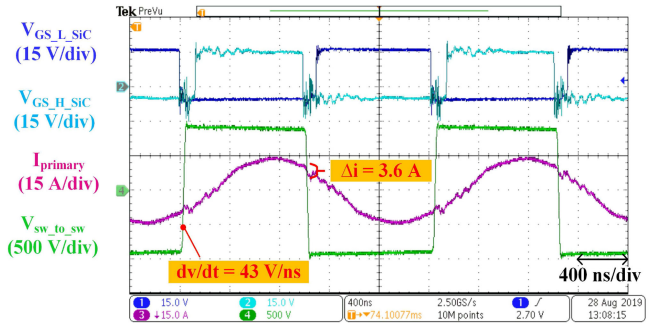

Fig. 27. Measured full-load primary-side waveforms of *CLLC* resonant converter prototype 2 (450-V battery voltage and charging mode).

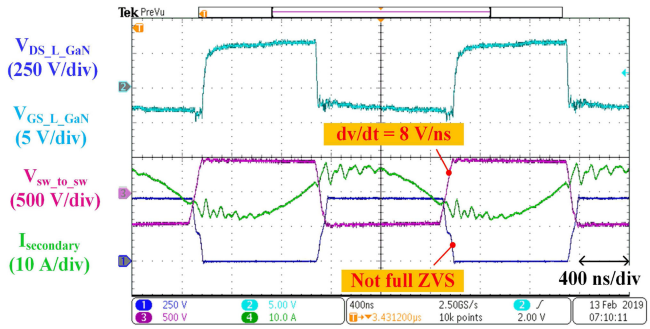

Fig. 28. Measured full-load secondary-side waveforms of *CLLC* resonant converter prototype 1 (450-V battery voltage and charging mode).

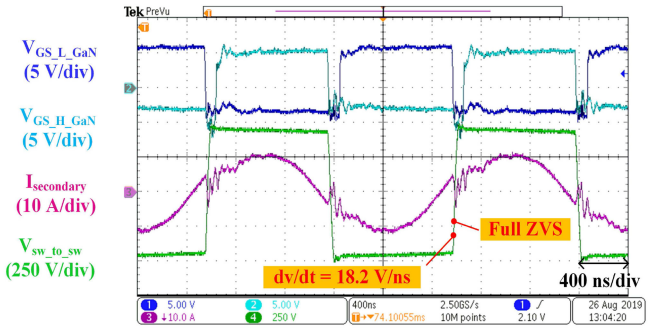

Fig. 29. Measured full-load secondary-side waveforms of *CLLC* resonant converter prototype 2 (450-V battery voltage and charging mode).

However, prototype 1 presents a soft-switching implementation with much lower dv/dt on the primary side and partial hard switching on the secondary side. As shown in Figs. 26 and 27, on the primary side, the dv/dt of prototype 2 is 1.75 times of the dv/dt for prototype 1. Here, the dv/dt labeled in the figures occurs between the two switching nodes. The dv/dt that arises between the device drain-to-source is half of the labeled value. This 1.75 times dv/dt increase is due to two reasons. One is that the four times smaller winding stray capacitance in prototype 2 will draw much less current from the magnetizing inductance, and the majority of the magnetizing current is used to charge and discharge the device junction capacitance during the switching transient. This can also be verified from the observation on the primary-side current drop at the beginning of the dead time. The magnitude of the current drop in prototype 1 (7.2 A, as shown in Fig. 26) is twice than the current drop in prototype 2 (3.6 A, as shown in Fig. 27). Another reason for the dv/dt increase is that the primary device in prototype 2 has 27.5% smaller junction capacitance, which results in 27.5% higher dv/dt. Since the final dv/dt increases by 75% from prototype 1 to prototype 2, the majority of the improvement comes from the winding stray capacitance reduction. This dv/dt improvement can benefit the efficiency (less switching loss). On the secondary side, the measured waveforms for prototypes 1 and 2 are shown in Figs. 28 and 29, respectively. The ZVS is not fully achieved in prototype 1 due to the lack of the charging and discharging current during the switching transient, so additional hard-switching loss will be generated. For prototype 2, thanks to the significantly reduced winding stray capacitance, the sufficient magnetizing current is diverted to the secondary side and ZVS is completely achieved at all operating conditions.

Third, the efficiency of prototype 2 is improved due to the stray capacitance reduction. Since prototypes 1 and 2 employ the same magnetizing inductance value, the conduction loss of the converters is similar. However, the much higher dv/dt in prototype 2 brings lower switching loss. Moreover, based on the testing waveforms for prototype 2, the dv/dt finishes much earlier than the end of the dead time, which means the magnetizing current is sufficient to charge and discharge much larger junction capacitance. If the switch with higher current rating is selected, the conduction loss will be significantly reduced due to the lower Rdson.

Fourth, the ac waveform quality in prototype 2 is improved, which can bring transformer loss reduction. The frequency of the ripple current increases from 10–15 to 20–30 MHz (resonance between the resonant inductor and the winding stray capacitance), so the total harmonic distortion is reduced significantly.

For the second challenge mentioned in the introduction section, the high interwinding capacitance is due to the conventional interleaved winding structure, the proposed design addresses it very well. The primary and secondary windings are placed on top and bottom layers, respectively, to cut down the large interwinding capacitance, which is verified by the impedance curve in Fig. 25 and experiment waveforms of Figs. 26–29. The total winding stray capacitance is reduced by 75%. At the same time, the leakage inductance and the ac winding factor (the ratio of ac winding loss by dc winding loss) have been reduced as well. The measured leakage inductance for transformer 1 is around 350 nH, and for transformer 2, it is around 100 nH, which is reduced by 72%. According to the measured efficiency for the two *CLLC* converter prototypes, the power loss breakdown for the two converters can be conducted, which are shown in Figs. 30 and 31, respectively. Based on the measured efficiency and the power loss breakdown, the winding loss of transformer 1 is 30 W, and the winding loss of transformer 2 is 24.6 W. The variance from the theoretical calculation is probably due to the connection and termination in the windings. The dc winding loss (calculated by winding DCR) in transformer 1 is 11 W, and in transformer 2, it is 16.7 W. Therefore, the ac winding factor of transformer 2 is 46% lower than transformer 1. For transformer 1, since the

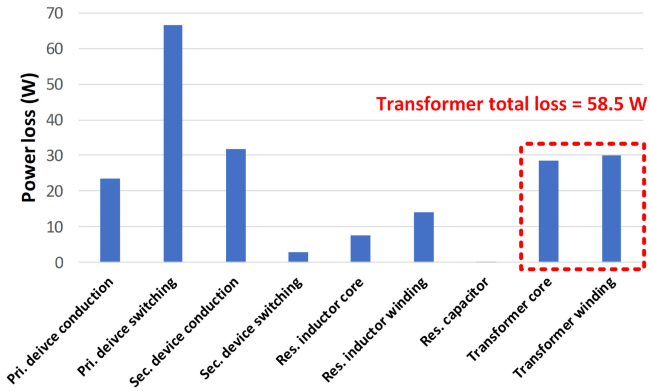

Fig. 30. Power loss breakdown of *CLLC* resonant converter prototype 1 (450-V battery voltage and charging mode).

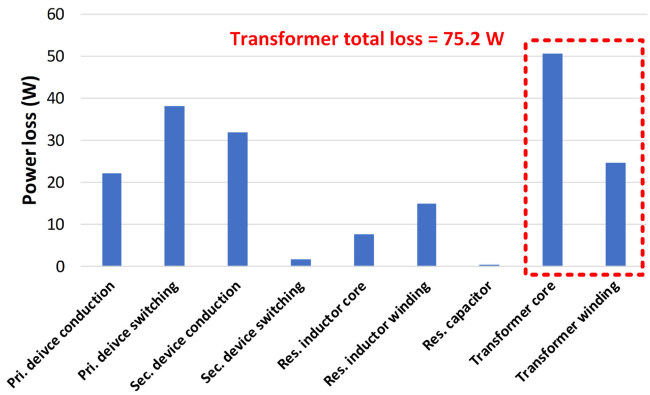

Fig. 31. Power loss breakdown of *CLLC* resonant converter prototype 2 (450-V battery voltage and charging mode).

interleaved winding structure is utilized, the leakage inductance and ac winding loss should be minimized. However, in practical implementation, since the PCB turns in the two nonadjacent layers need to be connected, the windings on the adjacent layers will not be perfectly vertically overlapped due to the insulation distance. Therefore, the leakage inductance and corresponding ac winding loss are increased due to the partial misalignment [see Fig. 11(c)]. For the proposed winding structure, because no connections are needed for nonadjacent layers, the primary and secondary windings can be perfectly vertically overlapped. The experimental results prove the characteristics of low leakage inductance and low ac winding loss of the proposed winding structure.

The third challenge mentioned in the introduction section is thermal management of the transformer; the proposed design addresses it very well. The pain point of the thermal management in transformer is the temperature rise at the winding. By placing all the windings on top and bottom layers of the PCB only, the temperature rise can be kept low enough to avoid the need for heat sinks. Extra eddy current loss in the heat sinks will be produced if heat sinks are utilized to cool down the magnetic cores and windings [46]. The improvement is verified by the temperature measurements during the full power testing. To compare the thermal performance of the two

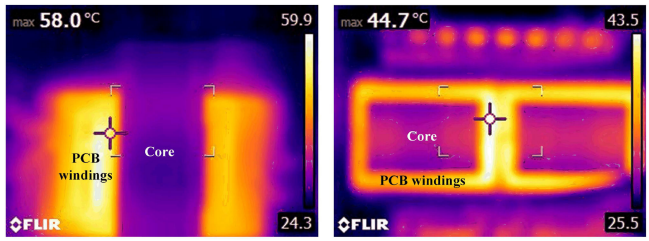

Fig. 32. (a) Thermal image of transformer 1 under full-load testing. (b) Thermal image of transformer 2 under full-load testing.

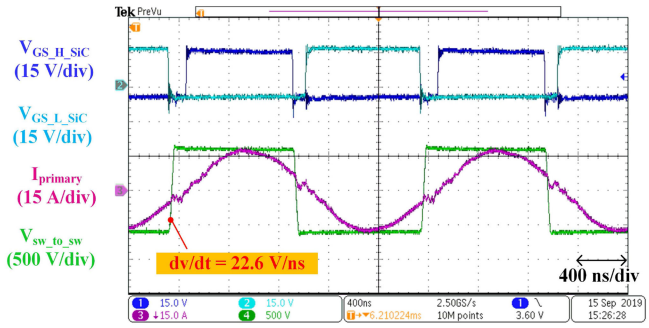

Fig. 33. Measured full-load primary-side waveforms of *CLLC* resonant converter prototype 2 (300-V battery voltage and charging mode).

transformers, the two *CLLC* prototypes are tested under the same ambient temperature (20 °C) and the same cooling condition. The corresponding thermal images are shown in Fig. 32. The maximum temperature of transformer 2 is 44.7 °C at its winding hot spot. The maximum temperature of transformer 1 is 58 °C at its winding hot spot. The temperature rise of transformer 2 is 13.3 °C lower than transformer 1, even though the winding current density of transformer 2 is 1.6 times higher. The proposed winding structure has much better thermal dissipation capability. It should be mentioned that the experimental temperature rise for transformer 2 seems lower than the CFD simulation in Fig. 18. The testing time may not be long enough for the transformer to reach its real thermal equilibrium, which results in the lower temperature rise, but the temperature distribution of the CFD simulation basically coincides with the experiment result.

Except addressing these three challenges, the optimization design methodology of the transformer and the *CLLC* system proposed in Sections II and IV brings significant improvements on the converter efficiency and power density.

To verify the efficiency improvement, the efficiency measurements are conducted for the 6.6-kW/500-kHz high-power-density *CLLC* resonant converter (prototype 2) under different battery voltage scenarios. The circuit operates at the constant current mode (22 A) at the low battery voltage range (250–300 V) and the constant power mode (6.6 kW) at the higher battery voltage range (300–450 V). The experimental waveforms for the 300-V battery voltage and charging mode case are shown in Figs. 33 and 34, and waveforms for the 320-V battery voltage and discharging mode case are shown in Figs. 35 and 36.

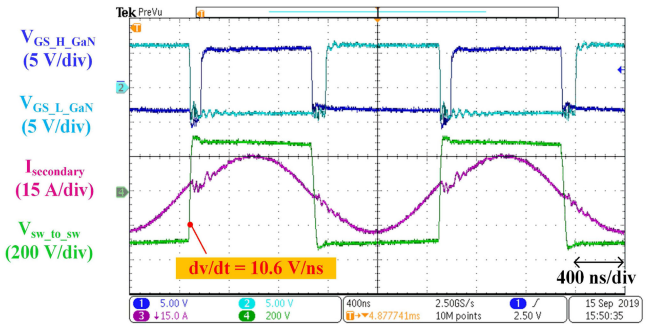

Fig. 34. Measured full-load secondary-side waveforms of *CLLC* resonant converter prototype 2 (300-V battery voltage and charging mode).

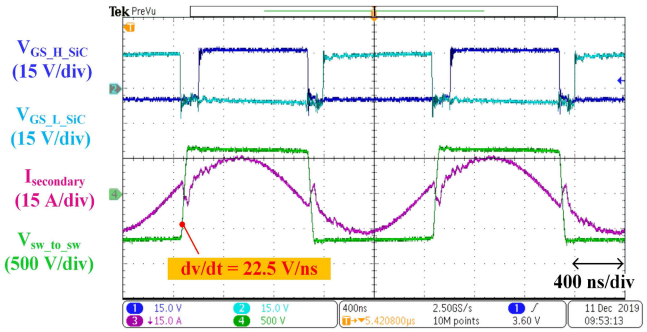

Fig. 35. Measured full-load secondary-side waveforms of *CLLC* resonant converter prototype 2 (320-V battery voltage and discharging mode).

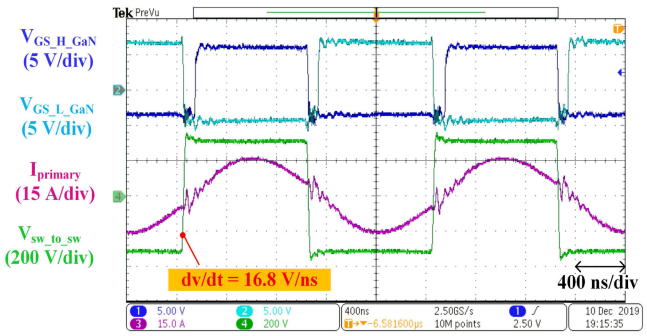

Fig. 36. Measured full-load primary-side waveforms of *CLLC* resonant converter prototype 2 (320-V battery voltage and discharging mode).

The efficiency is measured by the Yokogawa WT500 Power Analyzer. The measured efficiency with respect to different battery voltages in the charging mode is shown in Fig. 37. It is shown that the peak efficiency of the converter reaches 97.85% at the battery voltage of 400 V. The full-load efficiency (battery voltage $\geq$300 V) maintains above 97% for the entire battery charging profile. Compared to prototype 1, the system efficiency improves by 0.15–0.45%, as shown in Fig. 37. Compared to the state-of-the-art GaN-based [47] and Si-based [48] counterparts, the proposed design (prototype 2) exhibits 0.45–1.85% peak efficiency improvement and 0.54–2.08% average efficiency improvement, as shown in Fig. 37.

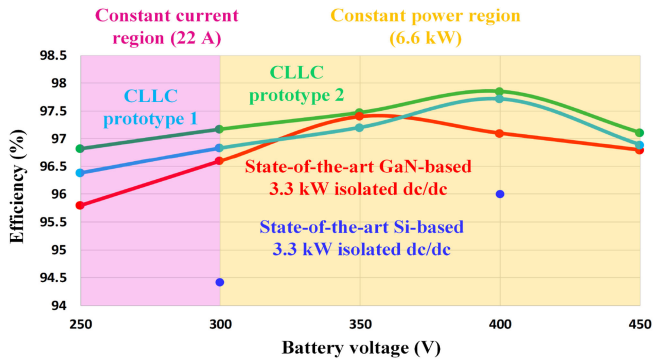

Fig. 37. System efficiency curves for different battery voltages (charging mode).

In terms of the power density, both the transformer and converters demonstrate significantly improved power density. For the transformer, the dimension changes from 11.9 cm $\times$ 9.4 cm $\times$ 3.3 cm to 14 cm $\times$ 6.8 cm $\times$ 2.1 cm, as shown in Fig. 22. Therefore, it is concluded that the proposed split core matrix transformer design and the winding configuration enhance the power density of the transformer by 46%. For the entire power converter, the dimension shrinks from 14 cm $\times$ 60.5 cm $\times$ 4 cm to 14 cm $\times$ 13 cm $\times$ 5.2 cm, as shown in Figs. 23 and 24. Therefore, the *CLLC* system power density is increased by 78%.

VI. Conclusion

This article proposes a novel core and winding configuration of a planar transformer to address the challenges of high intrawinding capacitance, high interwinding capacitance, and thermal management in the conventional planar transformers. The new design is verified through sufficient experimental tests. The test results validate that the proposed method can effectively address the three challenges, to achieve lower switching loss, lower transformer and converter loss, higher power density, and better thermal dissipation all at the same time. Moreover, the generalized design methodologies are proposed for the planar transformer and the *CLLC* system, respectively. It is validated through experiments that the optimized efficiency and power density can be achieved by following the proposed design steps and rules. Two 6.6-kW/500-kHz *CLLC* resonant converter prototypes are built, tested, and compared in the laboratory. Prototype 2, which employs the proposed transformer structure and the design methodologies, presents the outstanding 97.85% peak efficiency and 114-W/in^3 power density.

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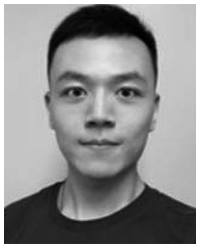

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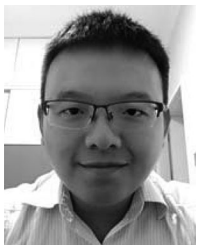

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