Fractal Approach Based Simplified and Generalized Sector Detection in Current Error Space Phasor Based Hysteresis Controller Applied to Multilevel Front-End Converters

M. T. Shah, *Member, IEEE*, Siddharthsingh K. Chauhan, *Member, IEEE*, and P. N. Tekwani, *Senior Member, IEEE*

***Abstract*—The current error space phasor (CESP) based hysteresis controller employed for front-end converter requires two (inner and outer) hysteresis bands for vector selection and sector detection, respectively. As a result of this, the CESP moves out of the fixed (hexagonal) inner boundary many times in one fundamental cycle (and touches outer hysteresis band) to detect appropriate sector. This distorts the supply current waveform and increases the implementation complexity. To provide effective solution to the said issue, in this article, a fractal approach with a triangularization technique is proposed and analyzed to eliminate the outer hysteresis band and lookup table for sector change detection. The novelty proposed in this article is the integration of the fractal approach to CESP-based hysteresis controller, which reduces the complexity of the implementation of CESP-based hysteresis controller for any general multilevel front-end converter. The detailed analysis of the proposed technique for sector detections is presented considering the voltage space phasor structure of three-level and five-level converters. A generalized flowchart for any multilevel converter employing CESP-based hysteresis controller with proposed sector detection technique is developed and presented. Laboratory prototype is developed for a three-level flying capacitor front-end converter with an effective capacitor voltage balancing scheme. The experimental results are presented to validate the effectiveness of the proposed current controller in terms of unity power factor and low harmonic distortion in the line current under various practical conditions.**

***Index Terms*—Current controller, fractal approach, generalized technique, multilevel front-end converter (FEC), sector detection, space phasor, triangularization.**

I. Introduction

INSULATED gate bipolar transistor (IGBT) based multilevel front-end converter (FEC) has become very popular for high power industrial, traction, and utility applications [1]–[4]. Most of the high-performance applications employ the current controller for FEC to get a fast dynamic response [5]–[8]. The current error space phasor based hysteresis controller (CESP-based HC) deals with the combined effect of the current errors in all the individual phases and monitors the movement of CESP. This controller allows switching of only adjacent voltage vectors in a given sector of voltage space phasor structure (VSPS) of FEC, which eliminates the selection of random voltage vectors, as encountered in the conventional hysteresis current controller (HCC) [6]. CESP-based HC requires two hysteresis bands and two lookup tables: inner hysteresis band for voltage vector selection and outer hysteresis band for sector selection. CESP has to hit the outer hysteresis band to detect the sector changeover, as discussed in detail for two-level FEC in [9]. As one moves on to the selection of higher levels of the multilevel converter (for high power rating and better power quality) [10], number of devices, sectors, switching states, voltage vectors, and implementation complexity increase. In one fundamental cycle of supply voltage, the CESP moves out of the inner hexagonal boundary many times (depending on the level of the converter) to hit the outer hysteresis (e.g., 6 times, 18 times, and 42 times for two-level, three-level, and five-level converter, respectively) to detect the sector changeover. This puts a serious limitation on the improvement of the harmonic spectrum of the supply current and at the same time increases the complexity in real-time implementation [11]. Various sector change detection techniques for multilevel inverters have been reported in the literature. The direct vector quantization technique is proposed and discussed in [12] for multilevel inverter applications with sigma–delta modulator. Each sigma–delta modulator consists of a difference node, a discrete-time integrator, and a space vector quantizer. The input to the integrator is the difference between the reference voltage vector and the quantized value of the voltage vector. This error is given to the integrator to produce the integrated error vector and quantized to the nearest inverter switching vectors by the principle of vector quantization. This method does not require any separate sector identification logic; however, the computational requirement is more. This technique uses a voltage control scheme and applied to the inverter topology.

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The authors are with the Department of Electrical Engineering, Nirma University, Ahmedabad 382481, India (e-mail: manisha.shah@nirmauni.ac.in; siddharthsingh.chauhan@nirmauni.ac.in; pn.tekwani@nirmauni.ac.in).

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Sector detection with online hysteresis boundary computation is presented in [13] and [14] for multilevel inverter employing CESP-based HC. The presented method detects the sector, calculates the switching timing of the adjacent voltage vectors, and dynamically computes the current error boundary at every sampling interval, as presented in [14]. This technique requires many computations to be carried out in a sampling time to achieve adequate control of multilevel inverters. This scheme is very complex to implement and requires a very fast real-time processor for implementation. For the technique presented in [15], the voltage space phasor of the multilevel inverter is divided into the number of layers according to the level of the inverter. To identify any layer in which the tip of the supply voltage vector is located, the mathematical expressions are presented. After having information on a particular layer, using sector mapping and reverse sector mapping, voltage vectors are identified. This technique is integrated with voltage-controlled space vector modulation (SVM) to control multilevel inverter. The generation of space vector pulsewidth modulation (PWM) signal using the sampled amplitudes of reference phase voltages for the multilevel inverter is discussed in [16]. In this scheme, a carrier-based level-shifted technique with offset injection is integrated with space vector modulation to calculate the switching time for each selected voltage vector. This scheme involves the online computation of various offsets, which needs to be injected in a carrier wave to select appropriate voltage vectors for voltage-controlled PWM technique. In [17], a general space vector modulation technique is proposed for an *N*-level inverter. The claim of the article is that the mathematical computations remain the same for any number of levels, and the scheme does not demand a fast real-time controller. The technique proposed in this article does not detect the sector but selects the nearest voltage vector by synthesizing a reference voltage vector. The simulation results presented only for the linear range of modulation index adopting voltage-controlled PWM technique. The technique proposed in [18] is to select the small hexagon equivalent to a two-level inverter from VSPS of *N*-level inverter. This is done by locating the closest center to the tip of the reference voltage vector. Then after, the origin of the reference voltage vector is shifted to the center of the selected two-level hexagon and all the mathematical computations are done as per two-level inverter. The technique is supported by simulation results in a steady state within the linear range of modulation with voltage-controlled SVM. A reverse mapping based voltage-controlled space vector PWM strategy is proposed in [19] for *N*-level NPC multilevel inverters. The space vector is expressed as a sum of a contender vector and an error vector. In this scheme, sector information is not needed. The voltage vector nearest to the reference space vector is the contender vector. By calculating the error vector, the difference between the contender vector and the voltage reference vector is determined. The error vector is translated to the origin of the space vector diagram using a translation method.

Fractal approach based sector detection is proposed in [20] for multilevel inverters. This is an effective way of sector detection without any complex computational requirements, as discussed in [21], for multilevel inverters employing voltage-controlled PWM techniques. Feasibility levels and implementation complexity of these schemes are different for different levels of multilevel inverters, and many of the sector detection techniques are verified for voltage-controlled multilevel inverters. Hence, the generalization of the technique of sector detection for any multilevel FEC is very essential for providing a versatile solution for a current-controlled PWM technique (CESP-based HC).

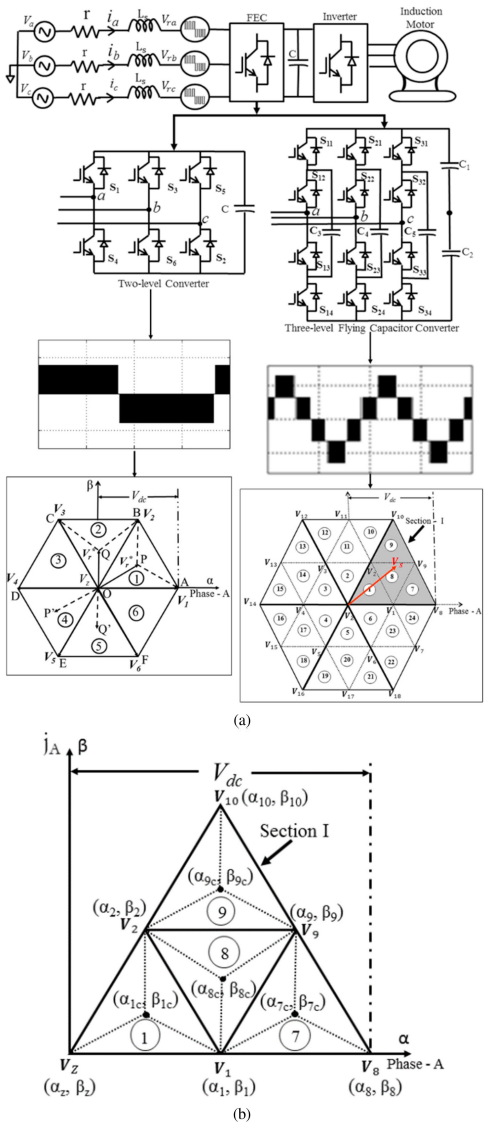

Fig. 1. (a) Schematic of two-level and three-level FEC with their VSPS and converter voltage waveform, showing VSPS of a two-level and three-level converter. (b) Centroid of each sector of Section I.

The novelty presented in this article is the integration of the fractal approach based sector detection with CESP-based HC (current controller) to eliminate the outer hysteresis band and lookup table for any multilevel FEC. This technique reduces the complexity in the real-time implementation of CESP-based HC.

II. Fractal Approach of Sector Detection for Three-Level and Five-Level FECs

Any multilevel converter is realized by the number of semiconductor switches with discrete switching states. The equivalent power schematic of two-level/three-level FEC connected to an industrial load is shown in Fig. 1(a), with their respective

TABLE I
SECTIONS AND CORRESPONDING SECTORS OF THREE-LEVEL FEC

Sections of three-level converter VSPS equivalent to two-level VSPS	Sectors of three-level converter
Section I	Sectors: 1, 7, 8, 9
Section II	Sectors: 2, 10, 11, 12
Section III	Sectors: 3, 13, 14, 15
Section IV	Sectors: 4, 16, 17, 18
Section V	Sectors: 5, 19, 20, 21
Section VI	Sectors: 6, 22, 23, 24

VSPS and converter voltage waveforms. In this article, three-level flying capacitor topology is adopted as multilevel FEC. In the fractal approach, any multilevel converter VSPS is realized as equivalent to two-level VSPS [22].

The proposed controller uses the inherent fractal structure of VSPS of three-level FEC. The VSPS of two-level FEC, which is shown in Fig. 1(a), consists of 6 sectors, whereas the VSPS of three-level FEC is formed by 24 sectors. The VSPS of three-level FEC is viewed as equivalent to a two-level VSPS by considering six sections of three-level VSPS equivalent to six sectors of the two-level converter, as shown in Fig. 1(a). Outer six voltage vectors of a three-level converter $(V_8,\ V_{10},\ V_{12},\ V_{14},\ V_{16},\ V_{18})$ represent the three-level VSPS equivalent to two-level VSPS (as a dc-link voltage of both, two-level as well as three-level, converters is same, i.e., $V_{\rm dc}$) as in Fig. 1(a). Section I of a three-level converter consists of four triangular subsections, which are the sectors of three-level FEC, as shown in Fig. 1(a). Each section of the three-level converter is comprised of four unique sectors, as listed in Table I. Considering Section I [see Fig. 1(b)], the midpoints $V_1,\ V_2$, and V_9 of the sides $\overline{V_zV_8}$, $\overline{V_{10}V_z}$, and $\overline{V_8V_{10}}$, respectively, can be calculated using (1)–(3) from the equilateral triangle $\Delta V_zV_8V_{10}$, as shown in Fig. 1(b). This will further divide Section I into four equilateral triangles. So, Section I consists of four triangles $\Delta V_zV_1V_2$, $\Delta V_1V_8V_9$, $\Delta V_1V_9V_2$, and $\Delta V_2V_9V_{10}$ referred to as sectors 1, 7, 8, and 9, respectively. This process is referred to as triangularization [21].

$$\alpha_1 = \frac{\alpha_Z + \alpha_8}{2}, \quad \beta_1 = \frac{\beta_Z + \beta_8}{2} \tag{1}$$

$$\alpha_2 = \frac{\alpha_Z + \alpha_{10}}{2}, \quad \beta_2 = \frac{\beta_Z + \beta_{10}}{2} \tag{2}$$

$$\alpha_9 = \frac{\alpha_8 + \alpha_{10}}{2}, \quad \beta_9 = \frac{\beta_8 + \beta_{10}}{2}. \tag{3}$$

A. Section Selection in Multilevel FEC

The supply voltage vector continuously rotates in the VSPS of the converter. In the proposed technique, sector change detection takes place based on the position of the tip of the supply voltage vector. Position of the supply voltage vector in a particular section is identified by comparing the instantaneous values of three-phase supply voltages V_a, V_b, and V_c, as shown in Fig. 2(a) and listed in Table II [21]. After detection of the section, the appropriate sector in which the tip of the supply voltage vector

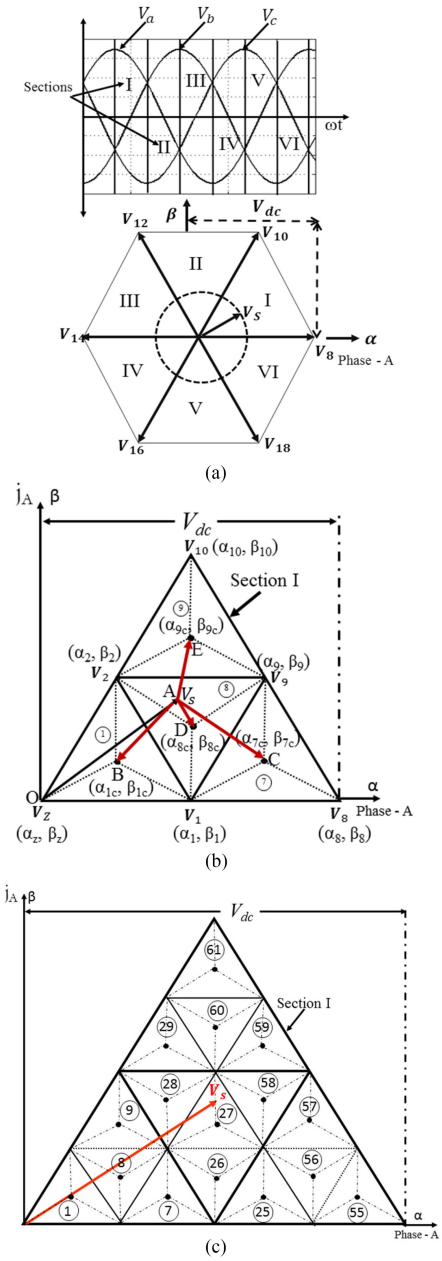

Fig. 2. (a) Section identification comparing instantaneous values of supply voltages. (b) Distance between the tip of the supply voltage vector and the centroid of each sector in Section I. (c) Centroid of each sector in Section I for VSPS of a five-level FEC.

lies is identified by calculating the distance between the tip of the supply voltage vector and centroid of the four sectors of that section (for three-level FEC). The minimum distance between the centroid of a particular sector and the tip of the supply voltage vector gives sector identification. To explain this in detail, consider that the section change logic has detected as Section I in which $\boldsymbol{V_s}$ (OA) is lying, having a tip at A in Section I of a three-level VSPS, as shown in Fig. 2(b). Four sectors 1, 7, 8, and 9 ($\Delta V_zV_1V_2$, $\Delta V_1V_8V_9$, $\Delta V_1V_9V_2$, and $\Delta V_2V_9V_{10}$, respectively) have centroids at points B, C, D, and E, respectively. As these four triangles are equilateral, the coordinates of centroids α_{xC} and β_{xC} (where $x = 1, 7, 8,$

and 9) of these four triangles can be found using (4)–(7) for sectors 1, 7, 8, and 9, respectively. Similarly, the centroid for all other sectors is calculated by applying triangularization to each section. Distance from the tip of the supply voltage vector *A* to centroids *B*, *C*, *D*, and *E* is defined as S_{AB}, S_{AC}, S_{AD}, and S_{AE} and calculated using (8)–(11), respectively. For the sector in which the tip of the supply voltage vector is located, the minimum distance is evaluated, which in turn provides information about the particular sector in that section as per (12). The same process is repeated for the other five sections of three-level VSPS (each consisting of four sectors) for accurate sector identification. Similarly, the centroid of each sector in Section I for a five-level FEC can be found [see Fig. 2(c)] and the corresponding sector can be detected accordingly.

$$\alpha_{1C} = \frac{\alpha_Z + \alpha_1 + \alpha_2}{3}, \quad \beta_{1C} = \frac{\beta_Z + \beta_1 + \beta_2}{3} \tag{4}$$

$$\alpha_{7C} = \frac{\alpha_Z + \alpha_8 + \alpha_9}{3}, \quad \beta_{7C} = \frac{\beta_Z + \beta_1 + \beta_2}{3} \tag{5}$$

$$\alpha_{8C} = \frac{\alpha_Z + \alpha_2 + \alpha_9}{3}, \quad \beta_{8C} = \frac{\beta_Z + \beta_2 + \beta_9}{3} \tag{6}$$

$$\alpha_{9C} = \frac{\alpha_Z + \alpha_9 + \alpha_{10}}{3}, \quad \beta_{9C} = \frac{\beta_Z + \beta_9 + \beta_{10}}{3} \tag{7}$$

$$S_{AB} = \sqrt{(V_{s\alpha} - \alpha_{1c})^2 + (V_{s\beta} - \beta_{1c})^2} \tag{8}$$

$$S_{AC} = \sqrt{(V_{s\alpha} - \alpha_{7c})^2 + (V_{s\beta} - \beta_{7c})^2} \tag{9}$$

$$S_{AD} = \sqrt{(V_{s\alpha} - \alpha_{8c})^2 + (V_{s\beta} - \beta_{8c})^2} \tag{10}$$

$$S_{AE} = \sqrt{(V_{s\alpha} - \alpha_{9c})^2 + (V_{s\beta} - \beta_{9c})^2} \tag{11}$$

$$\text{Current Sector} = \min(S_{AB}, S_{AC}, S_{AD}, S_{AE}). \tag{12}$$

Supply voltage vector can take any trajectory (e.g., two-level mode of operation to the five-level mode of operation in a five-level FEC) based on the required load voltage ($V_{\rm dc}$) and/or magnitude of three-phase supply voltages. Sector change detection is accordingly assured by this approach. In the proposed CESP-based HC, the fractal approach is integrated to identify the sector without using any outer hysteresis band and lookup tables [11]. It further enhances the quality of supply current as CESP does not move outside the prescribed (inner) hexagonal boundary for several times (depending on the level of operation) in a fundamental cycle of the supply voltage. This fractal approach based sector detection also reduces the complexity of implementation of the proposed CESP-based HC for multilevel converters. Sector change detection logic can be generalized for any multilevel (*N*-level) converter topology employing CESP-based HC. The generalized flowchart for the proposed scheme is shown in Fig. 3.

III. Simulation Studies and Analysis

Detailed simulation analysis is done to verify the performance of a fractal approach under various steady-state and dynamic conditions with CESP-based HC FEC system, as shown in Fig. 4(a). The width of the VSPS of FEC depends on the required dc-link voltage of the load. As dc-link voltage increases, VSPS expands, and it shrinks when the dc-link voltage decreases. In case of FEC, the possibility of the reference voltage vector ($\boldsymbol{V}_s$) following different trajectories arises based on two conditions. First, when supply voltage $\boldsymbol{V}_s$ is variable but dc-link voltage $V_{\rm dc}$ remains constant, and second, when dc-link voltage is changing but supply voltage remains constant. When supply voltage $\boldsymbol{V}_s$ is equal to $\boldsymbol{V}_{s1}$, it follows trajectory *a* (trajectory passes through sectors 1–6), as shown in Fig. 4(b), which makes the converter to operate in two-level mode. When $\boldsymbol{V}_s$ increases from $\boldsymbol{V}_{s1}$ to $\boldsymbol{V}_{s2}$, it follows trajectory *b* (passes through corner sectors 8-11-14-17-20-23-8), which makes the converter to operate from two-level to three-level mode. Similarly, when $\boldsymbol{V}_s$ increases to $\boldsymbol{V}_{s3}$, $\boldsymbol{V}_{s4}$, and $\boldsymbol{V}_{s5}$, respectively, it follows the trajectories *c*, *d*, and *e*, as shown in Fig. 4(b), and makes the converter to operate in a three-level normal mode to overmodulation. As in most of the industrial applications, FEC is connected to a grid (where the supply voltage is constant within the tolerable range), the second possibility, in which the dc-link voltage is changing but the supply voltage remains constant, is also considered and analyzed in the proposed work. In this situation, as the dc-link voltage increases, the width of VSPS also increases, which makes the converter to operate from a three-level mode of operation to a two-level mode of operation. To verify both the conditions, simulation analysis is done by keeping the dc-link voltage constant at 350 V and varying the supply voltage to 100 V and 175 V, as shown in Fig. 5(a) and (b), respectively [FEC follows the trajectories *a* and *b*, as per Fig. 4(b)]. Similarly, keeping the supply voltage constant at 230 V and varying the dc-link voltage, as shown in Fig. 5(c) and (d), the converter follows the trajectories *d* and *e*. The performance of the fractal approach is also verified in dynamic conditions, keeping the dc-link voltage constant and suddenly varying the supply voltage and vice-versa, as shown in Fig. 5(e) and (f), respectively, which makes the converter to operate from a two-level mode of operation to a three-level mode of operation and vice-versa. In both steady-state and dynamic conditions, the fractal approach works perfectly well and changes sector detection pattern according to the trajectory followed by the supply voltage vector, as evident from all presented simulation results in Fig. 5.

TABLE II
Identification of Section of Any Multilevel FEC

Instantaneous values of three-phase supply voltages	Corresponding Section of Multilevel FEC
$V_a \geq V_b \geq V_c$	I
$V_b \geq V_a \geq V_c$	II
$V_b \geq V_c \geq V_a$	III
$V_c \geq V_b \geq V_a$	IV
$V_c \geq V_a \geq V_b$	V
$V_a \geq V_c \geq V_b$	VI

IV. Principle of CESP-Based HC

In this article, space vector modulation is applied to the hysteresis current controller to minimize the limitations of the conventional HC. The proposed CESP-based HC utilizes the

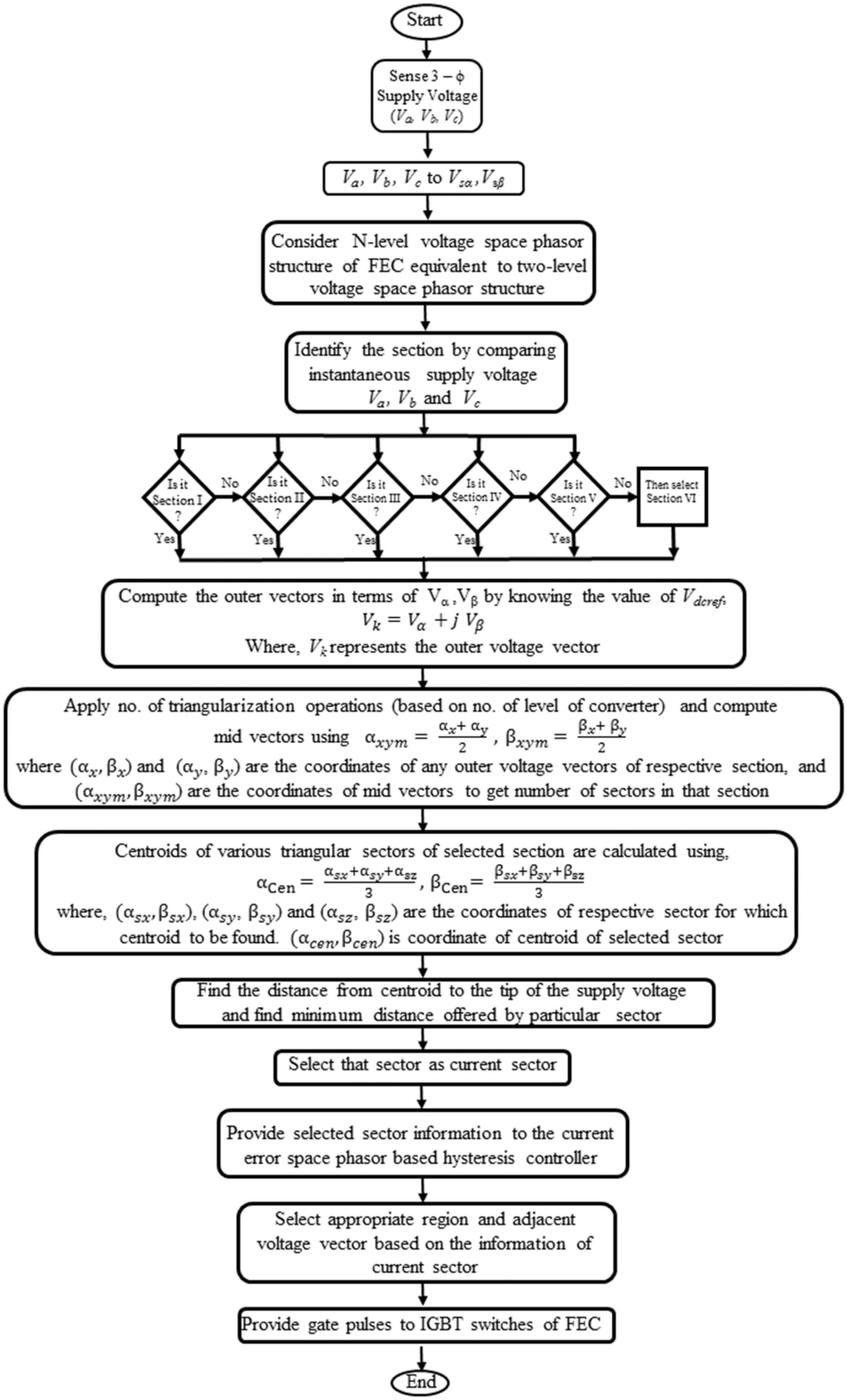

Fig. 3. Generalized flowchart of the proposed fractal-based controller for any *N*-level FEC.

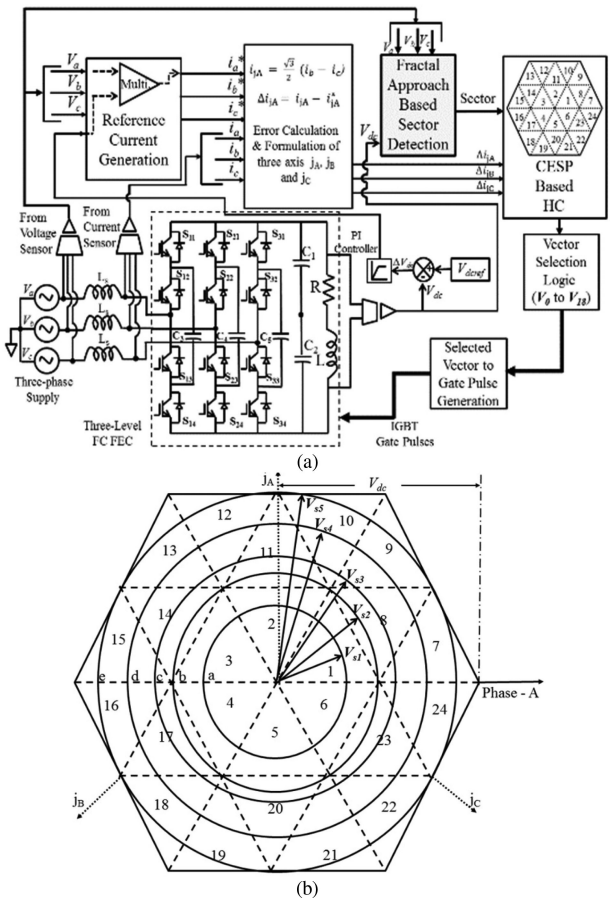

Fig. 4. (a) Block diagram of the proposed FEC system. (b) Various trajectories created by varying supply voltage with the constant dc-link voltage.

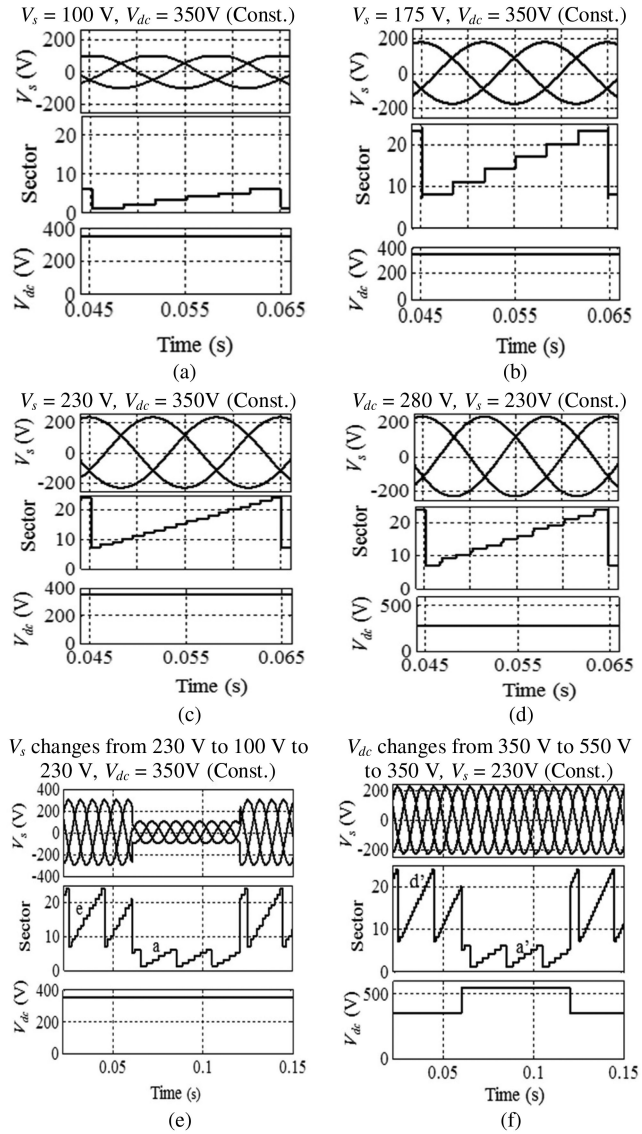

Fig. 5. Simulation analysis of fractal approach for three-level FEC. (a)–(f) Trajectory followed by the supply voltage vector under different values of the supply voltage or reference dc-link voltage.

information of direction and magnitude of current errors in all the three phases to select the appropriate voltage vectors. The proposed CESP-based HC ensures switching of voltage vectors adjacent to $\boldsymbol{V}_s$ in a sector of FEC. In the VSPS of three-level FEC, as shown in Fig. 1(a), $\boldsymbol{V}_1$ to $\boldsymbol{V}_{18}$ are the active voltage vectors and $\boldsymbol{V}_z$ is a zero-voltage vector. The three-phase supply voltage vector $\boldsymbol{V}_s$, three-phase supply current vector $\boldsymbol{I}_s$, and converter voltage vector $\boldsymbol{V}_r$ are presented respectively as follows:

$$\boldsymbol{V_s} = V_a + aV_b + \ a^2V_c \tag{13}$$

where $a = e^{j\frac{2\pi}{3}}$

$$\boldsymbol{I_s} = i_a + ai_b + \ a^2 i_c \tag{14}$$

$$\boldsymbol{V_r} = V_{ra} + a\ V_{rb} + \ a^2\ V_{rc}. \tag{15}$$

To generate the reference currents $i_a^*,\ i_b^*$ and i_c^*, the output dc-link voltage $V_{\rm dc}$ is sensed and compared with the required reference dc-link voltage to generate voltage error $\Delta V_{\rm dc}$, as shown in Fig. 4(a). This $\Delta V_{\rm dc}$ is fed to a proportional integral (PI) controller, and the output of the PI controller is multiplied with a sinusoidal envelope (availed by sensing supply voltage). Generated reference currents $i_a^*,\ i_b^*$, and i_c^* are able to satisfy the input power requirement in order to maintain the constant dc-link voltage at the output of the converter. These reference currents $i_a^*,\ i_b^*$, and i_c^* are then compared with actual line currents $i_a,\ i_b$, and i_c, respectively, to get current errors $\Delta i_a,\ \ \Delta i_b$, and Δi_c of phases *A*, *B*, and *C*, respectively, as mentioned in (16). A three-phase CESP is defined in (17). From the equivalent circuit of FEC, as shown in Fig. 1(a), voltage equation for three-phase FEC is written as (18). Substituting (16) into (18) gives (19). The converter reference terminal voltage vector $\boldsymbol{V_r^*}$ can be expressed, as shown in (20). Substituting (20) into (19) gives (21). If $\boldsymbol{V_r}$ is equal to $\boldsymbol{V_r^*}$ at every instant, the actual supply current will be same as the reference current. But since the converter can generate only one of the 19 distinct voltage vectors ($\boldsymbol{V}_1$ to $\boldsymbol{V}_{18}$, and $\boldsymbol{V}_z$ for three-level FEC), it would result into deviation in actual supply current leading to CESP, as defined in (22). The CESP moves in different directions for different converter voltage vectors based on (22) for a desired value of $\boldsymbol{V_r^*}$. The proposed current controller monitors current errors along three

axes j_A, j_B, and j_C, which are perpendicular to the phases *A*, *B*, and *C*, respectively. CESP is restricted within a hexagonal boundary by selecting a unique voltage vector among three adjacent vectors based on the information of the present sector. This brings CESP within the predefined boundary whenever it hits the hexagonal boundary [9].

Considering the position of reference voltage vector $\boldsymbol{V}_r^*$ (OA) in sector 7 of VSPS of three-level FEC, as shown in Fig. 6(a), the direction of CESP can be along *AB*, *AC,* or *AD* based on the switching of voltage vectors $\boldsymbol{V}_8$, $\boldsymbol{V}_9$, or $\boldsymbol{V}_1$, as per (22). Similarly, when $\boldsymbol{V}_r^*$ takes the position of *OE* in sector 8, CESP moves along the directions *EC*, *EF,* or *ED* based on the switching of $\boldsymbol{V}_9$, $\boldsymbol{V}_2$, or $\boldsymbol{V}_1$, as evident from Fig. 6(a). This is valid for all odd and even sectors of three-level VSPS. This forms triangular boundary *XYZ* for odd sectors and $\Delta\bar{X}\ \bar{Y}\ \bar{Z}$ for even sectors, as shown in Fig. 6(b) [9]. Each triangular boundary is divided into three regions R_1, R_2, and R_3 for odd sectors and $\overline{R_1}$, $\overline{R_2}$, and $\overline{R_3}$ for even sectors, as shown in Fig. 6(b). The boundaries are placed at a distance *h* along the j_A, j_B, and j_C axis for odd sectors and along $-j_A$, $-j_B$, and $-j_C$ for even sectors. When these two triangular boundaries are combined, a combined boundary termed as starfish boundary is formed, as shown in Fig. 6(c). In starfish boundary, CESP travels to double the distance along $-j_A$, $-j_B$, and $-j_C$ axis in case of odd sectors and along j_A, j_B, and j_C axis for even sectors. For all odd and even sectors, if boundaries (comparators) are placed along all six axes, it would result in a hexagonal boundary, as shown in Fig. 6(c). In his article, this hexagonal boundary is selected and the CESP is held always within the limit of the hexagonal boundary. As per the comparator status of the respective axis, region is detected to select the appropriate voltage vector, which brings CESP back into the hysteresis boundary [9].

The method discussed for the detection of sections by comparing the instantaneous values of the supply voltage (see Fig. 2(a), Table II) can be used for a two-level converter for sector detection, as it has only six sectors. But as one selects three-level topology as FEC, the said logic of sector detection could not be extended for a three-level converter because of 24 sectors in VSPS of it. So, a second pair of comparators is placed little further from the first pair of comparators along all six axes, as shown in Fig. 6(d). Whenever $\boldsymbol{V}_r^*$ crosses from one sector to the next sector, the CESP increases along the axis, which is perpendicular to the boundary of those sectors and hits the outer hysteresis band. For example, if $\boldsymbol{V}_r^*$ crosses from sector 7 to sector 8, current error increases in the direction of the j_c axis, which is perpendicular to the boundary of sector 7 and sector 8 and follows the path GH-HI-IJ-JK-KL, as shown in Fig. 6(d). When CESP hits the outer boundary placed at j_c axis, sector change is detected by the status of the outer comparator. Thus, CESP moves out of the inner hysteresis boundary 18 times for a three-level converter to detect the sector change in a fundamental cycle. This deteriorates the harmonic spectrum of supply current [11]

$$\Delta \boldsymbol{i} \ = \ \boldsymbol{I_s} - \boldsymbol{i}^* \tag{16}$$

$$\Delta \boldsymbol{i} = \ \Delta i_a + a\Delta i_b + \ a^2 \Delta i_c \tag{17}$$

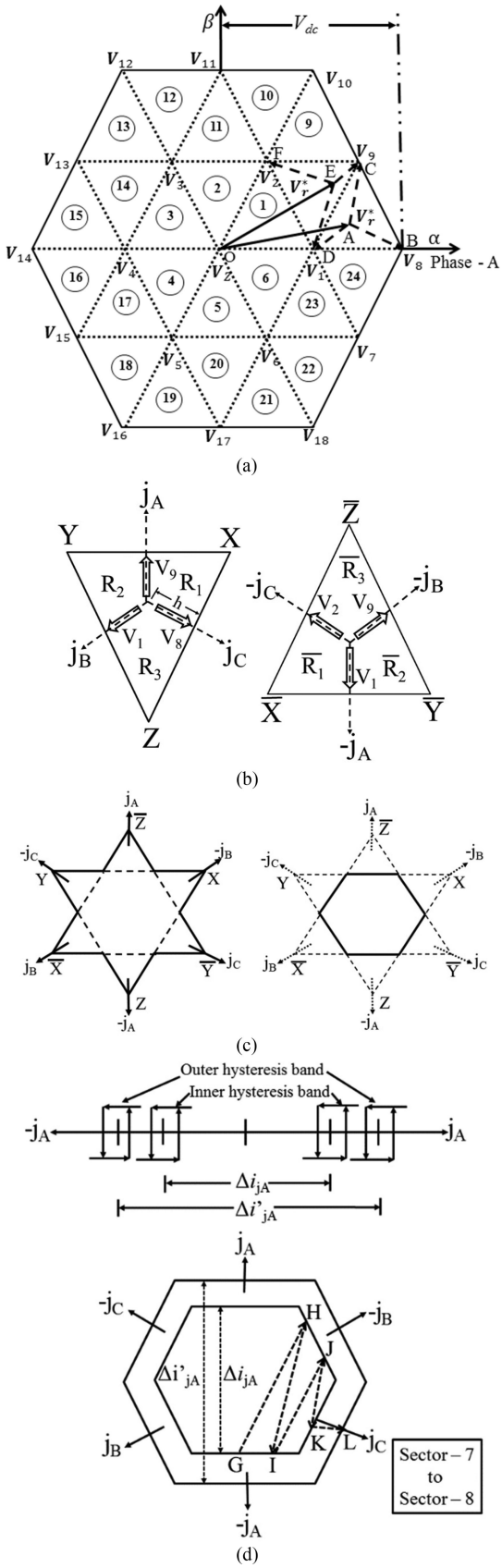

Fig. 6. (a) VSPS of the three-level FEC. (b) Triangular boundary formed by odd and even sectors. (c) Starfish boundary formed by $\Delta \boldsymbol{i}$ and modified hexagonal boundary. (d) Sector changeover detection using outer hysteresis band.

TABLE III
SWITCHING TABLE OF THREE-LEVEL FLYING CAPACITOR FEC

V_{aO}	S_{11}	S_{12}	S_{13}	S_{14}
$+V_{dc}/2$	1	1	0	0
0	0	1	0	1
0	1	0	1	0
$-V_{dc}/2$	0	0	1	1

$$\boldsymbol{V_r} = L_s\frac{d\boldsymbol{I_s}}{dt} + r\boldsymbol{I_s} + \boldsymbol{V_s} \tag{18}$$

$$\boldsymbol{V_r} = L_s\frac{d\Delta\boldsymbol{i}}{dt} + r\Delta\boldsymbol{i} + L_s\frac{d\boldsymbol{i}^*}{dt} + r\boldsymbol{i}^* + \boldsymbol{V_s} \tag{19}$$

$$\boldsymbol{V_r^*} = L_s\frac{d\boldsymbol{i}^*}{dt} + r\boldsymbol{i}^* + \boldsymbol{V_s} \tag{20}$$

$$\boldsymbol{V_r} = L_s\frac{d\Delta\boldsymbol{i}}{dt} + \boldsymbol{V_r^*} \tag{21}$$

$$\frac{d\Delta\boldsymbol{i}}{dt} = \frac{\boldsymbol{V_r} - \boldsymbol{V_r^*}}{L_s}. \tag{22}$$

As one selects the higher level of the converter, CESP moves many times out of the inner hysteresis band and deteriorates the supply current waveshape and also needs the second pair of comparators and a lookup table for the sector change detection. Hence, to improve the waveshape of line current, sector change detection logic without using any outer comparators and a lookup table for any multilevel converter is essential to employ CESP-based HC, which is not reported in the literature yet. Fractal approach based sector detection integrated with CESP-based HC is the uniqueness of the work presented in this article.

Three-level flying capacitor topology is used as FEC in this article. It offers redundant switching states for zero-voltage level at the pole, which is used to balance the voltage of flying capacitors. Three-phase three-level flying capacitor topology, as shown in Fig. 4(a), consists of 12 IGBT switches. The switching states for one leg of three-level flying capacitor (FC) topology are given in Table III in which "1" indicates "ON" status of the switch and "0" indicates "OFF" status of the switch. From Table III, it is observed that switches S_{11} and S_{14}, and S_{12} and S_{13} are forming two different complementary pairs. This topology has two redundant switching states for zero-voltage level at the pole, which helps in charging and discharging of inner (flying) capacitors. Equivalent circuits of charging and discharging of flying capacitor C_3 during these zero switching states are shown in Fig. 7(a) and (b), respectively, for the forward direction of converter current. Flying capacitor topology suffers from the capacitor voltage unbalance and the same is also observed during the simulation analysis. Making use of these redundant switching states at zero-voltage level, the capacitor voltage balancing scheme is designed and implemented with the proposed work, as shown in Fig. 7(c). In the proposed scheme, the actual voltage at inner capacitor C_3 V_{c3} is sensed and compared with half of the reference dc-link voltage ($V_{\mathrm{dcref}}/2$). The error ΔV_{c3} is processed to voltage HC having a band of ± 1 V, as shown in Fig. 7(c), for the selection

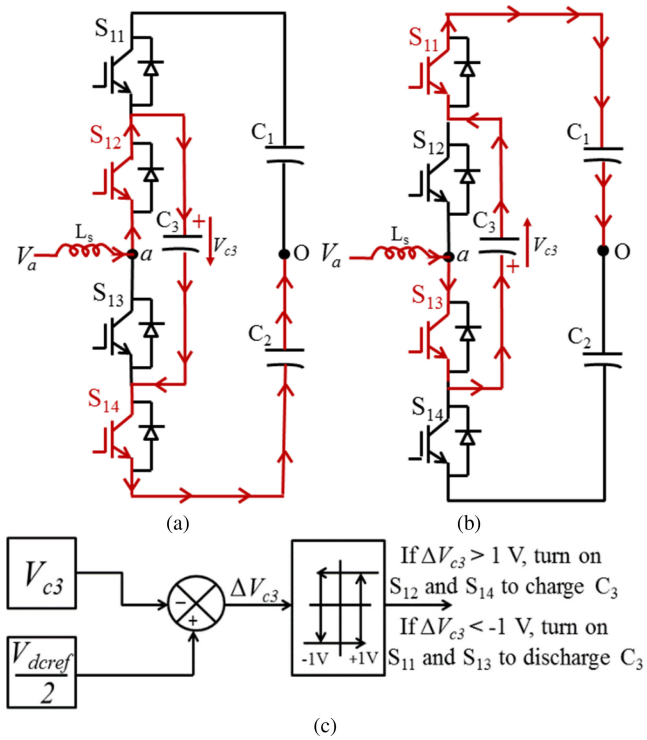

Fig. 7. (a) Equivalent circuit of a 3-L FC when S_{12} and S_{14} are turned ON, causing charging of flying capacitor (C_3). (b) When S_{11} and S_{13} are turned ON, causing discharging of C_3. (c) Capacitor voltage balancing scheme.

of a particular switching state for zero voltage at the pole. For the given direction of converter current, if ΔV_{c3} is greater than 1 V, it indicates discharging of capacitor C_3, so switches S_{12} and S_{14} are switched ON to make capacitor C_3 to charge, as shown in Fig. 7(a). Same way, when capacitor C_3 is overcharged, i.e., when ΔV_{c3} becomes negative, then switches S_{11} and S_{13} are switched ON to make capacitor C_3 to discharge, as per Fig. 7(b). The same approach is used to maintain the capacitor voltage of the other two inner capacitors C_4 and C_5 of the other two legs of the FEC.

V. DESIGN OF BOOST INDUCTOR AND DC-LINK CAPACITOR

IGBT-based FEC is connected to the grid through an inductor. This input inductor represents the combined effect of the line inductance and boost inductance based on the system parameters [23]. The boost inductor facilitates as an input filter also and filters out higher order current harmonics (introduced because of PWM switching) from line current. The harmonic profile of the input current depends on the type of PWM technique adopted to control the FEC. The boost inductance for FEC can be calculated using (23), as discussed in [24], with the upper and lower limits of its value based on the system parameters

$$L_s = \sqrt{\frac{\boldsymbol{V}^2_{\boldsymbol{r}\,(\boldsymbol{pk})} - \boldsymbol{V}^2_{\boldsymbol{s}(\boldsymbol{pk})}}{\omega^2 \quad \boldsymbol{I}^2_{\boldsymbol{s}(\boldsymbol{pk})}}}. \tag{23}$$

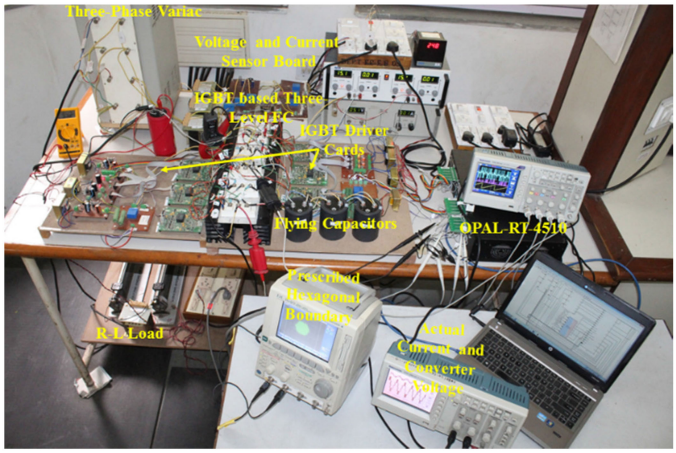

Fig. 8. Hardware setup of the proposed scheme with three-level FC FEC.

For maintaining the output dc-link voltage at a desired voltage level with allowable ripple voltage, the selection of the dc-link capacitor plays an important role. The output dc-link voltage has a constant component and a fluctuating component of twice the supply frequency of power. This second-order harmonic component should pass through the dc-link capacitor (filter), such that the voltage ripple (ΔV) should be within the allowable limit of $V_{\rm dc}$. Hence, to keep ΔV within the limit, governing design expression for the dc-link capacitor is expressed as follows:

$$C \geq \frac{\boldsymbol{V_r I_s}}{8\pi f_s V_{\rm dc} \Delta V}. \tag{24}$$

VI. Experimental Setup, Results, and Discussions

The proposed CESP-based HC for three-level FEC is implemented (with both the strategies of sector detection, i.e., using outer hysteresis band and fractal approach eliminating outer band) using a real-time hardware in-loop simulator OPAL-RT-4510 under rapid control prototyping system design mode. Semikron make 1200 V, 75 A dual-pack IGBT modules (SKM75GB12T4) are used to fabricate three-level FEC, as shown in Fig. 8. Three boost inductors of 1.5 mH each are connected at the input side of the three-phase FEC. At the output side of the FEC, a dc-link capacitor of 3300 μF, 400 V is connected in parallel with an *R–L* load of 500-Ω rheostat and 5 mH inductor. Three LEM hall effect voltage transducers (LV-20-P) are used to sense three-phase supply voltages, which are used by the reference current generation scheme and proposed sector detection technique. So, the proposed technique of sector detection for multilevel FEC does not involve any additional cost of voltage sensors. Three 3300 μF, 400 V capacitors are used as flying (clamping) capacitors. To achieve clamping capacitor voltage balance, three additional LEM hall effect voltage transducers (LV-20-P) are used to sense the clamping capacitor voltage for the proposed capacitor voltage balancing scheme, as shown in Fig. 7(c).

A. Experimental Verification of Fractal Approach Based Sector Detection for Multilevel FECs

The fractal approach of sector detection for any multilevel FEC is verified experimentally by considering three-level VSPS of FEC. Three-phase supply voltages of phases *A*, *B*, and *C* are sensed using voltage transducers and given to analog to digital converter (ADC) channels of the real-time controller. The dc-link voltage is considered as a set constant value to perform the experimental verification. In the presented results, three-phase supply voltages and dc-link voltage are taken from digital to analog converter (DAC) channels of the controller. The output dc-link voltage is kept at a constant value of 150 V and variation in the supply voltage is kept in the range from 40 (phase rms) to 140 V (phase rms) using a three-phase autotransformer. As the dc-link voltage is constant, the width of space phasor structure remains constant, but variation in the supply voltage makes $\boldsymbol{V_s}$ to follow different trajectories, as shown in Fig. 9(a)–(d). Similarly, keeping the supply voltage constant and changing the dc-link voltage to 80–220 V, as shown in Fig. 9(e) and (f), the converter operates in the three-level mode of operation and two-level modes of operation, respectively, due to change in the size of hexagonal VSPS.

Transient performance of the fractal approach is also checked by suddenly changing the supply voltage from 40 to 95 V and keeping the dc-link voltage at 150 V. Here, $\boldsymbol{V_s}$ follows the trajectories from two-level to the three-level mode of operation [see Fig. 9(g)]. Similarly, keeping $\boldsymbol{V_s}$ constant and varying $V_{\rm dc}$ from 150 to 220 V, $\boldsymbol{V_s}$ makes the converter to operate from two-level to three-level mode of operation, as evident from Fig. 9(h).

B. Experimental Verification of CESP-Based HC With Outer Hysteresis Band

The proposed controller works satisfactory with three-level FEC and gives supply current in-phase with a supply voltage, as shown in Fig. 10(a), for dc-link voltage of 150 V. The technique of sector detection with the outer hysteresis band is able to identify the appropriate sector, as shown in Fig. 10(b). Actual current tracks the reference current very closely, but it losses the tracking when current error moves out of the inner hysteresis boundary and hits the outer hysteresis band (during sector changeover), as evident from Fig. 10(b). In three-level FEC, $\Delta \boldsymbol{i}$ has to move many times (18 times in a fundamental cycle of the input voltage) out of the inner hysteresis band to detect the appropriate sector, as shown in Fig. 10(c), for normal three-level operation. This distorts the line side current and puts restriction on the improvement of harmonic profile of line current. The %THD (9.29%) of the supply current is shown in Fig. 10(d), which is above the allowable limit of the standards. To further improve the harmonic profile of input current, CESP has to be restricted in the inner prescribed hexagonal boundary by integrating fractal approach for sector change detection (without using any outer hysteresis band) with CESP-based HC.

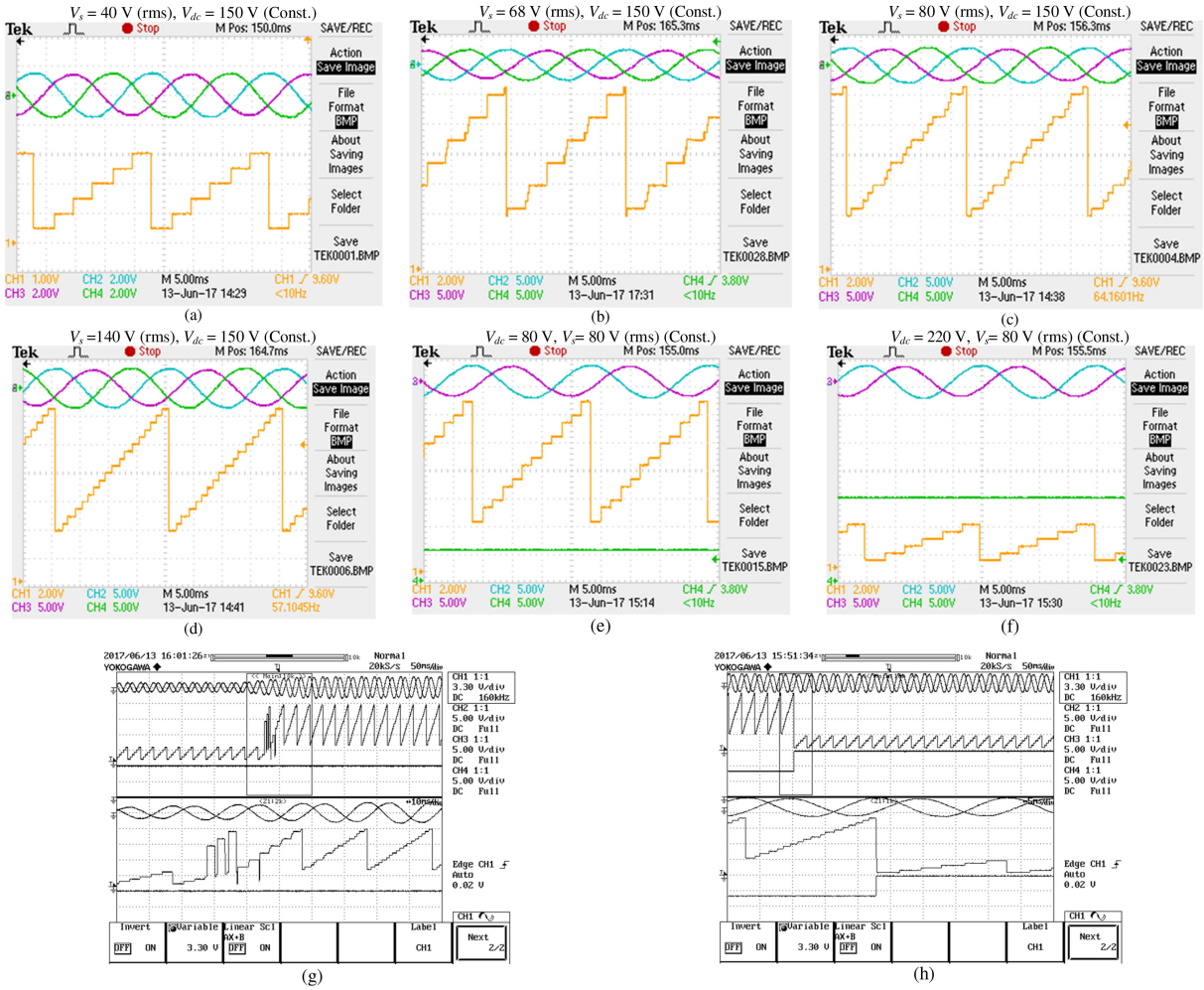

Fig. 9. (a)–(f) FEC operation with different values of supply voltages and dc-link voltage. (a)–(d) [Channel 1: sector and Channels 2, 3, and 4: supply voltages of phases *A*, *B*, and *C*, respectively]. (e)–(h) [Channel 1: sector, Channels 2 and 3: supply voltages of phases *A* and *B*, respectively, and Channel 4: dc-link voltage ($V_{\rm dc}$)].

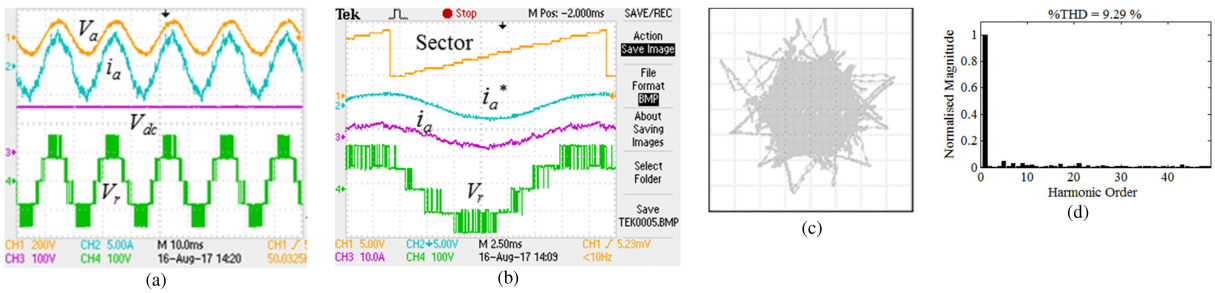

Fig. 10. (a) and (b) Performance of three-level FC FEC at $V_{\rm dcref} = 150$ V. (c) $\Delta \boldsymbol{i}$ forming hexagonal boundary (moving many times out of the inner hysteresis band for sector change detection), Δi_α: *x*-axis: 1 V/div. (DAC output), and Δi_β: *y*-axis: 1 V/div. (DAC output). (d) Harmonic profile of supply current.

C. Experimental Verification of Fractal Approach Employing CESP-Based HC (Without Outer Hysteresis Band)

Three-level flying capacitor FEC with the proposed controller is tested with different dc-link voltages of 200 and 150 V to validate its performance. The controller, when operated on the mentioned reference dc-link voltages, is able to provide a satisfactory performance, as shown in Fig. 11(a) and (b), for 200 and 150 V, respectively. The desired dc-link voltage and sinusoidal source current for the set values of reference dc-link voltages are evident from Fig. 11(a) and (b), respectively. The proposed CESP-based HC employing fractal approach makes input current sinusoidal and offers a unity power factor, as shown in Fig. 11(c). The actual line current precisely follows

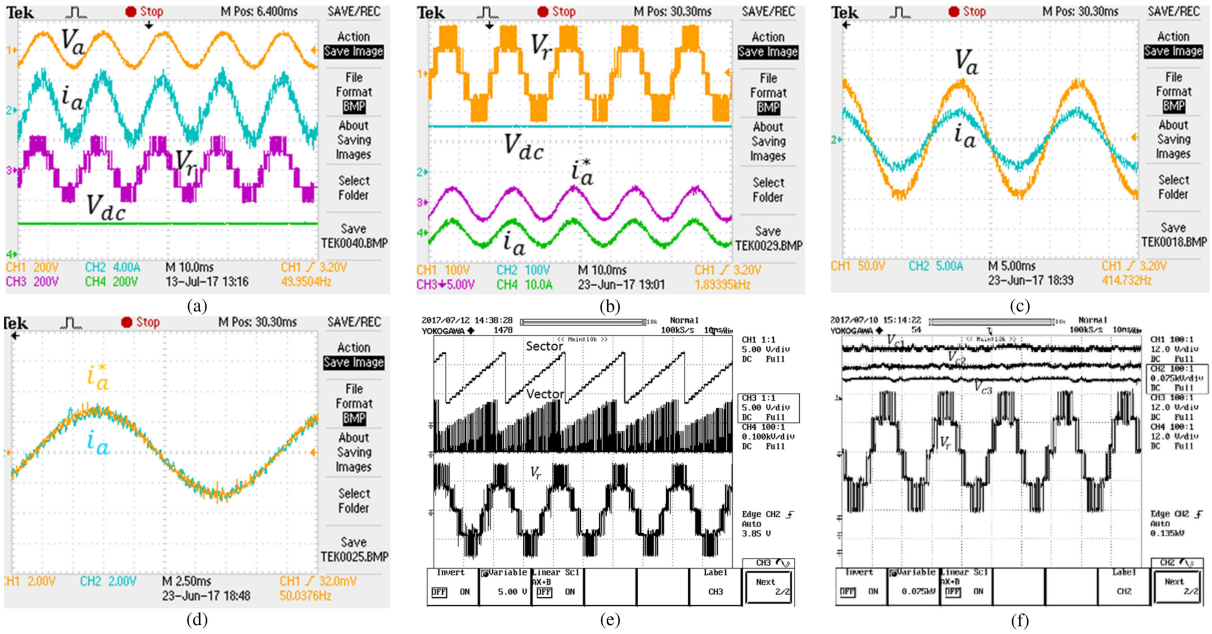

Fig. 11. Performance of three-level FEC with the proposed CESP-based HC employing fractal approach at (a) $V_{\rm dc} = 200$ V and (b) $V_{\rm dc} = 150$ V. (c) Unity power factor offered at supply side. (d) Actual current tracking reference current. (e) Identification of sector and selection of adjacent voltage vector. (f) Performance of capacitor voltage balancing scheme for flying capacitors.

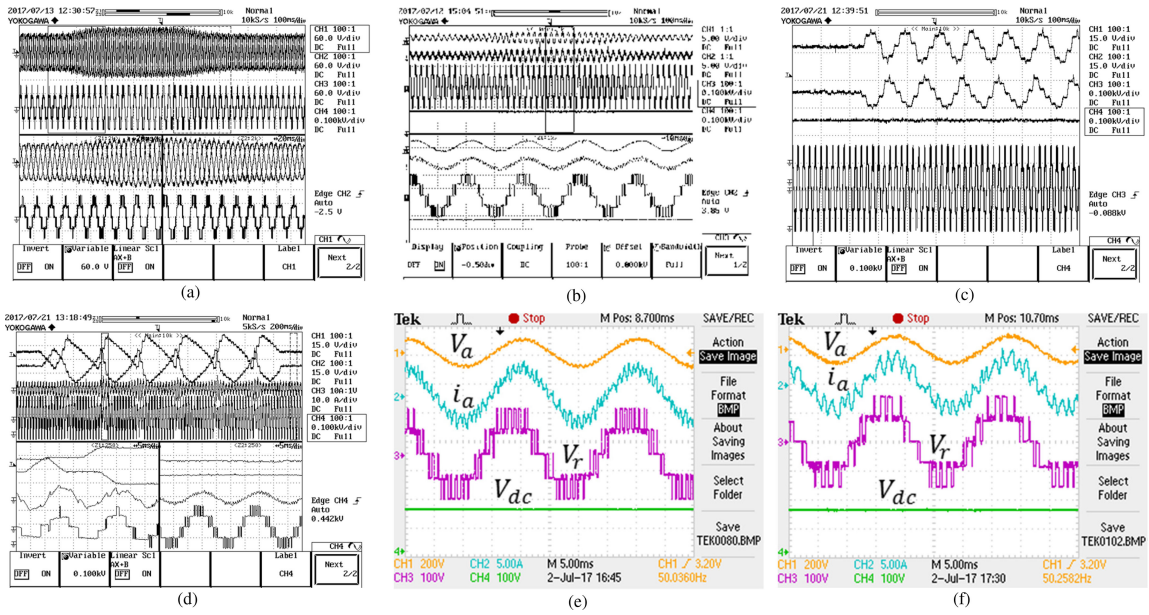

Fig. 12. (a) Line-side variation [Channels 1, 2, and 3: V_a, V_b, and V_c, respectively, and Channel 4: $\boldsymbol{V}_r$]. (b) Load variation [Channel 1: i_a^*, Channel 2: i_a, Channel 3: $\boldsymbol{V}_r$, and Channel 4: $V_{\rm dc}$]. Performance of FEC when capacitor voltage band is changed to (c) $\pm$ 10 V [Channels 1 and 2: V_{c3} and V_{c4}, respectively, Channel 3: $V_{\rm dc}$, and Channel 4: $\boldsymbol{V}_r$], and (d) $\pm$ 20 V [Channels 1 and 2: V_{c3} and V_{c4}, respectively, Channel 3: $\boldsymbol{V}_r$]. Proposed controller is operated at higher hysteresis band of (e) 1–1.3 A and (f) 1.5–1.8 A.

the reference current, as shown in Fig. 11(d). As discussed, the controller identifies the present sector using a fractal approach, and based on the information of the present sector, CESP-based HC selects an appropriate adjacent voltage vector to operate a three-level converter adequately (without any random switching of voltage vectors). This fact is quite evident from Fig. 11(e). The capacitor voltage balancing scheme is able to maintain the flying capacitor voltage at half of the dc-link voltage (75 V), as shown in Fig. 11(f), with the capacitor voltage band of $\pm$1 V, which gives symmetrical FEC output voltage.

The scheme is tested for variations on line side and load side, as shown in Fig. 12(a) and (b), respectively. During the supply side variation, to satisfy the constant load demand and to make a balance between the input power and output power, the controller generates the reference currents accordingly and maintains the dc-link voltage constant, as evident from Fig. 12(a). The scheme

is tested for dynamic loading condition by varying load resistance using a rheostat. The loading is increased by varying the load resistance from 200 to 100 Ω, keeping the supply voltage constant. As seen in Fig. 12(b), to accommodate the increased load demand, the reference current magnitude is also increased by the controller. The actual current follows the reference current to keep the load voltage ($V_{\rm dc}$) constant, as indicated in Fig. 12(b). Considering 75 V with allowable voltage deviation of ±1 V, i.e., between 74 to 76 V, as shown in Fig. 11(f), for the capacitor voltage balancing scheme, flying capacitor voltages are allowed to deviated ±1 V from the desired voltage of $V_{\rm dc}/2$. If FEC is operated at a dc-link voltage of 150 V, then the flying capacitors are holding the voltage of very satisfactory operation of three-level FEC. To check the performance of the scheme with the higher band, the capacitor voltage band is increased ±10 V, allowing flying capacitor voltage to swing between 65 to 85 V, as shown in Fig. 12(c). This deviation in flying capacitor voltages disturbs the FEC output voltage waveform, as reflected in Fig. 12(c). However, at the same time, the controller keeps the dc-link voltage at a desired value with a slight increase in ripple voltage. To observe the worst case, the capacitor voltage band is increased to ±20 V. The supply current gets highly distorted, as predicted and shown in Fig. 12(d), when the capacitor voltage band is changed from ±1 to ±20 V. Due to the huge variation in capacitor voltages, converter voltage also gets unbalanced, as witnessed in Fig. 12(d), first zoomed window. When the capacitor voltage band is again changed from ±20 to ±1 V, all the three capacitors are again balanced at the desired voltage level with sinusoidal input current and proper converter voltage, as shown in Fig. 12(d), second zoomed window. This proves the effectiveness of the capacitor voltage balancing scheme. The proposed CESP-based HC being fixed band controller works inherently on the variable switching frequency. Performance (sharpness/quality of the line current) is governed by the selection of the value of the hysteresis band for the current error. To validate this, the controller is operated at various values of hysteresis bands, and the experimental results are presented for the same. The results presented in Fig. 11 are for the hysteresis band 0.5–0.8 A. To observe the effect of variation in the hysteresis band, the controller is also operated on different hysteresis band values of 1–1.3 A and 1.5–1.8 A, respectively, as shown in Fig. 12(e) and (f). With larger hysteresis band, switching frequency reduces, which in turn reduces the switching losses and, thereby, improves the efficiency of FEC. However, at the same time, the line current has more ripple, as evident from Fig. 12(e) and (f). By reducing the hysteresis band, more sinusoidal shape of the line current can be achieved at the cost of higher switching frequency (and losses) of the converter. In practice, there is always a tradeoff between the switching frequency (corresponding efficiency) of the converter and the quality of the input current waveform. Also, higher switching frequency operation demands high-speed processors for the control (that also adds to the cost).

During the eventualities, the controller operates FEC in overmodulation (two-level overmodulation or three-level overmodulation) to satisfy the load demand depending on the value of supply voltage and dc-link voltage. As presented in Fig. 13(a)–(c), FEC is operated in three-level six-step operation (extreme case),

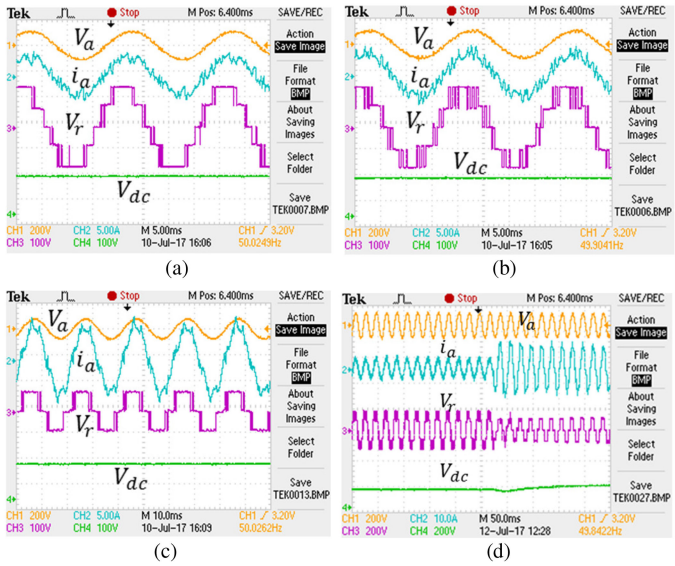

Fig. 13. FEC operation in overmodulation when supply voltage reduced with constant load demand showing (a) extreme case of overmodulation, (b) Starting of overmodulation in three-level operation, (c) overmodulation in two-level mode of operation, and (d) FEC operation in overmodulation when reference dc-link voltage increased with constant supply voltage.

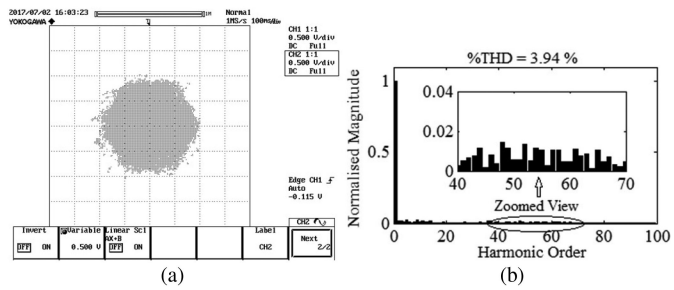

Fig. 14. (a) CESP restricted to the inner hexagonal boundary [Channel 1: Current error on α–phase (Δi_α) (DAC o/p), and Channel 2: Current error on β–phase (Δi_β), (DAC o/p)]. (b) Harmonic profile of line current.

three-level overmodulation with lesser switching, and two-level overmodulation, respectively, as supply voltage decreased keeping the load constant. The controller makes FEC to operate in the overmodulation that demonstrates the self-adaptive nature of the scheme. Needed during contingencies, however, overmodulation is not a preferred mode of operation, as it injects harmonics and distorts input current waveform. At the lower value of supply voltage, to feed the load demand of 150 V dc, FEC is operating at extreme case overmodulation, as shown in Fig. 13(c). This makes the supply current more distorted as compared with the cases, as shown in Fig. 13(a) and (b). Reference dc-link voltage may also rise based on the type of application; to visualize the same, $V_{\rm dcref}$ is increased from 150 to 180 V and vice-versa, keeping the supply voltage constant. When $V_{\rm dcref}$ is increased from 150 to 180 V, due to the enlargement of VSPS, FEC operates in overmodulation (two level), as visible in Fig. 13(d), which shows the self-adaptive nature of the proposed controller.

Here, sector detection is done by fractal approach and it maintains CESP within the prescribed inner hexagonal boundary

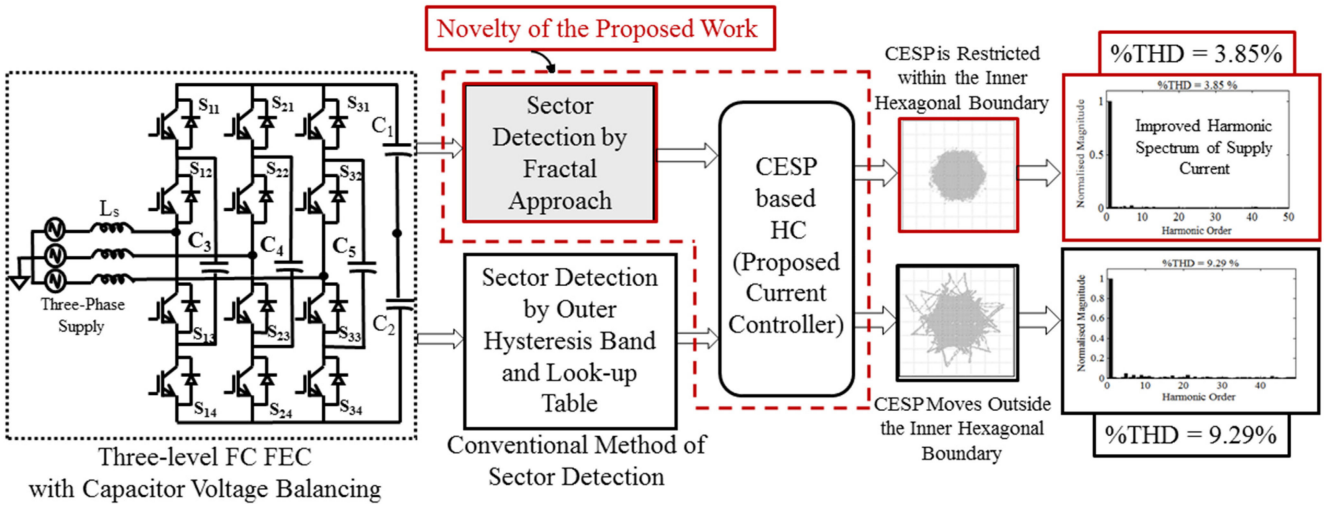

Fig. 15. Improvement in THD% of input current by implementing CESP-based HC employing fractal approach on three-level FC FEC.

(in the absence of outer band), as shown in Fig. 14(a). This makes the source current sinusoidal with %THD 3.85% [see Fig. 14(b)], well below the allowable limit of prescribed standards.

Also, Fig. 15 shows the qualitative (shape) and quantitative (%THD) comparison of the line current of the proposed controller with conventional dual-band CESP-based hysteresis current controller (HCC). Hence, a holistic solution is proposed in the present work for current-controlled multilevel FECs providing easy extension with reduced complexity and better current quality.

VII. Conclusion

A generalized sector detection technique is proposed and analyzed for multilevel FEC employing CESP-based HC. Applying triangularization operations, the fractal approach enables sector detection by locating the tip of the supply voltage vector. This information of sector is used by the CESP-based HC to control FEC. The detailed flowchart is presented to integrate a fractal approach with the CESP-based HC. The scheme does not require any outer hysteresis band or any other auxiliary circuit to detect the sector and can be extended for any general (N-level) multilevel FEC. The elimination of the outer hysteresis band improves the harmonic profile of the source current. The proposed controller employing the fractal approach is implemented on a three-level flying capacitor FEC with a flying capacitor voltage balancing scheme. The performance of the controller is verified for various steady-state and dynamic conditions. The presented experimental results prove the effectiveness of the proposed controller. The controller also operates the converter in overmodulation to satisfy the load demand during any contingency and regains normal operation, once the contingencies are over. This demonstrates the self-adaptive nature of the controller. The controller maintains the unity power factor at the line side and provides low %THD (3.85%) in supply current with constant output dc voltage at the load side under all steady-state conditions.

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M. T. Shah (Member, IEEE) received the B.E. degree from Gujarat University, Ahmedabad, India, in 2003, the M.Tech. and Ph.D. degrees from Nirma University, Ahmedabad, India, in 2005, and 2017, respectively, all in electrical engineering.

Since 2005, she has been a member of the Faculty with the Institute of Technology, Nirma University, Ahmedabad, India. She is a Life Member of the Indian Society for Technical Education. She has authored or coauthored more than 50 research papers at national and international levels and guided more than 50 major projects at UG and PG levels. Her areas of interest include power electronics converters, power supplies, multilevel converters, power quality improved devices, and renewable source integration to grid.

Siddharthsingh K. Chauhan (Member, IEEE) received the B.E. degree from Gujarat University, Ahmedabad, India, M.E. degree from Sardar Patel University, Anand, India, and Ph.D. degree from Nirma University, Ahmedabad, India, all in electrical engineering, in 2003, 2005, and 2014, respectively.

He is currently an Associate Professor with the Department of Electrical Engineering, Institute of Technology, Nirma University, Ahmedabad, India. His research interests include power quality improvement devices, advanced current controllers, digital signal processor based power electronic systems, power electronics' applications to power systems, and applications of artificial intelligence to power electronic systems.

P. N. Tekwani (Senior Member, IEEE) received the B.E. degree in power electronics, the M.E. degree in electrical engineering (industrial electronics), and the Ph.D. degree from the Indian Institute of Science, Bangalore, India, in 1995, 2000, and 2006, respectively.

From 1995 to 1996, he was with Amtech Electronics Pvt., Ltd., Gandhinagar. From 1996 to 2001, he was with the Electrical Research and Development Association, Vadodara. Since 2001, he has been a member of the Faculty with the Institute of Technology, Nirma University, Ahmedabad, India. He is currently a Director of the Directorate of Research and Innovation, the Dean of the Faculty of Doctoral Studies and Research, and a Professor of Electrical Engineering with Nirma University. He is a Life Member of the Indian Society for Technical Education and Young Associate of the Indian National Academy of Engineering. He has authored or coauthored more than 95 research papers at national and international levels and guided more than 75 major projects at UG and PG levels. His research interests include induction motor drives, power quality, active power filters, front-end pulsewidth modulation converters, and multilevel inverters.

Dr. Tekwani was a recipient of several national awards from ISTE, INAE, and IEI.