Design of a Paralleled SiC MOSFET Half-Bridge Unit With Distributed Arrangement of DC Capacitors

Jianzhen Qu, Qianfan Zhang, *Member, IEEE*, Xue Yuan, and Shumei Cui

***Abstract*—Discrete silicon carbide (SiC) MOSFETs are usually connected in parallel to increase their current carrying capacity. However, unequal switching losses and unequal transient current overshoot can limit the maximum switching frequency and maximum current carrying capacity of the paralleled unit. In this article, a paralleled half-bridge unit is proposed to improve the transient current sharing performance, which is characterized by a distributed arrangement of dc capacitors. First, the main causes of the transient current imbalance in traditional power layout are analyzed theoretically for the first time. Then, the traditional power layout is optimized by the ANSYSEM cosimulation techniques to improve the transient current sharing performance. The layout of the gate driver is also optimized to reduce the transmission delay of the gate drive signal. The double pulse tests are carried out to verify the current sharing performance under normal and short-circuit operating conditions. Compared with traditional power layout, the difference in a transient current overshoot of the low-side paralleled SiC MOSFETs is decreased significantly from 10.22% to 2.78% and the difference in switching losses is also reduced. A boost converter is constructed based on the paralleled half-bridge unit. A more uniform temperature distribution indicates the improved current sharing performance by optimizing the power layout.**

***Index Terms*—Current balancing, current distribution, parallel connection, silicon carbide (SiC) MOSFET.**

I. Introduction

COMPARED with silicon technology, silicon carbide (SiC) technology will push the performance limits of switching devices in three directions, higher blocking voltage, higher operating temperature, and higher switching speed [1]–[3]. By using SiC devices in power converters, the system power density can be further increased by reducing the size of cooling systems or passive components [3]–[8]. However, considering the fabrication yields, the available SiC chip sizes at present and in a foreseeable future will not be sufficient for single-chip high-current switches [9]–[12]. To reach the high-current carrying capacity required by high-power converters, it often requires a parallel connection of discrete devices or using multichip power module [1], [8], [10]. Parallel-connected discrete devices, such as the SiC MOSFETs in TO-247 housings, are often used instead of power modules for their lower parasitic parameters and improved power density [12], [13].

For the paralleled operation of discrete SiC MOSFETs, the steady-state current distributions can be balanced by the positive temperature coefficient (PTC) characteristic of the ON-state resistance $R_{\rm on}$ [14], [15]. However, the unequal transient current distribution can cause unequal switching losses, which can affect the thermal distributions and, therefore, limit the maximum switching frequency of the paralleled unit. The current carrying capacity and operating reliability of the paralleled unit are also limited by different transient current overshoots, which may be out of the safe operating area of paralleled SiC MOSFETs [15]–[21]. The main purpose of this work is to balance peak currents during switching transients.

There are generally two main causes of transient current imbalance, the mismatched device parameters and the asymmetrical circuit layout [10], [16], [19], [22]–[27]. The threshold voltage ($V_{\rm th}$) is the most critical device parameter that affects the transient current sharing performance [10], [14], [20]. The $V_{\rm th}$ differences decrease as the fabrication processes are improved [10]. These problems can also be solved, to some extent, by sorting the SiC MOSFETs [9]. The asymmetrical circuit layout will result in unequal parasitic parameters, which can mask and distort the effects of inconsistent device parameters in a realistic setup [8], [10], [11]. It is found in [16], [28], and [29] that the root cause of transient current imbalance in the SiC power module is the source voltage potential difference caused by the mismatched common source parasitic inductance. The transient current distributions can also be affected by the gate drivers, such as the inconsistent gate signal propagation delay [1], [9], [17], [22], [26]. The drive signal levels and transmission delays should be similar to apply synchronized switching signals to the paralleled devices [22].

A lot of research has been performed to improve the transient current sharing performance. The peak currents between two paralleled SiC MOSFETs are balanced in [14] by adding driver source resistors and coupled power source inductors. However, this method may not be applied easily for paralleling more than two devices, and the size of the coupled power source inductors needs to be further minimized. The unbalanced current between paralleled SiC MOSFETs is suppressed in [21] by adding a differential mode choke (DMC). However, the volume of DMC and the interaction mechanism between DMC and SiC MOSFET should be further addressed. There are methods for controlling

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the current imbalance by employing closed-loop control in the gate driver [11], [20], [30]. However, it requires high bandwidth current sensors and amplifiers and may not be applied easily for paralleling more than two devices. The transient current distribution inside the SiC power module is improved in [31]–[33] by optimizing the direct bonded copper (DBC) layout. It is found in [31] that with paralleling half-bridges, the high-side paralleled devices have much smaller transient current imbalance than the low-side paralleled devices. It is found in [32] that the Kelvin connection can partially decouple the parasitic emitter inductance from the gate loop, accelerate the switching speed, and reduce the switching losses. It is found in [33] that the auxiliary source connections can also reduce common source stray inductance, but they cannot completely decouple the gate loop and power loop. Generally, it is costly and time consuming to design novel and effective DBC layouts for paralleling SiC MOSFETs. Additionally, an absolutely symmetrical DBC layout does not exist, so it is a very challenging task to suppress the imbalanced current using the optimized DBC [21]. It is found in [18] that using multiple separate gate drivers can avoid the common source parasitic inductances between paralleled devices. However, the gate signal propagation delay and the driving voltage level of each gate driver must be guaranteed for synchronous switching. It is found in [9] and [11] that using a single gate driver can reduce the problems mentioned when using multiple separate gate drivers. However, the coupling between the power part and the gate driver part needs to be carefully optimized.

The paralleled SiC MOSFET half-bridge unit with the distributed arrangement of dc capacitors is first mentioned in [13]. The large dc capacitors required by the converter are replaced by a distributed arrangement of small paralleled dc capacitors to reduce the switching loop parasitic inductance and improve the transient current sharing performance [8]. Fig. 1 shows the typical working states of the low-side paralleled SiC MOSFETs in this paralleled unit in the double pulse test setup. Fig. 1(a) shows the OFF-state (just before the turn-ON transition state) of the low-side SiC MOSFETs, where the load current flows through the body diodes of the high-side SiC MOSFETs. Fig. 1(b) shows the ON-state (just after the turn-ON transition state) of the low-side SiC MOSFETs. Fig. 1(c) shows the turn-ON transition state of the low-side paralleled SiC MOSFETs, where the distributed dc capacitors supply the transient current. With the distributed arrangement of dc capacitors, the parasitic inductances between the low-side paralleled devices, such as the L_{n1}–L_{n3} as shown in Fig. 1(c), will not experience transient current during the turn-ON transition. Therefore, the current coupling effects between the low-side paralleled SiC MOSFETs as mentioned in [16], [28], [29], [31], and [33] are eliminated. The low-side SiC MOSFETs are turned ON at the same conditions. However, the experimental test results as given in [13] show that the transient current difference during turn-ON transition is about 13%. The main cause of the transient current difference is not analyzed in [13]. For the paralleled unit working in hard-switched and high-frequency applications, the transient current imbalance could lead to unbalanced switching losses and, therefore, need to be minimized.

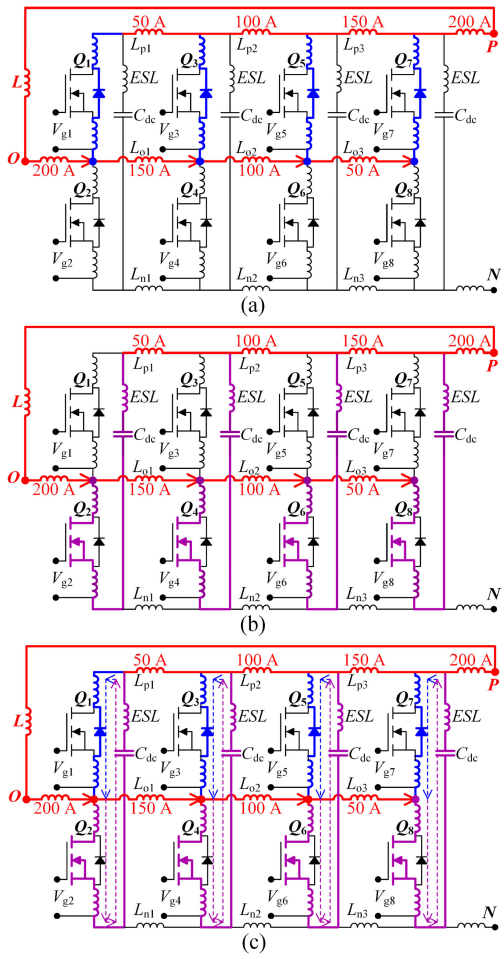

Fig. 1. Working states of the low-side SiC MOSFETs in double pulse test circuit. (a) OFF state. (b) ON state. (c) Turn-ON transition state.

In this article, the design goal is a half-bridge unit that can switch a peak current of 200 A at a dc voltage of 800 V. This half-bridge unit will be operated as a boost converter. At the beginning of this design, the SiC MOSFETs that can be obtained easily is the C2M0040120D. The proposed half-bridge unit is shown in Fig. 2. Eight discrete SiC MOSFETs, labeled as Q_1–Q_8,are used with the distributed arrangement of dc capacitors, labeled as C_1 to C_8. Two gate drivers with separate gate resistors are used to drive the high-side and the low-side paralleled SiC MOSFETs, respectively. In Section II, the main causes of the transient current imbalance in traditional power layout are analyzed for the first time. In Section III, the traditional power layout is optimized by utilizing the AnsysEM cosimulation techniques [34] to improve the transient current sharing performance without adding extra components. The layout of the gate driver is also optimized in this section to reduce the differences in gate signal transmission delay. In Section IV, the double pulse tests are carried out to verify the current sharing performance under normal and short-circuit operating conditions. A boost converter is constructed based on the paralleled half-bridge unit to evaluate the steady-state temperature distributions. Finally, conclusions are drawn in Section V.

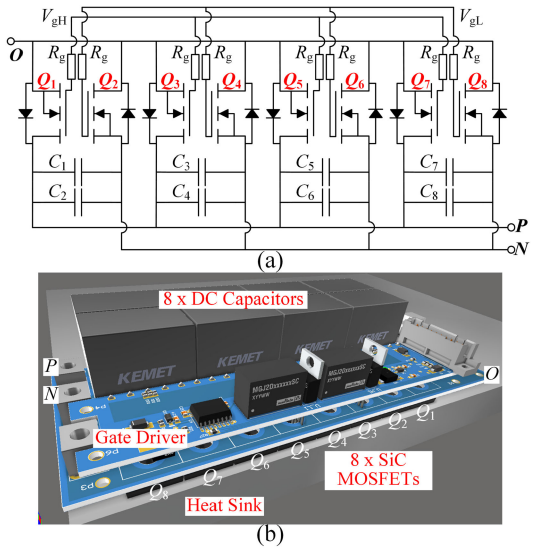

Fig. 2. Proposed half-bridge unit. (a) Schematic. (b) Prototype.

II. Analysis of Transient Current Imbalance

The traditional power layout of the paralleled half-bridge unit with the distributed arrangement of dc capacitors is shown in Fig. 3(a), which is almost the same layout as that given in [13]. The equivalent circuit diagram of the traditional power layout is shown in Fig. 3(b), where L_{s1} and L_{d1} represent the package parasitic inductance of the source and drain leads of SiC MOSFET Q_1, respectively, the L_{o12} represents the layout parasitic inductance between the source lead of Q_1 and the drain lead of Q_2. The layout parasitic inductances L_{o12}, L_{o34}, L_{o56}, and L_{o78} are caused by the layout used to connect the high-side SiC MOSFET and the low-side SiC MOSFET to form the four small half-bridges, respectively. The layout parasitic inductances L_{o23}, L_{o45}, and L_{o67} are caused by the layout used to connect the four small half-bridges to form the paralleled half-bridge unit. However, in the traditional layout, the L_{o12}, L_{o34}, L_{o56}, and L_{o78} are alternately connected in series with the L_{o23}, L_{o45}, and L_{o67}, which results in the mutual couplings among the four small paralleled half-bridges, which ultimately affects the transient current sharing performance.

The mechanism of the transient current imbalance caused by these coupling effects is analyzed by the turn-ON process of the low-side paralleled SiC MOSFETs. Fig. 3(c), which is equivalent to Fig. 3(b), shows the OFF-state (just before the turn-ON transition state) of the low-side SiC MOSFETs, where the load current flows through the body diodes of high-side paralleled SiC MOSFETs. The steady-state current is evenly distributed by optimizing the layout and sorting the paralleled SiC MOSFETs. At this stage, the current at each point remains constant. The potentials at the following points are equal as shown:

$$V_{s1} = V_{s3} = V_{s5} = V_{s7} = V_{d2} = V_{d4} = V_{d6}. \quad (1)$$

Fig. 3(d) shows the turn-ON transition state of the low-side paralleled SiC MOSFETs, where the distributed dc capacitors supply the transient current. During the turn-ON current rising stage, there are positive current changes *di/dt* through the L_{o12}, L_{o34}, L_{o56}, and L_{o78}. Since the mounting height of the SiC MOSFETs is guaranteed to be the same as much as possible, the package parasitic inductance of each part is almost the same. The potentials at the following points are expressed as:

$$V_{s1} = V_{s3} = V_{s5} = V_{s7} > V_{d2} = V_{d4} = V_{d6}. \quad (2)$$

Therefore, there are negative potentials and negative currents through the L_{o23}, L_{o45}, and L_{o67} as shown in Fig. 3(d). For example, the L_{o12}, L_{o34}, L_{o56}, and L_{o78} are about 3.3 nH and the L_{o23}, L_{o45}, and L_{o67} are about 6.8 nH, which are extracted in the Q3D. Assuming that the *di/dt* is 1 A/ns, there will be a potential of -3.3 V and a *di/dt* of -0.49 A/ns across the L_{o23}, L_{o45}, and L_{o67}. The transient current distributions will be expressed as (3), where the I_{ds2}, I_{ds4}, I_{ds6}, and I_{ds8} represent the currents flow through the low-side paralleled SiC MOSFETs

$$I_{ds2} > I_{ds4} > I_{ds6} > I_{ds8}. \quad (3)$$

The measured turn-ON current distributions of the low-side paralleled SiC MOSFETs is shown in Fig. 3(e), which is consistent with the above theoretical analysis, where the measurement setup will be given in Section IV-A. During the turn-ON process of the low-side paralleled SiC MOSFETs, the current distributions of the high-side paralleled body-diodes is almost the same as shown in Fig. 3(f). This indirectly proves that the turn-ON current imbalance of the low-side paralleled SiC MOSFETs is caused by the coupling effects between the four small paralleled half-bridges.

The turn-OFF process of the low-side paralleled SiC MOSFETs can also be analyzed in the same way. The difference is that there are negative *di/dt* through the L_{o12}, L_{o34}, L_{o56}, and L_{o78}, and there are positive potentials and positive currents through the L_{o23}, L_{o45}, and L_{o67}. The transient current distributions will be expressed as (4), where the I_{sd1}, I_{sd3}, I_{sd5}, and I_{sd7} represent the current's flow through the body diodes of high-side paralleled SiC MOSFETs. The measured results are shown in Fig. 3(h), which agrees with the theoretical analysis

$$I_{sd1} < I_{sd3} < I_{sd5} < I_{sd7}. \quad (4)$$

According to the above analysis, in order to improve the transient current sharing performance, it is necessary to reduce the L_{o12}, L_{o34}, L_{o56}, and L_{o78} or increase the L_{o23}, L_{o45}, and L_{o67}. The easiest way is to increase the L_{o23}, L_{o45}, and L_{o67} by extending the distance between the four small half-bridges.

However, in some applications, the size of the power layout is limited and cannot be increased due to system requirements. It is, therefore, impossible to extend the distance between the four small paralleled half-bridges.

In order to reduce these aforementioned mutual couplings, the traditional power layout can be improved by adding separation slots [35] as shown in Fig. 4(a). The expected ideal equivalent circuit diagram of the improved power layout is shown in Fig. 4(b), where the L_{o12}, L_{o34}, L_{o56}, and L_{o78} are no longer alternately connected in series with the L_{o23}, L_{o45}, and L_{o67}. The turn-ON process of the low-side paralleled SiC MOSFETs is shown in Fig. 4(c) and (d), where the mutual couplings between the four small half-bridges are removed.

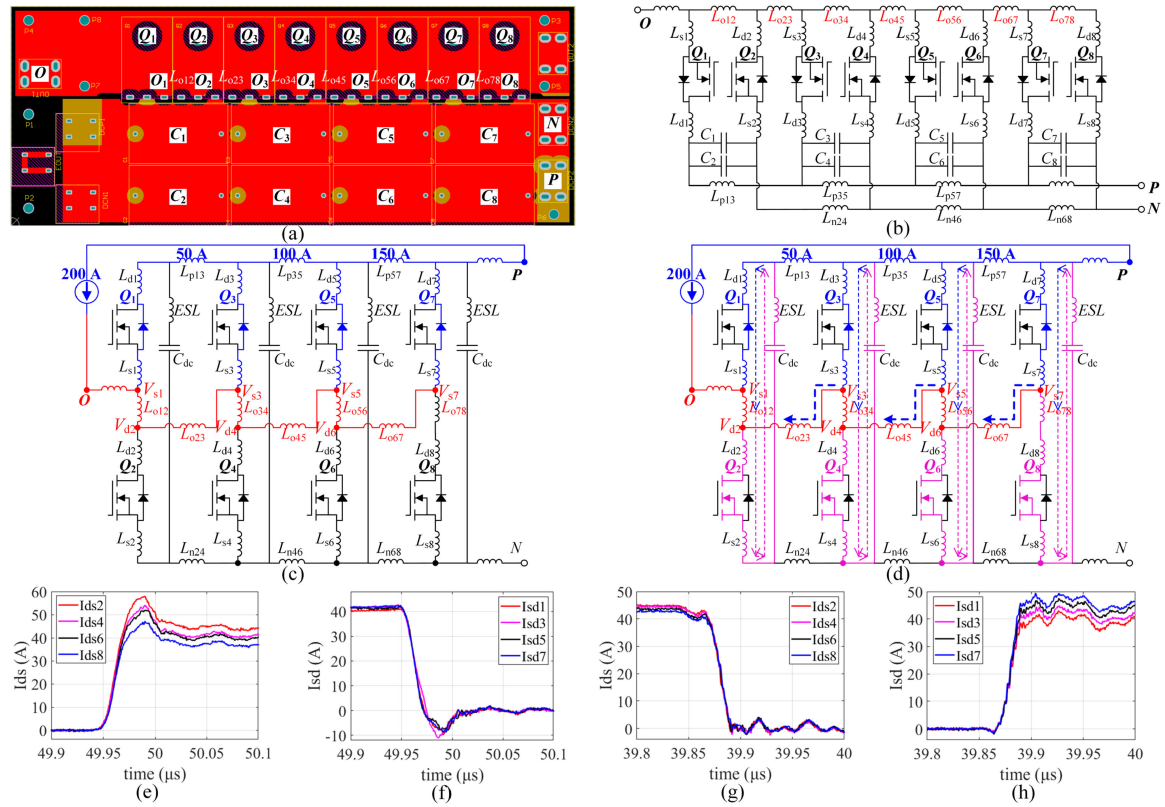

Fig. 3. Analysis of the transient current imbalance in the traditional power layout. (a) Traditional power layout. (b) Equivalent circuit diagram. (c) Load current flows through the body diodes of the high-side SiC MOSFETs. (d) Turn-ON transition of the low-side SiC MOSFETs. (e) Measured turn-ON current distributions of the low-side SiC MOSFETs. (f) Measured turn-OFF current distributions of the high-side body-diodes. (g) Measured turn-OFF current distributions of the low-side SiC MOSFETs. (h) Measured turn-ON current distributions of the high-side body-diodes.

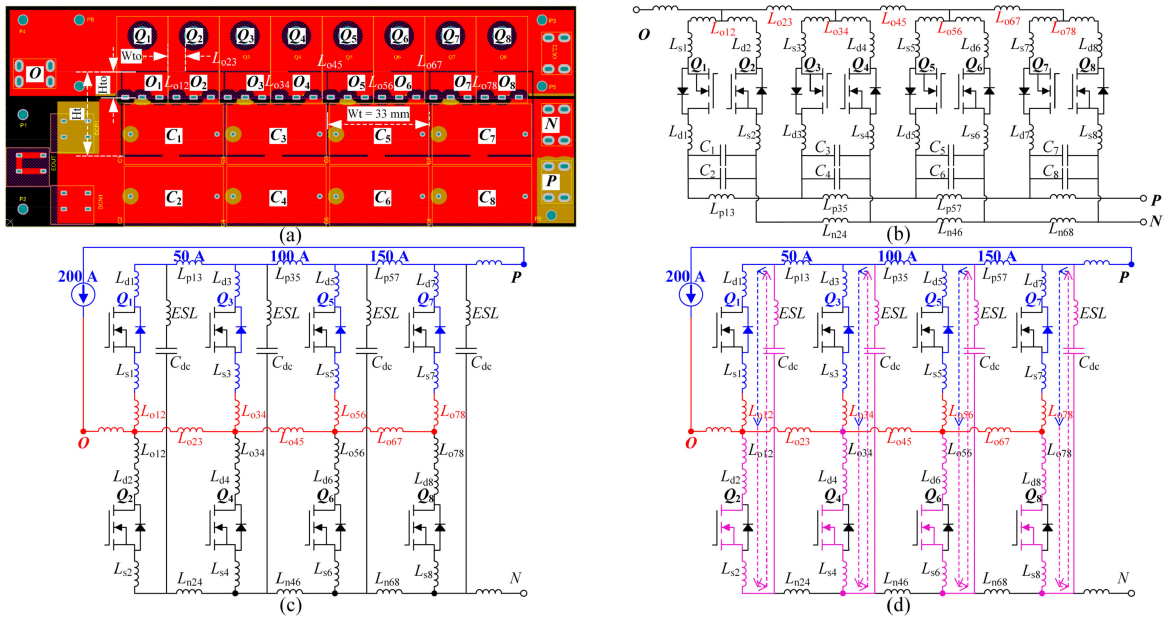

Fig. 4. Analysis of the expected transient current sharing performance in the improved power layout. (a) Improved power layout. (b) Equivalent circuit diagram. (c) Load current flows through the body diodes of the high-side SiC MOSFETs. (d) Turn-ON transition of the low-side SiC MOSFETs.

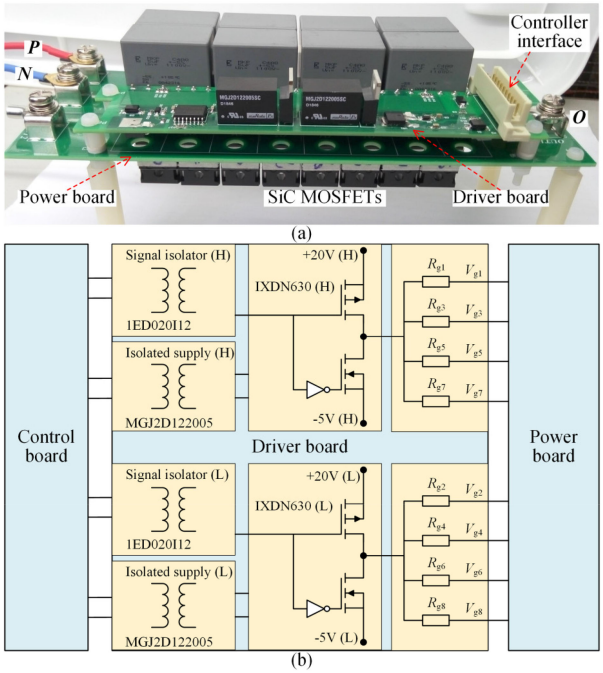

Fig. 5. Proposed gate driver. (a) Dedicated driver board installed in the paralleled half-bridge unit. (b) Schematic of the gate driver.

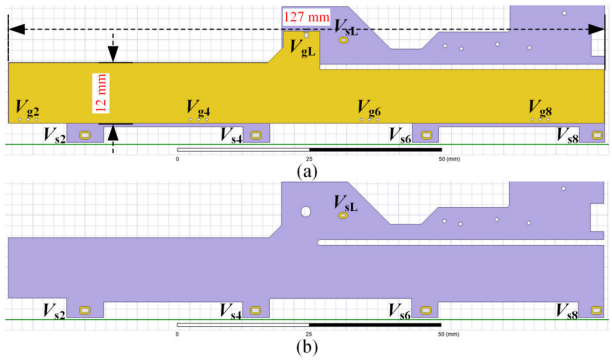

Fig. 6. Layout for the V_{gL}. (a) Complete layer. (b) Bottom layer.

TABLE I
GATE LOOP PARASITIC INDUCTANCES

	V_{g1}	V_{g3}	V_{g5}	V_{g7}	V_{g2}	V_{g4}	V_{g6}	V_{g8}
$L_{gs(pcb)}$ (nH)	6.58	5.98	6.26	6.87	5.86	5.28	5.36	6.17
$L_{gs(loop)}$ (nH)	27.48	26.88	27.16	27.77	26.76	26.18	26.26	27.07

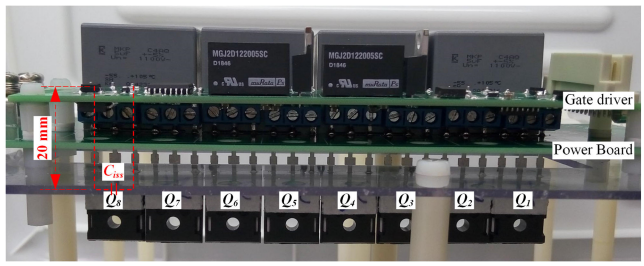

Fig. 7. Gate driver board installed on the power board.

However, the above analysis is performed under ideal conditions. It is difficult to achieve in practice, especially in some applications, such as the size of the power layout and the location of the input and output ports are fixed. Therefore, it is necessary to optimize the size of the separation slots. The difficulty with this optimization is that the relationship between the size of the separation slots and the improvement in transient current sharing performance cannot be simply quantified, but can only be qualified approximately by simulation. The optimization process will be given in Section III-B.

III. Optimize the Layouts of the Half-Bridge Unit

In this section, the design of the gate driver used in the paralleled half-bridge is given first. Then the process of optimizing the size of the separation slots through the circuit cosimulation techniques is given.

A. Design of the Gate Driver

For driving the paralleled SiC MOSFETs, compared with multiple separate gate drivers, the single gate driver could handle both parameters spread and circuit asymmetries in a better way to improve the current sharing performance with the reduced component count and cost [9], [10]. In the proposed half-bridge unit, two single drivers are implemented on a dedicated board as shown in Fig. 5(a) to drive the high-side and low-side paralleled SiC MOSFETs, respectively. The schematic diagram of the gate driver is shown in Fig. 5(b). The 1ED020I12 is used as the signal isolator [13], which also provides the desaturation protection under short-circuit conditions. The SiC MOSFET C2M0040120D requires a gate drive current of 5.81 A. Considering the drive current of the 1ED020I12 is limited to 2 A, one push-pull stage IXDN630 is added, which can supply a peak current of 30 A. The gate voltage is generated by an isolated dc/dc converter. Separate gate resistors are used for the paralleled SiC MOSFETs, which help to prevent the self-oscillations on the gate side when using a common gate resistor [19]. The external gate resistors used in this article are 2.5 Ω, which is the recommended value given in the datasheet of the C2M0040120D.

The asymmetric gate driver layout can affect the transient current distributions between the paralleled devices [17]. The gate driver signal propagation delay is affected by the mismatch of the gate loop parasitic parameters [13]. The layout of the gate driver must be optimized in such a way that the various parasitic inductances will be distributed equally [9]. In the proposed unit, the gate driver layout is optimized by utilizing the bus-bar techniques [36], as shown in Fig. 6, to reduce and balance the gate loop parasitic inductances. The extracted gate loop parasitic inductances $L_{gs(pcb)}$ caused by the layout are shown in Table I. The terminal inductance L_{gs} in the TO-247 package at the lead length of 20 mm, as shown in Fig. 7, is extracted as 20.90 nH. The total gate loop parasitic inductances $L_{gs(loop)}$ are shown in Table I, which are dominated by the terminal inductances L_{gs} and the differences in $L_{gs(pcb)}$ can be neglected.

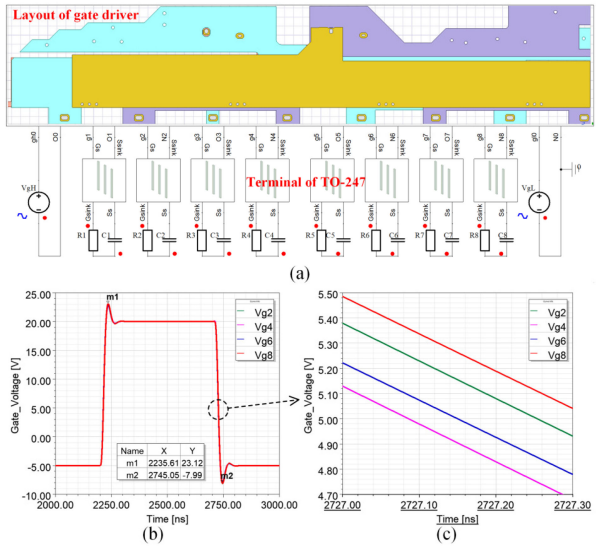

Fig. 8. Simulation of the gate waveforms. (a) Cosimulation model. (b) Simulated gate waveforms. (c) Close-up view during falling edge.

However, the parasitic capacitance of the proposed layout as shown in Fig. 6 will increase, which will increase the gate driver losses. The parasitic capacitance is extracted as 319 pF. However, considering the input capacitance ($C_{\rm iss}$) of a SiC MOSFET is 1893 pF and the total $C_{\rm iss}$ in the paralleled unit is 7572 pF, the parasitic capacitance added by the gate driver layout is only about 4.21%, which can be neglected.

The circuit cosimulation model is developed to analyze the gate switching voltage spikes and the differences in the gate signal propagation delay. The frequency-dependent parasitic models of the layout and the TO-247 package are dynamically linked in the model as shown in Fig. 8(a), where the gate driver signal is applied by an ideal trapezoidal voltage waveform with a rising time of 13 ns and the $C_{\rm iss}$ is replaced by an ideal linear capacitor of 1893 pF for simplicity. The simulated gate voltage waveforms are shown in Fig. 8(b) with the voltage overshoot of 23.12 V and the voltage undershoot of −7.99 V, which are within the maximum ratings (+25/−10 V) of the SiC MOSFET C2M0040120D. The close-up view of the gate voltage waveforms during the falling edge is shown in Fig. 8(c), where the maximum propagation delay is 0.24 ns, which is negligible compared with the total gate turn OFF transition time of approximately 16 ns.

In this subsection, the gate driving voltage levels of the four paralleled SiC MOSFETs are guaranteed by using a single common gate driver, and the gate drive signal propagation delay is guaranteed by optimizing the driver layout. Therefore, the synchronized identical switching signals are applied to the paralleled SiC MOSFETs.

B. Optimization of the Power Layout

As mentioned in Section II, the relationship between the size of the separation slots and the improvement in transient current sharing performance cannot be simply quantified. In this section, the size of the separation slots as shown in Fig. 4(a) is optimized qualitatively by simulation.

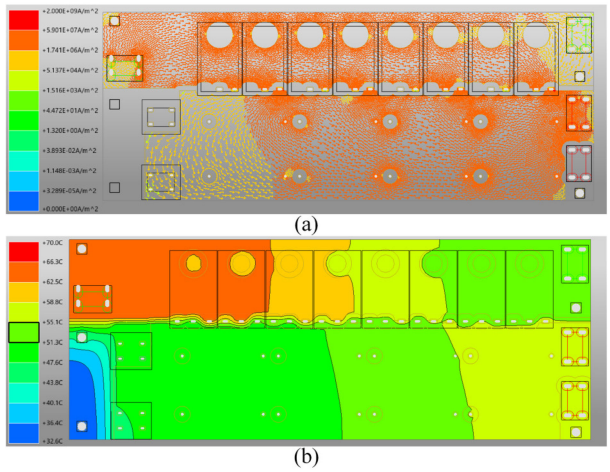

Fig. 9. Power loss and temperature rise of the traditional power layout. (a) Current density simulated in the SIwave. (b) Temperature rise obtained by the cosimulation of SIwave and Icepak.

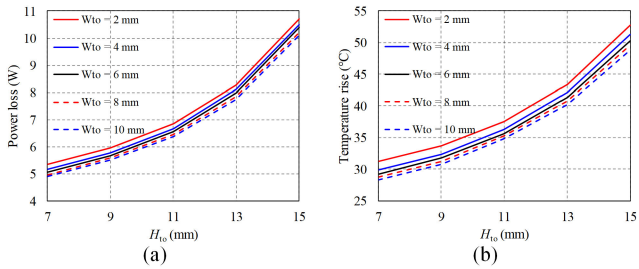

Fig. 10. Relationship between the size of the separation slot and the steady-state loss and the resulting temperature rise of the power layout. (a) Power loss. (b) Temperature rise.

Due to the width limitation of the power layout, the width W_t of the separation slot is fixed, and the value is 33 mm. The opening width $W_{\rm to}$ and the height $H_{\rm to}$ of the separation slot can be optimized. After the $H_{\rm to}$ is fixed, the total height H_t needs to be adjusted to ensure the steady-state current sharing performance. The limiting factors for adjusting the $W_{\rm to}$ and the $H_{\rm to}$ are the steady-state power loss and the resulting temperature rise of the power layout.

Through the simulations performed in the SIwave and the Icepak, the relationship between the size of the separation slot and the steady-state loss and the resulting temperature rise of the power layout can be obtained. Fig. 9(a) shows the current density in the traditional power layout and the power loss is simulated as 4.43 W. Fig. 9(b) shows the corresponding temperature distribution, where the average temperature is 51.2 °C. The simulated ambient temperature is set as 25 °C and, therefore, the temperature rise is 26.2 °C. It should be noted that the peak current of the parallel unit designed in this article is 200 A (30 s), where the steady-state current is 100 A. The above simulation is performed under a steady current of 100 A. The relationship between the size of the separation slot and the steady-state loss and the resulting temperature rise of the power layout is shown in Fig. 10.

The following is a simulation model for establishing the relationship between the size of the separation slots and the

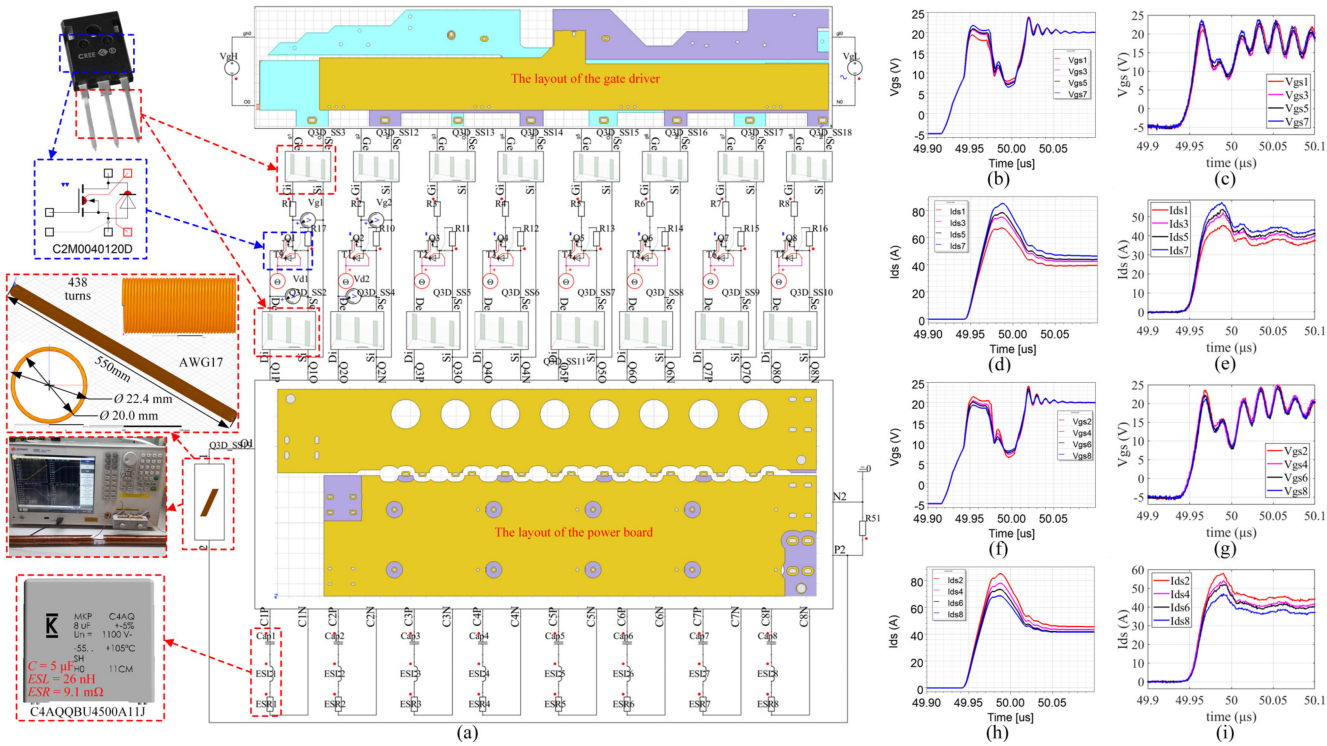

Fig. 11. Simulation model of the double-pulse test platform. (a) Circuit cosimulation model, (b) and (c) Simulated and measured gate voltage waveforms for the high-side SiC MOSFETs. (d) and (e) Simulated and measured current waveforms for the high-side SiC MOSFETs. (f) and (g) Simulated and measured gate voltage waveforms for the low-side SiC MOSFETs. (h) and (i) Simulated and measured current waveforms for the low-side SiC MOSFETs.

improvement in transient current sharing performance. The circuit cosimulation model is developed in the Simplorer as shown in Fig. 11(a), where the frequency-dependent parasitic models of the TO-247 package, the power layout, the gate driver layout, and the air-core load inductor are dynamically linked in the model. Fig. 11(b)–(i) shows the simulated and measured switching waveforms. By comparing Fig. 11(d) and (e), and (h) and (i), the transient current distributions are qualitatively the same.

In this article, the percentage error (E_P) of the current distributions among the paralleled SiC MOSFETs is defined as (5), where the $I_{\max}$, the $I_{\min}$, and the I_{avg} represent the maximum, the minimum, and the average current, respectively

$$E_P = (I_{\max} - I_{\min})/(2 \times I_{\text{avg}}). \tag{5}$$

The simulated transient current difference for the low-side paralleled SiC MOSFETs as shown in Fig. 11(h) is 11.73%, where the measured value as shown in Fig. 11(i) is 10.22%. The mismatches between the simulated and measured waveforms are caused by the modeling accuracy of SiC device models. Developing the model of power devices, considering the simulation accuracy, the simulation time, and the convergence problems, is the future major research work [37]. The relationship between the size of the separation slots and the transient current sharing performance is shown in Fig. 12.

Considering the relationship between the size of the separation slot and the power loss, the temperature rises and the

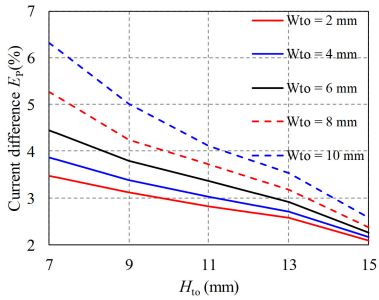

Fig. 12. Relationship between the size of the separation slot and transient current sharing performance for the low-side paralleled SiC MOSFETs.

transient current sharing performance, the size of the separation slot is selected as follows: the W_{to} is selected as 4 mm, and the H_{to} is selected as 9 mm. The transient current difference decreased from 11.73 to 3.39% as shown in Fig. 12, whereas the power loss increased by 30%, from 4.43 to 5.77 W, as shown in Fig. 10(a), and the temperature rise increased by 6.17 °C as shown in Fig. 10(b).

C. Comparison of the Traditional and Improved Power Layout

Two power layouts are fabricated as shown in Fig. 13. Fig. 13(a) shows the traditional power layout. Fig. 13(b) shows the improved power layout, which is characterized by adding four identical separation slots.

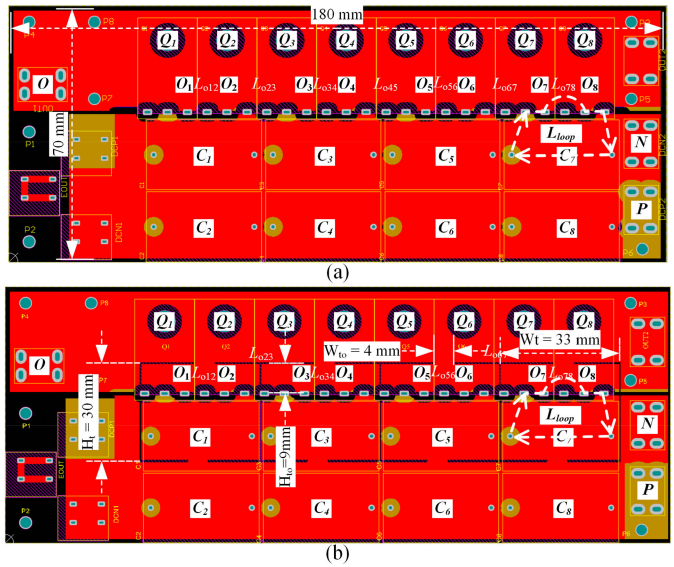

Fig. 13. Two fabricated power layouts for comparison purposes. (a) Traditional power layout. (b) Improved power layout.

TABLE II
DC CURRENT DISTRIBUTIONS FOR THE HIGH-SIDE SiC MOSFETs

Layout	I_{Q1}	I_{Q3}	I_{Q5}	I_{Q7}	I_{diff} (E_P)
Traditional	50.24 A	49.71 A	49.75 A	50.30 A	0.59 A (0.59%)
Improved	50.62 A	49.53 A	49.46 A	50.39 A	1.16 A (1.16%)

TABLE III
DC CURRENT DISTRIBUTIONS FOR THE LOW-SIDE SiC MOSFETs

Layout	I_{Q2}	I_{Q4}	I_{Q6}	I_{Q8}	I_{diff} (E_P)
Traditional	50.12 A	49.60 A	49.66 A	50.62 A	1.02 A (1.02%)
Improved	50.61 A	49.53 A	49.46 A	50.41 A	1.15 A (1.15%)

The parasitic parameters of power layout can have a significant impact on the steady-state current distributions, especially for the paralleled SiC MOSFETs with low R_{on} [1]. The steady-state current distributions in the power layout are determined directly by the simulations in the SIwave. The steady-state current distributions for the high-side and low-side paralleled devices in the two power layouts are shown in Tables II and III with a total current of 200 A and the R_{on} of 40 mΩ. The steady-state current differences are less than 1.16%.

The power layouts are exported to the Q3D to extract the parasitic inductances. The effective frequency f_e is calculated by (6), where the t_f equals 35 ns, which is the typical switching time of the C2M0040120D

$$f_e = 1/(\pi t_f) = 9.1 \text{ MHz}. \quad (6)$$

The local switching loop inductance (L_{loop}) as shown in Fig. 13 caused by the parasitic inductances of the power layout are extracted as shown in Table IV. The L_{loop} is almost equal, which means the transient switching conditions among the four paralleled half-bridges in the two power layouts are almost the same [12].

In this section, without adding extra components, the transient current sharing performance are improved by optimizing the power layout without influencing the L_{loop} as shown in Table IV and the steady-state current distributions as shown in Tables II and III, whereas the power loss in the improved layout is increased by 30%, from 4.43 to 5.77W, and the temperature rise increased by 6.17 °C, which can be accepted.

TABLE IV
LOCAL PARASITIC SWITCHING LOOP INDUCTANCES (nH)

Layout	Q_1-Q_2	Q_3-Q_4	Q_5-Q_6	Q_7-Q_8
Traditional	7.83	7.84	7.81	7.74
Improved	8.20	8.20	8.21	8.13

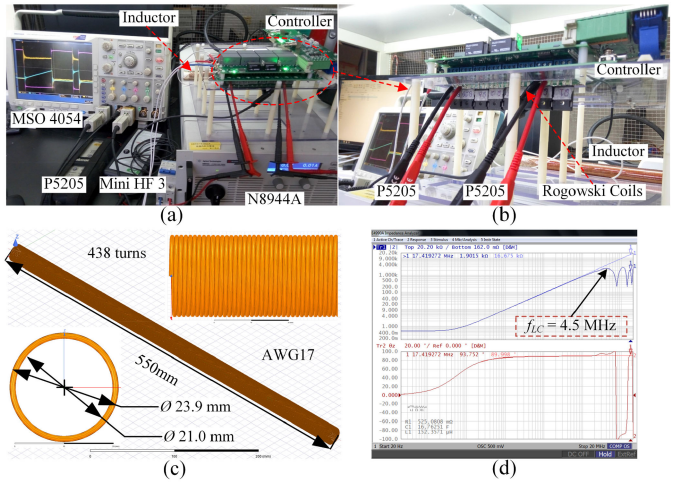

Fig. 14. Experimental verification. (a) and (b) Double pulse test setup. (c) Air-core load inductor. (d) Measured impedance of the inductor.

IV. EXPERIMENTAL VERIFICATION

In this section, experiments are carried out to verify the current sharing performance of the paralleled half-bridge unit under normal and short-circuit working conditions. A boost converter is constructed based on the paralleled half-bridge unit to evaluate the steady-state temperature distributions.

A. Experimental Setup

The current sharing performance of the paralleled SiC MOSFETs in the half-bridge unit is evaluated with a double pulse test setup as shown in Fig. 14(a) and (b), which consists of a dc power supply N8944A, an air-core inductor (150 μH), and the half-bridge unit installed with dc capacitors (40 μF) [38]. The half-bridge unit operates up to 700 V and 160 A.

The air core inductor used in the double-pulse tests is constructed of one layer of windings (AWG17) to minimize the equivalent parallel capacitance (EPC) as shown in Fig. 14(c). Structure parameters of the air-core inductor are the winding turns (N = 438), the winding length (l = 540 mm), and the winding diameter (d = 20 mm). The inductance is 152.36 μH and the EPC is 8.23 pF measured by an impedance analyzer E4990A as shown in Fig. 14(d). Considering the output capacitance of the SiC MOSFET C2M0040120D is 600 pF (four devices in parallel).

TABLE V
DIFFERENCES OF CURRENT DISTRIBUTIONS IN THE TRADITIONAL AND IMPROVED LAYOUTS

		Transient current differences				Steady state current differences			
		M(1/3/5/7)(e)	M(2/4/6/8)(g)	D(1/3/5/7)(j)	D(2/4/6/8)(l)	M(1/3/5/7)(f)	M(2/4/6/8)(h)	D(1/3/5/7)(i)	D(2/4/6/8)(k)
Traditional (Fig. 15)	I_{avg}	52.45	52.85	45.60	46.50	43.05	43.90	41.30	41.80
	I_{max}	57.80	58.00	49.40	50.40	44.20	44.80	41.80	42.40
	I_{min}	45.60	47.20	41.80	42.80	42.40	42.80	40.40	40.80
	E_P	11.63 %	10.22 %	8.33 %	8.17 %	2.09 %	2.28 %	1.69 %	1.91 %
Improved (Fig. 16)	I_{avg}	52.70	53.95	46.70	46.70	43.10	43.55	41.15	41.85
	I_{max}	55.00	55.40	48.80	47.80	44.20	44.40	42.20	42.60
	I_{min}	48.60	52.40	45.20	45.60	42.20	42.40	40.40	41.00
	E_P	6.07 %	2.78 %	3.85 %	2.36 %	2.32 %	2.30 %	2.19 %	1.91 %

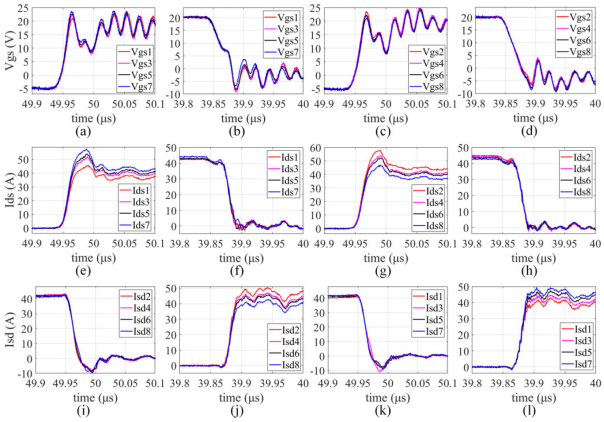

Fig. 15. Experimental waveforms for the traditional layout. (a)–(d) Gate voltage waveforms. (e)–(h) Current waveforms for the MOSFETs. (i)–(l) Current waveforms for the body diodes.

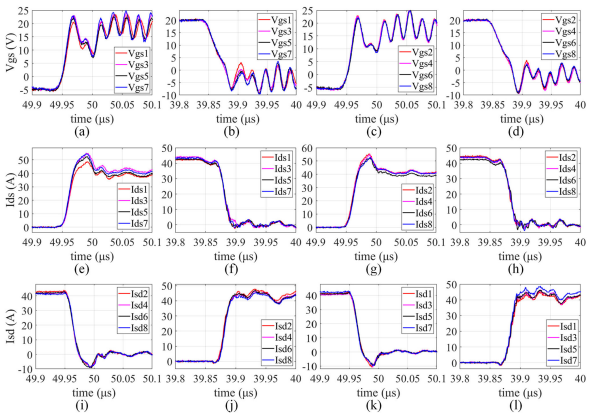

Fig. 16. Experimental waveforms for the improved layout. (a)–(d) Gate voltage waveforms. (e)–(h) Current waveforms for the MOSFETs. (i)–(l) Current waveforms for the body diodes.

The EPC of the air core inductor can be neglected for the analysis of switching dynamics.

For SiC devices, dynamic measurements require sensors with large bandwidths [1], [38]. The collector voltage and the gate voltage are measured by the MSO4054B oscilloscope with the high-voltage probes P5205 (100 MHz). For the current measurements, the use of four coaxial shunts is deemed too complicated in terms of the layout design and could have led to overheating in steady-state converter operation [1]. Consequently, the current measurements are performed with the Rogowski coils PEMUK CWT miniHF 3 with bandwidths of 12 Hz–30 MHz. Although these sensors introduce time delays in the measurements, they provide an accurate image of the current waveforms [1]. This was previously validated in [2] on a single and double-pulse test bench using a current coaxial shunt. The test position of the Rogowski coil remains unchanged, and each set of waveforms has been measured several times, and these waveforms have basically remained essentially unchanged.

B. Switching Waveforms

The current distributions in the traditional and the improved layouts are presented in Figs. 15 and 16, respectively, where the I_{ds1}, I_{ds3}, I_{ds5}, and I_{ds7} represent the currents through the high-side paralleled SiC MOSFETs, the I_{sd1}, I_{sd3}, I_{sd5}, and I_{sd7} represent the currents through the body-diodes of the high-side paralleled SiC MOSFETs, the I_{ds2}, I_{ds4}, I_{ds6}, and I_{ds8} represent the currents through the low-side paralleled SiC MOSFETs, the I_{sd2}, I_{sd4}, I_{sd6}, and I_{sd8} represent the currents through the body-diodes of the low-side paralleled SiC MOSFETs. The switching waveforms include the gate voltage V_{gs} and the drain-source current I_{ds}.

Fig. 15 shows the switching waveforms in the traditional power layout, which show that the transient current imbalance mainly occurs during the turn-ON transients, as shown in Fig. 15(e), (g), (j), and (l), and the turn-OFF transient current sharing performance is satisfactory, as shown in Fig. 15(f), (h), (i), and (k). The relative magnitudes of the transient current overshoot in Fig. 15(e), (g), (j), and (l) are shown in (7), (8), (9), and (10), respectively, which are consistent with the theoretical analysis in Section II

$$I_{ds1} < I_{ds3} < I_{ds5} < I_{ds7} \tag{7}$$

$$I_{ds2} > I_{ds4} > I_{ds6} > I_{ds8} \tag{8}$$

$$I_{sd2} > I_{sd4} > I_{sd6} > I_{sd8} \tag{9}$$

$$I_{sd1} < I_{sd3} < I_{sd5} < I_{sd7}. \tag{10}$$

Fig. 16 shows the switching waveforms in the improved power layout. The transient current sharing performance is improved significantly as shown in Fig. 16(e), (g), (j), and (l).

The current sharing performance in the two power layouts is compared in Table V and Fig. 17. The turn-ON transient current sharing performance is improved significantly for the improved layout as shown in Fig. 17(a). Fig. 17(b) shows that the steady-state current distributions for the two power layouts are within

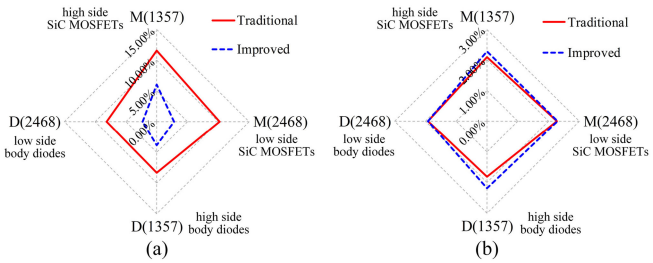

Fig. 17. Comparison of current sharing performance (E_P) in the traditional and improved power layouts. (a) Turn-ON transient current sharing performance. (b) Steady-state current sharing performance.

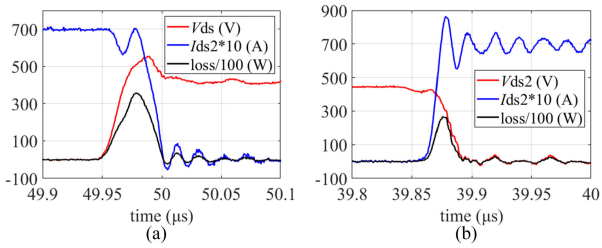

Fig. 18. Calculation of the switching losses. (a) Turn-ON switching loss calculation. (b) Turn-OFF switching loss calculation.

TABLE VI
DIFFERENCES OF SWITCHING LOSSES IN THE TRADITIONAL AND IMPROVED LAYOUTS

		Switching loss differences (mJ)			
		E_{on}(1/3/5/7)	E_{off}(1/3/5/7)	E_{on} (2/4/6/8)	E_{off} (2/4/6/8)
Traditional	E_{avg}	0.985	0.379	1.007	0.365
	E_{max}	1.067	0.387	1.090	0.377
	E_{min}	0.866	0.372	0.900	0.354
	E_P	10.20 %	2.15 %	9.42 %	3.01 %
Improved	E_{avg}	0.958	0.383	0.961	0.376
	E_{max}	0.994	0.392	0.984	0.385
	E_{min}	0.896	0.375	0.940	0.362
	E_P	5.15 %	2.38 %	2.32 %	3.21 %

2.32%, which verifies the validity of the steady-state current simulations in Sections III-C.

Apart from the switching transient current overshoots, it is also important to investigate the associated switching losses. The switching losses have been determined using measured data for the current and the voltage of the SiC MOSFET [9]. The switching energies are calculated by the integration of instantaneous power ($I_{ds} * V_{ds}$) during the turn-ON and turn-OFF transients as shown in Fig. 18 [14]. The delays between the current probe and the voltage probe have been compensated to obtain accurate switching energy.

The switching loss differences in the two power layouts are compared in Table VI and Fig. 19. The switching losses are more balanced in the improved layout as shown in Fig. 19.

C. Short-Circuit Protection

The SiC MOSFETs have smaller chip area and higher current density than the Si power devices and, therefore, tend to have lower short-circuit withstand capability [39]. One of the key reliability issues of the paralleled SiC MOSFET unit is the short-circuit withstand capability [40]. A hard switching fault

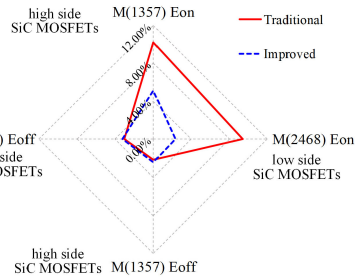

Fig. 19. Comparison of switching loss differences (E_P) in the traditional and improved power layouts.

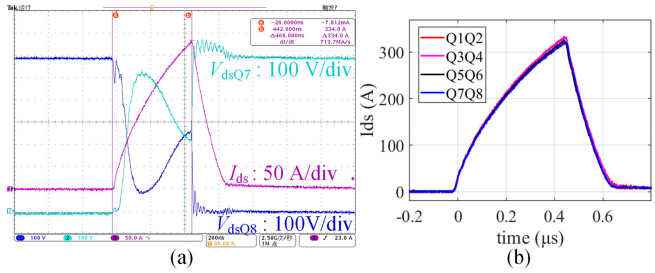

Fig. 20. HSF short-circuit test. (a) Switching waveforms for the SiC MOSFETs Q_7 and Q_8. (b) Comparison of the I_{ds} waveforms in the proposed paralleled half-bridge unit.

(HSF) short-circuit test is performed in this section. During the test, the upper SiC MOSFETs in the paralleled unit are kept in the ON-state, while a short-circuit pulse of 1 μs is applied to the gate of the lower SiC MOSFETs. Fig. 20(a) shows the HSF test switching waveforms of the SiC MOSFETs Q_7 and Q_8 in the proposed half-bridge unit. The gate driver detects the HSF condition within approximately 470 ns and then turns OFF the SiC MOSFETs in 200 ns. During this period of time, the current has already increased to 334 A, which is five times higher than the rated current (60 A) of a single SiC MOSFET.

The HSF current waveforms for the paralleled SiC MOSFETs in the proposed half-bridge unit are shown in Fig. 20(b), which show that the current sharing performance during the HSF short-circuit conditions is also satisfactory.

D. Steady-State Operation

In order to evaluate the impact of the improvement of the transient current distribution on the normal operating performance of the power converter, the paralleled SiC MOSFET half-bridge unit is installed on a heat sink and tested as a boost converter as shown in Fig. 21(a) and (b). The input voltage (400 V) is stepped up to a 750 V with a switching frequency of 50 kHz. A total output power of 45 kW was reached as shown in Fig. 21(d) with the load resistor set as 12.5 Ω. Fig. 21(e) and (f) shows infrared images of the SiC MOSFETs under steady-state operating conditions. Table VII presents the temperature values of each paralleled SiC MOSFETs in the half-bridge unit. The maximum temperature difference of the traditional paralleled unit is 4.5 °C, where the improved unit is 1.2 °C. It is concluded that compared with the traditional parallel unit, the loss distribution of the improved paralleled unit is more uniform.

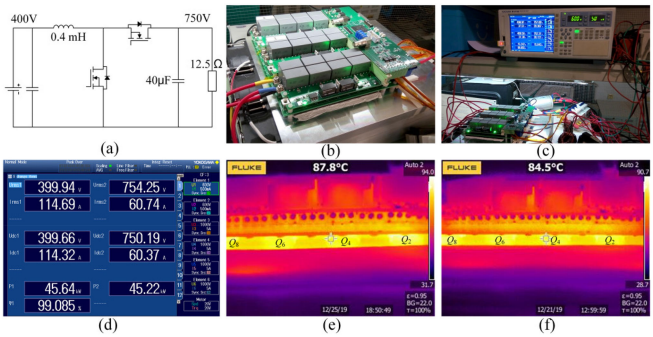

Fig. 21. Steady-state temperature distribution test. (a) Schematic of the synchronous boost converter. (b) Assembly of the half-bridge unit. (c) Steady-state test setup. (d) Screenshot of measurements. (e) Thermal image for the traditional paralleled unit. (f) Thermal image for the improved paralleled unit.

TABLE VII
COMPARISON OF STEADY-STATE TEMPERATURE DISTRIBUTIONS

°C	Q_2	Q_4	Q_6	Q_8	T_{diff}	Q_1	Q_3	Q_5	Q_7	T_{diff}
Traditional	91.1	87.8	87.1	86.6	4.5	73.5	71.9	72.7	72.5	1.6
Improved	85.1	84.5	84.2	83.9	1.2	70.7	71.0	71.7	71.6	1.0

V. CONCLUSION

This article optimized a paralleled half-bridge unit with the distributed arrangement of dc capacitors. The main causes of the transient current imbalance in traditional power layout are analyzed theoretically for the first time and verified by experimental measurements. The power layout is optimized through the AnsysEM cosimulation techniques to reduce the mutual coupling effects by adding separation slots. The gate driver layout is also optimized to guarantee the synchronous switching of the paralleled SiC MOSFETs. Compared to the traditional paralleled half-bridge unit, the differences in the transient current overshoots of the low-side paralleled SiC MOSFETs are decreased significantly from 10.22% to 2.78% and the differences in switching losses are also reduced. The transient current distributions under short-circuit conditions are also satisfactory. A boost converter is constructed based on the paralleled half-bridge unit to evaluate the steady-state temperature distributions, which is more uniform in the improved paralleled unit.

APPENDIX

A. *Sorting the SiC* MOSFETs

In order to solely analyze the effects of layout on the transient current sharing performance of the proposed half-bridge unit, the differences in the intrinsic parameters of the SiC MOSFETs used in the two prototypes are minimized by sorting devices. Thirty arbitrarily selected SiC MOSFETs denoted as M_1 through M_{30} are tested in the laboratory.

The R_{on} and the V_{th} are measured with the simple measurement setup as shown in Fig. 22(a), which includes an oscilloscope or a multimeter, a dc power supply, a thermal imager (not required), and a test fixture. The SiC MOSFETs are mounted with fan cooling as shown in Fig. 22(b).

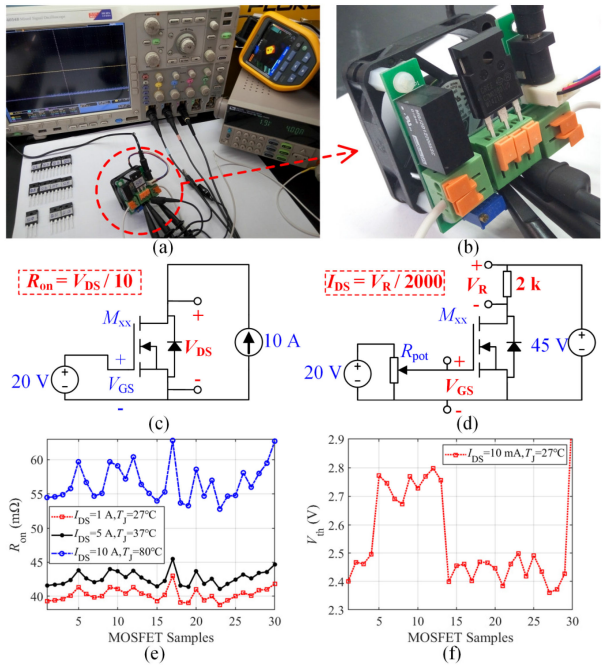

Fig. 22. Sorting the SiC MOSFETs: (a) and (b) measurement setups, (c) and (d) equivalent measurement circuits, and (e) and (f) measurement results.

TABLE VIII
SORTED SiC MOSFETs FOR THE TRADITIONAL LAYOUT

	Q_1 (M_1)	Q_3 (M_{14})	Q_5 (M_{21})	Q_7 (M_{24})		Q_2 (M_2)	Q_4 (M_3)	Q_6 (M_{16})	Q_8 (M_{25})	
R_{on} (mΩ)	54.5	55.1	54.7	54.7	0.55 %	54.6	54.9	55.3	54.8	0.64 %
V_{th} (V)	2.40	2.40	2.38	2.42	0.83 %	2.47	2.46	2.46	2.49	0.61 %

TABLE IX
SORTED SiC MOSFETs FOR THE IMPROVED LAYOUT

	Q_1 (M_{20})	Q_3 (M_{22})	Q_5 (M_{26})	Q_7 (M_{29})		Q_2 (M_{15})	Q_4 (M_{18})	Q_6 (M_{19})	Q_8 (M_{23})	
R_{on} (mΩ)	58.6	57.5	58.1	58.0	0.95 %	54.0	53.7	53.3	53.0	0.93 %
V_{th} (V)	2.45	2.46	2.44	2.42	0.82 %	2.46	2.47	2.47	2.50	0.81 %

The R_{on} is measured with the gate-source voltage (V_{GS}) kept constant at 20 V and the power supply operated in the current source mode as shown in Fig. 22(c). Then, the drain-source voltage (V_{DS}) is measured after the V_{DS} or case temperature of the tested MOSFET becomes stable. The R_{on} variations are plotted in Fig. 22(e) under different currents. The highest R_{on} (M_{17}) is about 1.11 times that of the lowest R_{on} (M_{23}) under the case temperature of 37 °C. The differences in R_{on} will increase at high constant currents due to their PTC effects, which is useful for sorting the devices.

The V_{th} is measured by adjusting the R_{pot} as shown in Fig. 22(d) with the power supply operated in the voltage source mode and kept constant at 45 V, where the voltage V_R is measured to determine the I_{DS}. The V_{th} variations are plotted in Fig. 22(f). The difference between the highest V_{th} (M_{12}) and the lowest V_{th} (M_{27}) is 0.44 V under the I_{ds} of 10 mA.

TABLE X
COMPARISON OF THE PROPOSED PARALLELED UNIT WITH THE SiC POWER MODULE

Power devices @ 25 °C	R_{on}	I_{ds}	Volume	Weight	Price	E_{on}	E_{off}
The paralleled unit 8 x C2M0040120D	10 mΩ	220 A	0.179 L Fig. 23(a)	180 g	$ 309 From MOUSER	4.0 mJ (I_d=160A, V_{ds}=800V)	1.6 mJ (I_d=160A, V_{ds}=800V)
The module & driver 1 x CAS300M12BM2	13 mΩ	193 A	(0.197+0.196) L Fig. 23(b)(c)	290 g	$ 374 From MOUSER	3.71 mJ (I_d=160A, V_{ds}=800V)	1.21 mJ (I_d=160A, V_{ds}=800V)

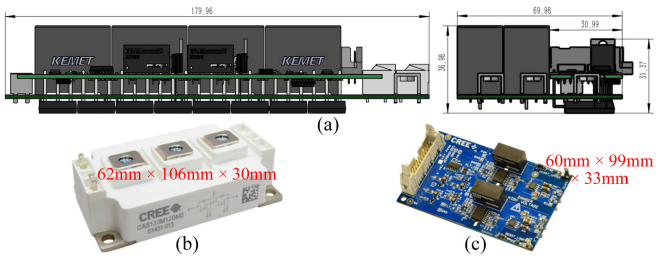

Fig. 23. Comparison of the proposed half-bridge unit with the SiC power module. (a) Structure dimensions of the proposed half-bridge unit. (b) SiC power module CAS120M12BM2 from Cree. (c) Associated gate driver CGD15HB62P1 for the CAS120M12BM2.

The sorted SiC MOSFETs used in the two prototypes are shown in Tables VIII and IX, where the differences in R_{on} are less than 0.95% and that in V_{th} are less than 0.83%.

B. Comparison With the SiC MOSFET Power Modules

The structure dimensions of the proposed paralleled SiC MOSFET half-bridge unit is shown in Fig. 23(a). Considering that the dc capacitor required by the power converter system is utilized by the proposed paralleled unit, the volume of the unit is 0.179 L (180 mm × 31 mm × 32 mm) without including the distributed dc capacitors.

The SiC MOSFETs used in the paralleled half-bridge unit is C2M0040120D, and the maximum current carrying capacity is 60 A (25 °C). Therefore, the theoretical peak output current of the paralleled unit is 240 A, but considering the impact of transient current sharing deviation, the maximum peak current should be lower than 220 A. The SiC power MOSFET power module with the same current carrying capacity of the proposed paralleled unit is CAS300M12BM2 as shown in Fig. 23(b), where the associated gate driver is shown in Fig. 23(c).

The comparisons in terms of volume, weight, and performance are shown in Table X. Compared with SiC MOSFET power module, the proposed paralleled unit is smaller, lighter, and lower cost, but the switching loss is slightly larger, which may be solved by paralleling other SiC MOSFETs with the same package and smaller switching losses.

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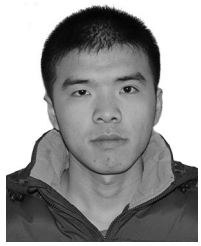

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