

Current Balancing Control Methods Using Advanced Carrier-Based Modulation for Five-Level Current Source Rectifiers

Lisandra Kittel Ries [✉] and Marcelo Lobo Heldwein [✉], *Senior Member, IEEE*

Abstract—In an ideal ac–dc five-level current source multilevel converter, the dc current is equally divided between the two converters connected in parallel. However, current imbalances occur due to the nonidealities of the system, making the current balancing control to improve the multilevel converter performance. This article proposes two different methods for dc current balancing control for a five-level current source rectifier using an advanced carrier-based modulation strategy implemented through three different modulation patterns. A 6-kW prototype is constructed to demonstrate the current balancing control and a comparison among the methods is presented.

Index Terms—Carrier-based modulation, current source converter (CSC), dc current balancing control, multilevel converter.

I. INTRODUCTION

POWER electronics has undergone much evolution in the last decades [1]. The trends of higher electrification levels and control for commercial, industrial, transportation, and medical applications created a significant increase in its role [2]. Three-phase ac–dc current source converters (CSCs) have been gaining attention in several applications, typically where a single-stage nonisolated converter is able to perform active power factor correction and tight control of the dc-side current. An example of a five-level CSC (5L-CSC) circuit is shown in Fig. 1, where higher performance than a three-level topology can be achieved regarding physical dimensions and efficiency mainly due to potentially lower current efforts and better losses distribution. It can be seen that two conventional three-level six-switch CSCs are connected at their dc ports through two interphase transformers IPT_j, with $j = \{p, n\}$. This transformer is used with the aim of dividing the current I_{dc} between the two converters and limit the circulating currents among them. The polarity of the transformer is reversed in order to cancel the local

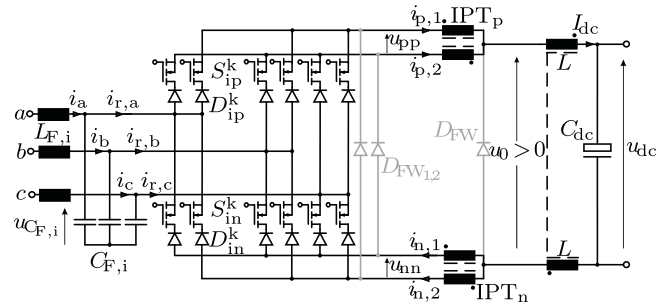


Fig. 1. 5-L CSC formed by paralleling two three-phase CSCs by means of interphase transformers IPT_j, with $j = \{p, n\}$.

average transformer core flux. Fully separated inductors could also be used in place of the interphase transformers (IPTs) and dc-side inductors while resulting in similar waveforms at the ac- and dc-side ports.

For the operation of two six-switch CSCs in parallel, a total of 12 switches with pulsewidth modulation (PWM) shall be commanded. This is achieved here by an interleaving modulation based on two sawtooth carriers with switching period T_{sw} and phase-shifted of π rad. More details of the modulation are found in [3]. This can be generalized for N_c CSCs operating in parallel employing a phase-shift modulation (PS-PWM) implementation that leads to a current converter with $2N_c + 1$ levels. A total of N_c symmetrically phase-shifted carriers for an angle of $\alpha_c = 2\pi/N_c$ within a switching period would be required. This results in that the first current harmonic bands are observed at $N_c f_{sw}$ in the dc-port capacitor filter.

Another advantage of a 5L-CSC, in addition to improving the harmonic distortion rate of three-phase currents when compared to a three-level CSC, is the cancellation of odd harmonics. The first current harmonic appears at twice the switching frequency ($2f_{sw}$) employing a proper modulation strategy. With this feature, the size of the ac- and dc-side filter components can be reduced [4]. Another property is the distribution of the dc-side current between the two converters, which tends to reduced conduction and switching losses [5]. In practice, however, current imbalances might occur mainly due to the nonidealities of the converter components, imperfect gate drive pulses, and the fact that the line voltages vary, even if only a little, during a switching period. Therefore, modulation-based balancing techniques can be used to reduce undesirable unbalances, which

Manuscript received July 23, 2019; revised October 29, 2019 and January 21, 2020; accepted March 16, 2020. Date of publication March 18, 2020; date of current version June 23, 2020. Recommended for publication by Associate Editor M. A. Perez. (Corresponding author: Lisandra Kittel Ries.)

Lisandra Kittel Ries is with the Electrotechnical Department, Federal Institute of Education, Science and Technology of Santa Catarina, Florianopolis 88020-300, Brazil (e-mail: lisandra.ries@ifsc.edu.br).

Marcelo Lobo Heldwein is with the Department of Electronics and Electrical Engineering, Federal University of Santa Catarina, Florianopolis 88040-970, Brazil (e-mail: heldwein@inep.ufsc.br).

Color versions of one or more of the figures in this article are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2020.2982051

are to be avoided because they would lead to concentration of losses in some components and a nonideal behavior regarding the cancellation of harmonics due to interleaving. These effects would cause thermal concerns and over-dimensioned passive components.

One way of balancing the current between N_c -paralleled dc–dc converters is the duty-cycle adjustment through different techniques. These include: carrier modification using ramp-amplitude adjustable current balance, pseudoramp current balance, or time-shift current balance techniques [6], [7]. Other alternative is to directly change the modulation signals as in [8]–[11]. When applied to three-phase multilevel converters, the key point to balancing current control is how to select the appropriate switching combination from the redundant switching states. Many active balancing strategies are explored in [5], [12]–[19]. Those are based on controlling the magnetizing voltages or currents in order to achieve zero average flux in the core within each switching period. A simple implementation method used for a three-phase five-level current source inverter selects the switching combinations using trilogic carrier phase-shifted technique according to the value of the dc inductors current and their voltage polarity [13]. The harmonic performance of the bilogic–trilogic modulation is typically not as high as other modulation techniques and it requires logic resources to be implemented. Redundant switching vectors can be selected to provide the balanced dc-link currents in a space vector modulation (SVM) [14]. SVM typically requires more computation resources than carrier-based ones and this is even more demanding when having to decide on redundant states to promote the current balance. Other alternative using SVM is to vary the on time of an additional free-wheeling state to act on the rate of change of the currents in the dc-side inductors [12]. This additional free-wheeling state happens via an extra active switching state, increasing switching losses. In order to minimize this losses, different control methods can be implemented [15]. Including an additional free-wheeling state to enable the current balance leads to a modified frequency spectrum. The two balancing current techniques proposed in this article are based on a high-performance carrier-based modulation, which prevents the problem of sliding intersections at the changes of the sextants and, thus, enables low distortion ac-side waveforms. The proposed balancing current techniques differ concerning coupling between the currents and additional switching losses. They are based on the modulation technique presented in [3]. However, no balance technique has been presented in that work.

This article begins by introducing the used five-level current source rectifier (5L-CSR) control strategy based on the carrier-based modulation and focusing in the balancing current loop. The basic definitions of the transformer are explained to define which current components are to be controlled. A circuit model of the converter employing IPTs is proposed and analyzed to obtain the balance control oriented model. The model shows that by varying the average voltage applied to the transformer, the value of the transverse current is accordingly modified. Two methods of balancing the currents for the converter are presented, namely: a first method that modifies the original modulation pattern and a

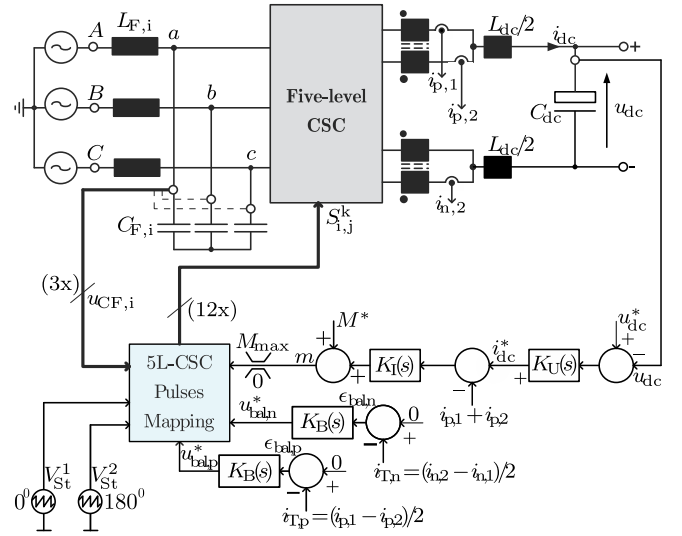


Fig. 2. Block diagram of the 5L-CSR control strategy using the interleaved PWM technique.

second one that modifies the modulation signals values in order to change the local average voltage applied to the IPTs. Finally, simulations and experimental results are presented in order to validate the balancing techniques.

II. 5L-CSR CONTROL STRATEGY

The objectives of the 5L-CSR control strategy are as follows:

- 1) to control the dc-side voltage, where a ramp reference is used for the connection to the grid;
- 2) to control the dc-side current (i_{dc}), including a current limiting function that uses the converter ability to operate with well-controlled current even when a short circuit is applied to its dc-side terminals;
- 3) to guarantee the current balancing of the IPTs currents; and
- 4) to achieve high power factor at the ac-side.

The inherent perturbations to the system are the ac grid voltages, load variations and inaccuracies in the pulses inherent to the analog and digital components used to drive the semiconductors, and to sense the electric quantities of interest. The actuation of the control is performed through the switching functions $s_{i,p/n}^*$ that are generated from the modulation signals using the carrier-based modulation presented in [3]. The closed-loop control scheme that regulates the output voltage u_{dc} and the currents of the IPT $i_{p,1}$, $i_{p,2}$, $i_{n,1}$, and $i_{n,2}$ is seen in Fig. 2.

The external loop is used to regulate the output voltage according to the reference value u_{dc}^* . The output of this loop generates the reference current i_{dc}^* . The current loop ensures that the sum of the currents in the interphase transformers IPT_j have the desired dc value, i.e., $i_{p,1} + i_{p,2} = I_{dc}$ and $i_{n,1} + i_{n,2} = I_{dc}$. A current loop produces the modulation index M that is used to compute the duty ratios δ_i according to

$$\delta_i = M \frac{|u_{CF,i}|}{\hat{U}_g}, \text{ with } i = \{a, b, c\}. \quad (1)$$

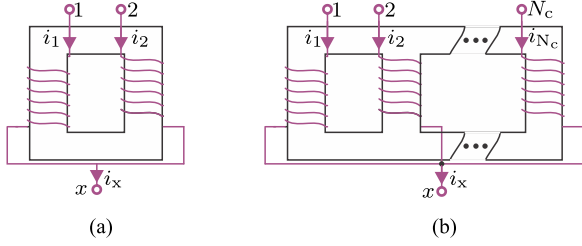


Fig. 3. IPTs used to connect converter legs in parallel. (a) 2-IPT. (b) N_c -IPT employing a single core.

The main focus of this article is the current loop responsible for the dc-side current balancing. The balancing concept is based on the generation of two voltage reference values $u_{bal,p}^*$ and $u_{bal,n}^*$, which are used to compute the balancing duty ratios $\delta_{bal,p}$ and $\delta_{bal,n}$ that are proportional to the conduction time of the modified switching states and are defined with

$$\delta_{bal,j} = |u_{bal,j}^*|, \text{ with } j = \{p, n\}. \quad (2)$$

A null reference value is used to control the transverse dc currents $i_{T,p}$ and $i_{T,n}$, i.e., the average difference of the currents at the output of each converter should be null. The related definitions and models are discussed in the following.

III. IPT DEFINITIONS

IPTs are historically used to improve the connection of power converters in parallel. A basic model of analysis is the composition of inductors in parallel with a negative inductor in series. For the connection of two converters in parallel, the transformer with two windings is used (2-IPT), as shown in Fig. 3(a). To connect N_c converters in parallel, there is the possibility of building a transformer with N_c inputs on the same core, forming the N_c -IPT shown in Fig. 3(b). Other magnetic component arrangements can present the same functionality and would lead to diverse constructive characteristics [20], but lead to similar external waveforms.

The definitions used here for the directions of the currents, voltages, flux linkages, and coupling polarities for the 2-IPT are given in Fig. 4(a). The IPT equivalent circuit model assuming constant permeability and lossless materials is composed of two inductances with value $L_s(k+1)$ and a negative series inductance $-M$, as shown in Fig. 4(b). The IPT circuit symbol employed in this article is in Fig. 4(c). L_1 and L_2 are the self-inductances, M is the mutual inductance, and k is the coupling factor given by $k = \sqrt{1 - \sigma}$ with the dispersion factor $\sigma \in [0, 1]$. Thus, the mutual inductance is given by $M = k\sqrt{L_1 L_2} \geq 0 \mu\text{H}$ [21]. The windings typically present the same turns number, $N = N_1 = N_2$, and thus, the self-inductances are identical ($L_1 = L_2 = L_s$ and $M = kL_s$).

The circuit of Fig. 4(b) also characterizes the longitudinal mode i_L and transverse mode i_T currents, which are defined in terms of the average value of the dc currents i_1 and i_2 as

$$i_L = \frac{\bar{i}_1 + \bar{i}_2}{2}, \quad i_T = \frac{\bar{i}_1 - \bar{i}_2}{2}. \quad (3)$$

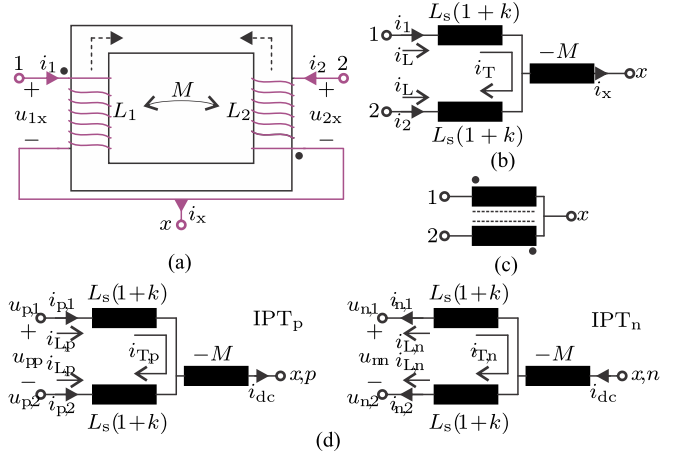


Fig. 4. Definitions for an IPT: (a) component structure, (b) equivalent circuit, (c) circuit symbol, and (d) equivalent circuits used in transformers IPT_p and IPT_n of Fig. 1. Note that the direction of the dc current i_{dc} is reversed in transformer IPT_n .

The discussed notation is applied to the two transformers IPT_j of the 5L-CSC (see Fig. 1), where the voltages across the transformer windings are named u_{pp} and u_{nn} , as shown in Fig. 4(d).

For each transformer IPT_j , with $j = \{p, n\}$, the longitudinal $i_{L,j}$ and transverse $i_{T,j}$ mode currents are defined according to (4) and using the notation presented in Fig. 4. Thus

$$i_{L,p} = \frac{\bar{i}_{p,1} + \bar{i}_{p,2}}{2}, \quad i_{T,p} = \frac{\bar{i}_{p,1} - \bar{i}_{p,2}}{2}$$

$$i_{L,n} = \frac{\bar{i}_{n,1} + \bar{i}_{n,2}}{2}, \quad i_{T,n} = \frac{\bar{i}_{n,2} - \bar{i}_{n,1}}{2}. \quad (4)$$

A. IPT Analysis

The voltages u_{1x} and u_{2x} across the IPT windings are computed with

$$u_{1x} = (1+k)L_s \frac{di_1}{dt} - kL_s \frac{di_x}{dt}$$

$$u_{2x} = (1+k)L_s \frac{di_2}{dt} - kL_s \frac{di_x}{dt} \quad (5)$$

where $i_x = i_1 + i_2$ and considering the polarity marks shown in Fig. 4(b).

Equation (5) can be rewritten in terms of i_1 and i_2 . Thus

$$u_{1x} = L_s \frac{di_1}{dt} - M \frac{di_2}{dt}$$

$$u_{2x} = L_s \frac{di_2}{dt} - M \frac{di_1}{dt}. \quad (6)$$

The circuit given in Fig. 5 assumes that the converter arm voltages are u_1 and u_2 and includes the inductor and filter capacitor. The voltage across the output capacitor C_{dc} is named u_{dc} . This circuit is analyzed in the following with the intention of finding expressions for the current variations in the IPT windings, i.e., $\frac{di_1}{dt}$ and $\frac{di_2}{dt}$.

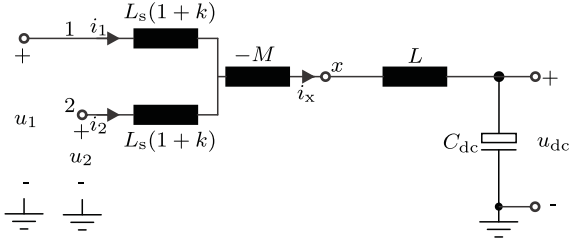


Fig. 5. Complete circuit for finding expressions for the currents variation in the IPT.

The filter inductor L is connected to the x node. The direction of the flows generated by the current low-frequency components of the transformer is verified in Fig. 4(a) and it was concluded that the low-frequency component is virtually canceled within the IPT, given its polarity, connection, and high coupling factor.

Equating the external and internal loops of the circuit, considering that $u_{1dc} = u_1 - u_{dc}$ and $u_{2dc} = u_2 - u_{dc}$ leads to

$$\begin{aligned} u_{1dc} - (L_s + L) \frac{di_1}{dt} + (kL_s - L) \frac{di_2}{dt} &= 0 \\ u_{2dc} - (L_s + L) \frac{di_2}{dt} + (kL_s - L) \frac{di_1}{dt} &= 0. \end{aligned} \quad (7)$$

Equation (7) can be rewritten as

$$\begin{aligned} \frac{di_1}{dt} &= \frac{u_{1dc}(L_s + L) + u_{2dc}(kL_s - L)}{L_s^2(1 - k^2) + 2L(1 + k)L_s} \\ \frac{di_2}{dt} &= \frac{u_{2dc}(L_s + L) + u_{1dc}(kL_s - L)}{L_s^2(1 - k^2) + 2L(1 + k)L_s}. \end{aligned} \quad (8)$$

Assuming $k \approx 1$ and $L_s \gg L$ leads to

$$\frac{di_1}{dt} \approx \frac{di_2}{dt} \approx \frac{u_{1dc} + u_{2dc}}{4L}. \quad (9)$$

Consequently, the output inductor L is the component that mainly influences the ripple of the winding currents i_1 and i_2 and the IPT has little influence on this parameter.

The next objective is to find the IPT transverse mode current as a function of the input voltages of the circuit. According to Figs. 4 and 5

$$u_{12} = u_{1x} - u_{2x}. \quad (10)$$

Replacing (6) into (10) gives

$$u_{12} = (L_s + M) \frac{di_1}{dt} - (L_s + M) \frac{di_2}{dt}. \quad (11)$$

The definition of the transverse mode current is used, as in (3), and a perfect coupling is assumed ($k \approx 1$). Thus

$$\frac{di_T}{dt} \approx \frac{u_{12}}{4L_s}. \quad (12)$$

Thus, the rate of change of the transverse mode current is affected mainly by the difference voltage value u_{12} . This equation is applied to transformers IPT_j and the following transfer functions are obtained by applying the Laplace transform

$$\frac{\tilde{i}_{T,p}}{\tilde{u}_{pp}} = \frac{1}{s4L_s}, \quad \frac{\tilde{i}_{T,n}}{\tilde{u}_{nn}} = \frac{1}{s4L_s}. \quad (13)$$

IV. BALANCING METHOD 1: ADDITION OF ACTIVE SWITCHING STATES

The idea of current balancing method 1 is to change the original modulation patterns [3] so as to add in a given time interval a different state that modifies the average value of the voltages u_{pp} and u_{nn} within a switching period without creating distortions at the ac-side waveforms, i.e., the balancing modulation pattern must guarantee that the synthesized current vectors are the same, even though the employed switching states will be modified to reach the desired balancing effect. Method 1 was briefly introduced in [22]. However, its performance was not evaluated against other balancing methods.

Fig. 6 shows the proposed modifications to patterns 1, 2, and 3, with the addition of extra active states. The extra active states increase the number of commutations per cycle. This change is carried out in an interleaved way, i.e., first by changing the pulses created with the carrier phase-shifted at 180° , the modification is called active state 1 (AS = 1), and later by modifying the pulses generated with the carrier phase-shifted at 0° , the modification is called active state 2 (AS=2).

The extra active states have intervals of Δt_{3s} and Δt_{6s} and are proportional to the value of $\delta_{bal,j}$. Fig. 6 shows that the maximum periods of Δt_{3s} and Δt_{6s} are Δt_3 and Δt_6 , respectively. It turns out that Δt_3 and Δt_6 vary according to the change in the duty ratio δ_1 and this is dependent on location of the according sextant. The maximum value of δ_1 is proportional to the modulation index M . If the index is limited to $M_{max} = 0.9$, the theoretical maximum values for $\delta_{bal,j}$ are known and calculated according to

$$\delta_{bal,max} = 1 - \delta_1 - \delta_{ol} \quad (14)$$

where δ_{ol} is the ratio of the total overlap time used to prevent open circuits at the 5L-CSC over the switching period.

A small value of $\delta_{bal,j}$, for instance much lower than 0.1, is typically enough to enable any required changes on the average values of the IPT voltages since the modulation patterns synthesize ideally balanced waveforms and, thus, only nonmodeled second-order effects would generate unbalances. A limiter for the duty ratio values of this additional active state is then considered. It follows that the duty ratio of $\delta_{bal,lim} = 0.1$ is available on the designed converter during all sextants within a mains period and to any point of operation.

The value of the voltage levels applied to the IPT are known. The voltage envelope has a fundamental frequency of $3f_g$, that is, the fundamental cycle repeats itself every third of the network period $T_g/3$.

The active states added during the intervals Δt_{3s} and Δt_{6s} cause another envelope to be considered. This envelope is used to modify the local average value of u_{pp} for transformer IPT_p and the average value of u_{nn} for IPT_n .

Table I lists the voltages applied to the IPT u_{pp} and u_{nn} and the direction of the variation of the currents $\Delta i_{p,1}$, $\Delta i_{p,2}$, $\Delta i_{n,1}$, and $\Delta i_{n,2}$ for the states of intervals Δt_{1-6} , Δt_{3s} , and Δt_{6s} for region 2 of sextant I and region 1 of sextant II in the case of pattern 3. The table also lists the result of the control action $u_{bal,p}^*$ and $u_{bal,n}^*$ with respect to the structure of Fig. 2.

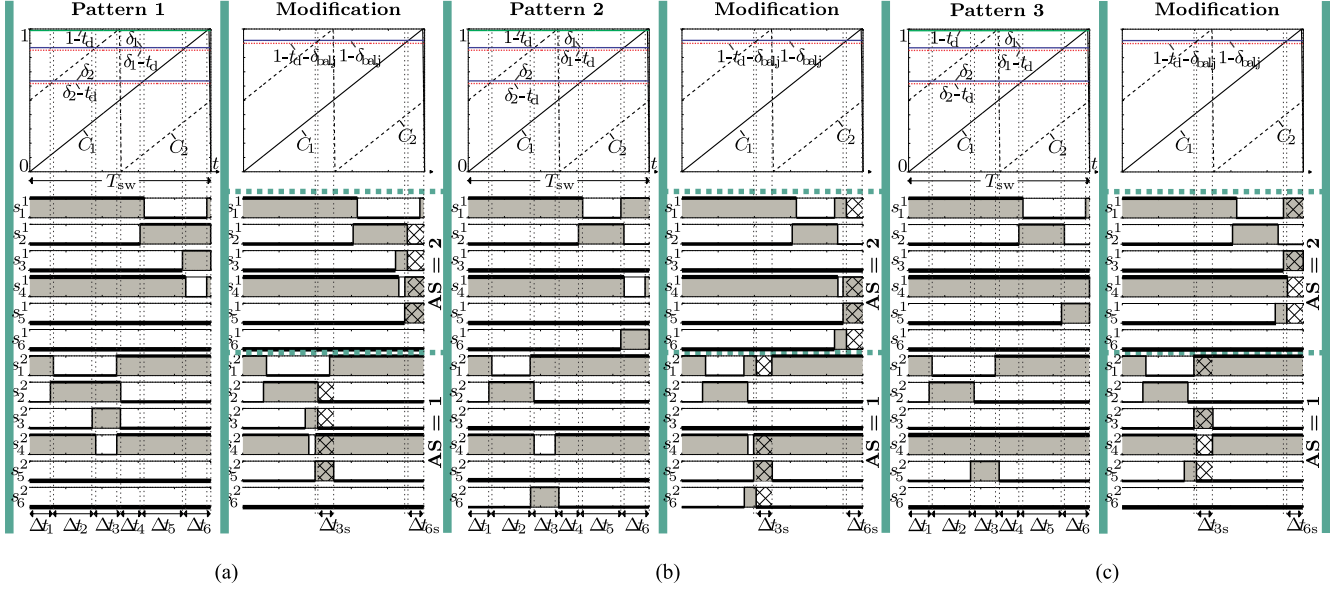


Fig. 6. Modification of the intervals Δt_6 and Δt_3 for the patterns 1–3, modifying the average value of the voltages on the IPTs. (a) Pattern 1. (b) Pattern 2. (c) Pattern 3.

TABLE I
VOLTAGE ON THE IPTS AND VARIATION RATE OF THE TRANSFORMER
CURRENTS FOR EACH SWITCHING INTERVAL WITHIN
A PERIOD T_{sw} FOR PATTERN 3

	Time	\vec{I}_v	u_{pp}	u_{nn}	$\Delta i_{p,1}$	$\Delta i_{p,2}$	$\Delta i_{n,1}$	$\Delta i_{n,2}$	$u_{bal,p}^*$	$u_{bal,n}^*$
Sextant I and Region 2	Δt_1	\vec{I}_8	0	u_{bc}	0	0	↓	↑	x	x
	Δt_2	\vec{I}_9	0	0	0	0	0	0	x	x
	Δt_3	\vec{I}_2	0	u_{ca}	0	0	↑	↓	x	x
	Δt_4	\vec{I}_8	0	u_{cb}	0	0	↑	↓	x	x
	Δt_5	\vec{I}_9	0	0	0	0	0	0	x	x
	Δt_6	\vec{I}_2	0	u_{ac}	0	0	↓	↑	x	x
AS 1	Δt_{3s}	\vec{I}_2	u_{ac}	0	↑	↓	0	0	> 0	x
AS 2	Δt_{6s}	\vec{I}_2	u_{ca}	0	↓	↑	0	0	< 0	x
Sextant II and Region 1	Δt_1	\vec{I}_9	0	0	0	0	0	0	x	x
	Δt_2	\vec{I}_{10}	u_{ab}	0	↑	↓	0	0	x	x
	Δt_3	\vec{I}_2	u_{ac}	0	↑	↓	0	0	x	x
	Δt_4	\vec{I}_9	0	0	0	0	0	0	x	x
	Δt_5	\vec{I}_{10}	u_{ba}	0	↓	↑	0	0	x	x
	Δt_6	\vec{I}_2	u_{ca}	0	↓	↑	0	0	x	x
AS 1	Δt_{3s}	\vec{I}_2	0	u_{ca}	0	0	↑	↓	x	< 0
AS 2	Δt_{6s}	\vec{I}_2	0	u_{ac}	0	0	↓	↑	x	> 0

According to Fig. 6(c), the switching functions s_1^1 , s_3^1 , s_4^1 , and s_5^1 are modified during the intervals Δt_{6s} if $u_{bal,p}^* < 0$. In case $u_{bal,p}^* > 0$, the pulses s_1^2 , s_3^2 , s_4^2 , and s_5^2 are modified during the interval Δt_{3s} . For operation as rectifier and during sextant I, if $i_{p,1} < I_{dc}/2$ ($i_{T,p} < 0$, $\epsilon_{bal,p} > 0$), the balance control should increase the rate of change of $i_{p,1}$. This will increase the average value of u_{pp} and make $u_{bal,p}^* > 0$. As presented in Fig. 6(c), s_1^2 , s_3^2 , s_4^2 , and s_5^2 are modified during the interval Δt_3 ($s_1^1 = 1$, $s_2^1 = 0$, $s_3^1 = 0$, $s_4^1 = 1$, $s_5^1 = 0$, $s_6^1 = 0$, $s_1^2 = 1$, $s_2^2 = 0$, $s_3^2 = 1$, $s_4^2 = 0$, $s_5^2 = 0$, $s_6^2 = 0$). By applying the additional state $u_{pp} = u_{ac}$ during Δt_{3s} , the mean value of the voltage across the transformer within a switching period T_{sw} is calculated as

$$\langle u_{pp} \rangle_{T_{sw}} = \frac{1}{T_{sw}} \int_{t-T_{sw}}^t u_{pp}(\tau) d\tau = \frac{u_{ac} \Delta t_3 s}{T_{sw}} > 0. \quad (15)$$

Supposing $i_{p,1} > I_{dc}/2$, the control should decrease the rate of change of $i_{p,1}$ by decreasing the mean value u_{pp} and making $u_{bal,p}^* < 0$. The additional active state $u_{pp} = u_{ca}$ is applied during Δt_{6s} . The average value of the voltage across the transformer within a switching period T_{sw} is accordingly computed with

$$\langle u_{pp} \rangle_{T_{sw}} = \frac{1}{T_{sw}} \int_{t-T_{sw}}^t u_{pp}(\tau) d\tau = \frac{u_{ca} \Delta t_6 s}{T_{sw}} < 0. \quad (16)$$

The major drawback of this technique is that the balancing control of one IPT is performed every 60° of the network phase, since it is only possible to act on one control action ($u_{bal,p}^*$ or $u_{bal,n}^*$) at a time depending on the sextant. In addition, the balancing actions are coupled, i.e., every time the corresponding state Δt_{3s} or Δt_{6s} is added, the original state Δt_3 or Δt_6 has its total period reduced, modifying the average value of the IPT in which the control is not directly acting. To overcome this obstacle, a second balancing technique is proposed in Section V.

A. Current Balance Control Loop Model

The objective of this section is to find a dynamic model that relates the duty ratio values of the additional state δ_{bal} with the transverse current values $i_{T,p}$ and $i_{T,n}$ that are the measurement variables for the balancing control loop according to Fig. 2. A relation of the transverse current values as a function of the voltage applied in the IPT is given in (13).

In order to calculate the global mean value of the voltage applied in the IPT, the angular interval $2\pi/3$ is considered. An integration is applied for the calculation of the local average value within a switching period T_{sw} and then a second integration for the calculation of the global average value, within the period $T_g/3$. The calculation of the global mean value is done within an angular range of 0 to $2\pi/3$ rad. Table II is used as a reference for the calculation. The modulation index $M = 1$

TABLE II
VOLTAGE ON THE IPTs AND TRANSFORMER CURRENTS CHANGE RATE FOR EACH SWITCHING INTERVAL WITHIN A PERIOD T_{sw} FOR PATTERNS 1–3

	Time	\vec{I}_v	Pattern 1						Pattern 2						Pattern 3					
			u_{pp}	u_{nn}	$\Delta i_{p,1}$	$\Delta i_{n,2}$	$u_{bal,p}^*$	$u_{bal,n}^*$	u_{pp}	u_{nn}	$\Delta i_{p,1}$	$\Delta i_{n,2}$	$u_{bal,p}^*$	$u_{bal,n}^*$	u_{pp}	u_{nn}	$\Delta i_{p,1}$	$\Delta i_{n,2}$	$u_{bal,p}^*$	$u_{bal,n}^*$
Sextant I and Region 2	Δt_1	\vec{I}_8	0	u_{bc}	0	↑	x	x	0	u_{bc}	0	↑	x	x	0	u_{bc}	0	↑	x	x
	Δt_2	\vec{I}_9	0	0	0	0	x	x	0	0	0	0	x	x	0	0	0	0	x	x
	Δt_3	\vec{I}_2	u_{ac}	0	↑	0	x	x	u_{ab}	u_{cb}	↑	↓	x	x	0	u_{ca}	0	↓	x	x
	Δt_4	\vec{I}_8	0	u_{cb}	0	↓	x	x	0	u_{cb}	0	↓	x	x	0	u_{cb}	0	↓	x	x
	Δt_5	\vec{I}_9	0	0	0	0	x	x	0	0	0	0	x	x	0	0	0	0	x	x
	Δt_6	\vec{I}_2	u_{ca}	0	↓	0	x	x	u_{ba}	u_{bc}	↓	↑	x	x	0	u_{ac}	0	↑	x	x
	Meth. AS 1	Δt_{3s}	\vec{I}_2	0	u_{ca}	0	↓	x	< 0	0	u_{ca}	0	↓	x	< 0	u_{ac}	0	↑	0	> 0
1 AS 2	Δt_{6s}	\vec{I}_2	0	u_{ac}	0	↑	x	> 0	0	u_{ac}	0	↑	x	> 0	u_{ca}	0	↓	0	< 0	x
Meth. Opt. 1	$\delta_{1,1}=\delta_1-\delta_{bal,j}$	\vec{I}_2	u_{ca}	0	↓	0	< 0	x	u_{ba}	u_{bc}	↓	↑	< 0	> 0	0	u_{ac}	0	↑	x	> 0
2 Opt. 2	$\delta_{1,2}=\delta_1-\delta_{bal,j}$	\vec{I}_2	u_{ac}	0	↑	0	> 0	x	u_{ab}	u_{cb}	↑	↓	> 0	< 0	0	u_{ca}	0	↓	x	< 0
Sextant II and Region 1	Δt_1	\vec{I}_9	0	0	0	0	x	x	0	0	0	0	x	x	0	0	0	0	x	x
	Δt_2	\vec{I}_{10}	u_{ab}	0	↑	0	x	x	u_{ab}	0	↑	0	x	x	u_{ab}	0	↑	0	x	x
	Δt_3	\vec{I}_2	u_{ab}	u_{cb}	↑	↓	x	x	0	u_{ca}	0	↓	x	x	u_{ac}	0	↑	0	x	x
	Δt_4	\vec{I}_9	0	0	0	0	x	x	0	0	0	0	x	x	0	0	0	0	x	x
	Δt_5	\vec{I}_{10}	u_{ba}	0	↓	0	x	x	u_{ba}	0	↓	0	x	x	u_{ba}	0	↓	0	x	x
	Δt_6	\vec{I}_2	u_{ba}	u_{bc}	↓	↑	x	x	0	u_{ac}	0	↑	x	x	u_{ca}	0	↓	0	x	x
	Meth. AS 1	Δt_{3s}	\vec{I}_2	u_{ac}	0	↑	0	> 0	x	u_{ac}	x	↑	0	> 0	x	0	u_{ca}	0	↓	x
1 AS 2	Δt_{6s}	\vec{I}_2	u_{ca}	0	↓	0	< 0	x	u_{ca}	x	↓	0	< 0	x	0	u_{ac}	0	↑	x	> 0
Meth. Opt. 1	$\delta_{1,1}=\delta_1-\delta_{bal,j}$	\vec{I}_2	0	u_{bc}	0	↑	x	> 0	u_{ab}	u_{ac}	↑	↑	> 0	> 0	u_{ca}	0	↓	0	< 0	x
2 Opt. 2	$\delta_{1,2}=\delta_1-\delta_{bal,j}$	\vec{I}_2	0	u_{cb}	0	↓	x	< 0	u_{ba}	u_{ca}	↓	↓	< 0	< 0	u_{ac}	0	↑	0	> 0	x
Sextant II and Region 2	Δt_1	\vec{I}_{10}	u_{ab}	0	↓	0	x	x	u_{ab}	0	↓	0	x	x	u_{ab}	0	↓	0	x	x
	Δt_2	\vec{I}_{11}	0	0	0	0	x	x	0	0	0	0	x	x	0	0	0	0	x	x
	Δt_3	\vec{I}_3	0	u_{cb}	0	↓	x	x	u_{ba}	u_{ca}	↑	↓	x	x	u_{bc}	0	↑	0	x	x
	Δt_4	\vec{I}_{10}	u_{ba}	0	↑	0	x	x	u_{ba}	0	↑	0	x	x	u_{ba}	0	↑	0	x	x
	Δt_5	\vec{I}_{11}	0	0	0	0	x	x	0	0	0	0	x	x	0	0	0	0	x	x
	Δt_6	\vec{I}_3	0	u_{bc}	0	↑	x	x	u_{ab}	u_{ac}	↓	↑	x	x	u_{cb}	0	↓	0	x	x
	Meth. AS 1	Δt_{3s}	\vec{I}_3	u_{bc}	0	↑	0	> 0	x	u_{bc}	0	↑	0	> 0	x	0	u_{cb}	0	↓	x
1 AS 2	Δt_{6s}	\vec{I}_3	u_{cb}	0	↓	0	< 0	x	u_{cb}	0	↓	0	< 0	x	0	u_{bc}	0	↑	x	> 0
Meth. Opt. 1	$\delta_{1,1}=\delta_1-\delta_{bal,j}$	\vec{I}_3	0	u_{bc}	0	↑	x	> 0	u_{ab}	u_{ac}	↓	↑	< 0	> 0	u_{cb}	0	↓	0	< 0	x
2 Opt. 2	$\delta_{1,2}=\delta_1-\delta_{bal,j}$	\vec{I}_3	0	u_{cb}	0	↓	x	< 0	u_{ba}	u_{ca}	↑	↓	> 0	< 0	u_{bc}	0	↑	0	> 0	x
Sextant III and Region 1	Δt_1	\vec{I}_{11}	0	0	0	0	x	x	0	0	0	0	x	x	0	0	0	0	x	x
	Δt_2	\vec{I}_{12}	0	u_{ca}	0	↓	x	x	0	u_{ca}	0	↓	x	x	0	u_{ca}	0	↓	x	x
	Δt_3	\vec{I}_3	u_{ba}	u_{ca}	↑	↓	x	x	u_{bc}	0	↑	0	x	x	0	u_{cb}	0	↓	x	x
	Δt_4	\vec{I}_{11}	0	0	0	0	x	x	0	0	0	0	x	x	0	0	0	0	x	x
	Δt_5	\vec{I}_{12}	0	u_{ac}	0	↑	x	x	0	u_{ac}	0	↑	x	x	0	u_{ac}	0	↑	x	x
	Δt_6	\vec{I}_3	u_{ab}	u_{ac}	↓	↑	x	x	u_{cb}	0	↓	0	x	x	0	u_{bc}	0	↑	x	x
	Meth. AS 1	Δt_{3s}	\vec{I}_3	0	u_{cb}	0	↓	x	< 0	0	u_{cb}	0	↓	x	< 0	u_{bc}	0	↑	0	> 0
1 AS 2	Δt_{6s}	\vec{I}_3	0	u_{bc}	0	↑	x	> 0	0	u_{bc}	0	↑	x	> 0	u_{cb}	0	↓	0	< 0	x
Meth. Opt. 1	$\delta_{1,1}=\delta_1-\delta_{bal,j}$	\vec{I}_3	u_{ab}	0	↓	0	< 0	x	u_{cb}	u_{ca}	↓	↑	< 0	> 0	0	u_{bc}	0	↑	x	> 0
2 Opt. 2	$\delta_{1,2}=\delta_1-\delta_{bal,j}$	\vec{I}_3	u_{ba}	0	↑	0	> 0	x	u_{bc}	u_{ac}	↑	↓	> 0	< 0	0	u_{cb}	0	↓	x	< 0

is exemplarily considered and, thus, only regions 1 and 2 are used. The mean is calculated for the voltage u_{pp} , following the relation $u_{bal,p}^* > 0$, for pattern 3.

For the angular interval 0 to $\pi/6$ rad, the reference current vector is located in sextant I (R2). The local mean value is computed with (17) by adding the active state in Δt_{3s} . Thus

$$\langle u_{pp} \rangle_{T_{sw}}^{SIR2} = \frac{u_{ac} \Delta t_{3s}}{T_{sw}} = u_{ac} \delta_{bal,p}. \quad (17)$$

For the angular interval $\pi/6$ to $\pi/2$ rad, the current vector is located in sextant II (R1 and R2). No additional active states are applied to the transformer IPT_p in sextant II. Thus, the voltage level $u_{pp} = 0$ is applied and the local mean is null

$$\langle u_{pp} \rangle_{T_{sw}}^{SIIR1} = \langle u_{pp} \rangle_{T_{sw}}^{SIIR2} = 0. \quad (18)$$

For the angular interval $\pi/2$ to $2\pi/3$ rad, the vector is located in sextant III (R1). In this sextant, the active state is added during Δt_{3s} . The resulting local mean is

$$\langle u_{pp} \rangle_{T_{sw}}^{SIII1} = \frac{u_{bc} \Delta t_{3s}}{T_{sw}} = u_{bc} \delta_{bal,p}. \quad (19)$$

The listed local mean expressions are used to calculate the global mean within an angular interval of $2\pi/3$

$$\begin{aligned} \frac{\langle u_{pp} \rangle_{\frac{2\pi}{3}}}{\langle \delta_{bal} \rangle_{\frac{2\pi}{3}}} &= \frac{3}{2\pi} \left(\int_0^{\frac{\pi}{6}} u_{ac}(\theta_n) d\theta_n + \int_{\frac{\pi}{2}}^{\frac{2\pi}{3}} u_{bc}(\theta_n) d\theta_n \right) \\ &= + \frac{3\sqrt{3}\hat{U}_g}{2\pi} = +V_{\delta_{bal}}. \end{aligned} \quad (20)$$

Similarly, following the relation $u_{bal,p}^* < 0$, for the sextant I, region 2, for the sextant II, regions 1 and 2, and for the sextant III, region 1, the active state is activated in Δt_{6s}

$$\begin{aligned} \frac{\langle u_{pp} \rangle_{\frac{2\pi}{3}}}{\langle \delta_{bal} \rangle_{\frac{2\pi}{3}}} &= \frac{3}{2\pi} \left(\int_0^{\frac{\pi}{6}} u_{ca}(\theta_n) d\theta_n + \int_{\frac{\pi}{2}}^{\frac{2\pi}{3}} u_{cb}(\theta_n) d\theta_n \right) \\ &= - \frac{3\sqrt{3}\hat{U}_g}{2\pi} = -V_{\delta_{bal}}. \end{aligned} \quad (21)$$

The transfer function that relates the duty ratio of the additional active state to the mean voltage applied in the IPT $T_{i,1}$ is found from (20) and (21) and is expressed by

$$\frac{\tilde{u}_{pp}}{\tilde{\delta}_{bal,p}} = |V_{\delta_{bal}}| \quad (22)$$

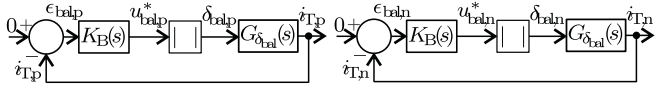


Fig. 7. Representation of the control loop of the voltage average values in the IPTs.

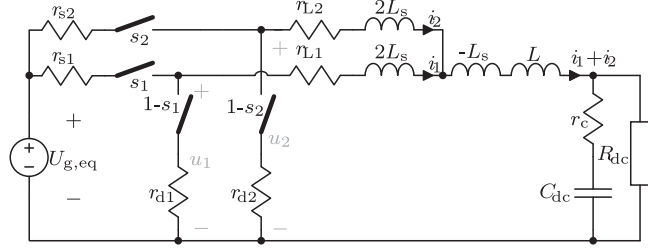


Fig. 8. Equivalent single-phase circuit for current balancing analysis.

where the module represents the variation of the average voltage, which can be negative or positive depending on the control action. The same procedure is applied to the interphase transformer IPT_n for the voltage u_{nn}

$$\frac{\tilde{u}_{nn}}{\tilde{\delta}_{bal,n}} = |V_{\delta_{bal}}|. \quad (23)$$

The balance plant transfer function that will be used to balance the currents in IPTs is obtained from (13), (22), and (23). It is given by

$$\begin{aligned} G_{\delta_{bal}}(s) &= \frac{\tilde{u}_{pp}}{\tilde{\delta}_{bal,p}} \frac{\tilde{i}_{T,p}}{\tilde{u}_{pp}} = \frac{\tilde{u}_{nn}}{\tilde{\delta}_{bal,n}} \frac{\tilde{i}_{T,n}}{\tilde{u}_{nn}} \\ &= \frac{\tilde{i}_{T,p}}{\tilde{\delta}_{bal,p}} = \frac{\tilde{i}_{T,n}}{\tilde{\delta}_{bal,n}} = \frac{|V_{\delta_{bal}}|}{4L_s s}. \end{aligned} \quad (24)$$

The currents balancing control loops are presented in Fig. 7.

V. METHOD 2: DIFFERENT MODULATION SIGNALS TO CHANGE THE MEAN VOLTAGE VALUE

A second current balancing method is proposed in this section. This method allows the current balance control for each IPT to be decoupled without increasing the switching losses of the semiconductors. A minor drawback of this technique is that the balancing control of each IPT can only be performed at every 60° of the mains cycle, but it is the same conditions for method 1.

A. Balancing for a Single-Phase Circuit

The unbalance caused in the equivalent single-phase circuit with the IPT and resistors in the switches, diodes, and windings is studied in this section. Two interleaving switches and diodes are used to simulate a simplified circuit instead of the three-phase circuit and to show the effects of current balancing.

The circuit under analysis is shown in Fig. 8, where the resistances r_{d1} , r_{s1} , r_{d2} , r_{s2} , r_{L1} , and r_{L2} represent the losses expected in the circuit components.

The simplified circuit of Fig. 9 is used here to analyze the steady-state behavior, where the average values of voltages u_1

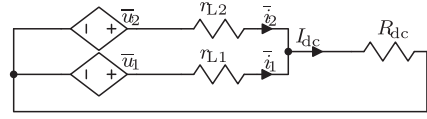


Fig. 9. Single-phase equivalent simplified circuit for analyzing the average value of currents I_1 and I_2 in steady state.

and u_2 are given by

$$\begin{aligned} \bar{u}_1 &= U_{g,eq} \bar{\delta}_1 - r_{s1} \bar{\delta}_1 \bar{i}_1 - r_{d1} (1 - \bar{\delta}_1) \bar{i}_1 \\ &= r_{L1} \bar{i}_1 + R_{dc} (\bar{i}_1 + \bar{i}_2) \\ \bar{u}_2 &= U_{g,eq} \bar{\delta}_2 - r_{s2} \bar{\delta}_2 \bar{i}_2 - r_{d2} (1 - \bar{\delta}_2) \bar{i}_2 \\ &= r_{L2} \bar{i}_2 + R_{dc} (\bar{i}_1 + \bar{i}_2). \end{aligned} \quad (25)$$

The asymmetries in the converter that cause an imbalance in the average value of the currents are given by the differences between the resistors r_{d1} , r_{d2} , r_{s1} , r_{s2} , r_{L1} , and r_{L2} .

Without balance control, it is possible to compute the average value of current i_T during steady-state considering that $\bar{\delta} = \bar{\delta}_1 = \bar{\delta}_2$ and $\bar{\delta}_{bal} = 0$, as in (26), shown at the bottom of the next page.

For a given value of duty ratio, it can be verified that when the converter presents asymmetries in relation to the constructive characteristics, in other words, differences between the resistance values, the average value of the current i_T will be different from zero. Fig. 10 illustrates two different cases when $\bar{\delta}_{bal} = 0$. In the first case, the asymmetry tends to rise the average value of the current i_1 in relation to i_2 , whereas the second case has the opposite effect.

To correct this imbalance, it is proposed to modify the modulation signal δ through the addition and subtraction of the control variable δ_{bal} . Thus, two different modulation signals are created to control each converter in parallel: $\delta_1 = \delta + \delta_{bal}$ and $\delta_2 = \delta - \delta_{bal}$. This change in the modulation signals can be seen in Fig. 11.

The average value of the control variable δ_{bal} needed to perform the balancing can be accordingly calculated. Considering that $\bar{i}_1 = \bar{i}_2 = I_{dc}/2$, it follows that

$$\begin{aligned} \bar{\delta}_{bal} &= \frac{\frac{I_{dc}}{2} (r_{d1} + r_{L1}) + R_{dc} I_{dc}}{2 \left[U_{g,eq} + (r_{d1} - r_{s1}) \frac{I_{dc}}{2} \right]} \\ &\quad - \frac{\frac{I_{dc}}{2} (r_{d2} + r_{L2}) + R_{dc} I_{dc}}{2 \left[U_{g,eq} + (r_{d2} - r_{s2}) \frac{I_{dc}}{2} \right]}. \end{aligned} \quad (27)$$

Fig. 10 shows that to balance the currents for case 1, a negative δ_{bal} must be added, in such a way reducing the average value of the current i_1 and increasing the value average of the current i_2 . For case 2, the addition of a positive δ_{bal} is made achieving the opposite effect.

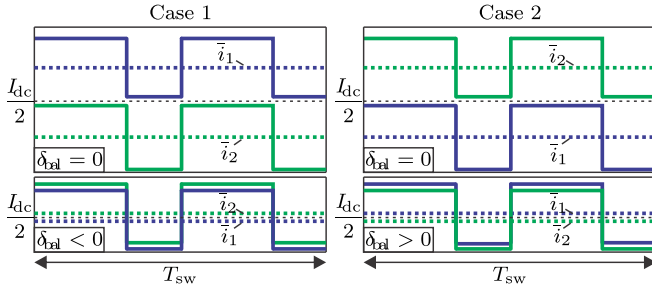


Fig. 10. Behavior of the currents i_1 and i_2 for two cases of converter asymmetry, without and with balancing control.

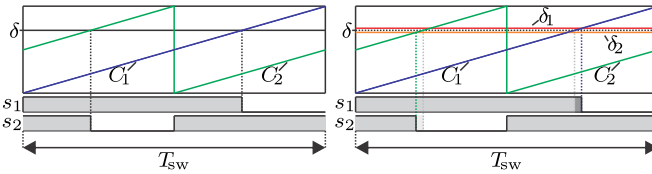


Fig. 11. Switches signals modified with the addition of the balance control variable δ_{bal} .

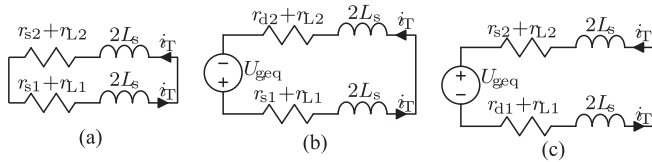


Fig. 12. Equivalent circuits for analysis of the balancing loop and respective average intervals during a switching period. (a) $(2\delta - 1)T_{sw}$. (b) $(1 - \delta + \delta_{bal})T_{sw}$. (c) $(1 - \delta - \delta_{bal})T_{sw}$.

The transfer function of the balancing loop considering the resistances is found by analyzing the circuits shown in Fig. 12 considering the switching signals shown in Fig. 11.

The following transfer function is found after averaging over the switching interval and linearizing (28), shown at the bottom of this page, where I_T is a function of Δ_{bal} and is given by (29) shown at the bottom of the next page. Considering that the circuit is not balanced, the average value in steady state of current i_T is known with (26) and the average value of the control variable δ_{bal} necessary to correct this unbalanced value from (27). When the operation point is $\Delta_{bal} = \bar{\delta}_{bal}$, the value of (29) has the opposite sign of (26).

Fig. 13 shows the Bode diagram of the balancing transfer function for the single-phase circuit. If the resistances are

disregarded, the loop dynamics is given by the value of the self-inductance $4L_s$. Using the Bode diagram, we may conclude that the unbalances have little influence on the dynamics of the loop. The behavior of the current balance model is that of a PT1 system with a very low corner frequency. The digital and switching delays are not considered in the current balancing loop since this loop is much slower than the output current control loop transverse mode current and the switching frequency is high. The unbalances caused by the differences between the resistances of the circuit have a greater influence on the steady-state value of the transverse mode current.

This method of addition and subtraction of the original modulation signals, using a balancing duty ratio δ_{bal} , can be applied to the 5L-CSR converter with carrier-based modulation. In this case, the effect of this addition and subtraction is analyzed in the following for all the sextants.

B. Balancing for 5L-CSR

The currents that must be balanced are: $i_{p,1}$, $i_{p,2}$, $i_{n,1}$, and $i_{n,2}$. The purpose of this control is to cancel the transverse mode currents $i_{T,p}$ and $i_{T,n}$ changing the modulation signal δ_1 , when adding or subtracting the control variables $\delta_{bal,p}$ and $\delta_{bal,n}$. In this way, the switching intervals are modified through the current balancing. Carriers are two sawtooth signals with 180° phase shift (C1 and C2). The modulation signal δ_1 is modified for comparison with these carriers. After this modification, this modulation signal can be renamed as $\delta_{1,1}$ when used for comparison with carrier C1. When compared with carrier C2, it can be renamed as $\delta_{1,2}$.

In the case where $i_{p,1}$ is greater than $i_{p,2}$, to cancel transverse mode current $i_{T,p}$, the current $i_{p,1}$ must decrease and $i_{p,2}$ must increase. This will be done when the control signal $u_{bal,p}$ is negative. When the control signal $u_{bal,p}$ is positive, the reciprocal case occurs. For the currents $i_{n,1}$ and $i_{n,2}$, the purpose is to cancel the transverse mode current $i_{T,n}$. The same logic modification of the modulation signals δ_1 and δ_2 is applied, but the used control signal is $u_{bal,n}$. The control variables $\delta_{bal,p}$ and $\delta_{bal,n}$ are obtained applying (2).

Fig. 14 presents the modification of the modulation signal δ_1 for all modulation patterns. When compared with carrier C1, the modified modulation signal δ_1 is renamed to $\delta_{1,1}$. It is verified that this modification increases the interval Δt_6 and reduces the interval Δt_5 . The voltage average value of the IPT is changed. The carrier C2 is compared with $\delta_{1,2}$, in this case, the intervals Δt_3 and Δt_2 are modified.

Table II presents the applied voltage of the IPT u_{pp} and u_{nn} and the direction of the variation of the currents $\Delta i_{p,1}$, $\Delta i_{p,2}$,

$$\bar{i}_T = \frac{U_{g,eq} \bar{\delta} [\bar{\delta} (r_{s2} - r_{s1} + r_{d1} - r_{d2}) + r_{L2} - r_{L1} + r_{d2} - r_{d1}]}{2[(R_{dc} + r_{L1} + r_{d1} + \bar{\delta} (r_{s1} - r_{d1})) (R_{dc} + r_{L2} + r_{d2} + \bar{\delta} (r_{s2} - r_{d2})) - R_{dc}^2]} \quad (26)$$

$$\frac{\tilde{i}_T}{\tilde{\delta}_{bal}} = \frac{2U_{g,eq} + I_T (r_{s2} - r_{s1} + r_{d1} - r_{d2})}{4L_s s + r_{L1} + r_{L2} + r_{d1} + r_{d2} + (r_{s1} - r_{d1})(\Delta + \Delta_{bal}) + (r_{s2} - r_{d2})(\Delta - \Delta_{bal})} \quad (28)$$

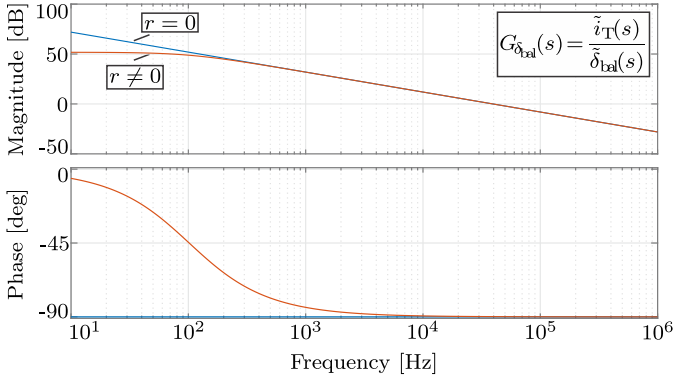


Fig. 13. Bode diagram for balancing current transfer function.

TABLE III
SUMMARY OF THE BALANCING CONTROL VARIABLES BEHAVIOR DEPENDING OF THE SEXTANT, METHOD, AND PATTERN

		Sextants I, III, V					
		Pattern 1		Pattern 2		Pattern 3	
Method	Modification	$u_{bal,p}^*$	$u_{bal,n}^*$	$u_{bal,p}^*$	$u_{bal,n}^*$	$u_{bal,p}^*$	$u_{bal,n}^*$
1	Δt_{3s}	x	< 0	x	< 0	> 0	x
	Δt_{6s}	x	> 0	x	> 0	< 0	x
2	$\delta_{1,1}=\delta_1-\delta_{bal,j}$	< 0	x	< 0	> 0	x	> 0
	$\delta_{1,2}=\delta_1-\delta_{bal,j}$	> 0	x	> 0	< 0	x	< 0
		Sextants II, IV, VI					
		Pattern 1		Pattern 2		Pattern 3	
Method	Modification	$u_{bal,p}^*$	$u_{bal,n}^*$	$u_{bal,p}^*$	$u_{bal,n}^*$	$u_{bal,p}^*$	$u_{bal,n}^*$
1	Δt_{3s}	> 0	x	> 0	x	x	< 0
	Δt_{6s}	< 0	x	< 0	x	x	> 0
2	$\delta_{1,1}=\delta_1-\delta_{bal,j}$	x	> 0	> 0	> 0	< 0	x
	$\delta_{1,2}=\delta_1-\delta_{bal,j}$	x	< 0	< 0	< 0	> 0	x

$\Delta i_{n,1}$, and $\Delta i_{n,2}$ for the conduction states of the intervals Δt_{1-6} for the region 2 of sextant I and region 1 of sextant II referring to the pattern 1. The table also shows the result of the control action $u_{bal,p}^*$ and $u_{bal,n}^*$.

The behavior of the balancing control variables is repetitive and depends on the operating sextant. For sextants I, III, and V, the control variables behave the same for sextant I. For sextants II, IV, and VI, the control variables behave as during sextant II. A summary of the applications of the $u_{bal,p}^*$ and $u_{bal,n}^*$ variables is given in Table III.

VI. SIMULATION RESULTS

The two balancing methods are tested by applying a fixed value of $u_{bal,p} > 0$. A positive value is applied to force the current $i_{p,1}$ to values larger than $I_{dc}/2$ and $i_{p,2}$ for values under $I_{dc}/2$. Results from method 1 are presented in Fig. 15. The modification of the voltage values u_{pp} for the three patterns is visible. The action of the control variable $u_{bal,p}$ is realized during sextants II, IV, and VI for patterns 1 and 2 and sextants I, III, and V for pattern 3, according to Table III for method 1. The balance with method 1 is coupled, as it simultaneously modifies

TABLE IV
5L-CSR MAIN SPECIFICATIONS

Phase voltage (rms) U_g^{rms}	220 V
Dc output voltage U_{dc}	380 V
Grid frequency f_g	60 Hz
Switching frequency f_{sw}	150 kHz
Rated power P_{out}	6 kW
Dc capacitor C_{dc}	50 μ F
Filter capacitor C_F	4.7 μ F
Filter inductor L_F	287 μ H
Dc inductor L_{dc}	70 μ H
IPT magnetizing inductance L_{mag}	470 μ H

currents $i_{n,1}$ and $i_{n,2}$. The currents $i_{T,p}$ and $i_{T,n}$ converge to a value other than zero because they are coupled.

Results from the second balancing method are presented in Fig. 16. According to the patterns given in Table III, the actuation of the control variable $u_{bal,p}$ is active during sextants I, III, and V for patterns 1 and 2 and during sextants II, IV, and VI for pattern 3. This method is decoupled since only current $i_{T,p}$ can be forced to a positive value other than zero for the three patterns.

The closed-loop performance is shown in Figs. 17 and 18 for both balancing methods. The balancing loop is activated at time t_b , showing that both methods are able to correct the average value of the transverse current to zero.

VII. EXPERIMENTAL RESULTS

The discussed current balancing techniques were tested in a 6-kW 5L-CSR prototype for all the proposed patterns with the output voltage control u_{dc} and current control i_{dc} loops enabled. The aim is to show that the average value of the current of the IPTs can be modified when the techniques are implemented. The prototype was constructed, as shown in Fig. 19, according to the specifications given in Table IV.

This system uses 1200-V SiC MOSFETs (*Cree* C3M0075-120 K) and 1200-V SiC diodes (*Rohm* SCS210KE2HR) as power switching devices. The directly coupled dc inductors and input filter inductors use iron powder toroidal cores (*Magnetics* XF60 0078439A7), whereas the IPTs $T_{i,1}$ and $T_{i,2}$ employ ferrite cores (*Epcos* N87 E55/28/25).

The interleaving modulation technique and the control scheme are implemented in a central control board, based on a floating-point digital signal controller (DSC) (Texas Instruments TMS320F28335) and an field programmable gate array (FPGA) (Intel Cyclone IV EP4CE22). The DSC receives the measured analog signals and is responsible for the control, protection, and supervision routines. The FPGA receives the DSC actuation variables via serial peripheral interface (SPI) communication and performs the modulation. The control signals of the 12 switches are synthesized by the FPGA.

The time behavior of the output voltage u_{dc} , input voltage u_a , and currents $i_{p,1}$ and $i_{p,2}$ are observed in Fig. 20 before and after the current balancing loop is activated at time t_b . The

$$I_T = \frac{2U_{g,eq}\Delta_{bal}}{r_{L1} + r_{L2} + r_{d1} + r_{d2} + (r_{s1} - r_{d1})(\Delta + \Delta_{bal}) + (r_{s2} - r_{d2})(\Delta - \Delta_{bal})} \quad (29)$$

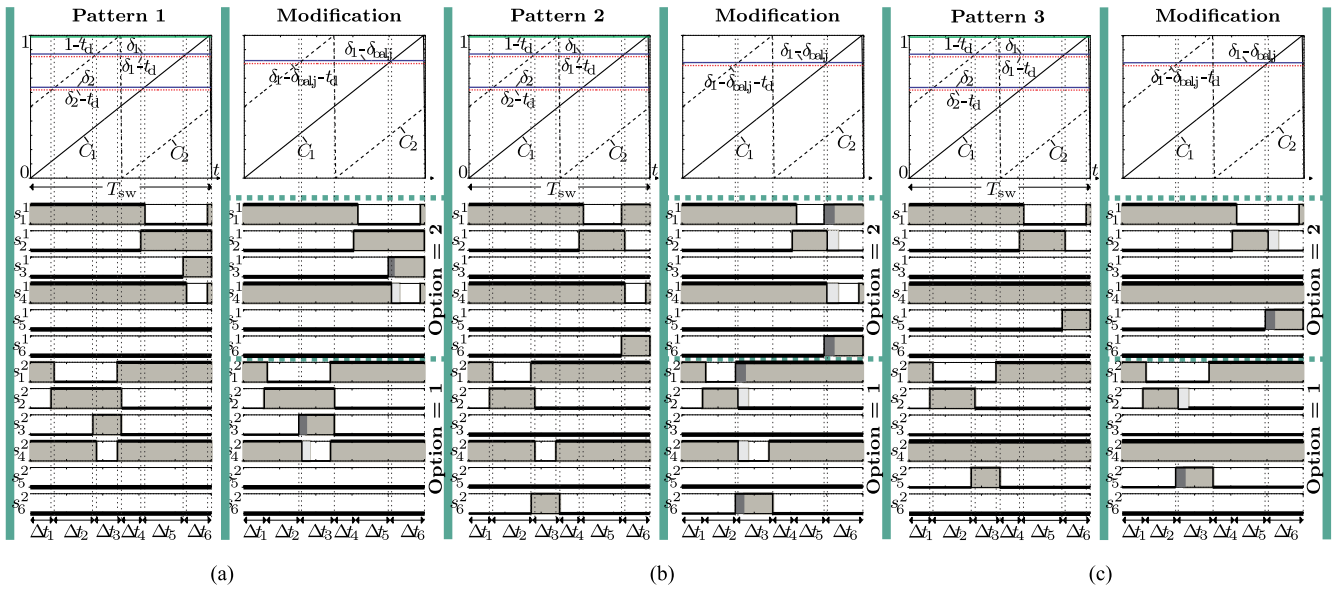


Fig. 14. Modulation signal modification δ_1 for patterns 1–3, changing the voltage average value of the IPTs. Dark gray areas are added active intervals and light gray areas are subtracted intervals for the given signal. (a) Pattern 1. (b) Pattern 2. (c) Pattern 3.

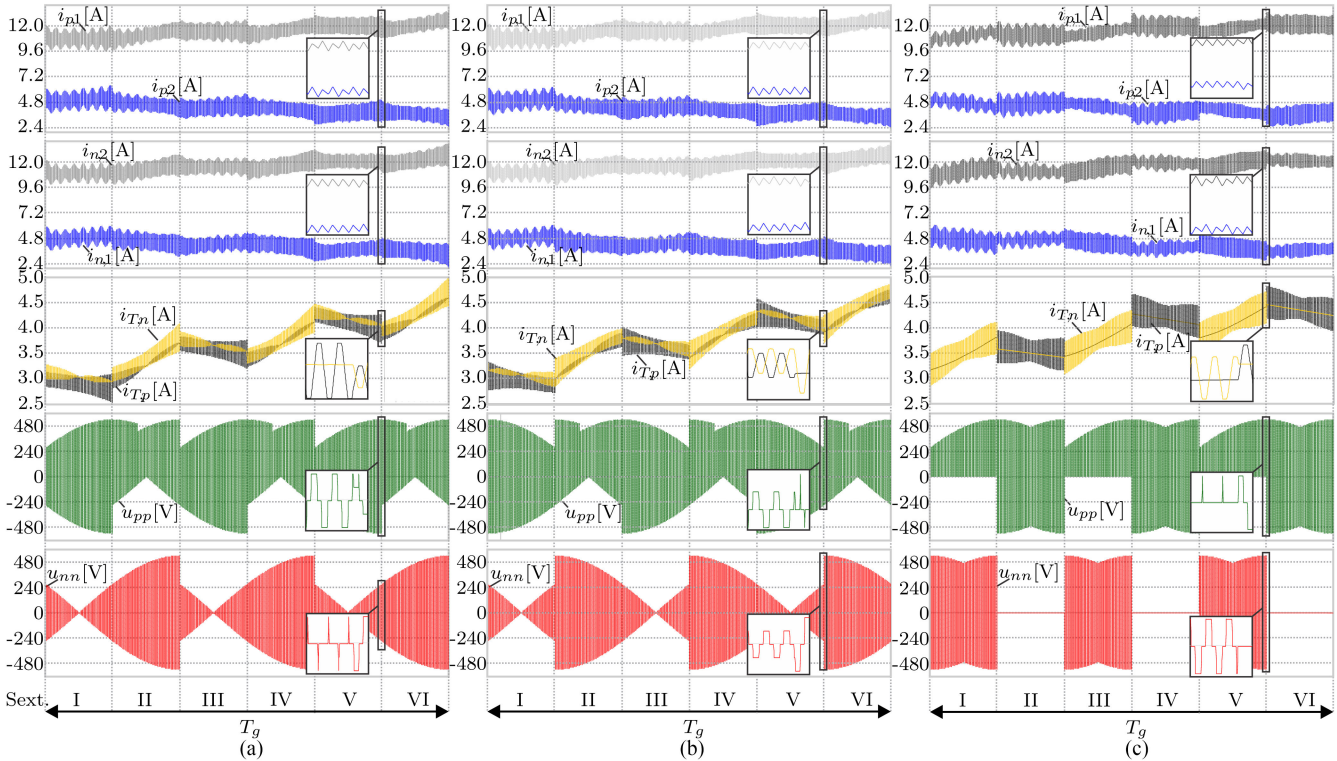


Fig. 15. Balancing control simulation results using method 1 forcing a value $u_{bal,p} > 0$ and $u_{bal,n} = 0$ for modulation patterns. (a) Pattern 1. (b) Pattern 2. (c) Pattern 3. A zoom of the simulated waveforms is performed between the transition of sextants V and VI.

two currents $i_{p,1}$ and $i_{p,2}$ are actively forced to be different by imposing a positive value of $u_{bal,p}$ before the current balancing loop is activated. After the balancing control is activated, the average value of the two currents is equalized. The operating

power during this test is the same of simulation results under the same circuit parameters, i.e., 6.0 kW. The output voltage and current remain controlled independent of the balancing control.

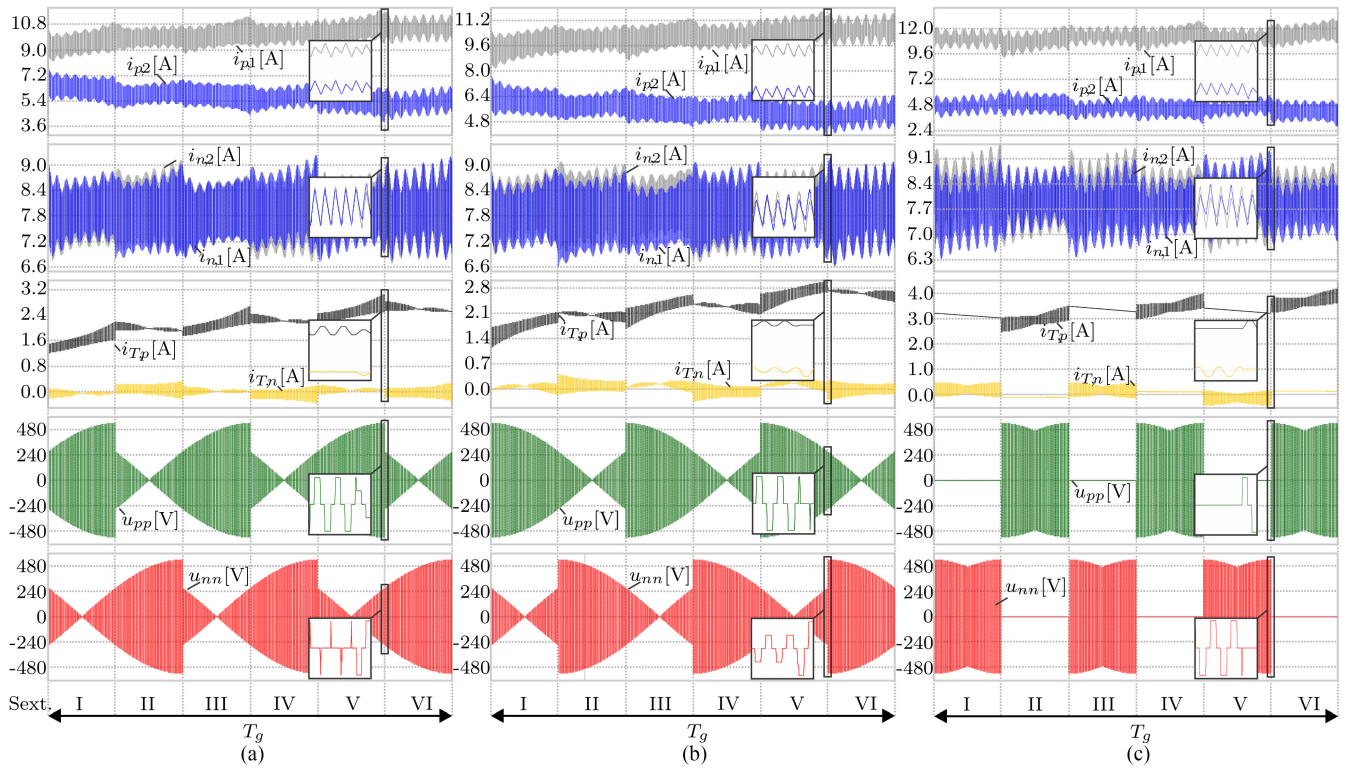


Fig. 16. Balancing control simulation using method 2 forcing a value $u_{bal,p} > 0$ and $u_{bal,n} = 0$ for modulation patterns. (a) Pattern 1. (b) Pattern 2. (c) Pattern 3. A zoom of the simulated waveforms is performed between the transition of sextants V and VI.

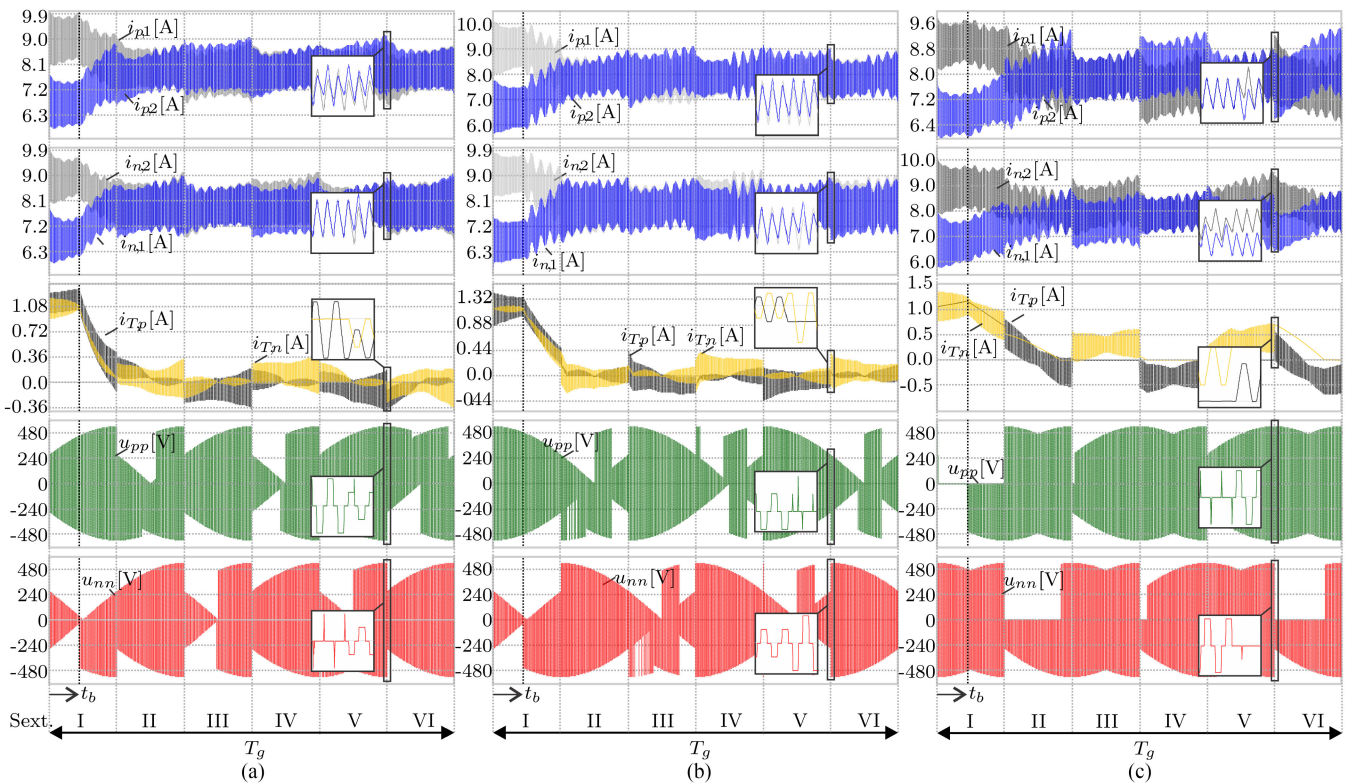


Fig. 17. Simulation results with the activation of the current balancing control in t_b using method 1. A zoom of the simulated waveforms is performed between the transition of sextants V and VI. (a) Pattern 1. (b) Pattern 2. (c) Pattern 3.

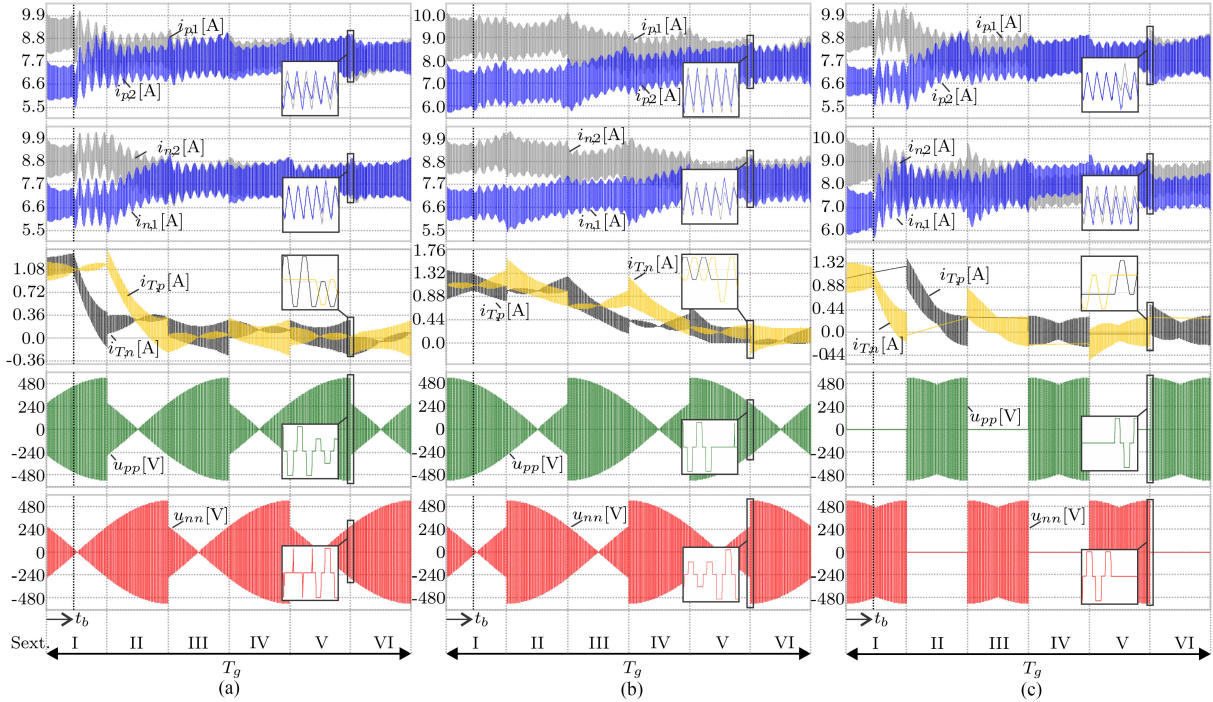


Fig. 18. Simulation results with the activation of the current balancing control in t_b using method 2. A zoom of the simulated waveforms is performed between the transition of sextants V and VI. (a) Pattern 1. (b) Pattern 2. (c) Pattern 3.

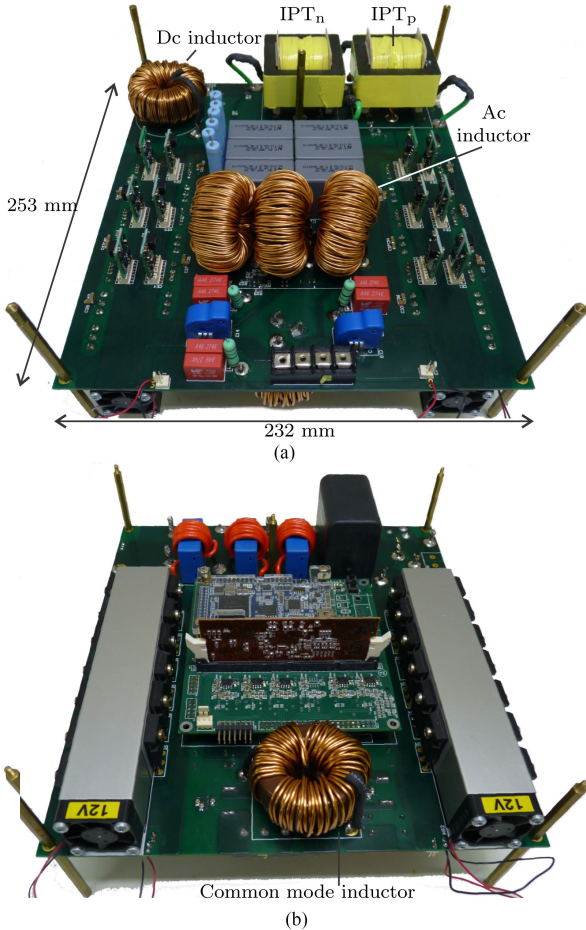


Fig. 19. 6.0-kW 5L-CSR prototype. (a) Upper view. (b) Bottom view.

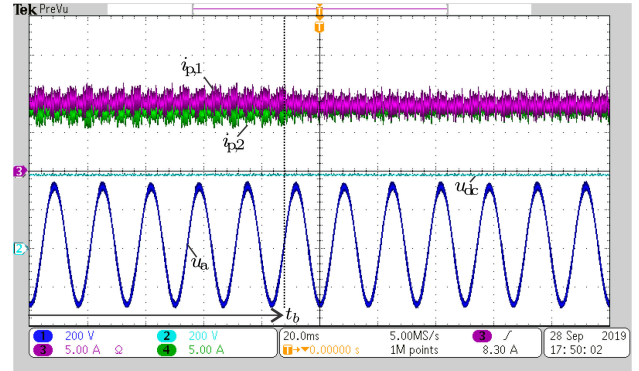


Fig. 20. Results of method 2 and pattern 3 showing that the currents $i_{p,1}$ and $i_{p,2}$ have the same average value after the balancing control is activated at t_b : u_{dc} (200.0 V/div and -400.0 V offset), u_a (200.0 V/div and -400.0 V offset), $i_{p,1}$ and $i_{p,2}$ (5.0 A/div). The time behavior of the dc-side currents is similar to all methods and patterns.

The dc offset between the measurement of currents $i_{p,1}$ and $i_{p,2}$ is presented in Table V for patterns 1–3, with and without applying methods 1 and 2, for the same operating point in Fig. 20. The difference between the currents is reduced whenever the balancing control is active. The most effective method for balancing the currents was method 2.

The balance controller was a proportional gain for all cases. Thus, a steady-state error that changes according to the operating point is seen. This error can be reduced using other controllers, but the achieved balance performance was judged sufficient and no additional dynamics were added.

Fig. 21 shows that near unity, power factor is achieved generating a sinusoidal current i_a on the input side, following the

TABLE V
MEASUREMENTS: AVERAGE VALUES OF CURRENTS $i_{p,1}$ AND $i_{p,2}$, COMPUTED LONGITUDINAL MODE $i_{L,p}$ CURRENT, TRANSVERSE MODE $i_{T,p}$ CURRENT, AND RESULTING EFFICIENCY

Pattern	Method	$i_{p,1}$ [A]	$i_{p,2}$ [A]	$i_{L,p}$ [A]	$i_{T,p}$ [mA]	η_{max}
1	Without	8.73	7.65	8.19	536.00	96.86%
	1	8.51	8.05	8.28	233.50	96.82%
	2	8.37	8.10	8.23	131.00	96.89%
2	Without	8.48	7.80	8.14	342.00	96.99%
	1	8.51	7.99	8.25	258.00	96.98%
	2	8.42	8.05	8.24	184.00	97.00%
3	Without	8.63	7.69	8.16	466.50	97.01%
	1	8.47	8.00	8.23	237.00	97.00%
	2	8.38	8.06	8.22	160.50	97.02%

Note: Methods are compared before and after their activation in a 6-kW operating point.

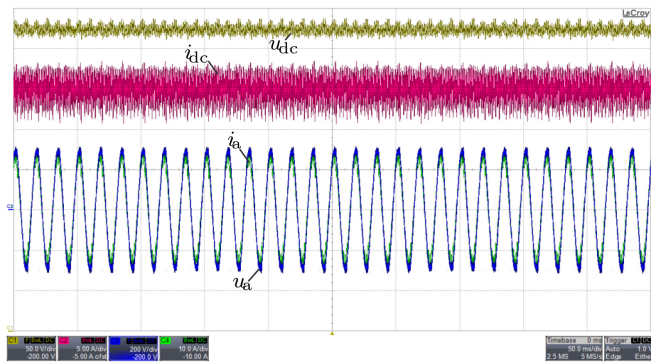


Fig. 21. Experimental results while operating with balancing method 2: u_{dc} (50.0 V/div and -200.0 V offset); i_{dc} (5.0 A/div and -5.0 A offset); u_a (200.0 V/div and -200.0 V offset); and i_a (10.0 A/div and -10.0 A offset). The 5L-CSR achieves high power factor since the current i_a follows the sinusoidal input phase voltage u_a .

sinusoidal input phase voltage u_a while maintaining the regulation of the output voltage u_{dc} and current i_{dc} . The proposed balancing techniques do not interfere in a sensible way on the input power factor.

For the converter efficiency analysis, the two balancing methods were compared with a load variation between 1.0 and 6.0 kW for patterns 1–3. The results are presented in Fig. 22. Even though the behavior of the three patterns was similar, the one that presented the highest efficiency was pattern 3, with a peak efficiency of $\eta_{max} \approx 97.0\%$. The difference from pattern 3 to patterns 1 and 2, with respect to the efficiency, is explained by the reduced number of commutations within a switching period T_{sw} . The number of commutations for a 12 switches converter driven by a sawtooth carrier is six for pattern 3 and eight for patterns 1 and 2. The higher the output power, the larger will be the difference between currents $i_{p,1}$ and $i_{p,2}$. When the balancing method 2 is activated, the difference between the two currents is reduced, making the distribution of semiconductor losses to be equalized between converters, increasing the efficiency when comparing the results without any balancing method. When the current balancing method 1 is activated, the difference between the two currents is also reduced but the switching losses are increased and reducing the overall efficiency. All the discussed balancing methods are applicable to the 5L-CSR. However, method 2 presents advantages and is generally preferable.

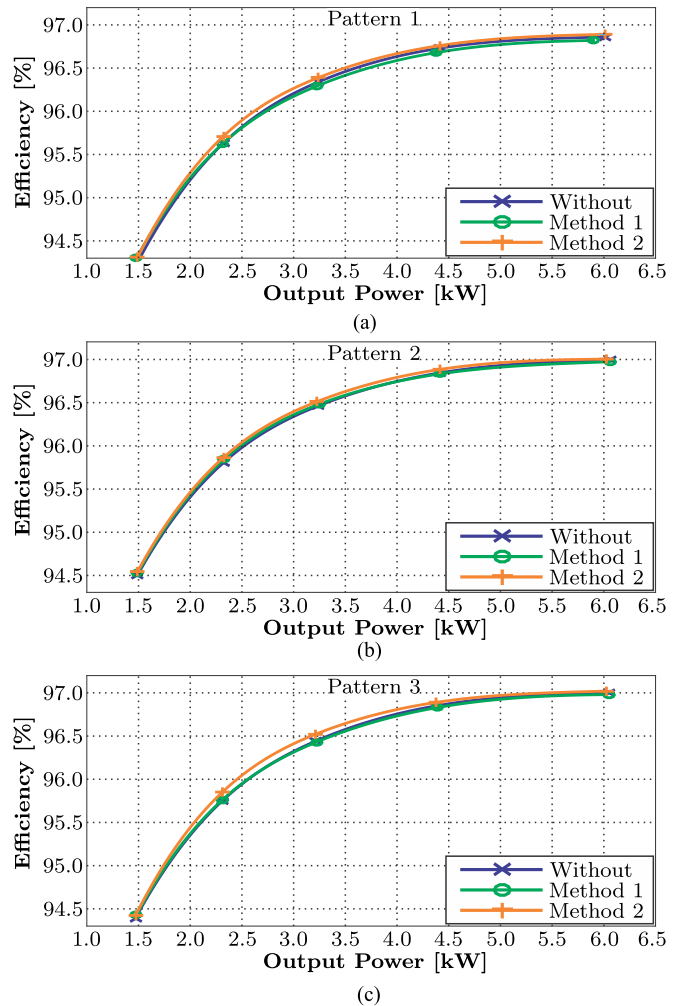


Fig. 22. Experimental efficiency curves. (a) Pattern 1. (b) Pattern 2. (c) Pattern 3. Conditions with and without balance control with methods 1 and 2 are shown.

VIII. CONCLUSION

The current balancing is an important feature for paralleled converters. Differences in currents and voltages applied to the positive and negative buses of the IPTs naturally occur due to nonideal conditions in real power converters. This can be caused by the difference in loops resistances, command signal generation, and on state voltage values of the converter diodes and semiconductors. In cases where the IPTs are realized with ferrite, the use of the balancing loop can prevent the saturation of the transformer core. Two methods for balancing the converter were proposed in this article. The first method is based on modifying the modulation pulse pattern to change the mean voltage value applied to each IPT. The second method modifies the modulation signal values, thereby varying the switching times of the vectors, also changing the mean values of the voltage. It is shown that both methods are based on the generation of different modulation patterns, which are used in an interleaved way because in each sextant, only one of the control variables is used, either $u_{bal,p}$ or $u_{bal,n}$. However, the only method that is decoupled is the second one because the control variables change only the respective

transverse current. Another advantage of the second balancing method is that it does not increase the switching losses. The first balancing method modifies the number of switching transitions and this can be seen in the waveforms of u_{nn} and u_{pp} . Although method 2 is more advantageous in terms of efficiency and decoupled control, both the two proposed closed-loop methods ensure the converter current balancing.

REFERENCES

- [1] B. K. Bose, "Power electronics and motor drives recent progress and perspective," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 581–588, Feb. 2009.
- [2] J. D. van Wyk and F. C. Lee, "On a future for power electronics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 2, pp. 59–72, Jun. 2013.
- [3] L. K. Ries, T. B. Soeiro, M. S. Ortmann, and M. L. Heldwein, "Analysis of carrier-based PWM patterns for a three-phase five-level bidirectional buck +boost-type rectifier," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6005–6017, Aug. 2017.
- [4] M. Baumann, U. Drofenik, and J. W. Kolar, "New wide input voltage range three-phase unity power factor rectifier formed by integration of a three-switch buck-derived front-end and a dc/dc boost converter output stage," in *Proc. 23rd Int. Telecommun. Energy Conf.*, 2000, pp. 461–470.
- [5] B. S. Dupczak, A. J. Perin, and M. L. Heldwein, "Space vector modulation strategy applied to interphase transformers-based five-level current source inverters," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2740–2751, Jun. 2012.
- [6] Y. Su, W. Chen, Y. Huang, Y. Lee, K. Chen, and H. Luo, "Pseudo-ramp current balance (PRCB) technique with offset cancellation control (OCC) in dual-phase dc-dc buck converter," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 22, no. 10, pp. 2192–2205, Oct. 2014.
- [7] Y. Su, W. Chen, Y. Huang, C. Chen, C. Ni, and K. Chen, "Time-shift current balance technique in four-phase voltage regulator module with 90% efficiency for cloud computing," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1521–1534, Mar. 2015.
- [8] J. Lin, K. Hu, and C. Tsai, "Digital multiphase buck converter with current balance/phase shedding control," in *Proc. IEEE Region 10 Conf.*, 2015, pp. 1–5.
- [9] J. Han and J. Song, "Phase current-balance control using dc-link current sensor for multiphase converters with discontinuous current mode considered," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4020–4030, Jul. 2016.
- [10] H. Maruta, T. Sakai, and F. Kurokawa, "Improvement of current balanced parallel soft-start operation for dc-dc converters with current prediction," in *Proc. Int. Conf. Renewable Energy Res. Appl.*, 2015, pp. 1058–1062.
- [11] H. Chen, C. Lu, and U. S. Rout, "Decoupled master-slave current balancing control for three-phase interleaved boost converters," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3683–3687, May 2018.
- [12] M. Baumann and J. W. Kolar, "Experimental evaluation of space vector oriented active dc-side current balancing of two parallel connected three-phase three-switch buck-type unity power factor rectifier systems," in *Proc. 24th Annu. Int. Telecommun. Energy Conf.*, 2002, pp. 317–324.
- [13] J. Bao, W. Bao, Z. Zhang, and W. Fang, "A simple current-balancing method for a three-phase 5-level current-source inverter," in *Proc. 35th Annu. Conf. IEEE Ind. Electron.*, 2009, pp. 104–108.
- [14] N. Binesh and B. Wu, "5-level parallel current source inverter for high power application with dc current balance control," in *Proc. IEEE Int. Elect. Mach. Drives Conf.*, 2011, pp. 504–509.
- [15] M. Baumann and J. W. Kolar, "Parallel connection of two three-phase three-switch buck-type unity-power-factor rectifier systems with dc-link current balancing," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3042–3053, Dec. 2007.
- [16] B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, and M. Cousineau, "PD modulation scheme for three-phase parallel multi-level inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 690–700, Feb. 2012.
- [17] S. A. D. Contreras, P. C. Cortizo, and M. A. S. Mendes, "Simple control technique for interleaved inverters with magnetically coupled legs," *IET Power Electron.*, vol. 6, no. 2, pp. 353–363, Feb. 2013.
- [18] F. B. Grigoletto and H. Pinheiro, "A hybrid modulation strategy for voltage fed converters with multiple parallel legs," in *Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2011, pp. 1046–1051.
- [19] G. J. Capella, J. Pou, J. Ceballos, S. Zaragoza, and V. G. Agelidis, "Current-balancing technique for interleaved voltage source inverters with magnetically coupled legs connected in parallel," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1335–1344, Mar. 2015.
- [20] I. G. Park and S. I. Kim, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Proc. 28th Annu. IEEE Power Electron. Specialists Conf.*, 1997, vol. 2, pp. 1164–1170.
- [21] D. O. Boillat and J. W. Kolar, "Modeling and experimental analysis of a coupling inductor employed in a high performance ac power source," in *Proc. Int. Conf. Renewable Energy Res. Appl.*, 2012, pp. 1–18.
- [22] L. K. Ries and M. L. Heldwein, "DC current balancing control of a three-phase five-level bidirectional buck+boost-type converter," in *Proc. IEEE 13th Brazilian Power Electron. Conf. 1st Southern Power Electron. Conf.*, 2015, pp. 1–6.



Lisandra Kittel Ries received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 2010, 2013, and 2018, respectively, and the B.S. and M.S. degrees in electrical engineering from the Institut National Polytechnique of Toulouse, Toulouse, France, in 2010.

She is currently an Adjunct Professor with the Electrotechnical Department, Federal Institute of Education, Science and Technology of Santa Catarina, Florianópolis, Brazil.



Marcelo Lobo Heldwein (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Florianópolis, Brazil, in 1997 and 1999, respectively, and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH Zurich), Zurich, Switzerland, in 2007.

He is currently an Associate Professor with the Department of Electronics and Electrical Engineering, UFSC. From 1999 to 2003, he was with industry, including R&D activities with the Power Electronics

Institute, Brazil and Emerson Network Power, Brazil and Sweden. He was a Postdoctoral Fellow with the ETH Zurich and UFSC from 2007 to 2009. His research interests include power electronics, advanced power distribution technologies, and electromagnetic compatibility.

Dr. Heldwein is a member of the Brazilian Power Electronic Society. He is also a member of the Advisory Board of PCIM Europe and an Associated Editor for the *IET The Journal of Engineering*.