Letters

An Active Z-Source DC Circuit Breaker Combined With SCR and IGBT

Ji Shu, Shunliang Wang, *Member, IEEE*, Junpeng Ma, *Member, IEEE*, Tianqi Liu, *Senior Member, IEEE*, and Zhiyuan He, *Member, IEEE*

***Abstract*—SCR-based solid-state dc circuit breaker (SCR-DCCB) topologies have been widely studied for replacing the traditional expensive insulated-gate bipolar transistor (IGBT) based DCCB. Yet, the existing SCR-DCCB cannot be actively turned-OFF since SCR is a half-controlled device. In this letter, an active Z-source DCCB (AZ-DCCB) is proposed by the combination of IGBT and SCR. The proposed AZ-DCCB has advantages of simple and compact topology, economical design, low conduction losses, and active and bidirectional current breaking capacity. The operation process of the proposed AZ-DCCB is discussed in detail, and the designing principle of circuit parameters is also presented. Experimental results verified the effectiveness of the proposed AZ-DCCB.**

***Index Terms*—DC circuit breaker, insulated-gate bipolar transistor (IGBT), SCR, Z-source.**

I. Introduction

AT PRESENT, direct current circuit breaker (DCCB) is considered as an effective approach to selectively and quickly isolate fault in dc system [1]. However, due to the absence of zero current crossing point and high fault current rising rate, the fault current interruption in dc system is much more difficult than ac system. Therefore, the availability of DCCB becomes so critical, making it one of the key enabling technologies for dc system.

Numerous DCCB topologies have been published and patented, and hybrid DCCB scheme is now considered as an acceptable solution [2], and has been applied to Zhoushan project in China [3]. However, there are some drawbacks to the hybrid DCCB topology as follows.

1) The mechanical ultrafast disconnector (UFD) slows the current breaking process.
2) Mechanical UFD increases the weight, volume, and investment of DCCB.
3) A large number of full-controlled semiconductors, such as insulated-gate bipolar transistors (IGBTs) or integrated gate-commutated thyristors, in the main breaker increase the investment severely [4].

Compared with hybrid DCCB, IGBT-based solid-state DCCB (SSCB) schemes have advantages of much simpler topology, faster reaction, and smaller volume, but the conduction losses are too high, and manufacturing cost is also expensive [5]. Recently, SiC-based wide-bandgap semiconductor devices are applied to design SSCB and hybrid DCCB. Wide-bandgap semiconductors have the advantages of higher blocking voltage and smaller conduction losses. After the technology is fully mature, it will be expected to be widely used in DCCB [6], [7]. Compared with full-controlled device IGBT, half-controlled device thyristor (SCR) with much smaller conduction losses, larger capacity, and lower price is now gradually applied to design SSCB [8]. However, since the turn-OFF process of SCR requires reverse voltage, the most important issue when designing an SCR-based SSCB (SCR-DCCB) is reliably to generate a reverse voltage on SCR during the turn-OFF process. Therefore, many SCR-DCCB topologies have been proposed [9]–[11], but most of them are too complicated to be applied into project. There are some simpler topologies, in which coupled inductors or Z-source schemes are used to generate the required reverse voltage on SCR during the turn-OFF process [9]–[11]. In those schemes, the transient fault current through capacitors is used to generate a reverse voltage on SCRs. Therefore, those SCR-DCCB schemes can only be passively turned-OFF in the condition of the high current rising rate. This will bring disadvantages, which are as follows.

1) The fault current rising rate may not be sufficiently high when a minor fault occurs [11].
2) DCCBs may be triggered by mistake during transient process.
3) The operating current cannot be actively interrupted by those existing DCCBs.

Therefore, these existing SCR-DCCB schemes are not suitable for project application. In [11], a manual tripping mechanism is proposed. This method provides sufficient high current rising rate of SCR-DCCB by manually inducing fault in the dc system, and thereby turn it OFF actively. Obviously, this tripping mechanism will bring additional damages to dc system and is not the best choice. In [12], three active SCR-DCCB schemes

Manuscript received December 28, 2019; revised January 27, 2020 and February 25, 2020; accepted March 9, 2020. Date of publication March 12, 2020; date of current version June 23, 2020. This work was supported by the National Key R&D Program of China under Grant 2018YFB0904600. (*Corresponding author: Shunliang Wang*.)

Ji Shu, Shunliang Wang, Junpeng Ma, and Tianqi Liu are with the College of Electrical Engineering, Sichuan University, Chengdu 610025, China (e-mail: shuji_scu@163.com; slw_scu@163.com; junpeng_ma@163.com; tpliu@scu.edu.cn).

Zhiyuan He is with the State Key Laboratory of Advanced Transmission Technology, Global Energy Interconnection Research Institute, Beijing 102202, China (e-mail: hezhiyuan@geiri.sgcc.com.cn).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.2980543

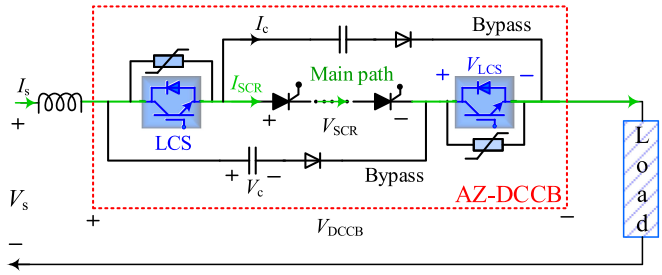

Fig. 1. Topology of proposed AZ-DCCB.

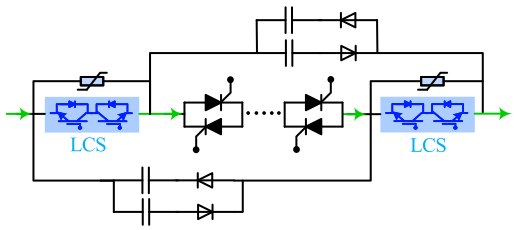

Fig. 2. Topology of bidirectional AZ-DCCB.

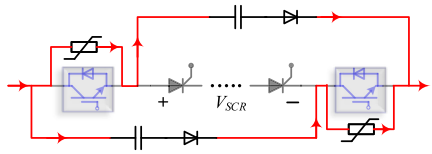

Fig. 3. Fault current breaking process of AZ-DCCB: Capacitors are charged by fault current.

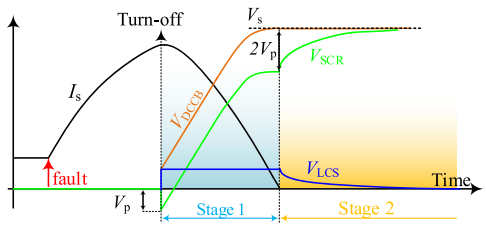

Fig. 4. Fault current breaking process of AZ-DCCB: Fault current and voltage.

are proposed, but all those schemes severely increase both the complexity and cost of DCCB.

In this letter, the full-controlled IGBT and half-controlled SCR are combined to design an active Z-source DCCB (AZ-DCCB) for medium- or high-voltage dc system. IGBT here is just an example, it can be other fully controlled device. This proposed AZ-DCCB combines the advantages of fully controlled device and half-controlled device. The conduction losses are effectively reduced compared to traditional SSCB. Both the fault current and operating current can be actively interrupted by the proposed scheme. Meanwhile, compared to the traditional DCCB schemes, the topology is simple, economical, and reliable.

II. Proposed Topology

A. Topology Introduction

The topology of the proposed AZ-DCCB is shown in Fig. 1, where subscript "c," "s," and "SCR" indicate capacitor, dc system, and SCR parameters, respectively. V_{DCCB} and V_{LCS} are the voltage of AZ-DCCB and line commutation switch (LCS) module. The current limiting reactor is not part of AZ-DCCB, but an independent device of dc transmission system.

During normal operation, dc current flows through the main path, which is composed of two LCS modules and a set of SCRs in series connection. $I_{\mathrm{SCR}} = I_s$ and $I_c = 0$ during normal operation. Both LCS modules are protected by parallel mental oxide arrestors (MOAs), and they will be switched OFF to interrupt the current, which will flow into the bypass branches during the current breaking process. The dc system voltage V_s is borne by off-state SCRs in series connection after breaking the current. Diodes in both bypass branches can prevent oscillation. Moreover, both LCS modules include snubber circuits (energy dissipating resistors and bypass capacitors), which are not shown in Fig. 1.

Only a few IGBTs are needed in each LCS module, and the protection voltage of the parallel MOA V_p for LCS modules is thus much smaller than the system voltage. With the number of IGBTs decreased, this topology becomes more economical than traditional IGBT-based DCCB schemes. The proposed solution can be further improved with bidirectional current breaking capability by connecting an identical structure in the reverse direction, as shown in Fig. 2.

B. Fault Current Breaking Process

The fault current breaking process of the proposed AZ-DCCB is simple: both LCS modules in the main path will be switched OFF while the fault is detected, as shown in Fig. 3. The fault current and voltage waveforms are presented in Fig. 4. There are two stages to interrupt fault current.

Stage 1: Initially, SCRs connected in series still are on-state, LCS voltage V_{LCS} will suddenly increase while LCSs are turned OFF, but it is strictly limited to the protection voltage V_p by the parallel MOA. The capacitors in both bypass branches are connected to the dc system. As shown in Figs. 3 and 4, the fault current will keep charging capacitors from zero-voltage state until fault current decreases to zero.

Stage 2: Stage 2 begins at the instant of zero fault current. The equivalent resistance of one LCS module is much smaller than that of off-state SCRs connected in series, LCS voltage V_{LCS} will gradually decrease to zero and SCR voltage V_{SCR} will increase to system voltage V_s.

At the beginning of stage 1 during the current breaking process, the capacitor voltage V_c gradually increases from zero but it is smaller than the protection voltage V_p, and a reverse voltage V_{SCR} ($V_{\mathrm{SCR}} = V_c - V_p$) will hereby be generated. As mentioned earlier, SCRs can only be passively turned-OFF by a reverse voltage process. The duration of reverse voltage should be larger than the requested recovery time of SCRs to turn them OFF reliably. A detailed discussion about the reverse voltage duration is presented in Section III.

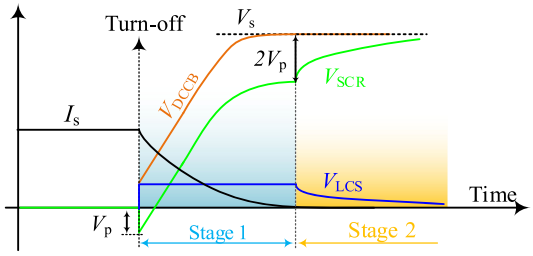

Fig. 5. Operating current breaking process of AZ-DCCB: Current and voltage.

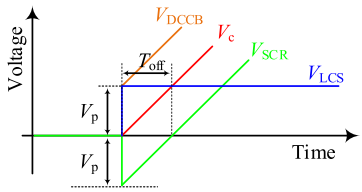

Fig. 6. Turn-OFF process of AZ-DCCB: Reverse voltage on SCR.

C. Operating Current Breaking Process

As mentioned earlier, SCR-DCCB schemes are "half-controlled," because those schemes can only be passively turned-OFF by the transient process with high current rising rate, so the operating current cannot be interrupted. However, the proposed AZ-DCCB with the merit of IGBT can realize a controllable and active turn-OFF process.

The operating current breaking process of AZ-DCCB is demonstrated in Fig. 5. When current breaking signal is received, LCS modules will be triggered to turn-OFF, and operating current will start to decrease immediately. Similar to the fault current breaking process, the AZ-DCCB will also experience the same stages 1 and 2.

III. Design Considerations

The most important issue of designing parameters for the proposed AZ-DCCB is to make sure that the duration of reverse voltage on SCRs must be larger than the minimum requested recovery time of SCR. Based on the opening process of AZ-DCCB presented earlier, the SCR voltage $V_{\rm SCR}$ can be expressed as

$$V_{\rm SCR} = V_c - V_p. \tag{1}$$

When the capacitor voltage V_c is smaller than the protection voltage V_p, $V_{\rm SCR}$ is negative. There will be a reverse voltage on SCRs. When the capacitor voltage V_c exceeds the protection voltage of MOA V_p, the reverse voltage process of SCRs will be finished, this process is shown in Fig. 6. The duration of reverse voltage on SCRs $T_{\rm off}$ depends on the capacitor charging current and the protection voltage of MOAs V_p. It is assumed that the system current I_s keeps constant during the reverse voltage process. $T_{\rm off}$ can be roughly calculated by (2), where C is the capacitance in the bypass branch

$$T_{\rm off} = 2CV_p/I_s. \tag{2}$$

TABLE I
Typical Parameters of AZ-DCCB for 200 kV/2 kA System

V_s	I_o	I_{max}	V_p	C	T_R	α
200kV	2kA	4kA	10kV	80μF	200μs	1.5

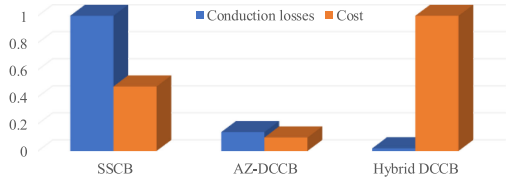

Fig. 7. Relative conduction losses and costs of three DCCB schemes.

To meet the minimum recovery time of SCR under the worst situation, capacitance in both bypass branches can be chosen according to (3), where T_R is the minimum recovery time of SCRs and $I_{\rm max}$ is the maximum allowed breaking current of AZ-DCCB. To prevent AZ-DCCB from being mistriggered by inrush current, the proposed AZ-DCCB should not be triggered until the current breaking signal is received from the protection system. α is the redundancy factor and it must be larger than 1. The choosing principle of α depends on turn-OFF characteristic of different SCRs. A larger redundancy factor α increases the reliability of AZ-DCCB, but the capacitor value becomes larger. A redundancy factor of 1.5∼3 is generally preferred

$$C = \alpha T_{\rm R} I_{\rm max}/\left(2V_p\right). \tag{3}$$

According to the parameters design principle presented earlier, typical parameters of AZ-DCCB suitable for a 200-kV/2-kA dc system are presented in Table I, where I_o is the normal operating current.

The proposed AZ-DCCB is compared with SSCB and the hybrid DCCB to elaborate on the advantages of the proposed solution. The relative conduction losses and costs of three DCCB schemes in the same voltage level are shown in Fig. 7, where the ordinate is a relative value and "1" represents the maximum. As can be seen, the conduction loss in the proposed AZ-DCCB is smaller than that in SSCB, but higher than that in hybrid DCCB. However, the cost of the proposed solution is much lower than that of hybrid DCCB. Considering the conduction losses and costs together, the proposed solution is the optimal one in comprehensive performance.

Moreover, the IGBT in the AZ-DCCB is just an example of fully controlled device. Using wide-bandgap devices, the conduction losses of the proposed AZ-DCCB will be further decreased. Parallel connecting the IGBTs in the LCS module or even SCRs can also decrease the conduction loss of AZ-DCCB, but the investment of AZ-DCCB will be increased, there exist a trade-off between lower conduction loss and higher investment.

IV. Experiment Results

A scaled-down experimental setup is built for verifying the effectiveness of proposed AZ-DCCB, as shown in Fig. 8. Both bypass capacitors have a capacity of 30 μF and the protection

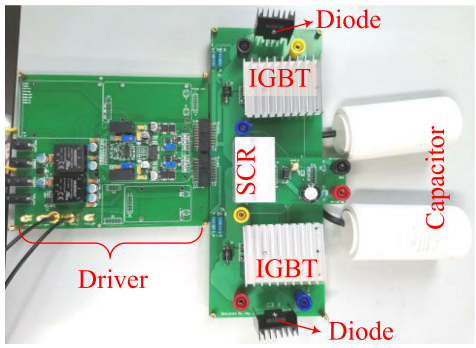

Fig. 8. Low voltage prototype of AZ-DCCB.

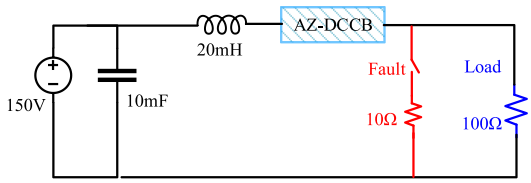

Fig. 9. Experimental 150-V/1.5-A dc system.

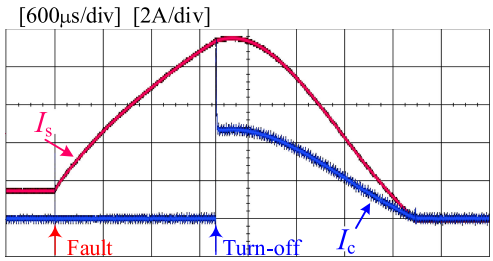

Fig. 10. Fault current breaking process of AZ-DCCB: Fault current.

voltage V_p of MOA is 20 V. The dc-voltage and current are 150 V and 1.5 A, respectively, in this setup, which is shown in Fig. 9. Considering that the bidirectional AZ-DCCB topology is a reverse connection of two unidirectional AZ-DCCBs; therefore, the verification for the current opening process of unidirectional one is enough.

A serious short-circuit fault is manually induced for testing the performance of the proposed AZ-DCCB, and the line current of dc system will rise from 1.5 to 15 A within 10 ms.

A. Fault Current Breaking Process

The fault current breaking process of the proposed AZ-DCCB is presented in Figs. 10 and 11. As shown in Fig. 10, when LCSs are turned-OFF, the fault current is successfully interrupted in 5 ms by the proposed AZ-DCCB. The breaking current is more than seven times higher than the operating current.

The voltage waveforms during the fault current breaking process are presented in Fig. 11. As can be observed, LCS voltage is strictly limited to the protection voltage 20 V. When capacitor voltage V_c exceeds protection voltage V_p, SCR voltage changes from negative to positive, reverse voltage process

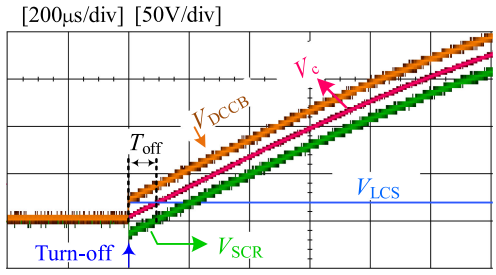

Fig. 11. Fault current breaking process of AZ-DCCB: Reverse voltage process.

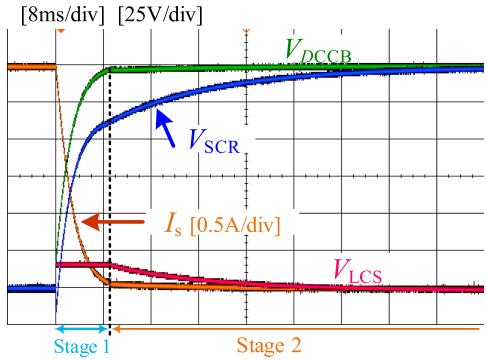

Fig. 12. Operating current breaking process of AZ-DCCB.

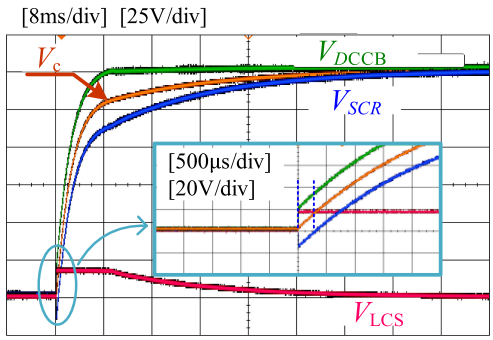

Fig. 13. Voltage waveforms during operating current breaking process.

ends. Experimental results shown in Fig. 11 consistent with the theoretical analysis presented in Fig. 6.

B. Operating Current Breaking Process

Traditional SCR-DCCB cannot break operating current actively, but the opening process proposed AZ-DCCB is fully controllable. The operating current breaking process is presented in Fig. 12. The load of the dc system is changed manually, operating current increased from 1.5 to 3 A. As can be seen in Fig. 12, when AZ-DCCB is triggered to turn-OFF, the operating current is successfully interrupted during stage 1 and voltage of SCRs V_{SCR} increase to system voltage during stage 2.

Experiment consistent with the theoretical analysis is shown in Fig. 5. The voltage waveforms during the operating current breaking process are shown in Fig. 13. A similar reverse voltage process on SCRs can be observed.

V. Conclusion

Combining the merits of IGBT and SCR, an AZ-DCCB is proposed in this letter. Detailed current interrupting process of proposed AZ-DCCB is analyzed, the parameter design principle is also presented. A scaled-down experimental test successfully verified the effectiveness of the proposed method. This proposed AZ-DCCB topology has the following advantages.

1) The topology design is economical and simple.
2) Conduction losses are relatively small.
3) The current breaking process is actively controllable and bidirectional, and the normal operation current can hereby be actively turned-OFF.

References

[1] C. M. Franck, "HVDC circuit breakers: A review identifying future research needs," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 998–1007, Apr. 2011.

[2] M. Callavik, A. Blomberg, J. Hafner, and B. Jacobson, "Break-through! ABB's hybrid HVDC breaker, an innovation breakthrough enabling reliable HVDC grids," *ABB Rev.*, no. 2, pp. 7–13, 2013.

[3] W. Zhou *et al.*, "Development and test of a 200kV full-bridge based hybrid HVDC breaker," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–7.

[4] X. Zhang, Z. Yu, Z. Chen, B. Zhao, and R. Zeng, "Optimal design of diode-bridge bidirectional solid-state switch using standard recovery diodes for 500-kV high-voltage DC breaker," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1165–1170, Feb. 2020.

[5] M. K. Bucher and C. M. Franck, "Fault current interruption in multiterminal HVDC networks," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 87–95, Feb. 2016.

[6] Z. J. Shen, G. Sabui, Z. Miao, and Z. Shuai, "Wide-bandgap solid-state circuit breakers for DC power systems: Device and circuit considerations," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 294–300, Feb. 2015.

[7] X. Song, C. Peng, and A. Q. Huang, "A medium-voltage hybrid DC circuit breaker, Part I: Solid-state main breaker based on 15 kV SiC emitter turn-OFF thyristor," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 278–288, Mar. 2017.

[8] S. Beheshtaein, R. M. Cuzner, M. Forouzesh, M. Savaghebi, and J. M. Guerrero, "DC microgrid protection: A comprehensive review," *IEEE J. Emerg. Sel. Topics Power Electron.*, to be published.

[9] Y. Wang, W. Li, X. Wu, and X. Wu, "A novel bidirectional solid-state circuit breaker for DC microgrid," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5707–5714, Jul. 2019.

[10] A. Ray, K. Rajashekara, S. N. Banavath, and S. K. Pramanick, "Coupled inductor-based zero current switching hybrid DC circuit breaker topologies," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5360–5370, Sep./Oct. 2019.

[11] A. H. Chang, B. R. Sennett, A. Avestruz, S. B. Leeb, and J. L. Kirtley, "Analysis and design of DC system protection using Z-source circuit breaker," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1036–1049, Feb. 2016.

[12] C. Meyer and R. W. De Doncker, "Solid-state circuit breaker based on active thyristor topologies," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 450–458, Mar. 2006.