A Novel DCM Soft-Switched SEPIC-Based High-Frequency Converter With High Step-Up Capacity

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***Abstract*—A novel discontinuous conduction mode (DCM) soft-switched single ended primary inductor converter (SEPIC)-based high-frequency converter is presented in this article with the advantages of high voltage gain and low voltage stress. In order to achieve higher voltage gain, it integrates a switched inductor with a coupled inductor–based modified SEPIC converter, and a resonant cell is built with integration of a resonant capacitor, which enables the switches to work under zero voltage switching (ZVS). Therefore, the working principle is changed and better performance is obtained. The proposed converter can operate in both continuous conduction mode (CCM) and DCM, but ZVS can only be achieved in the discontinuous mode; hence, DCM is more suitable for high-frequency applications. Mode analysis, parameter design, and boundary of the two working modes are all presented in detail. For higher efficiency, a 500-kHz/54-W DCM prototype with 15 voltage gain has been designed to demonstrate theoretical analysis. Obtained efficiency was up to 93.4% at full load. Experimental results show good accordance with theoretical analysis.**

***Index Terms*—High frequency, high step up, SEPIC, soft switching.**

I. Introduction

In THE recent years, much attention has been paid to high step-up dc–dc converters because of the growing demand in applications such as photovoltaic systems, micro-fuel cells, vehicle power supply, and uninterruptable power supplies [1]–[5]. In practical applications, the former stages of photovoltaic (PV) inverter and LEDs of automotive headlight both need high output voltage. The most common step-up converter is boost with a simple structure and grounded switch. Limited by duty cycle, conventional boost converters are not available because of large conduction loss and severe diode reverse recovery problems. Besides, the high voltage stress of the power switch also limits its application for higher output voltages [6], [7]. Therefore, many new technologies, such as switched-capacitor [8]–[11] and coupled-inductor [12]–[15], are proposed recent years to achieve higher voltage gain with moderate duty cycle. The switched-capacitor technique can achieve a high step-up gain as well as high power density because of the absence of magnetic components; however, the main switch suffers high surge current and increased conduction loss, which may decrease both power density and efficiency, limiting its application to some extent. As for coupled inductors, one main constraint is that the leakage inductance will cause a high voltage spike across the switch. Accordingly, passive clamp circuits are essential to suppress the switch voltage spikes and recycle the leakage energy. This means that an extra active switch is needed, and it results in high conduction losses, high cost, and circuit complexity. Another common technique is the cascading of boost converters for higher voltage gain at low duty cycles; its voltage gain is multiplied by every stage. However, as the number of stages increases, the control of converters becomes complex. In addition, this converter still suffers from high voltage stress [16]–[18]. Based on the aforementioned analysis, satisfactory high-voltage-gain converters should have advantages of simple structure, easy control, and low voltage stress.

With the increasing requirements of power electronic converters, high frequency has become a general trend with the advantages of compact volume and high power density. As for high-voltage-gain converters, high frequency is also an inevitable development direction. However, the increase of switching frequency will also lead to the increase of switching loss; therefore, how to reduce switching loss becomes a vital problem in the design of high-frequency converters. The soft-switching characteristic has become one of the most important properties to evaluate the performance of converters.

In recent years, single ended primary inductor converter (SEPIC) and modified SEPIC converters are also widely used in electronics and industrial applications. A modified SEPIC circuit integrated with a voltage multiplier, which was composed of a diode and a capacitor, for obtaining high voltage gain and low voltage stress with a simple structure was proposed in [19] and [20]. But the switch worked in hard-switching mode

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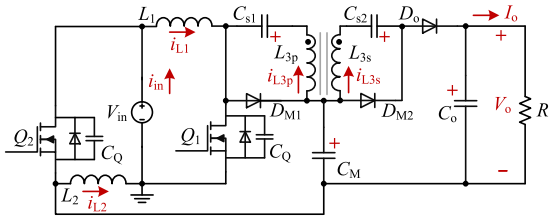

Fig. 1. Proposed SEPIC-based circuit.

and the switching loss would be quite large when applied to high-frequency applications. In order to solve this problem, a modified zero voltage switching (ZVS) SEPIC circuit with a resonant network, maintaining high voltage gain and low voltage stress, was proposed in [21], and this converter achieved 93.1% efficiency under 1 MHz. A noncoupled inductor SEPIC converter is proposed in [22]; compared with the converter in [19], switched inductor technique is adopted to obtain higher voltage gain. This also means one more power switch and one more inductor are added [23]. CCM and DCM are both analyzed in detail, and CCM experimental results are presented. However, this converter works in hard-switching mode, which contributes dramatically to high switching loss when applied to high-frequency applications.

Therefore, based on the previous work, a novel soft-switched SEPIC-based high-frequency high step-up converter is presented in this article, which is capable of meeting the requirements of high voltage gain, low voltage stress, and low system loss. The proposed converter incorporated a switched inductor with a modified SEPIC converter to achieve higher voltage gain. Compared with the converter in [22], a coupled inductor is added to further increase the voltage gain; besides, a resonant cell is also built with the integration of a resonant capacitor, which enables the switches to work under ZVS. Voltage gain of the proposed converter depends on both duty cycle and windings turns ratio, which helps to avoid duty cycle or windings turns ratio becoming too large. However, the input current is sum of the inductor current and the switch current; therefore, the input current ripple is higher, and there is a tradeoff between the voltage gain and the input current ripple. The working principle and the voltage gain are both different from the previous work. This converter is also able to operate under both CCM and DCM, but ZVS can only be achieved in DCM. Mode analysis and parameter design of both working modes are all presented in detail, and voltage gain of both working modes and the boundary of CCM and DCM are also derived.

This article is organized as follows. In Section II, the operational principles of the converter in CCM and DCM are described briefly; the parameters design of different working modes are introduced in detail in Section III, while Section IV shows the experimental results of DCM prototype. Finally, Section V concludes this article.

II. Operational Principle of the Modified SEPIC

The novel SEPIC-based converter with ZVS characteristic proposed in this article is illustrated in Fig. 1, where $V_{\rm in}$ is the input voltage, V_o is the output voltage, the load is represented by a resistor R, and the output current is shown as I_o. The proposed converter consists of three diodes $D_{M1,2}$ and D_o; two switches Q_1 and Q_2; four capacitors $C_{s1,2}$, C_M, and C_o; two inductors L_1 and L_2 and a coupled inductor L_{3p} and L_{3s}; and the capacitor C_Q, which represents the sum of the parasitic capacitance of the switch and the additional capacitance in parallel.

First, the proposed SEPIC-based converter achieves high voltage gain by adding the auxiliary capacitor C_M and the diode D_{M1}, which form a voltage multiplier. When the switches turn OFF, C_M is charged through D_{M1} and then the energy stored in C_M is transferred to L_{3p} when the switches turn ON. Therefore, the energy stored in L_{3p} is larger than traditional SEPIC and higher voltage gain is obtained. Another set of inductor and switch L_2 and Q_2 are added to double the voltage gain. It is noted that the inductances of L_1 and L_2 are equal, and the drive signals of Q_1 and Q_2 are synchronous. Finally, the coupled inductor is designed to further increase the output voltage, and the relationship between the inductance of its primary and secondary sides is $L_{3s} = n^2 \cdot L_{3p}$, where n is the turns ratio of the coupled inductor.

It is noted that the voltage stress of the proposed converter is reduced to less than half of that of the classical SEPIC converter, which is the sum of the input voltage and the output voltage. Moreover, soft switching of the MOSFETs in the circuit significantly contributes to system loss saving.

The proposed SEPIC-based converter is able to operate under both CCM and DCM, depending on whether the current flowing through D_o is already zero by the time the next driving signal comes. Both of the working states are introduced in detail in the following sections.

A. Continuous Conducting Mode

When operating under CCM, the three working modes in a switching period are shown in Fig. 2. There is no resonant period in the continuous mode, so under this circumstance, C_Q is the only parasitic capacitor of the switches $C_{\rm oss}$, and therefore, the charge and discharge periods of this small capacitor is very short, which could be neglected. As a result, main waveforms in a switching period are illustrated in Fig. 3, where v_{gs} is the drive signal of the switches; v_{ds} is the drain-source voltage; $i_{\rm DM1}$ and i_{Do} are the current flowing through the two diodes, while $i_{L1,2}$ is current flowing through L_1 and L_2; and $v_{L1,2}$ is the voltage stress of $L_{1,2}$.

Mode 1 (t_0–t_1): Both switches are turned ON at t_0, and then L_1 and L_2 are charged in parallel by the input voltage, while L_{3p} is charged through $V_{\rm in} - Q_2 - L_{3p} - Q_1 -$ GND, and L_{3s} is discharged through $L_{3s} - D_{M2} - C_{s2}$. In fact, the leakage inductance of the coupled inductor limits the current, and the energy transference occurs in a resonant way; therefore, the two switches turn ON with ZCS.

Mode 2 (t_1–t_2): After the switches are turned OFF, D_{M1} is turned ON since the voltage $v_{\rm ds}$ rises rapidly. The current flowing through the inductors declines as energy is transferred to the output side. In this interval, current flowing through D_o rises

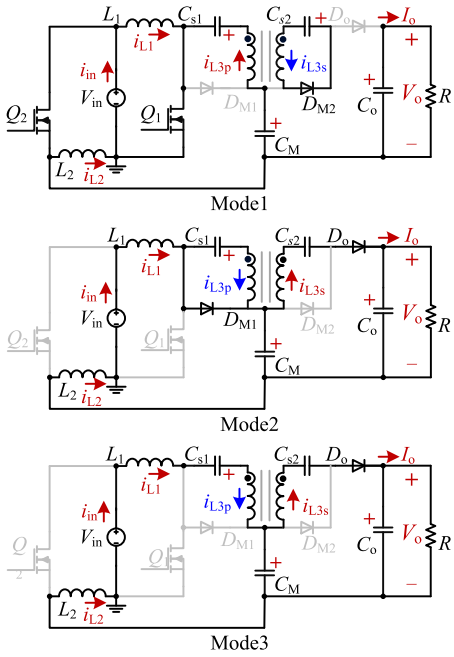

Fig. 2. Working modes of the proposed modified SEPIC circuit (CCM).

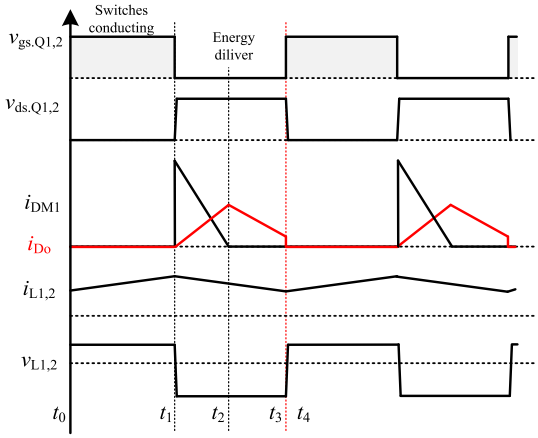

Fig. 3. Main voltage and current waveforms under CCM.

linearly while that of D_{M1} declines linearly. When i_{DM1} finally reaches zero at t_3, mode 2 ends.

Mode 3 (t_2–t_3): As D_{M1} is turned OFF, the value of i_{L3p} becomes equal to that of i_{L1}. i_{Do} drops linearly in this mode. And when the next driving signal reaches, the switches are turned ON simultaneously, which means that an entire switching period ends.

B. Discontinuous Conducting Mode

However, in order to realize zero voltage turn ON of the MOSFETs, the circuit is designed to operate under discontinuous mode, which means that the current flows through D_o is supposed to be zero when the turn-ON signal v_{gs} arrives.

While operating under DCM, there are seven working modes in a whole switching period, which are shown in Fig. 4, and correspondingly, the key waveforms are illustrated in Fig. 5.

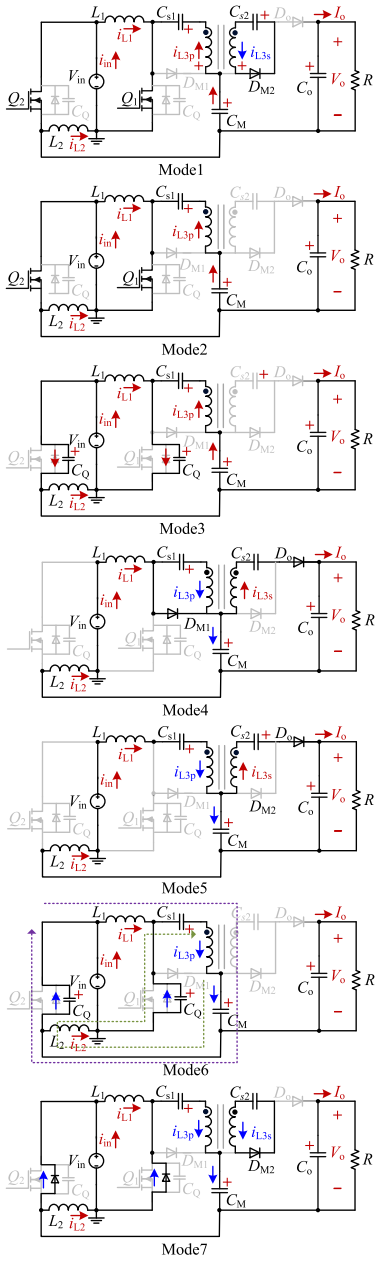

Fig. 4. Working modes of the proposed modified SEPIC circuit (DCM).

Mode 1 (t_0–t_1): Since the body diodes are turned ON before t_0, both switches can turn ON with zero voltage, and then the working state of the three inductors in the circuit is the same as that under CCM. Meanwhile, energy in the output capacitor C_o is transferred to the load. The voltage relationship between each component in this mode is written as

$$v_{L(\mathrm{mode1})} = V_{\mathrm{in}} \tag{1}$$

$$v_{L3p(\mathrm{mode1})} = V_{\mathrm{in}} + V_{C_M} - V_{C_{s1}} \tag{2}$$

$$V_{C_{s2}} = v_{L3s(\mathrm{mode1})} = n \cdot v_{L3p(\mathrm{mode1})}. \tag{3}$$

Here, $v_{L(\mathrm{mode1})}$ and $v_{L3p(\mathrm{mode1})}$ represent the voltage of $L_{1,2}$ and L_{3p} in this mode, while V_{CM} and $V_{Cs1,2}$ are the voltage stress of the three capacitors.

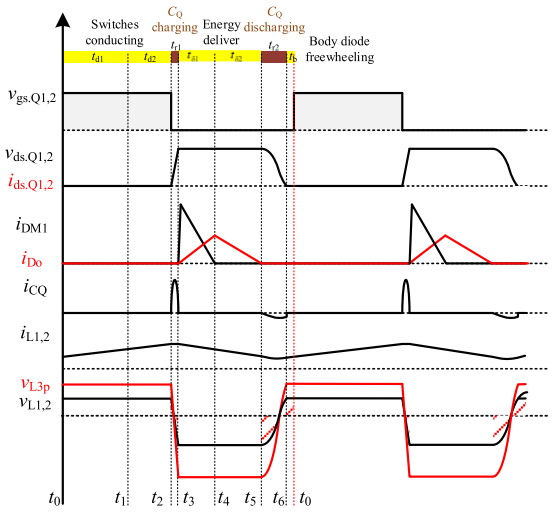

Fig. 5. Main voltage and current waveforms under DCM.

Mode 2 (t_1–t_2): The current flowing through L_{3s} reaches zero at t_1, but the inductors are still charged and i_{L3p} keeps rising. This mode ends when the turn-OFF signal comes at t_2.

The sum of the interval of these two modes above is defined as $t_d = t_2 - t_0 = D \cdot T_s$, where D is the duty cycle and T_s is time of a whole switching period. These two modes are defined as conducting modes.

Mode 3 (t_2–t_3): Both Q_1 and Q_2 are turned OFF at t_2, while at the same time, the voltage of the switches begins to rise because of the charging of its parallel capacitors C_Q. Moreover, the charging time is defined as $t_{r1} = t_3 - t_2 = D_{r1} \cdot T_s$; this interval is very short as the capacitance of C_Q is small. When $v_{dsQ1,2}$ finally reaches $(V_{C_M} + v_{L(\text{mode3})})$ at t_3, the charging finishes and this mode ends.

Mode 4 (t_3–t_4): The increase of v_{ds} and the decrease of v_{L3} provide the conduction condition for D_{M1} and D_o, and therefore, energy from L_1 and L_2 is transferred to C_M through D_{M1}. Furthermore, energy from three capacitors is also transferred to C_o through D_o. The voltage relationships in this mode are given by (4)–(6), where $v_{L(\text{mode4})}$ and $v_{L3p(\text{mode4})}$ are, respectively, the voltage of $L_{1,2}$ and L_{3p} in mode 4. The current flowing through D_M rises linearly and that of D_o shows an opposite tendency. Mode 4 lasts for $t_{\delta 1}$ and ends by the time i_{DM} reaches zero. Therefore, the relationship between the current flowing through the inductors at t_4 can be written as (7)

$$v_{L(\text{mode4})} = \frac{V_{\text{in}} - V_{C_M}}{2} \tag{4}$$

$$v_{L3p(\text{mode4})} = -V_{Cs1} \tag{5}$$

$$V_{CM} + nV_{\text{Cs1}} + V_{Cs2} = V_o \tag{6}$$

$$i_{L1,2}(t_4) = -i_{L3}(t_4). \tag{7}$$

The capacitance of C_M and $C_{s1,2}$ is designed to be large enough to maintain the voltage constant. The working state of $L_{1,2}$ and L_{3p} is the same during each mode, so their voltages are also proportional, as shown in Fig. 5. Then according to the voltage relationship of the input side in mode 1 and mode 4, respectively, we can get $v_{L3p} = 2v_L$, where v_{L3p} and v_L are the instantaneous voltage of L_{3p} and $L_{1,2}$, respectively.

As a result, the voltage of capacitors and the relationship between voltage of L_1 and L_{3p} in this interval can be obtained according to (1)–(6), which is given by

$$V_{C_M} = \frac{V_o - nV_{\text{in}}}{n+1} \tag{8}$$

$$V_{C_{s1}} = \frac{V_o - (2n+1)V_{\text{in}}}{n+1} \tag{9}$$

$$V_{C_{s2}} = 2n \cdot V_{\text{in}} \tag{10}$$

$$v_{L3p(\text{mode4})} = 2v_{L(\text{mode4})} = \frac{(2n+1)V_{\text{in}} - V_o}{n+1}. \tag{11}$$

Mode 5 (t_4–t_5): At t_4, D_{M1} is turned OFF, so the current of L_{3p} i_{L3p} is equal to i_L, and accordingly, i_{Do} declines linearly from its peak value as well. Time of this mode is defined as $t_{\delta 2}$, and by the time i_{Do} reaches zero, mode 5 ends.

The output diode D_o is always working in modes 4 and 5, so energy is delivered to the load during t_3–t_5, which is defined as the energy deliver mode: $t_\delta = t_5 - t_3 = D_\delta \cdot T_s$.

Mode 6 (t_5–t_6): All the diodes are turned OFF in this interval, and the two parallel capacitors resonant with the inductors respectively through the two loops in the circuit. According to Fig. 4, the current flowing through C_Q i_{CQ} is sum of i_L and i_{L3p}; therefore, each capacitor is considered to resonant with an equivalent inductor, whose value is given by

$$L_{\text{eq}} = \frac{L_{3p}}{2} \parallel L = \frac{L \cdot L_{3p}}{2L + L_{3p}} \tag{12}$$

where $L_1 = L_2 = L$. This interval ends when C_Q is entirely discharged; in other words, the drain-source voltage of both switches is zero at the moment. The time interval is $t_{r2} = t_6 - t_5 = D_{r2} \cdot T_s$.

Mode 7 (t_6–t_7): The inductor current is able to freewheel through their body diodes before the switches are turned ON again. This interval lasts for $t_b = t_0 - t_6 = D_b \cdot T_s$, and it ends when the drive signal of the next switching cycle is received.

III. Parameter Design of the Modified SEPIC

In the following sections, the design procedure of the converter under both continuous and discontinuous operating modes are analyzed in detail and the value of the boundary inductance is presented as well.

A. Voltage Gain

1) Continuous Conducting Mode: As for CCM, the voltage of inductor L_1 in modes 1 and 2 is, respectively, equal to that of DCM in modes 1 and 4, which are shown in (1) and (11). So the volt–second balance principle of L_1 can be expressed as

$$V_{\text{in}} \cdot D + \frac{(2n+1)V_{\text{in}} - V_o}{2(n+1)}(1-D) = 0. \tag{13}$$

Then the voltage gain of CCM M_{CCM} can be deduced by

$$M_{\text{CCM}} = \frac{V_o}{V_{\text{in}}} = \frac{2n+1+D}{1-D}. \tag{14}$$

Generally, the entire switching cycle of CCM can only be divided into two intervals, where mode 1 is defined as the conducting interval, which lasts for t_d, and modes 2 and 3 are defined as the energy deliver interval, which lasts for t_δ in total. Thus, their relationship in CCM is written as

$$t_\delta = \left(\frac{1}{D} - 1\right) t_d. \tag{15}$$

2) Discontinuous Conducting Mode: When operating under discontinuous mode, as t_{r1} and t_{r2} are relatively short compared to the other intervals, the inductor voltage is approximately linearized during two resonant modes, so the volt–second balance principle of $L_{1,2}$ in a switching cycle can be expressed by (16)

$$V_{\text{in}}\left(t + t_b\right) + \bar{v}_L \cdot t_{r1} + \frac{\left(2n+1\right)V_{\text{in}} - V_o}{2\left(n+1\right)} \cdot t_\delta + \bar{v}_L \cdot t_{r2} = 0. \tag{16}$$

Here, $\bar{v}_L = \left(v_{L(\text{mode1})} + v_{L(\text{mode4})}\right)/2$ represents the average voltage of $L_{1,2}$ in the resonant modes, and the total time of resonant period can be obtained through the other intervals, which is shown in (17). Therefore, the voltage gain of the DCM converter M_{DCM} is illustrated in (18)

$$t_{r1} + t_{r2} = T_s - t_d - t_\delta - t_b \tag{17}$$

$$M_{\text{DCM}} = \frac{V_o}{V_{\text{in}}} = \frac{(4n+3) + (D + D_b) - D_\delta}{1 - (D + D_b) + D_\delta}. \tag{18}$$

According to Fig. 5, $i_{L1,2}(t_0)$ is considered to be approximately equal to $i_{L1,2}\,(t_5)$; as a result, the relationship of the time between the conducting interval and the energy deliver interval of DCM is given by

$$t_\delta = \frac{2\left(n+1\right)}{M_{\text{DCM}} - (2n+1)} t_d. \tag{19}$$

As a result, if the design parameters are given, the energy deliver time can be calculated by (19), and then, the total resonant time is correspondingly obtained.

B. Inductor and Coupled Inductor Design

The inductance in the proposed converter is designed according to the ampere–second balance principle of the output capacitor C_o whose current $i_{C_o} = i_{D_o} - I_o$.

The output current $I_o = V_o/R$. As i_{Do} is always zero except in modes 4 and 5 and it changes linearly in these two modes, the expression can be written as

$$i_{D_o} = \begin{cases} k_r \cdot (t - t_3), & t_3 < t \le t_4 \\ k_r \cdot t_{\delta 1} - k_f \cdot (t - t_4), & t_4 < t \le t_5 \end{cases}. \tag{20}$$

Here, k_r and k_f are, respectively, the rising and falling rates of i_{Do}, both of which are to be determined, and respective analysis of these two modes are given in the following sections.

1) Continuous Conducting Mode: First, the auxiliary diode D_{M1} only works during mode 2 when its current equals to the sum of i_{L1} and i_{L3p}. Thus, as shown in Fig. 3, since the sum of i_{L1} and i_{L3p} is considered to be zero at t_0, the peak current of

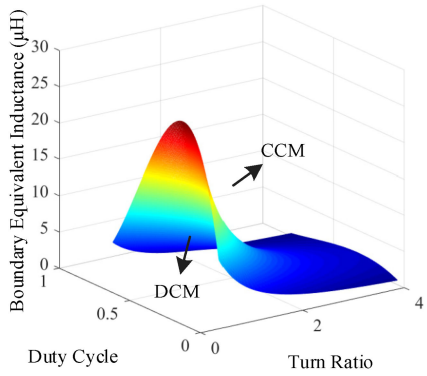

Fig. 6. Boundary equivalent inductance of the circuit with different duty cycle and turns ratio.

D_{M1} $I_{\text{DM1\_peak}}$ can be rewritten as

$$I_{DM1\_\text{peak}} = \frac{V_{\text{in}} t_d}{L_{\text{eq}}}. \tag{21}$$

Moreover, the average current of the three diodes in a whole switching cycle is equal to I_o, so the time of mode 2 is obtained by

$$t_{\delta 1} = \frac{2 I_o L_{\text{eq}}}{V_{\text{in}} D} = \frac{2 M_{\text{DCM}} L_{\text{eq}}}{RD}. \tag{22}$$

Further, in terms of mode 3, the relationship of the current and voltage of the coupled inductor is given by

$$\begin{cases} \left[2L + (L_{3p} - M)\right] \dfrac{di_p}{dt} + M \dfrac{di_s}{dt} = 0 \\ \dfrac{di_p}{dt} = -\dfrac{(2n+1)V_{\text{in}} - V_o}{2\left(n+1\right)L} \end{cases}. \tag{23}$$

Here, the coupling coefficient of the coupled inductor is K, and the mutual inductance of both primary and secondary sides of T is $M = K \cdot \sqrt{L_{3p} \cdot L_{3s}} = K \cdot n \cdot L_{3p}$.

As a result, the coefficient of i_{Do} during its falling period is given by

$$k_f = \frac{(2n+1)V_{\text{in}} - V_o}{2n\left(n+1\right)L_{\text{eq}}}. \tag{24}$$

According to the waveform of i_{Do} in Fig. 3, its value at t_3 is presented as $i_{Do}(t_3) = k_r t_{\delta 1} + k_f t_{\delta 2}$, so its average value in a whole switching cycle is given by

$$\frac{k_r {t_{\delta 1}}^2 + k_f {t_{\delta 2}}^2}{2T_s} = I_o. \tag{25}$$

It is noted that the absolute value of k_f lowers as L_{eq} increases, which means that the value of i_{Do} is relatively higher at t_3. So the boundary conduction mode happens when i_{Do} is zero by the end of the energy deliver mode. Considering $i_{Do}(t_3) = 0$, (24), and (25), the boundary equivalent inductance is obtained by

$$L_{\text{eq\_BCM}} = \frac{R(1-D)^2 D T_s}{2\left(2n+1+D\right)\left(Kn+1\right)}. \tag{26}$$

Fig. 6 is obtained following (26), which reveals the boundary inductance with different D and n. It also means that when the equivalent inductance of the circuit is higher than L_{eq}_BCM,

the circuit is able to operate under CCM, while if the equivalent inductance is lower than it, the circuit operates under DCM and will have the potential to realize zero voltage switching.

2) Discontinuous Conducting Mode: As shown in Fig. 5, i_{Do} reaches zero at t_5; therefore, the relationship between the two coefficients in (20) is

$$k_r t_{\delta 1} = -k_f \left(t_\delta - t_{\delta 1}\right). \tag{27}$$

Similar to its waveform in CCM, the peak current of i_{DM1} is $i_L(t_3) + i_{L3p}(t_3)$, which is equal to the sum of the current ripples of i_{L1} and i_{L3p} during mode 4. However, because the value of C_Q is much larger than that in continuous mode, t_{r1} in discontinuous mode cannot be neglected in terms of $t_{\delta 1}$. To be specific, the sum of the current ripples of i_{L1} and i_{L3p} during modes 1 and 2 is equal to that during modes 3 and 4, as compared to (21), I_{DM1_peak} in DCM is obtained by

$$I_{\mathrm{DM1\_peak}} = \frac{V_{\mathrm{in}} t_d}{L_{\mathrm{eq}}}\left(1 - \frac{t_{r1}}{t_{\delta 1}}\right). \tag{28}$$

Similarly, since the average current of D_{M1} is equal to I_o, the time of its conducting mode is given by

$$t_{\delta 1} - t_{r1} = \frac{2M_{\mathrm{DCM}} L_{\mathrm{eq}}}{\mathrm{RD}}. \tag{29}$$

As the operating mode 5 of DCM is same as mode 3 in CCM, the coefficient of i_{Do} during its falling period is already given by (24)

Finally, substituting (24), (25), (27), and (29), the equivalent inductance of DCM is achieved by (29). Further, the specific value of $L_{1,2}$ and $L_{3s,p}$ can be designed by combining (12) and (29)

$$L_{\mathrm{eq\_DCM}} = \frac{(n+1)}{\left(Kn + \frac{t_{\delta 1}}{t_{\delta 1} - t_{r1}}\right)} \frac{\mathrm{RD}}{M_{\mathrm{DCM}}^2 - (2n+1) M_{\mathrm{DCM}}} t_d. \tag{30}$$

Apparently, the output voltage of DCM can be seen as a function of many parameters, including the turns ratio, the duty cycle, the frequency, the equivalent inductance, and the load, which is given by

$$M_{\mathrm{DCM}}^2 - (2n+1) M_{\mathrm{DCM}} = \frac{(n+1) RD^2 T_s}{\left(Kn + \frac{t_{\delta 1}}{t_{\delta 1} - t_{r1}}\right) L_{\mathrm{eq}}}. \tag{31}$$

Fig. 7 illustrates the voltage gain M_{DCM} as a function of inductors and the turns ratio of the coupled inductor in the system. According to the figure, we can get that instead of the specific value of each inductor, the voltage gain M_{DCM} is only influenced by their equivalent value, and as a result, the specific value of both $L_{1,2}$ and L_{3p} can correspondingly change. When the equivalent inductance is smaller, the current ripple during its charge or discharge period is relatively larger; consequently, the final output voltage will be higher. The voltage gain also rises with the turns ratio.

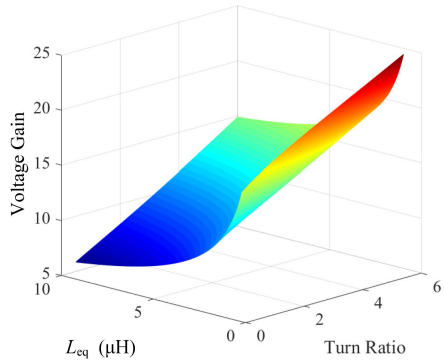

Fig. 7. Voltage gain with different L_{eq} and turns ratio.

C. Resonant Capacitor Design

The additional parallel capacitor C_Q only exists in DCM, so the analysis mentioned later is in terms of the discontinuous operating mode.

First, as t_{r1} is very short, the inductor voltage is considered to fall linearly in this period, which means that C_Q is charged by an approximately constant current, I_{CQ}, in this interval. As a result, the parallel capacitors' charging time t_{r1} is obtained by

$$t_{r1} = \frac{v_{C_Q}(t_3)}{i_{CQ}} \cdot C_Q = \frac{V_{C_M} + v_L(t_3)}{V_{\mathrm{in}} D T_s} \cdot L_{\mathrm{eq}} \cdot C_Q. \tag{32}$$

In terms of the energy deliver mode, the sum of v_{L1} and v_{CQ} is V_{in}. Therefore, according to the relationship between current and voltage of the capacitor, we obtain

$$C_Q \frac{dv_{C_Q}(\tau)}{d\tau} = \int_0^t \frac{V_{\mathrm{in}} - v_{C_Q}(\tau)}{L_{\mathrm{eq}}} d\tau. \tag{33}$$

Here, t represents t_5: $t = \tau - t_5$. And after simplifying, (32) is written as

$$L_{\mathrm{eq}} \cdot C_Q \cdot \frac{d^2 v_{C_Q}(\tau)}{d\tau^2} + v_{C_Q}(\tau) = V_{\mathrm{in}}. \tag{34}$$

After solving this differential equation, we obtain the voltage across C_Q, as a function of time

$$v_{C_Q}(t) = \sqrt{C_1^2 + C_2^2}\cos\left(\frac{t}{\sqrt{L_{eq} C_Q}} + \alpha\right) + V_{\mathrm{in}},\ \tan\alpha = \frac{C_2}{C_1} \tag{35}$$

where C_1 and C_2 are the coefficients to be determined.

According to the waveforms of current and voltage during the resonant period in Fig. 8, the voltage of C_Q reaches its peak when $t = 0$. Moreover, in order to turn ON the body diodes D_Q in the next mode, voltage of C_Q is considered to be –0.7 V by the time this interval ends, so applying the voltage at $t = 0$ and $t = t_{r2}$ into (34), we obtain

$$\begin{cases} u_{C_Q}(0) = V_L + V_{C_M}, & \alpha = 0 \\ u_{C_Q}(t_{r2}) = \dfrac{V_o - (2n+1) V_{\mathrm{in}}}{2(n+1)} \cos\left(\dfrac{t_{r2}}{\sqrt{L_{\mathrm{eq}} C_Q}}\right) \\ \qquad\qquad + V_{\mathrm{in}} = -0.7\mathrm{V} \end{cases} \tag{36}$$

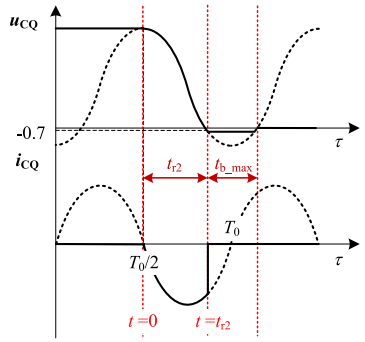

Fig. 8. Waveforms of C_Q during the resonant period.

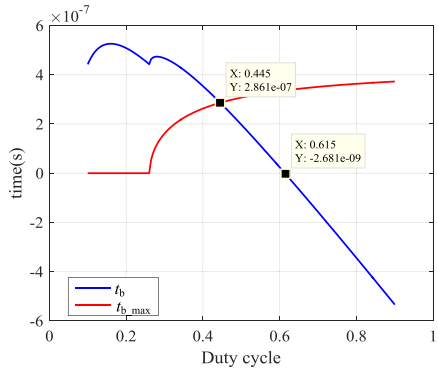

Fig. 9. Duty cycle available range of ZVS.

TABLE I
SPECIFICATIONS AND PARAMETERS OF THE MODIFIED SEPIC CIRCUIT

Electrical specifications	
Input Voltage	12V
Output Voltage	180V
Output Current	300mA
Switching frequency	500kHz
Parameters of main components	
$L_{1,2}$	6.91uH
$L_{3p,s}$	3.88uH / 8.73uH
C_Q	12.9nF
C_M, $C_{s1,2}$	1uF
C_o	10uF
$D_{M1,2}$, D_o	SS320
$Q_{1,2}$	Si7454DDP

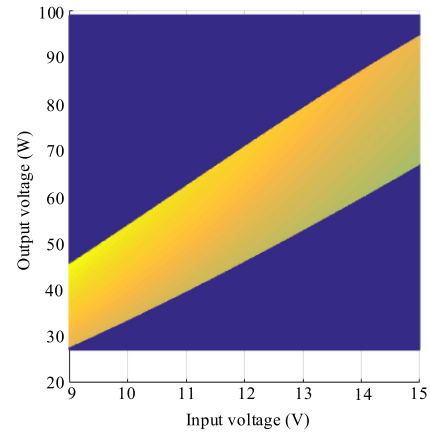

Fig. 10. Input voltage and output power range of ZVS.

Here, T_0 represents the time taken in a whole resonant period, which is given by

$$T_0 = 2\pi\sqrt{L_{\text{eq}}C_Q}. \tag{37}$$

Therefore, substituting (18), (36), and (37), the value of the required resonant capacitor C_Q is obtained by

$$C_Q = \frac{9\Delta - 12\pi\sqrt{\Delta} + 4\pi^2}{9(M+3)^2} \cdot \frac{4t_d^2}{L_{\text{eq}}}. \tag{38}$$

where $\Delta = \frac{4\pi^2}{9} + (3+M)\cdot\frac{1-t_d-t_\delta-t_b}{t_d}$.

According to the aforementioned analysis, a DCM prototype is implemented to realize ZVS and, therefore, reduce the switching loss under a high-frequency application. The design indicators and specific parameters of the circuit are presented in Table I.

If capacitances and inductances in the circuit have already been designed, the time of each mode can be calculated, and as a result, the freewheeling time t_b is obtained by (17). In order to realize soft switching, t_b is required to meet the condition: $0 < t_b < t_{b\_\max}$, where $t_{b\_\max}$ is the maximum freewheeling time for the circuit to realize soft switching and is equal to $T_0 - 2t_{r2}$.

Based on the aforementioned analysis, the value of t_b and $t_{b\_\max}$ with changing duty cycle is shown in Fig. 9. In order to achieve ZVS, t_b and $t_{b\_\max}$ should be larger than zero and the red curve needs to be above the blue curve. When the other parameters are selected according to Table I, the available range of duty cycle is supposed to be $0.445 < D < 0.615$.

Actually, according to (31), the input voltage, the output power, and the duty cycle are mutually conditioned. Based on the parameters in Table I, when the input voltage varies from 9 to 15 V, the output power range of ZVS is shown in Fig. 10. ZVS can be realized when the output power changes in the highlighted area in the middle of the diagram. And the corresponding duty cycle can also be calculated with a fixed output voltage, as shown in Fig. 11.

D. Voltage Stress Analysis

The voltage relationship between each component in the circuit is the same in both continuous and discontinuous modes. When the switches are turned OFF, their voltage stress reaches the peak in the energy deliver mode, as shown in Fig. 5, which is expressed as

$$V_{\text{ds\_}Q1} = V_{C_M} + V_L = \frac{V_{\text{in}} + V_o}{2(n+1)} \tag{39}$$

$$V_{\text{ds\_}Q2} = V_{\text{in}} - V_L = \frac{V_{\text{in}} + V_o}{2(n+1)}. \tag{40}$$

It is noted that the switches' voltage stress is much lower than the output voltage, and it is significantly reduced compared to

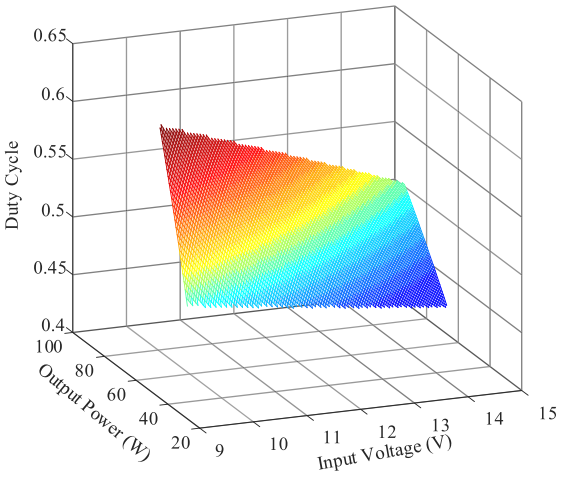

Fig. 11. Duty cycle of ZVS with different input voltage and output power.

TABLE II
VOLTAGE STRESS OF DIFFERENT COMPONENTS

Voltage Stress	proposed	Ref [22]
Q_1, Q_2	$(V_{in}+V_o)/2(n+1)$	$(V_o+3V_{in})/4$
D_{M1}	$(V_o+V_{in})/(n+1)$	$(V_o+3V_{in})/2$
D_{M2}, D_o	$n(V_o+V_{in})/(n+1)$	$(V_o+3V_{in})/2$
C_M	$(V_o-nV_{in})/(n+1)$	$(V_o+V_{in})/2$
C_{S1}	$[V_o-(2n+1)V_{in}]/(n+1)$	$(V_o-V_{in})/2$
C_{S2}	$V_{Cs2}=2n\cdot V_{in}$	-

that of the classical SEPIC converter, whose voltage stress is sum of the input and output voltages.

Similarly, the values of C_M and $C_{s1,2}$ are large enough to maintain their voltage, so they are approximately constant in the whole switching period, which is given by (8)–(10), respectively. The voltage stress of the diodes $D_{M1,2}$ and D_o is presented as

$$V_{D_{M1}} = V_{Cs1} + v_{L3p(\text{mode1})} = \frac{1}{n+1}(V_o + V_{\text{in}}) \tag{41}$$

$$V_{D_{M2}} = V_{Cs2} - v_{L3s(\text{mode4})} = \frac{n}{n+1}(V_{\text{in}} + V_o) \tag{42}$$

$$V_{Do} = V_o - V_{C_M} = \frac{n}{n+1}(V_o + V_{\text{in}})\,. \tag{43}$$

The peak voltage of D_{M1} and D_o is relatively higher, so the higher reverse voltage diodes should be selected according to their voltage stress. The voltage stress of all the components of the proposed converter and the converter in [22] are shown in Table II.

IV. EXPERIMENTAL RESULTS

The proposed SEPIC-based converter was implemented according to the parameters in Table I, and the components used in this system are also presented in the table. Fig. 12 shows the prototype, the PCB area is 6 cm × 5.4 cm, and the power

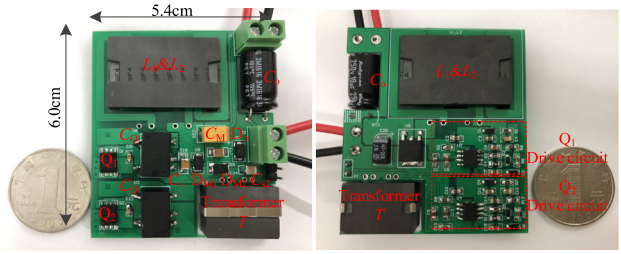

Fig. 12. Prototype.

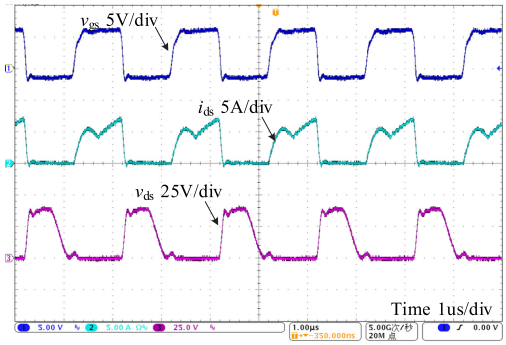

Fig. 13. Drive voltage and voltage stress and current of Q_1.

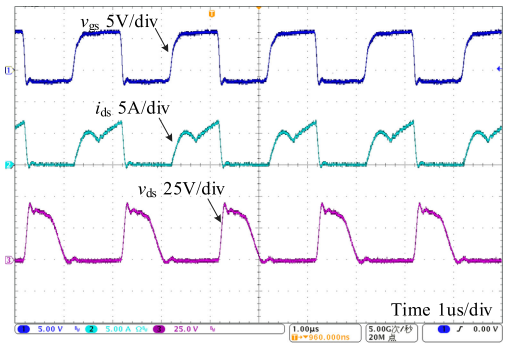

Fig. 14. Drive voltage and voltage stress and current of Q_2.

density is 27.3 W/in^3. The magnetic components adopt the 3F4 planar core of Ferroxcube, and the coupled inductor uses EQ20, L_1 and L_2 use EI32. L_1 and L_2 adopted integrated schemes, which are physically coupled on the same core but magnetically decoupled. The coupled inductor adopted a partly interleaved structure, which can achieve lower parasitic capacitance and leakage inductance at the same time. The integrated scheme and the coupled inductor model are explained in detail in [21].

The voltage and current waveforms of both switches and their driving signals are illustrated in Figs. 13 and 14. As shown in the figure, both two switches achieved zero voltage turn ON since v_{ds} had already fallen to zero before the next driving signal came.

The input and output voltage and current waveforms are shown in Fig. 15. According to this figure, the voltage gain and the output power of the converter can be obtained, and the efficiency can also be calculated with the measured average input current. The output power is 54 W, and the input power is 57.8 W; therefore, the calculated efficiency is 93.4%.

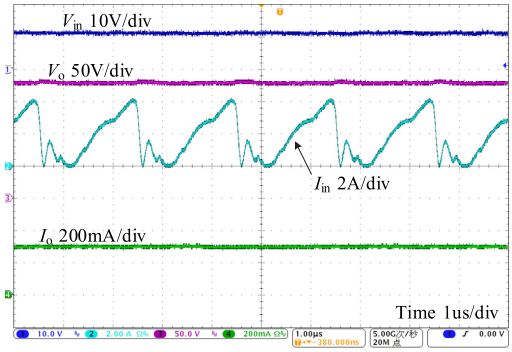

Fig. 15. Input/output voltage and input/output current.

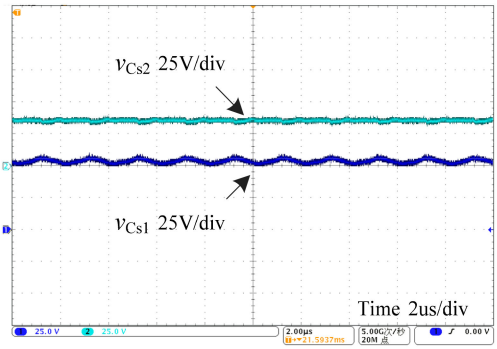

Fig. 16. Voltage stress of C_{s1} and C_{s2}.

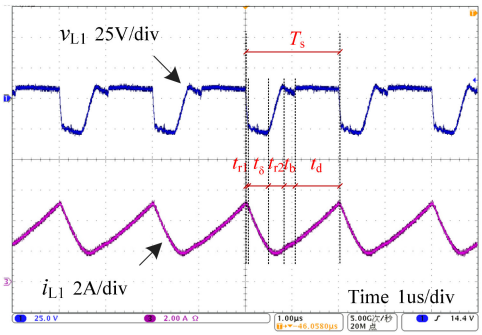

Fig. 17. Voltage and current of L_1.

Fig. 16 shows the voltage stress of C_{s1} and C_{s2} as 52.8 and 36 V, respectively, and the value is consistent with the theoretical calculations.

Waveforms of the voltage stress and the current flowing through the inductors are presented in Fig. 17, which demonstrates the five main working intervals in a switching period.

Moreover, Fig. 18 divides the energy deliver mode into two parts: $t_{\delta 1}$ when i_{Do} is rising, and $t_{\delta 2}$ when i_{Do} is falling. Further, by the time i_{Do} reaches zero, this interval ends and v_{ds} begins to decline as the parallel capacitors C_Q resonant with the inductor.

Fig. 19 shows the waveforms of the output voltage, the output current, and the duty cycle. According to the former analysis, voltage gain of the proposed converter is determined by the parameters of the converter and the duty cycle. Once the parameters of the converter are determined, as given in Table I and according

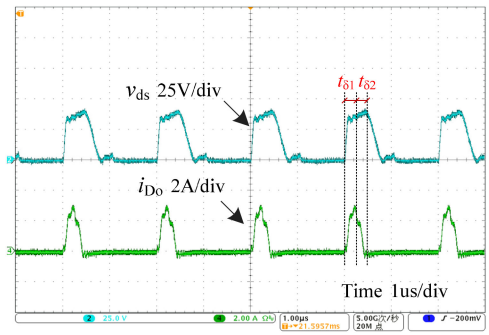

Fig. 18. Drain-source voltage of Q_1 and current flowing through D_o.

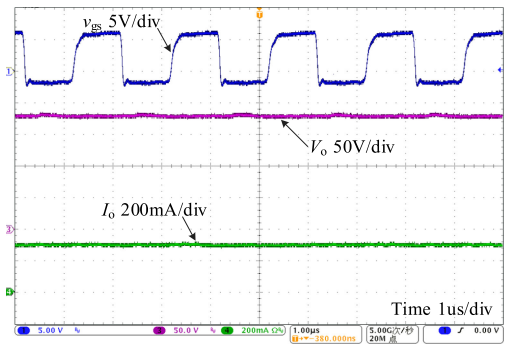

Fig. 19. Waveforms of output voltage, output current and the duty cycle.

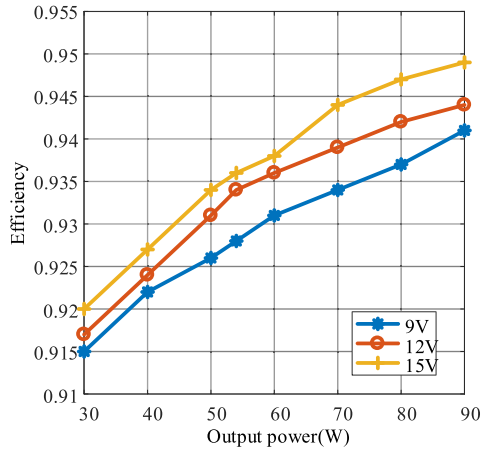

Fig. 20. System efficiency with changing loads.

to (29) and (32), the voltage can be calculated according to (31). With the designed parameters and 0.5 duty cycle, the voltage gain is 15, which is in accordance with Fig. 19.

Fig. 20 shows the efficiency curve with different input voltage and output power. As can be seen from the figure, when the output power changes from 30 to 90 W, the efficiency of the system increases gradually, it also increases with higher input voltage, and the efficiency is up to 93.4% with normal input voltage at rated power. Compared with the converter in [22], the proposed converter achieves soft switching and increases the efficiency with higher switching frequency.

TABLE III
COMPARISON OF THE PROPOSED CONVERTER WITH CURRENT SOLUTIONS

Symbol	Switching frequency	Power level	Efficiency
Proposed	500kHz	54 W	93.4%
CLCL [24]	1 MHz	25 W	90.9%
Buck [25]	1MHz	37.5 W	85%
SEPIC [26]	2 MHz	10 W	88.2%
LLC [27]	5 MHz	100 W	91.28%

Table III compares the proposed converter with some current solutions in terms of switching frequency, power level, and efficiency. As shown in the table, the efficiency of the proposed converter is also comparable among high-frequency converters.

V. CONCLUSION

In this article, a novel DCM soft-switched SEPIC-based high-frequency converter is proposed with the advantages of high voltage gain and low voltage stress. With the integration of some components, the intrinsic characteristics of the classical SEPIC converter are changed, and better properties are obtained. The working principle and the design process of both CCM and DCM are introduced, but DCM is more suitable for high-frequency applications because of ZVS. The experimental results of the proposed 500-kHz 54-W DCM converter corresponded well with the theoretical analysis, and the voltage gain is 15 with 0.5 duty cycle. The system achieved a high efficiency (93.4%) at full load.

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