A High Step-Up Nonisolated DC–DC Converter With Flexible Voltage Gain

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***Abstract*—In this article, a high step-up nonisolated dc–dc converter is proposed to provide high voltage gain with low voltage stress on semiconductors. The main feature of the proposed structure is its flexibility in providing constant output voltages with a reasonable range of voltage stress. This flexibility of the voltage gain is achieved by different combinations of duty cycles. Also, this feature improves the efficiency of the proposed converter. The structure consists of three switches, two inductors, three capacitors, and four diodes. In this article, descriptions of continuous conduction mode, discontinuous conduction mode, boundary condition mode, nonideal model, and control method are presented. Comparisons between the proposed converter and other related structures show that in this converter, the voltage gain is improved and semiconductors voltage stresses are reduced. In order to verify the mathematical analysis, a 500-W laboratory prototype of the proposed converter is built and its experimental results are investigated completely.**

***Index Terms*—Active switched inductor (A-SL), high step-up converter, nonisolated dc–dc converters, switched capacitor (SC) cell.**

I. Introduction

EXCESSIVE consumption of fossil fuels to produce electricity has caused the emission of greenhouse gasses which has serious environmental issues. Renewable energy sources such as solar power [single photovoltaic (PV) modules] and fuel cells can be considered as an alternative solution to decrease these emissions. The problem, however, is that these sources generate low voltage levels and require a power electronic converter to use in the industry [1]–[3]. In order to feed the ac network or inverter, a voltage level of 200–400 V or more is required. PV or battery cells can be connected in series or preferably in parallel connection to prevent the voltage imbalance phenomena between the cells. However, with the parallel connection, the voltage level is low, and dc–dc converters are needed to increase the voltage level [4].

However, power switches, rectifier diodes, and the equivalent series resistance (ESR) of inductors and capacitors affect the voltage gain, also there is a serious problem of reverse recovery in extremely high duty cycles [5], [6]. In PV or fuel cells, not only is a high voltage gain needed, but also a regulated output voltage is required to connect the ac network [7], [8].

DC–DC converters have different categories which are reviewed in [9]–[11].

Nonisolated high step-up dc–dc converters are one of the main categories of dc–dc converters. This type of dc–dc converters is also divided into two generic categories—coupled inductor and noncoupled inductor. Nonisolated converters without coupled inductors have simple structures, low cost, low weight, and are often suitable for low-power applications [12], [15]–[19], and [20]. In [12] and [15], by utilizing a multistage diode-capacitor (MSDC) and active switched inductor (A-SL) network, high voltage gain is provided with low voltage stress across the power semiconductors. Also, a high step-up quasi-Z-source converter is presented in [13]. Similar to [12] and [15], this converter is capable of providing high voltage gain with low voltage stress. However, in this structure, the duty cycle is limited ($d \leq 0.5$).

In several new structures, a combination of different techniques is utilized to provide high voltage gain by nonisolated dc–dc converters [12], [15], [16]–[20]. In [16] and [17], a combination of A-SL network and switched capacitor (SC) cell provides high voltage gain. In this structure, although semiconductors act under hard switching conditions, the power efficiency is acceptable. However, the power diodes maintain high voltage stresses, which is a weakness for this structure. In terms of voltage gain and voltage stress, [17] is similar to [12]. The difference is that in [12], the MSDC cell and A-SL network are used to increase the voltage gain while the structure [16] utilizes SC cell and A-SL network approaches. In [18] is presented another structure which benefits from a combination of two methods for providing high voltage gain. In this structure, a combination of A-SL network and energized inductors acts as voltage step-up section. In this structure, one of the power switches should withstand the entire output voltage. Therefore, increasing the output voltage increases the related losses to this switch. In addition, using different combinations of duty cycles is a new and efficient method to reach high voltage gain in nonisolated dc–dc converters [19]–[22]. These structures are improved structures based on [18] which are capable of

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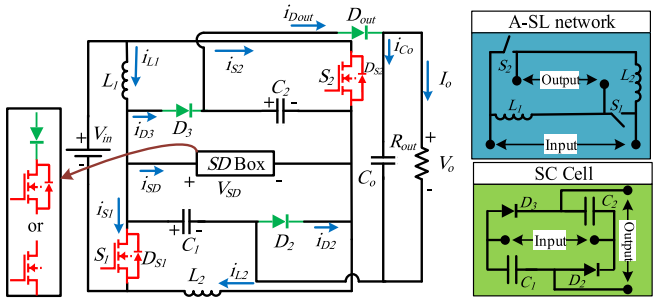

Fig. 1. Schematic of the proposed converter, SD box, SC cell, and A-SL network.

generating high voltage gain with different combinations of duty cycles. Although, these structures benefit from an efficient way to achieve high voltage gain, they suffer from high voltage stress across the semiconductors, which is their main drawback.

In [23] and [24], two nonisolated extendable structures are presented. In these structures, in addition to providing high voltage gain, the low output voltage ripple and low RMS currents of switches are provided. However, there are a lot of components in these structures. Therefore, these structures suffer from complexity and high cost.

In the proposed structure, SC cell and A-SL network are utilized to increase the voltage gain and clamp the voltage stress across the power semiconductors. In this structure, high voltage gain is achieved without utilizing coupled inductors and transformers. The main feature of the proposed converter is its flexibility in achieving a constant voltage gain by different combinations of duty cycles. Also, an improved control method is introduced to control the output voltage.

This article is organized as follows. In Section II, the proposed structure and steady-state analysis is described. In this section, continuous conduction mode (CCM), discontinuous conduction mode (DCM), and boundary condition mode (BCM) operations are investigated. The design considerations of the proposed converter are presented in Section III. In order to analyze the voltage gain and efficiency, the nonideal model of the proposed converter is presented in Section IV. The control method of the proposed converter is introduced in Section V. Also, the comparison results are presented in Section VI. In order to verify the theoretical analysis, a laboratory prototype of the presented converter is built and its experimental results are discussed in Section VII. Finally, in Section VIII, the overall conclusion of this article is presented.

II. Description of Proposed Structure and Steady-State Analysis

The schematic of the proposed converter is illustrated in Fig. 1. This converter contains an A-SL network with two inductors (L_1 and L_2) and two switches (S_1 and S_2). The flow of switch-diode (SD) box is unidirectional. Therefore, it can be expressed in two ways, which are presented in this figure. An SC cell is also used to increase the voltage gain and decrease the voltage stress on the switches. The SC cell consists of two diodes (D_2 and D_3) and two capacitors (C_1 and C_2). The switching frequency is denoted by f_s. The duty cycles of the switches S_1 and S_2 are denoted by d_1. Also, the duty cycle of the switch S_3 is indicated by d_2. In addition, it should be noticed that the summation of the duty cycles d_1 and d_2 should not exceed 1 ($d_1 + d_2 \leq 1$).

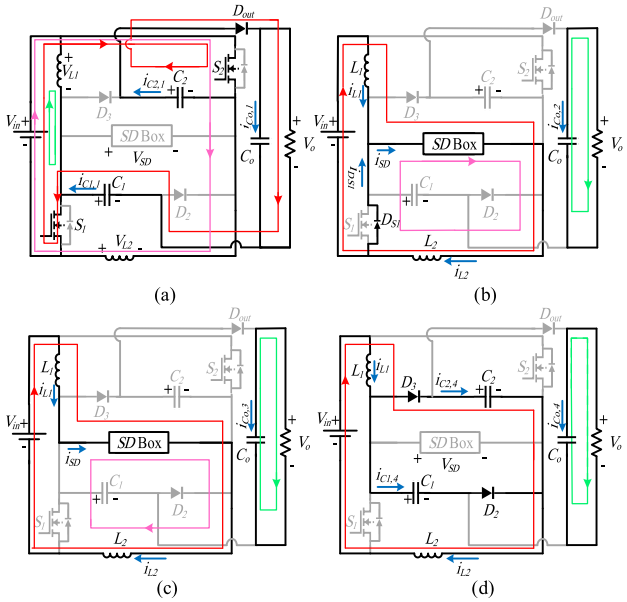

Fig. 2. Equivalent circuits in different operational modes: (a) mode 1; (b) mode 2; (c) mode 3; and (d) mode 4.

In this section, the detailed analysis of the proposed converter under CCM, DCM, and BCM is presented. In the following analysis, the following assumptions are considered.

1) The parasitic elements are neglected.
2) M_1 and M_2 are equal to $L_1/(L_1 + L_2)$ and $L_2/(L_1 + L_2)$, respectively.
3) The capacitors are large enough. Therefore, the capacitors' voltages are constant.
4) The input voltage (V_{in}) is constant.

A. CCM Operation

In the CCM operation, the proposed converter has four operational modes which can be described as follows.

Mode 1: In this mode, the switches S_1, S_2, and the diode D_{out} are in ON state. The input voltage is parallel with the inductors L_1 and L_2. Therefore, it energizes these inductors. Also, the capacitors C_1 and C_2 discharge in C_o. Fig. 2(a) shows the equivalent circuit of the proposed converter. By applying KVL and KCL, the current and voltage relations are obtained as

$$V_{\text{in}} = V_{L1} = L_1 di_{L1}/dt \tag{1}$$

$$V_{\text{in}} = V_{L2} = L_2 di_{L2}/dt \tag{2}$$

$$V_o = V_{\text{in}} + V_{C1} + V_{C2} \tag{3}$$

$$V_{SD} = -V_{\text{in}} \tag{4}$$

$$i_{C1,1} = i_{C2,1} = i_{Co,1} + I_o \tag{5}$$

$$i_{S1} = i_{S2} = i_{L1} + i_{C1,1} = i_{L2} + i_{C2,1} \tag{6}$$

$$I_{\text{in}} = i_{L1} + i_{L2} + i_{C1,1}. \tag{7}$$

In the relations (1) and (2), the inductors' currents are equal if the value of L_1 and L_2 are equal. Furthermore, if $L_1 \geq L_2$ or $L_1 \leq L_2$, it can be concluded that $di_{L2} \geq di_{L1}$ or $di_{L1} \geq di_{L2}$, respectively. Also, (4) represents that the *SD* box consists of unidirectional components such as one IGBT or a series diode with MOSFET.

Mode 2: This mode happens when the inductor values are different. Fig. 2(b) depicts the equivalent circuit of the proposed converter for $L_1 \geq L_2$. In this mode, the switch S_3 is in ON state and the switches S_1 and S_2 are in OFF state. Therefore, the following relations can be written:

$$V_{\text{in}} = V_{L1} \tag{8}$$

$$V_{L2} = 0 \tag{9}$$

$$i_{Co,2} = -I_o \tag{10}$$

$$i_{DS1} + i_{L1} = i_{L2}. \tag{11}$$

The current values of inductors in the start of this mode can be expressed as follows:

$$i_{L1}(0) = V_{\text{in}} d_1 T_s / L_1 \ , \ i_{L2}(0) = V_{\text{in}} d_1 T_s / L_2. \tag{12}$$

Here, $i_{L2} \geq i_{L1}$, by substituting (12) in (11), it can be derived as

$$i_{DS1} = i_{L2} - i_{L1} = V_{\text{in}} d_1 T_s \left(L_2^{-1} - L_1^{-1}\right). \tag{13}$$

Considering (13), mode 2 is removed if $L_1 = L_2$. On the other hand, if it is assumed that $L_2 \geq L_1$, $i_{L1} \geq i_{L2}$. In this condition, the reverse diode of S_2 (D_{S2}) is turned ON and the voltage across L_1 is equal to zero ($V_{L1} = 0$) and L_2 is charged by input voltage ($V_{L2} = V_{\text{in}}$).

Mode 3: Fig. 2(c) shows the equivalent circuit of the proposed structure in the third operational mode. At the beginning of this mode, the currents of inductors L_1 and L_2 are equal and the switch S_3 is in ON state. Also, the input voltage is in series with the inductors L_1 and L_2. The current and voltage relations can be written as follows:

$$V_{L1} = M_1 V_{\text{in}} \tag{14}$$

$$V_{L2} = M_2 V_{\text{in}} \tag{15}$$

$$i_{Co,3} = -I_o \tag{16}$$

$$I_{\text{in}} = i_{L1} = i_{L2}. \tag{17}$$

Mode 4: Fig. 2(d) illustrates the equivalent circuit of the proposed converter in this mode. The diodes D_2 and D_3 are in ON state and the inductors L_1 and L_2 get discharged. Also, the capacitors C_1 and C_2 get charged. The voltage and current equations can be written as follows:

$$V_{L1} = M_1(V_{\text{in}} - V_{C1}) \tag{18}$$

$$V_{L2} = M_2(V_{\text{in}} - V_{C1}) \tag{19}$$

$$V_{SD} = V_{C1} = V_{C2} \tag{20}$$

$$I_{\text{in}} = i_{L1} = i_{L2} \tag{21}$$

$$i_{L1} = i_{L2} = i_{C1,4} + i_{C2,4} \tag{22}$$

$$i_{Co,4} = -I_o. \tag{23}$$

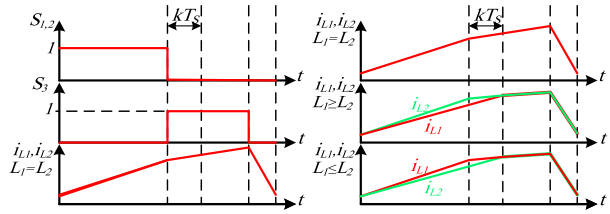

Fig. 3. Switching pattern and inductors current for different values of $L_{1,2}$.

Fig. 3 illustrates the inductors' currents for different values of the inductors.

1) Voltage Gain Calculation in the CCM Operation: In this section, the voltage gain of the proposed converter is calculated for different inductor values as follows.

a) $L_1 = L_2$*:* Considering this condition, as it resulted in the last section, the second mode is removed. Therefore, by applying the volt–second balance principle for the inductors, it can be written

$$\begin{aligned} L_1 &: V_{\text{in}} d_1 T_s + 0.5 V_{\text{in}} d_2 T_s \\ &\quad + 0.5 \left(V_{\text{in}} - V_{C1}\right)\left(1 - d_1 - d_2\right) T_s = 0 \\ L_2 &: V_{\text{in}} d_1 T_s + 0.5 V_{\text{in}} d_2 T_s \\ &\quad + 0.5 \left(V_{\text{in}} - V_{C1}\right)\left(1 - d_1 - d_2\right) T_s = 0. \end{aligned} \tag{24}$$

Considering (24), the voltage of the capacitor C_1 is obtained as

$$V_{C1} = \left(1 + d_1\right) V_{\text{in}} / \left(1 - d_1 - d_2\right). \tag{25}$$

Considering (3), (20), and (25), the output voltage of the proposed converter can be expressed as follows:

$$V_o = 2V_{C1} + V_{\text{in}} \tag{26}$$

$$G_{\text{CCM}} = V_o / V_{\text{in}} = \left(3 + d_1 - d_2\right) / \left(1 - d_1 - d_2\right). \tag{27}$$

b) $L_1 \geq L_2$*:* As it is shown, when $L_1 \geq L_2$, the difference between the inductors' currents creates the second mode. Therefore, the volt–second balance principle for these inductors is written as

$$\begin{aligned} L_1 &: V_{\text{in}} d_1 T_s + V_{\text{in}} k T_s + M_1 V_{\text{in}} \left(d_2 - k\right) T_s \\ &\quad + M_1 \left(V_{\text{in}} - V_{C1}\right)\left(1 - d_1 - d_2\right) T_s = 0 \\ L_2 &: V_{\text{in}} d_1 T_s + 0 k T_s + M_2 V_{\text{in}} \left(d_2 - k\right) T_s \\ &\quad + M_2 \left(V_{\text{in}} - V_{C1}\right)\left(1 - d_1 - d_2\right) T_s = 0. \end{aligned} \tag{28}$$

By simplifying (28), the coefficient k can be achieved as

$$k = d_1(L_1 - L_2)/L_1. \tag{29}$$

When the inductors values are equal, the coefficient k is zero and the second mode is deleted, as mentioned.

By substituting (29) in (28), the values of capacitors (C_1 and C_2) and the output voltage are achieved as mentioned in (25) and (27), respectively.

TABLE I
VOLTAGE AND CURRENT STRESS ACROSS THE POWER SWITCHES AND DIODES AT CCM

Dev.	Mode 1	Mode 2	Mode 3	Mode 4
$S_{1,2}$	$\frac{(1+d_1-d_2)I_o}{(1-d_1-d_2)d_1}$	$\frac{V_{in}}{2}$	$\frac{(2-d_2)V_{in}}{2(1-d_1-d_2)}$	$\frac{(2-d_2)V_{in}}{2(1-d_1-d_2)}$
SD box	$-V_{in}$	$\frac{2I_o}{1-d_1-d_2}$	$\frac{(1+d_1)V_{in}}{1-d_1-d_2}$	$\frac{(1+d_1)V_{in}}{1-d_1-d_2}$
$D_{2,3}$	$\frac{-(2-d_2)V_{in}}{1-d_1-d_2}$	$\frac{-(1+d_1)V_{in}}{1-d_1-d_2}$	$\frac{I_o}{1-d_1-d_2}$	$\frac{I_o}{1-d_1-d_2}$
D_{out}	$\frac{I_o}{d_1}$	$-V_{in}$	$\frac{-(2-d_2)V_{in}}{1-d_1-d_2}$	$\frac{-(2-d_2)V_{in}}{1-d_1-d_2}$

c) $L_1 \leq L_2$: Like in the previous section, it can be written

$$\begin{aligned} L_1 &: V_{\text{in}} d_1 T_s + 0 k T_s + M_1 V_{\text{in}} (d_2 - k) T_s \\ &\quad + M_1 (V_{\text{in}} - V_{C1}) (1 - d_1 - d_2) T_s = 0 \\ L_2 &: V_{\text{in}} d_1 T_s + V_{\text{in}} k T_s + M_2 V_{\text{in}} (d_2 - k) T_s \\ &\quad + M_2 (V_{\text{in}} - V_{C1}) (1 - d_1 - d_2) T_s = 0. \end{aligned} \tag{30}$$

The values of V_o and k are calculated as (27) and (29), respectively.

2) Current Gain Calculation: By applying the current–second balance principle for the capacitors C_1, C_2, and C_o, the current equations are obtained as

$$i_{Co,1} = ((1 - d_1) I_o) / d_1 \tag{31}$$

$$i_{C1,1} = i_{C2,1} = I_o / d_1 \tag{32}$$

$$i_{L1} = i_{L2} = 2 I_o / (1 - d_1 - d_2). \tag{33}$$

In the fourth operational mode, considering (22) and (33), the currents of the capacitors C_1 and C_2 can be achieved as

$$i_{C1,4} = i_{C2,4} = i_{L1}/2 = I_o / (1 - d_1 - d_2). \tag{34}$$

Therefore, the input current is calculated as follows:

$$I_{\text{in}} = (i_{L1} + i_{L2} - i_{C1,1}) d_1 + i_{L1} d_2 + i_{L1} (1 - d_1 - d_2). \tag{35}$$

Using (33)–(35), the current gain can be achieved as

$$I_o = (1 - d_1 - d_2) I_{\text{in}} / (3 + d_1 - d_2). \tag{36}$$

3) Voltage and Current Stress on the Switches and Diodes: Considering the obtained current and voltage equations, the voltage and current stress on the power switches and diodes can be expressed as Table I (it is assumed that $L_1 = L_2$).

B. DCM Operation

In the DCM operation, the proposed converter has four operational modes (it is assumed that $L_1 = L_2$). The first and second operational modes are similar to the CCM operation. In the third operational mode, the inductors' currents reach zero (d_3). In the fourth operational mode, all the switches and diodes are in OFF state and the inductors' currents are equal to zero.

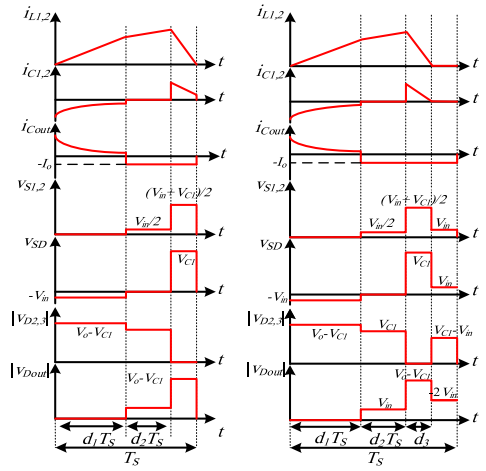

Fig. 4. Main waveforms of the proposed converter in CCM/DCM.

Therefore, in DCM operation, this relation can be written as

$$V_{\text{in}} d_1 + (V_{\text{in}}/2) d_2 + ((V_{\text{in}} - V_{c1})/2) d_3 = 0. \tag{37}$$

In DCM operation, the maximum current of the inductors is equal to the ripple of inductors; therefore, this can be achieved as

$$I_{L1,\text{peak}} = V_{\text{in}} (2d_1 + d_2) / 2 L f_s = d_3 (V_{c1} - V_{\text{in}}) / 2 L f_s. \tag{38}$$

Considering (37) and (38), d_3 is achieved as

$$d_3 = V_{\text{in}} (2d_1 + d_2) / (V_{c1} - V_{\text{in}}). \tag{39}$$

By applying ampere–second principle for C_1, the following can be written:

$$I_o = (I_{L1} d_3)/2. \tag{40}$$

By assuming ($I_L = I_{L,\text{peak}}/2$) and considering (37)–(40), the voltage gain of the proposed converter can be achieved as follows:

$$G_{\text{DCM}} = 1.5 \left[1 + \sqrt{1 + (D^2/9\tau_{\text{DCM}})}\right] \tag{41}$$

where D and τ_{DCM} can be expressed as (42) and (43), respectively, in the following:

$$D = 2d_1 + d_2 \tag{42}$$

$$\tau_{\text{DCM}} = L f_s / R_o. \tag{43}$$

Using the obtained relations, the main voltage and current waveforms can be plotted as Fig. 4.

C. BCM Operation

In this section, in order to calculate τ_{BCM}, it is assumed that the voltage gains of the proposed converter in CCM and DCM operations are similar. Therefore, τ_{BCM} can be obtained as

$$\tau_{\text{BCM}} = \left(2D^2\right) / 9 \left[((2G_{\text{CCM}}/3) - 1)^2 - 1\right]. \tag{44}$$

Fig. 5 illustrates τ_{BCM} versus d_1 based on four different values of d_2. Also, the CCM and DCM regions are shown based on each value of d_2. As it can be seen, the increase in duty cycle d_2 expands the CCM region of the proposed converter.

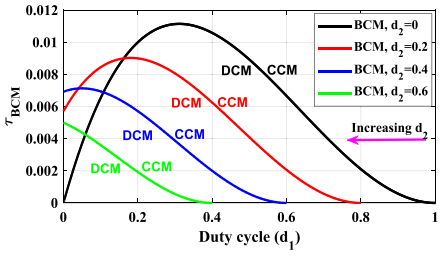

Fig. 5. Proposed converter's boundary conditions (for each of the d_2 values, the DCM regions are below the curves).

III. Parameter Design

A. Inductor Design

The inductor current ripples in the operational modes can be achieved as follows:

$$\Delta {i_L}^{\mathrm{I}} = V_{\mathrm{in}} d_1 / L_1 f_s \tag{45}$$

$$\Delta {i_L}^{\mathrm{II}} = V_{\mathrm{in}} d_2 / 2 L_1 f_s \tag{46}$$

$$\Delta {i_L}^{\mathrm{III}} = \left(V_{\mathrm{in}} - V_{c1}\right)\left(1 - d_1 - d_2\right) / L_1 f_s. \tag{47}$$

Signs I– III show modes 1, 2–3, and 4, respectively. In modes 1–3, the inductors are charged and the inductors are discharged in mode 4. Therefore, it can be written as follows:

$$\Delta {i_L}^{\mathrm{I}} + \Delta {i_L}^{\mathrm{II}} = \left|\Delta {i_L}^{\mathrm{III}}\right|. \tag{48}$$

In the fourth operational mode, the inductor voltage relations can be written as follows:

$$V_{L1} = V_{L2} = V_{\mathrm{in}} - V_{c1} = \left(L_1 \Delta {i_L}^{\mathrm{III}}\right) / \left(\left(1 - d_1 - d_2\right) T_s\right). \tag{49}$$

$\Delta i_L^{\mathrm{III}}$ indicates the inductor current ripple in the fourth operational mode. Therefore, the inductors' values can be calculated as follows:

$$L_1 = L_2 = V_{\mathrm{in}}\left(2d_1 + d_2\right) / 2 \Delta i_{L1} f_s. \tag{50}$$

In order to provide the required conditions for the proposed converter to operate in the CCM condition, the inductor currents should be more than half of their current ripples ($2i_L \geq \Delta i_L$). Therefore, the following can be written:

$$L_{1,2} \geq \left(V_{\mathrm{in}}^2 \left(2d_1 + d_2\right)\left(3 + d_1 - d_2\right) / 2 f_s P_o\right). \tag{51}$$

B. Capacitor Design

Considering (31) and (32), the following can be obtained:

$$C_1 = C_2 = I_o / f_s \Delta v_{c1} \tag{52}$$

$$C_o = \left(1 - d_1\right) V_o / f_s \Delta v_{Co} R_o. \tag{53}$$

In addition, the output voltage ripple can be achieved as

$$\%\left(\Delta v_{Co} / V_o\right) = \left(\left(1 - d_1\right) / C_o f_s R_o\right) \times 100\% \tag{54}$$

where Δv_C is the capacitors' voltage ripple.

C. S_1 and S_2 Design

Considering Tables I and III, the voltage stress across the power switches $S_{1,2}$ and S_2 are equal to 110 V. As a result, IRFB4228PbF with $V_{\mathrm{DSmin}} = 150$ V are chosen for these switches.

D. D_1, D_2, and D_{out} Design

Considering Tables I and III, the maximum voltage stress across the power diodes is equal to 220 V. Therefore, SBR10U300CT with $V_{\mathrm{RRM}} = 300$ V (maximum repetitive reverse voltage) are selected.

E. SD Box Design

If SD box is implemented with one IGBT and considering Tables I and III, the maximum voltage of S_3 in mode 3 is equal to 200 V. Therefore, one IGBT with $V_{\mathrm{DSmin}} = 250$ V, can be selected. On the other hand, if MOSFET and series diode are used, in mode 1, the following can be written:

$$V_{SD} = V_{D1} + V_{S3\max} = -V_{\mathrm{in}}. \tag{55}$$

As a result, diode D_1 must withstand 220 V. In this article, MOSFET IRFB4229PbF with $V_{\mathrm{DSmin}} = 250$ V and diode SBR30U300CT with $V_{\mathrm{RRM}} = 300$ V are chosen.

IV. Nonideal Model in CCM Operation

In the ideal model of dc–dc converters, it is assumed that the input power is equal to the output power. Therefore, ideal dc–dc converters are assumed as an ideal dc transformer. In reality, a dc converter consists of nonideal components. In this section, the internal resistances of the power switches, power diodes, inductors, and capacitors are denoted by $r_{S1} = r_{S2}, r_{S3}$, r_{D1}, $r_{D2} = r_{D3} = r_{D\mathrm{out}} = r_D$, $r_{L1} = r_{L2} = r_L$, and $r_{C1} = r_{C2} = r_{C\mathrm{o}} = r_C$, respectively. Also, the power diodes' forward voltages are denoted by V_{F1} and $V_{F2} = V_{F3} = V_{F\mathrm{out}} = V_F$.

A. Nonideal Components' Influence on Voltage Gain

By considering the influence of the parasitic elements, the output voltage can be obtained as follows:

$$V_o = \frac{\left(3 + d_1 - d_2\right) V_{\mathrm{in}} - 2V_{F1} d_2 - 3V_F\left(1 - d_1 - d_2\right)}{\left(1 - d_1 - d_2\right)\left(1 + \left(R_{\mathrm{eq}} / R_o\right)\right)}. \tag{56}$$

In (56), R_{eq} can be written as follows:

$$R_{\mathrm{eq}} = r_L D'_L + r_c D'_C + r_S D'_{S1} + r_{S3} D'_{S3} + r_{D1} D'_{D1} + r_D D'_{D2} \tag{57}$$

where D'_L, D'_C, D'_{S1}, D'_{S3}, D'_{D1}, and D'_{D2} can be achieved as

$$D'_L = \frac{8}{\left(1 - d_1 - d_2\right)^2} \quad D'_C = \frac{3 - d_1 - 3d_2}{d_1\left(1 - d_1 - d_2\right)}$$

$$D'_{S1} = \frac{2\left(1 + d_1 - d_2\right)^2}{d_1\left(1 - d_1 - d_2\right)^2}$$

$$D'_{S3} = \frac{4d_2}{\left(1 - d_1 - d_2\right)^2} \quad D'_{D1} = \frac{4d_2}{\left(1 - d_1 - d_2\right)^2}$$

$$D'_{D2} = \frac{1 + d_1 - d_2}{d_1\left(1 - d_1 - d_2\right)}. \tag{58}$$

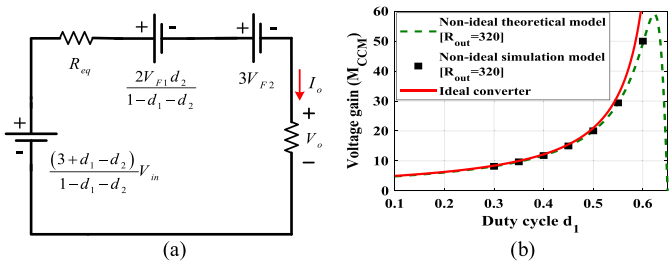

Fig. 6. Nonideal model of the (a) proposed converter and (b) simulation and theoretical voltage gain compared with ideal voltage gain.

Therefore, by considering the preceding relations, the nonideal model of the proposed converter is achieved and the simplified schematic of this model is illustrated in Fig. 6(a). The influence of the nonideal components on the voltage gain is investigated in Fig. 6(b). In this figure, the theoretical and simulation voltage gain curves of the nonideal model at 320 Ω output resistance are compared with the ideal voltage gain.

B. Nonideal Components' Influence on Efficiency

The components' resistance and the diodes' voltage drop losses can be calculated from the nonideal model as follows:

$$P_1 = \frac{2V_{F1}d_2}{1-d_1-d_2}I_o + 3V_F I_o + R_{\text{eq}} I_o^2. \tag{59}$$

According to [6], the switching losses can be expressed as

$$P_{sw} = \sum_{i=1}^{3} \left(P_{\text{Switching}[t_{\text{on}},t_{\text{off}}],i} + P_{\text{Coss}_i}\right). \tag{60}$$

$P_{\text{Switching [ton, toff]}}$ and P_{Coss} are equal to (59) and (60)

$$P_{\text{Switching}[t_{\text{on}},t_{\text{off}}],i} = 0.5 f_s \left(t_{fi} + t_{ri}\right) i_{av,si} V_{si}^2 \tag{61}$$

$$P_{\text{Coss},i} = 0.5 f_s C_{\text{oss}j} v_{si}^2. \tag{62}$$

As can be seen, the switching losses are related to turn OFF (t_{off}), turn ON (t_{on}), switching frequency (f_s), switch average current ($i_{av,s}$), voltage stress across power switch (V_s), and output capacitance (C_{oss}) of the power switches.

In this converter, utilized cores are *EE32* and based on its datasheet, the core losses at 46 kHz are 1.1 W for each core [23]. As a result, the following relation can be achieved:

$$P_{\text{Core}} = 2 \times (1.1) = 2.2\,\text{W}. \tag{63}$$

Therefore, the total losses can be achieved as follows:

$$P_{\text{loss}} = P_1 + P_{sw} + P_{\text{Core}}. \tag{64}$$

Hence, the theoretical efficiency can be calculated as follows:

$$\eta = 1/\left(1 + \left(P_{\text{loss}}/R_o I^2{}_o\right)\right). \tag{65}$$

V. Dynamic Model and Control Method

In order to control the proposed structure, there are three ways: 1) control d_1 when d_2 is fixed; 2) control d_2 when d_1 is fixed; and 3) control d_1 and d_2, simultaneously. The first and second control methods are simple and similar to the conventional boost converter, but the third method is a new method to achieve MPPT (maximum power point tracking) or constant output voltage in a package and users can select one of them. In this article, the third method is investigated.

The dynamic model can be described as

$$\dot{x} = Ax + Bu \quad y = Cx + Du \tag{66}$$

where x is the state-space vector matrix ($n \times 1$), y is the output vector matrix($n \times 1$), u is the input vector matrix, and n is the number of state-space variables.

In this method, it is possible to control the inductors' currents by the duty cycle of $S_{1,2}$ (d_1) or the output voltage can be controlled by the duty cycle of S_3 (d_2). The proposed converter has five storage elements. However, $i_{L1,2}$ and $v_{C1,2}$ have similar conditions (when $L_1 = L_2$ and $C_1 = C_2$). Also, the output voltage (v_{co}) depends on the capacitors' voltages (v_{C1}, v_{C2}) and input voltage. Therefore, the inductor's current (i_{L1}) and the capacitor's voltage (v_{C1}) are assumed as independent state-space variable vectors. Consequently, the state-space averaging method can be written as

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{v}_{C1} \end{bmatrix} = \begin{bmatrix} 0 & (d_1+d_2-1)/2L_1 \\ (1-d_1-d_2)/2C_1 & -2/R_oC_1 \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \end{bmatrix} + \begin{bmatrix} (1+d_1)/2L_1 \\ -1/R_oC_1 \end{bmatrix} [V_{\text{in}}]$$

$$\begin{bmatrix} i_{L1} \\ v_{C1} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [V_{\text{in}}]. \tag{67}$$

Every electrical signal includes two ac and dc parts [26]. As a result, this equation can be written as follows:

$$\dot{x} = \bar{X} + \tilde{x} \quad y = \bar{Y} + \tilde{y} \quad d = \bar{D} + \tilde{d} \quad u = \bar{U} + \tilde{u} \tag{68}$$

where $\bar{X}, \bar{Y}, \bar{U}$, and $\bar{D}$ are the equilibrium dc components. Also, $\tilde{x}, \tilde{y}, \tilde{u}$, and $\tilde{d}$ are small ac variations. In the equations above, $\overline{X} \gg \tilde{x}, \overline{Y} \gg \tilde{y}, \overline{U} \gg \tilde{u}$, and $\overline{D} \gg \tilde{d}$. Therefore, the new dynamic model can be rewritten as follows:

$$\tilde{x} = A'\tilde{x} + B'\tilde{u} + E'\tilde{d}, \;\; \tilde{y} = C'\tilde{x} + D'\tilde{u} + F'\tilde{d}\,. \tag{69}$$

In order to obtain the small signal models from the channel duty-cycle perturbation to the state variables, the input of the circuit is short circuited; thus, $\tilde{u} = 0$ [26]. By substituting (68) in (67), the matrixes A', E', C', and F' can be expressed as follows:

$$A' = \begin{bmatrix} 0 & \left(\bar{D}_1 + \bar{D}_2 - 1\right)/2L_1 \\ \left(1-\bar{D}_1-\bar{D}_2\right)/2C_1 & -2/R_oC_1 \end{bmatrix}$$

$$C' = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

$$E' = \begin{bmatrix} \bar{V}_{C1}/2L_1 & \left(\bar{V}_{C1} + \bar{V}_{\text{in}}\right)/2L_1 \\ -\bar{I}_{L1}/2C_1 & -\bar{I}_{L1}/2C_1 \end{bmatrix} \qquad F' = [0]. \tag{70}$$

For this system, the controllability matrix can be written as follows:

$$\Phi_c = \left[E' \middle| A'E' \middle| A'^2E' \middle| \ldots \middle| A'^{n-1}E'\right]. \tag{71}$$

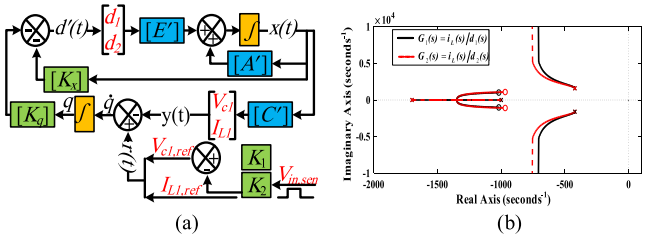

Fig. 7. Control strategy: (a) schematic of the close-loop control method and (b) pole placement of the proposed structure after closed-loop control.

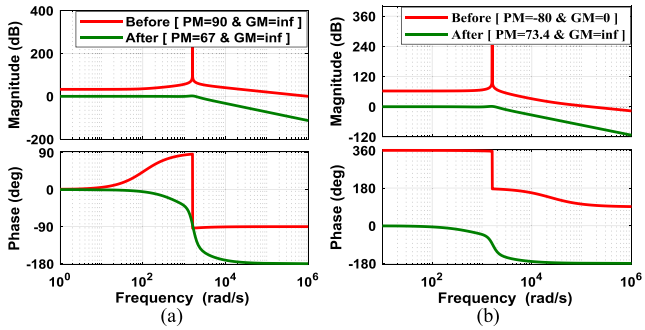

Fig. 8. Bode plot of the proposed converter: (a) inductor current (i_L) and (b) capacitor voltage (v_c).

For this system, if $rank(\Phi) = n = 2$, the system would be completely controllable.

The modified multi-input (d_1, d_2) multioutput (i_{L1}, v_{c1}) control method is illustrated in Fig. 7(a). In this method, by appropriate designing of the matrixes K_x and K_q, it is possible to put closed-loop poles in desired places. In this figure, q is the integrator output and r is the output reference vector which is compared with output values. For this system, the following equations can be written:

$$\dot{q}_1(t) = I_{L1,\mathrm{ref}} - I_{L1},\ \dot{q}_2(t) = V_{C1,\mathrm{ref}} - V_{C1} \tag{72}$$

$$\tilde{\mathrm{d}} = -\mathrm{K_x}\tilde{\mathrm{x}} - \mathrm{K_q q}. \tag{73}$$

In renewable energy sources, the input voltage is variable. As a result, the effect of this variable input voltage should be considered on the output voltage. Also, in this model, an approach is presented for converters in which their output voltage is equal to the summation of input voltage and capacitor voltage, such as [16] and [17]. In this method, the variation of input voltage is considered by utilizing a voltage sensor ($V_{\mathrm{in,\ sen}}$) for input supply. Therefore, it can be written as

$$V_{C1,\mathrm{ref}} = k_1 - k_2 V_{\mathrm{in,sen}}. \tag{74}$$

In (74), K_1 and K_2 are designed 210 and 0.5, respectively. The state space of the new system which presented in Fig. 7(a) can be described as

$$\begin{bmatrix}\dot{\tilde{x}}(t)\\ \dot{q}(t)\end{bmatrix} = \begin{bmatrix}A' & 0\\ -C' & 0\end{bmatrix}\begin{bmatrix}\tilde{x}(t)\\ q(t)\end{bmatrix} + \begin{bmatrix}E'\\ 0\end{bmatrix}\tilde{d}(t) + \begin{bmatrix}0\\ I\end{bmatrix} r(t)$$

$$y(t) = \begin{bmatrix}C' & 0\end{bmatrix}\begin{bmatrix}\tilde{x}(t) & q(t)\end{bmatrix}^T. \tag{75}$$

The controllability matrix of the new system can be given by

$$\overline{\Phi_c} = \begin{bmatrix}E' & A'\\ 0 & -C'\end{bmatrix}\begin{bmatrix}I & 0\\ 0 & \Phi_c\end{bmatrix} \Rightarrow M = \begin{bmatrix}E' & A'\\ 0 & -C'\end{bmatrix}. \tag{76}$$

If *rank(M)* is equal to *m*+*n*, the new system will be controllable. In the new control system, the feedback matrixes K_x and K_q provide the required conditions to settle the closed-loop poles in the appropriate places. By substituting (72) and (73) in (75), the new system can be described as follows:

$$\begin{bmatrix}\dot{\tilde{x}}(t)\\ \dot{q}(t)\end{bmatrix} = \begin{bmatrix}A' - E'K_x & -B'K_q\\ -C' & 0\end{bmatrix}\begin{bmatrix}\tilde{x}(t)\\ q(t)\end{bmatrix} + \begin{bmatrix}0\\ I\end{bmatrix} r(t)$$

$$y(t) = \begin{bmatrix}C' & 0\end{bmatrix}\begin{bmatrix}\tilde{x}(t) & q(t)\end{bmatrix}^T. \tag{77}$$

In order to achieve the desired values for gain margin and phase margin ($GM \geq 10$ and $60 \leq PM \leq 80$), the trial and error method is used to determine the places of the closed-loop poles [27].

In order to stabilize the system, the values of K_x and K_q are determined as follows

$$[K_x] = \begin{bmatrix}-0.1319 & 1.1933\\ 0.1469 & -1.3130\end{bmatrix}$$

$$[K_q] = \begin{bmatrix}449.3355 & -169.122\\ -494.6167 & 185.4253\end{bmatrix}. \tag{78}$$

By using MATLAB software, the pole and zero placements for $G_1(s) = i_{L1}(s)/d_1(s)$ and $G_2(s) = v_{C1}(s)/d_2(s)$ are extracted and shown in Fig. 7(b). As it can be seen, all system poles are placed in the left side imaginary axis. Therefore, the new system is completely stable. By these determinations, the transfer functions of $G_1(s)$ and $G_2(s)$ can be expressed as (79) and (80), respectively, in the following:

$$G_1(s) = \frac{2.317e05s^2 + 5.687e08s + 3.198e11}{s^4 + 2940s^3 + 2.698e06s^2 + 1.078e09s + 3.198e11} \tag{79}$$

$$G_2(s) = \frac{2.353e05s^2 + 5.092e08s + 3.198e11}{s^4 + 2940s^3 + 2.698e06s^2 + 1.078e09s + 3.198e11}. \tag{80}$$

The Bode diagram of the proposed converter is achieved by using MATLAB software and illustrated in Fig. 8. The values of phase margins are 67 and 73.4 for inductors' currents and capacitors' voltage, respectively. As a result, the values of *GM* and *PM* are in the desired range and the system is controlled.

VI. Comparison Study

In this section, in order to realize the advantages of the proposed converter, this structure is compared with some related structures and the results are gathered in Table II. In this comparison, the voltage gain, the voltage stress, and the number of components are compared. According to this table, it can be concluded that the voltage gain of the proposed converter is greater than other structures. Also, the voltage stresses across the power switches are lower than other related structures.

TABLE II
COMPARISON OF VOLTAGE GAIN, NORMALIZED VOLTAGE STRESS, AND NUMBER OF COMPONENTS BETWEEN THE PROPOSED CONVERTER AND SOME RELATED STRUCTURES

Ref.	Voltage gain (M)	Normalized voltage stress across the power		P_{out} [W]	Eff. [%] at V_{in}[V]	Input current	Components $S^*/D^*/L^*/C^*/L.I^*/T$
		switches V_S/V_o	diodes V_D/V_o				
[2]	$(2+d)/(1-d)^2$	$2M/(6M+1-(\sqrt{1+12M}))$	$2M/(6M+1-(\sqrt{1+12M}))$	250	93.36% - 12V	Non pulsating	2/5/3/6/-/16
[7], n=4	$(1+5M)/(1-d)$	$(1+5M)/(6M)$	$(M+1)/(M)$	200	95.9% - 30V	Pulsating	6/9/6/1/-/22
[8]	$2/(1-d)$	0.5	-	300	90% - 40V	Non pulsating	4/0/1/4/-/9
[12]	$(3+d)/(1-d)$	$(M+1)/(4M)$	$(M+1)/(2M)$	200	92.2% - 20V	Pulsating	2/3/2/3/-/10
[13]	$(2+d)/(1-2d)$	$(2M+1)/(5M)$	$(2M+1)/(5M)$	200	89.4% - 24V	Pulsating	1/5/3/7/-/16
[15]	$3/(1-d)$	0.33	0.33	150	93.9% - 30V	Non pulsating	1/5/1/5/-/12
[16]	$(1+3d)/(1-d)$	$(M+1)/(4M)$	$(M+1)/(2M)$	200	94.27 - 20V	Pulsating	2/2/3/3/-/10
[17]	$(3+d)/(1-d)$	$(M+1)/(4M)$	$(M+1)/(2M)$	200	94.26 - 20V	Pulsating	2/3/-/3/1/9
[18]	$(1+d_1)/(1-d_1-d_2)$	1	$(M+1)/(M)$	120	93.6% - 20V	Pulsating	3/2/2/1/-/8
[19]	$(2-d_2)/(1-d_1-d_2)$	$(M-1)/(M)$	$(M-1)/(M)$	500	95.47% - 38V	Pulsating	3/3/2/2/-/10
[20]	$(2)/(1-d_1-d_2)$	0.5	1	500	94.67% - 30V	Pulsating	3/3/2/2/-/10
[21]	$(3-d_1-2d_2)/(1-d_1-d_2)$	$(M-2)/M$	$(M-1)/M$	500	92.6% - 36V	Pulsating	3/4/2/3/-/12
[22]	$(3-d_1-d_2)/(1-d_1-d_2)$	0.5	1	500	96.8% - 30V	Pulsating	3/4/2/3/-/12
[23], n=2	$(1+7d)/(1-d)$	$(3M+1)/(4M)$	$(M+1)/(M)$	200	95.6 - 40V	Pulsating	6/8/9/1/-/24
*P.C.**	$(3+d_1-d_2)/(1-d_1-d_2)$	$(M+1)/(4M)$, $(M-1)/(2M)$	$(M+1)/(2M)$	500	93.4 - 20V 95.85 - 30V	Pulsating	3/4/2/3/-/12

S^*: Switch, D^*: Diode, L^*: Inductor, C^*: Capacitor, $C.I^*$: Coupled inductor, T^*: Total of components, $P.C.*$: Proposed converter.

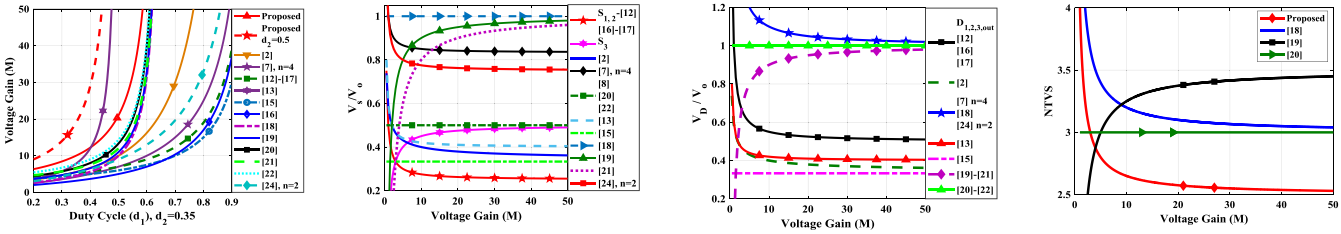

Fig. 9. Comparison of: (a) voltage gain; (b) voltage stress across the power switches; (c) voltage stress across the power diodes; and (d) NTVS.

Fig. 9(a) illustrates the voltage gain curves versus duty cycle. In order to prove the proposed converter's ability in providing flexible voltage gain, by selecting 0.35 and 0.5 for d_2, it is shown that there are a lot of combinations for duty cycles d_1 and d_2 to achieve the desired voltage gain. Considering Table II and Fig. 9(a), the voltage gain of the proposed converter is higher than the related structures, while the total number of components is lower than [2], [8], [13], and [24], greater than the structures in [8], [12], [16]–[19], and [20], and equal to [15].

The normalized voltage stress across the power switches are plotted in Fig. 9(b). As it can be seen, the voltage stress across the power switches S_1 and S_2 is lower than other structures. Also, the voltage stress across the power switch S_3 is in an acceptable range. In addition, it can be seen that some structures such as [18]–[20], which provide a flexible voltage gain, suffer from high voltage stress across the power switches.

The comparison of the voltage stress across the power diodes is shown in Fig. 9(c). From this figure, it can be seen that, in the proposed converter, the voltage stress across the power diodes is lower or almost equal to the related structures except [2] and [13].

The proposed structure has more elements than the structures in [18]–[20]. In order to realize the excellence of the presented structure, normalized total voltage standing (NTVS) is investigated. NVTS can be expressed as

$$\mathrm{NTVS} = \sum_{i=1}^{N_S} \frac{V_{Si}}{V_o} + \sum_{i=1}^{N_D} \frac{V_{Di}}{V_o} \tag{81}$$

where N_S, N_D, V_S/V_o, and V_D/V_o are the number of switches, number of diodes, normalized voltage stress across the switches, and normalized voltage stress across the diodes, respectively.

In order to provide the similar condition, the voltage stress across the power diode D_1 is ignored. Therefore, the NTVS of the proposed converter and [18]–[20] can be expressed as follows:

$$\mathrm{NTVS\,[Proposed]} = 2\,(M+1)\,/M + (M-1)\,/2M \tag{82}$$

$$\mathrm{NTVS\,[18]} = 1 + (2\,(M+1)\,/M) \tag{83}$$

$$\mathrm{NTVS\,[19]} = 1 + (2.5\,(M-1)\,/M) \tag{84}$$

$$\mathrm{NTVS\,[20]} = ((2M+4M)\,/2M)\,. \tag{85}$$

The NTVS curves versus the voltage gain are illustrated in Fig. 9(d). From this figure, it can be seen that the NTVS of the proposed converter is significantly lower than [18]–[20]. Therefore, it can be claimed that although the proposed converter has more components than some structures, it can provide higher voltage gain with lower NTVS.

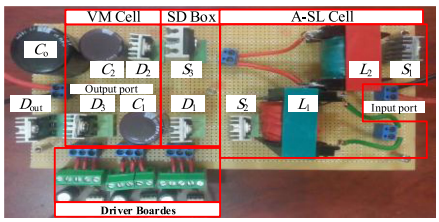

Fig. 10. Schematic of the proposed prototype.

TABLE III
COMPONENTS SPECIFICATION OF THE PROTOTYPE

Parameters	Values and Features
V_{in} and V_o	20 V and 394 V
f_s and P_{out}	46 kHz and 500 W
Duty ratio	d_1=0.5, d_2=0.35
Switches ($S_{1,2}$)	IRFB4228PbF, $r_{DS(on)}$=12 $m\Omega$, t_r=59 nS, t_f=33 nS
Switch (S_3)	IRFB4229PbF, , $r_{DS(on)}$=38 $m\Omega$, t_r=21 nS, t_f=31 nS
Diodes	D_1: SBR30U300CT, r_D=30 $m\Omega$, V_F=0.76 V $D_{2,3,out}$: SBR10U300CT, r_D=20 $m\Omega$, V_F=0.64 V
Inductors	100 μH, r_L=10 $m\Omega$
Capacitors	$C_{1,2}$:22 μF, 250 V, C_{out}:100 μF, 450 V

VII. EXPERIMENTAL RESULTS

In this section, in order to verify the theoretical analysis, a laboratory prototype of the proposed converter at 500 W output power is built and the experimental prototypes are shown in Fig. 10. The specifications of the proposed converter are illustrated in Table III. The experimental results are illustrated in Sections VII-A–VII-D. In Section VII-A and VII-B, the experimental results at 500 and 250 W output power are discussed, respectively. The waveforms of DCM operation are shown in Section VII-C at 150 W. Finally, the efficiency is investigated in Section VII-D.

A. Experimental Results at 500 W Output Power

Experimental waveforms at 500 W output power are illustrated in Figs. 11 and 12. The output voltage and voltage across capacitors C_1 are shown in Fig. 11(a). As illustrated, the output voltage and capacitors' voltage are equal to 394 and 188 V, respectively. The input voltage and current are shown in Fig. 11(b). In this figure, input current ripple is pulsating and the input voltage equals 20 V. Fig. 11(c) illustrates the voltage and current of L_1, as shown in the first and second operational modes, the inductor is charged by 20 and 10 V. Therefore, the inductor's current slope is positive. On the other hand, the voltage of inductors in the third operational modes is equal to -83 V. Therefore, in this mode, the inductor's current slope is negative and the inductor is discharged. The current and voltage across switch S_1 is shown in Fig. 11(d). In this figure, the maximum voltage stress across this switch is equal to 104 V. Fig. 11(e) illustrates the voltage and current of *SD* box, as shown in the first mode, the voltage of this branch is equal to -20 V. In order to create a unidirectional branch, a series diode (D_1) with S_3 is applied. Also, the maximum voltage stress equals 189 V. The voltage stress across diodes $D_{2,3}$ and $D_{\rm out}$ are illustrated in Fig. 11(f). In this figure, the maximum voltage stress equals 207 V. The dynamic response of the proposed converter is depicted in Fig. 12. Fig. 12(a) shows the output voltage variations at input voltage changes. As shown, a fixed output voltage is achieved when input voltage is changing from 20 to 30 V. Fig. 12(b) shows the output voltage at load changes. In this figure, for two output powers (500 and 250 W), the output voltage changes are shown. Finally, the dynamic response at duty cycle changes is shown in Fig. 12(c). In this figure, the duty cycle of switches $S_{1,2}$ are changing from 0.5 to 0.4. By increasing the duty cycle of switch S_3 (d_2), the output voltage is fixed. Summary of the calculated and measured voltages stress across the components at 500 W is presented in Table IV.

TABLE IV
MEASURED AND CALCULATED VOLTAGES AT 500 W OUTPUT POWER

Parameter	Calculated	Measured
Output voltage (V_o)	420 V	394 V
Capacitors voltage (V_{C1} and V_{C2})	200 V	188 V
Voltage stress across on the S_1 and S_2	110 V	104 V
Voltage stress across the S_3	200 V	189 V
Voltage stress across on the Diodes	220 V	207 V

B. Experimental Results at 250 W Output Power

In this section, experimental waveforms at 250 W output power are extracted in order to show the capability of the proposed converter at different output powers. In Fig. 13(a), the output current and voltage equals 400 V and 0.625 A. Also, the input current and voltage are illustrated in Fig. 13(b). Finally, the inductor's current and voltage across the inductor L_1 is depicted in Fig. 13(c). As it can be demonstrated in (46), at 20 V input voltage, the current ripple of inductors equals 2.7 A, which is illustrated in Fig. 13(c).

C. Experimental Results at DCM Operations

Considering parameter values as: $V_{\rm in} = 20$ V, $d_1 = 0.4$, $d_2 = 0.2$, $L_1 = L_2 = 20$ μH, $f_s = 20$ kHz, $P_{\rm out} = 150$ W, $R_{\rm out} = 200\,\Omega$, and using the relations achieved in Section II, the following values can be calculated:

$G_{\rm CCM} = 8$, $G_{\rm DCM} = 9$, $\tau_{\rm DCM} = 0.0046$, $\tau_{\rm BCM} = 0.0625$.

Based on values above, it can be seen that $\tau_{\rm BCM} \geq \tau_{\rm DCM}$. Therefore, at this condition, the proposed converter operates under DCM condition. The experimental results of DCM operation are illustrated in Fig. 14. The output voltage and output current are shown in Fig. 14(a), the output voltage and output current are equal to 174 V and 0.86 A, respectively. The inductor current and input current are illustrated in Fig. 14(b). As can be seen, the inductor's current and input current reach zero at DCM operation. The voltage stress across the $S_{1,2}$ and *SD* box are shown in Fig. 14(c). In addition, voltage stress across the power diodes is illustrated in Fig. 14(d).

D. Efficiency Analysis of the Proposed Converter

In this section, the proposed converter's efficiency is investigated. Fig. 15(a) illustrates the measured and theoretical

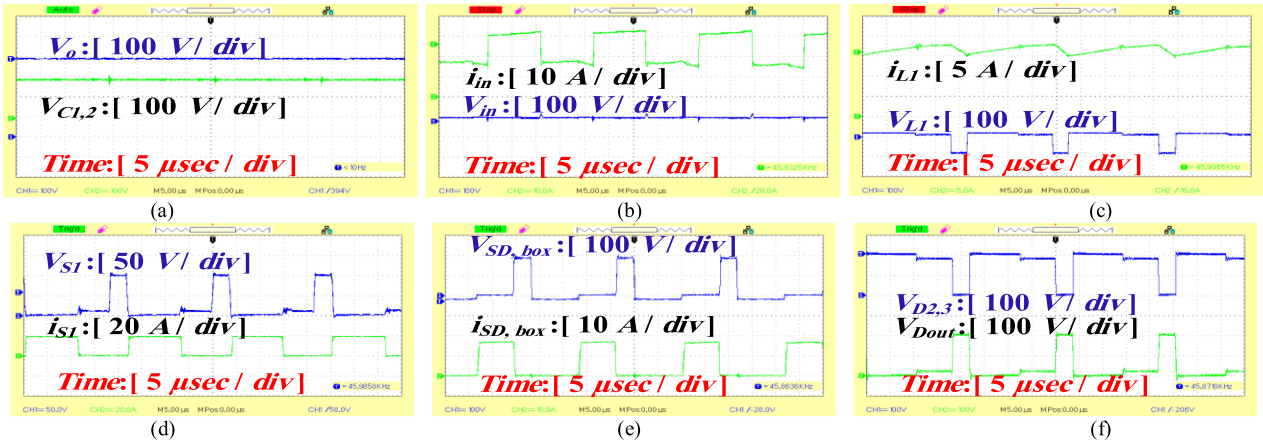

Fig. 11. Experimental waveforms at 500 W output power: (a) output voltage and voltage across the capacitor C_1; (b) input voltage and current; (c) voltage and current of inductor L_1; (d) voltage and current of switch S_1; (e) voltage and current of *SD box*; and (f) voltage stress across the power diodes $D_{2,3}$ and $D_{\rm out}$.

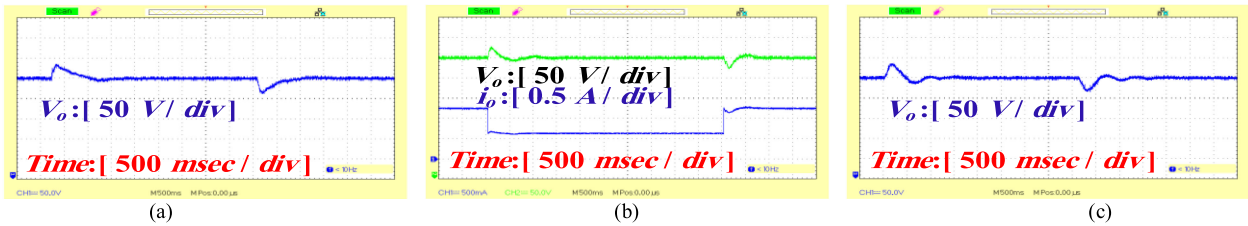

Fig. 12. Dynamic response at: (a) input voltage change; (b) load variations; and (c) duty cycle change.

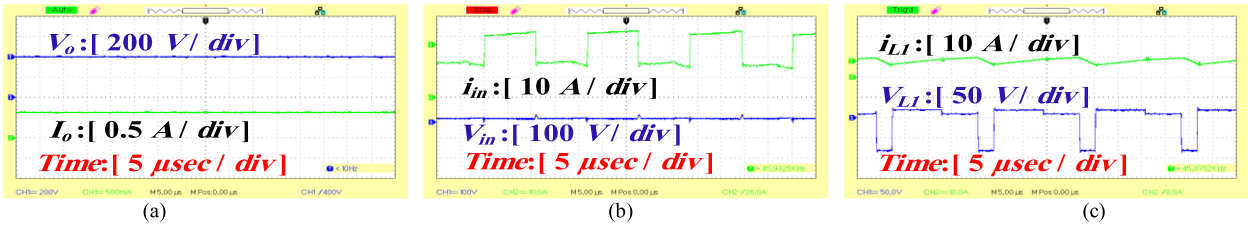

Fig. 13. Experimental waveforms at 250 W output power: (a) output voltage and current; (b) input voltage and current; and (c) inductor current (i_{L1}) and voltage (V_{L1}).

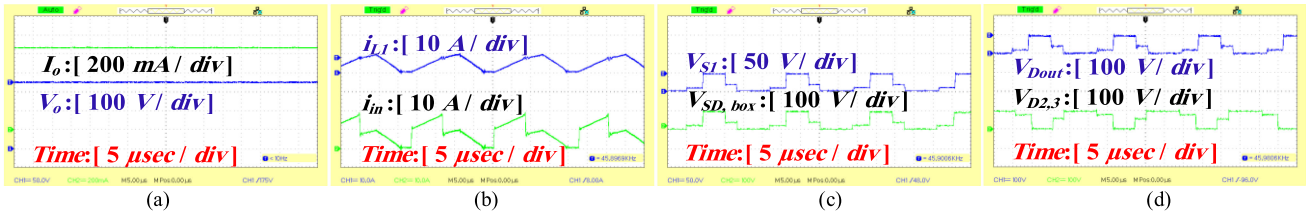

Fig. 14. Experimental waveforms of DCM operation: (a) output voltage and output current; (b) input current $(i_{\rm in})$ and inductor current (i_{L1}); (c) $S_{1,2}$ and *SD box* voltage stress; and (d) $D_{2,3}$ and $D_{\rm out}$ voltage stress.

efficiency of the proposed converter. In this figure, the efficiency curves versus output power are provided for two values of input voltage (20 and 30 V). Based on this figure, the maximum efficiencies are equal to 94.4% for $V_{\rm in} = 20$ V and 96.2% for $V_{\rm in} = 30$ V at 320 and 380 W output power, respectively. In Fig. 15(b), the measured efficiency of the proposed converter with $V_{\rm in} = 30$ V is compared with some other related structures. From this figure, it can be concluded that at output powers higher than 200 W, the efficiency of the proposed converter is higher than [16] and [17]. Also, it is obvious that the experimental efficiency of the proposed converter is considerably higher than [19] and [20].

Fig. 16 illustrates the theoretical proportion of losses for two different input voltage values (20 and 30 V) at 500 W

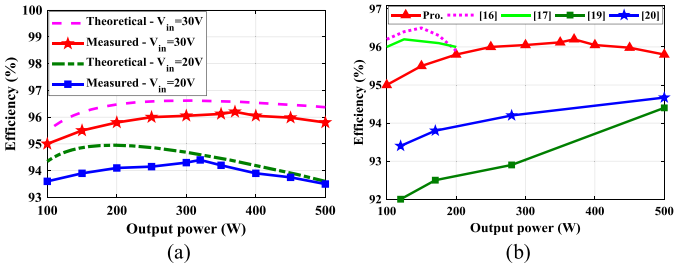

Fig. 15 Comparison of: (a) measured and theoretical efficiency of the proposed converter and (b) measured efficiency of the proposed converter and other related structures.

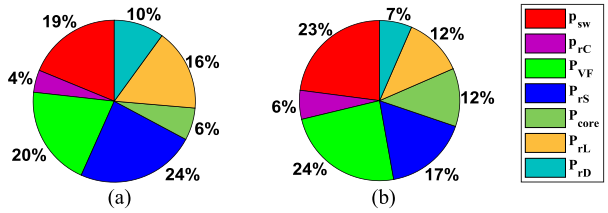

Fig. 16. Proportion of losses at output power = 500 W based on two different input voltages: (a) input voltage = 20 V, output voltage = 400 V, efficiency = 93.62% and (b) input voltage = 30 V, output voltage = 410 V, efficiency = 96.4%.

TABLE V
FLEXIBILITY IN VOLTAGE GAIN BY UTILIZING DIFFERENT DUTY CYCLE COMBINATIONS

V_{in}=20V and P_{out}=250W						
d_1	0.2	0.3	0.4	0.5	0.6	0.7
d_2	0.68	0.57	0.46	0.35	0.24	0.13
$V_{o,\,Theoretical}\,(V)$	398	402.4	405.9	408.7	411	413
$V_{o,\,Measurement}\,(V)$	390	394	398	400	403	405
$\eta_{\,Theoretical}\,(\%)$	92.5	93.54	94.34	95	95.53	96
$\eta_{\,Measurement}\,(\%)$	91.75	92.8	93.5	94.1	94.7	95.1
Increase of d_2, Increase of losses and decrease of efficiency						

output power. In fact, at a constant output power, increasing the input voltage decreases the elements' current. Therefore, the elements' resistance losses are reduced significantly.

Table V shows the flexibility of the proposed converter in providing the desired voltage gain by utilizing different combinations of duty cycles at constant output power (250 W). As it can be seen, there are many different duty cycle combinations to provide a high voltage gain. Also, the efficiency of the proposed converter is changed by altering the combinations of the duty cycles. From Table V, it can be concluded that increase in (d_1+d_2) or d_2 decreases the efficiency. In fact, as it was discussed in (59), increasing duty cycle d_2 increases the power losses.

The proposed converter has some features such as providing high voltage gain with low voltage stress across the power semiconductors, flexibility in control and providing an output voltage with different combinations of duty cycles, constant output voltage, high efficiency, and continues input current ripple. Considering the mentioned features, the proposed converter can be a suitable choice for dc microgrid applications.

VIII. CONCLUSION

In this article, a high step-up dc–dc converter with low voltage stress on semiconductors is presented. In this structure, there are different combinations of duty cycles (d_1 and d_2) to achieve a desired voltage gain. For example, by using ratios of ($d_1 = 0.5$ and $d_2 = 0.35$) or ($d_1 = 0.2$ and $d_2 = 0.68$), the voltage gain of 21 can be achieved. Despite many similar structures, lower duty cycles are needed to achieve high voltage gain in the proposed converter. Due to utilizing the power switch S_3, high voltage gain can be achieved with relatively lower duty cycles. In addition to this feature, this structure has the advantage of lower voltage stress across the semiconductors. In order to verify this claim, the proposed converter is compared with some similar structures in terms of voltage stress across the power semiconductors and NTVS. Also, it is explained that the proposed converter is completely controllable. In the mentioned control system, the duty cycle d_1 is used to control the inductors' current and the duty cycle d_2 is used to control the output voltage. Furthermore, steady-state analysis, nonideal model, and the component design are investigated. Finally, in order to verify the theoretical analysis, a laboratory prototype is built for 500 W output power.

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