7-kV 1-MVA SiC-Based Modular Multilevel Converter Prototype for Medium-Voltage Electric Machine Drives

Jianyu Pan, *Member, IEEE*, Ziwei Ke, *Member, IEEE*, Muneer Al Sabbagh, *Member, IEEE*, He Li, *Member, IEEE*, Karun Arjun Potty, *Member, IEEE*, Will Perdikakis, Risha Na, *Member, IEEE*, Julia Zhang, *Member, IEEE*, Jin Wang, *Senior Member, IEEE*, and Longya Xu, *Fellow, IEEE*

***Abstract*—This article presents the design and development of a 7-kV dc bus, 1-MVA, 0–1000 Hz modular multilevel converter (MMC) prototype for high speed medium-voltage variable frequency drives. The system is designed based on 1.7-kV silicon carbide (SiC) MOSFETs. First, the full in-depth design of the prototype is provided, including the submodules, arm inductors, and system integration. Then, the unique control scheme and the control hardware design are presented to achieve the full-frequency range operation. The power loss based on Si and SiC devices is analyzed. Finally, experimental results are presented to demonstrate the performance of both the SiC-based submodule and the full-scale MMC system. Compared with the traditional Si-based solution, the established SiC MMC can reduce the drive system volume by 75% and achieve 325% power density, and the peak energy efficiency reaches around 99.35%.**

***Index Terms*—Medium-voltage (MV) motor drive, modular multilevel converter (MMC), silicon carbide (SiC) device, submodule (SM) design.**

I. Introduction

ADVANCES in converter topologies and power electronics enable the next generation of high efficiency, high power density, and high-speed medium-voltage (MV) variable frequency drives (VFDs) [1]–[3]. The deployment of these MV VFDs to electric machines >500 HP high-power applications presents an energy savings opportunity of up to 3.2% of the total U.S. electricity consumption, leading to over $2 billion USD in annual energy saving [4], [5]. Among various multilevel converter topologies, the modular multilevel converter (MMC) for MV VFDs offers several advantages, such as scalability, modularity, high efficiency, superior output current quality, and can be designed without a heavy interface transformer [6]–[8]. Notably, compared with the neutral point clamped converter, the MMC can easily extend output voltage levels. When compared with the cascaded H-bridge topology, the MMC does not require a large number of isolated dc sources [9], [10]. Thus, MMC is a very promising topology as the next-generation high-power MV VFDs.

MMCs were introduced in 2002 [11], and the related control for the electric drive applications was presented in [12]–[16]. The major challenge occurs at low output frequencies (including zero) due to excessive voltage and energy pulsation in the submodule (SM) capacitors. Injecting a high-frequency common-mode voltage with the corresponding circulating current was proposed to mitigate the issue. Existing studies of MMC-based VFDs have a focus on the control schemes, such as capacitor voltage fluctuation reduction [12]–[15], circulating current regulation [17], [18], and modulation strategy [6], [19]. In [12]–[20], the power rating of the MMC-based VFD prototypes using the Si devices is less than 100 kVA, and the dc bus voltage is less than 1 kV. In HVdc transmission applications, a high-voltage MMC prototype with 2 MW power rating and 17 output voltage levels is presented in [21]. New MMC prototypes using silicon carbide (SiC) power semiconductors are also designed in [22] and [23], which present high-efficiency performance. However, their maximum power rating is 45 kW and 3 kVA, respectively, and the dc bus voltage is limited to 1 kV. Little work can be found on the design and development of MV megawatt-class MMCs for MV VFDs with the variable-frequency operation, not even mention the application of the wide bandgap devices (WBGs). Among the existing commercial MV VFDs listed in Fig. 1 illustrated that none of the industry companies, such as Siemens, ABB, and Alstom, have applied SiC devices to MV VFDs [1].

Using the MMC and SiC devices, the component and system design and implementation are entirely different from the traditional Si-based MV VFDs. Two critical aspects need to be considered. First, the SiC devices have much higher switching frequency than the traditional Si switches, and SM capacitor sizing reduction is the major issue in the MMC-based drives [4], [6], [8]. However, few articles have presented how

Manuscript received June 2, 2019; revised September 27, 2019 and January 12, 2020; accepted February 16, 2020. Date of publication March 5, 2020; date of current version June 23, 2020. This work was supported by the U.S. Department of Energy under Award DE-EE0007255. Recommended for publication by Associate Editor X. Wu. *(Corresponding author: Jianyu Pan.)*

Jianyu Pan is with the School of Electrical Engineering, Chongqing University, Chongqing 400044, China and also with the Department of Electrical and Computer Engineering, The Ohio State University, Columbus, OH 43210 USA (e-mail: pan.452@osu.edu).

Ziwei Ke, Muneer Al Sabbagh, He Li, Karun Arjun Potty, Will Perdikakis, Risha Na, Julia Zhang, Jin Wang, and Longya Xu are with the Department of Electrical and Computer Engineering, The Ohio State University, Columbus, OH 43210 USA (e-mail: ke.123@osu.edu; alsabbagh.2@osu.edu; li.2904@osu.edu; potty.1@osu.edu; perdikakis.1@osu.edu; na.123@osu.edu; zhang.564@osu.edu; wang.1248@osu.edu; xu.12@osu.edu).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.2978657

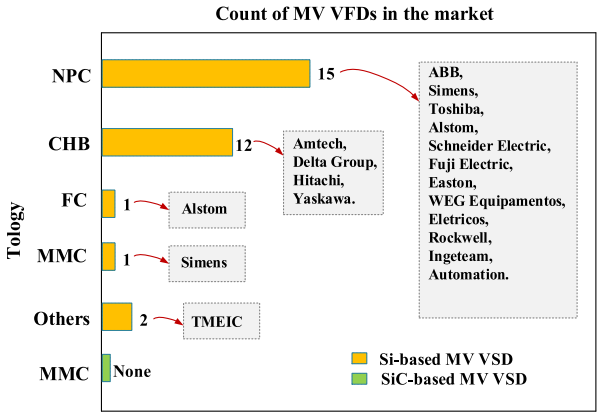


Fig. 1. Overview of existing MV VFDs in the market. The number respresents the accumulated count for the same topology flying capacitor (FC) converter.

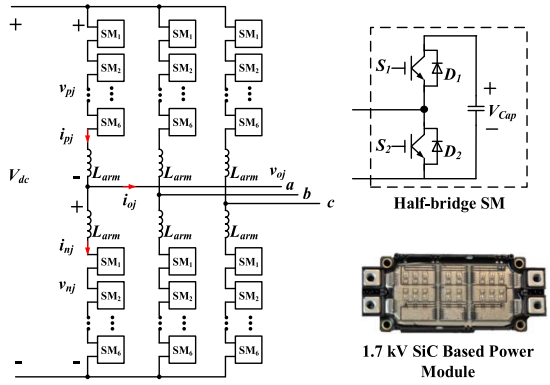


Fig. 2. Circuit configuration of the seven-level MMC.

TABLE I
7-KV SiC-BASED MMC SYSTEM SPECIFICATIONS

Parameter	Description
Circuit structure	7-level MMC
Operating voltage	7-kV V_{dc}/ 4.16-kV V_{ac}
Operating power	1 MVA
Rated current	138 A (RMS)
Rated frequency	1000 Hz
Operating frequency	0 ~ 1000 Hz
SM capacitor	0.6 mF
Arm inductor	0.13 mH
Rated SM voltage	1160 V
Switching Frequency	1 ~ 10 kHz
Capacitor ripple tolerance	15%

to take advantage of the SiC devices to shrink the capacitor size, not to mention the MV experimental investigation. Second, much faster *dv/dt* caused by the SiC devices switching introduces greater challenges to the SM and system integration in the MV and high-power condition [1], [5]. Without proper design, the driving circuits of SM may easily trigger malfunctions, and the overall system becomes bulky due to a large number of components. It is difficult to minimize SM and overall system dimension while satisfying isolation, electromagnetic interference (EMI), and reliability requirements simultaneously.

This article is a major revision of the conference paper [22]. It presents the design and development of a 7-kV 1 -MVA MMC prototype using the 1.7-kV SiC MOSFETs, the first MV VFD system using WBG devices drive systems in the world. The major contribution includes the following aspects.

1) It presents the method of using high-frequency SiC devices to reduce the capacitor size. The implementation of SiC devices can dramatically reduce the SM capacitor size by over 50% compared with the Si-based solution.
2) It illustrates the compact design of SiC-based SMs with strong EMI immunity.
3) It presents the small-volume design of the full-integrated MMC system. With the sophisticated design, the MMC prototype can integrate all the hardware components with a small size, but sufficient isolation and cooling capability.
4) It proposes an extra-wide frequency control of the MMC with the lab-designed control board.
5) It studies the power loss and the efficiency of the 7-kV 1-MVA SiC-based MMC prototype.

Validated by simulated and testing results, the SM and MMC system with the proposed design can successfully operate at MV high-power conditions, and present excellent steady-state and dynamic performance. The analyzed switch power loss is matched well with the tested result, and the system tested peak efficiency is approximately 99.35%. The developed SiC-based MMC prototype achieves 75% volume reduction, resulting in 325% of the power density compared with the existing Si-based MV VFDs. Thus, the developed MMC prototype can significantly advance the performance of the next-generation MV VFDs.

II. HARDWARE DESIGN AND IMPLEMENTATION

This section presents the detailed hardware design of the 7-kV MMC-based VFD using the 1.7-kV SiC power modules, including the capacitor selection, SM, arm inductor, and system integration.

A. System Overview

The power portion of a 4.16-kV/1-MVA high-speed VFD with 7-kV dc bus voltage is created based on the commercially available SiC devices. The drive topology is a seven-level MMC using 1.7-kV power modules for the SM design. Fig. 2 shows the MMC circuit configuration, and Table I lists the overall system requirements and specifications.

For the MMC circuit shown in Fig. 2, each arm consists of six SMs and an arm inductor. With a total bus voltage of 7 kV, the operating voltage of each switch is around 1160 V, which allows for a margin of 30% of the maximum voltage. In the following discussion, $V_{\rm dc}$ is the input dc voltage and v_{oj} $(j = a, b, c)$ is the output voltage of phase *j*. Likewise, i_{oj} is the corresponding output current of each phase. The upper and lower arm voltages are expressed as v_{pj} and v_{nj}, where the *p* and *n* denote the upper (positive) and lower (negative) arms, respectively. i_{pj}, i_{nj}, and i_{zj} are the upper arm, lower arm, and circulating currents of Phase *j*, respectively. $L_{\rm arm}$ and $R_{\rm arm}$ are the arm inductance and resistance. $V_{\rm cap}$ is the SM capacitor voltage.

Most existing MV motor drives are normally operated at low-speed range (<=3600 r/min) [5]. A mechanical gearbox

TABLE II
COMPARISON OF THE EVALUATED 1.7-KV SiC POWER MODULES

Manufacturer	Part Number	Current	$R_{ds}(on)$ at 25 °C	$T_{j.max}$
Wolfspeed	CAS300M17BM2	225 A	8 mΩ	150 °C
GeneSiC	GA100JT17-227	160 A	10 mΩ	175 °C
Rohm	BSM0015A	250 A	8 mΩ	175 °C

is needed to increase the speed of the load. If a high-speed drive (>10 000 r/min) is directly integrated with the load, the gearbox can be removed, resulting in the significantly improved system efficiency and power density. Thus, the high-speed electric machine drive is preferred in the next-generation drive applications. This article considers the operating frequency from 0 to 1000 Hz, corresponding to a 30 000/15 000 r/min high-speed machine with two/four-pole pairs.

B. SiC Device Selection

A comprehensive device evaluation was conducted to select the best candidate among all of the available 1.7-kV SiC devices. Three power modules were tested, and their information is listed in Table II. $T_{j.\max}$ represents the highest junction temperature. Among the investigated SiC power modules, BSM0015A shows excellent electrical performance, lower thermal impedance, and higher junction temperature. The parasitic inductance is only 13 nH, which is preferred by the high-speed switching. According to the converter power rating, the designed MMC needs 36 SMs for three phases. Under low-frequency operation, the highest current stress for each SM is around 140 A rms, which matches its capability very well. Thus, BSM0015A is selected and used in the 4.16-kV/1-MVA high-speed VFD prototype.

C. Capacitor Sizing With SiC Devices

The SM capacitor selection for MV VFDs is different from the HVdc applications due to the variable frequency nature of the drive. The worst scenario is at low frequency, such as 1 Hz. By injecting a feedforward common-mode voltage and controlling the resulting circuit current [14], [15], the capacitor voltage ripple can be minimized for a given capacitor value. The arm energy fluctuation ΔE in one period of the common-mode voltage for the upper arm is derived in (1), the relationship of capacitor voltage ripple V_{ripple} and common-mode voltage v_{com} refers to [6], which is obtained in (2) as

$$\begin{aligned}\Delta E &= \int_0^{T_s} v_{pj}\cdot i_{pj}\,dt \\ &= \int_0^{T_s}\left(\frac{1}{2}V_{\text{dc}} - v_{oj} - v_{\text{com}}\right) \\ &\quad\times\left(i_Z\left(v_{\text{com}}, v_{oj}, V_{\text{dc}}, i_{oj}\right) + \frac{1}{2}i_{oj}\right) t\,dt \end{aligned} \tag{1}$$

$$V_{\text{ripple}} = \frac{\int_0^{T_s}\left(\frac{1}{2}V_{\text{dc}} - v_{oj} - v_{\text{com}}\right)\left(i_Z\left(v_{\text{com}}, v_{oj}, V_{\text{dc}}, i_{oj}\right) + \frac{1}{2}i_{oj}\right) t\,dt}{C_{\text{sub}}\cdot V_{\text{dc}}} \tag{2}$$

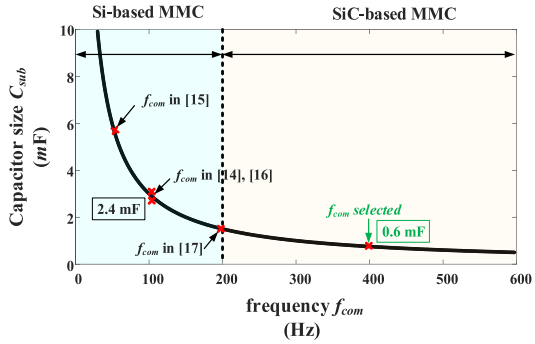


Fig. 3. Relationship of the common voltage frequency and the SM capacitance. The load frequency is 1 Hz with the full load current (138 A) and $V_{\text{ripple}} = 10\%$.

where T_s represents the period of the v_{com}. $i_Z(v_{\text{com}}, v_{oj}, V_{\text{dc}}, i_{oj})$ is the corresponding circulating current reference generated by v_{com}, V_{dc}, v_{oj}, and i_{oj} [14], [15]. C_{sub} is the SM capacitance. For the extra low frequency conditions, V_{dc}, v_{oj}, and i_{oj} and magnitude of v_{com} are relatively constant. Thus, the common-mode voltage frequency f_{com} brings the freedom to reduce the capacitor voltage ripples, resulting in capacitor size reduction.

Fig. 3 illustrates the relationship of the common-mode voltage frequency and SM capacitance for the 7-kV/1-MVA MMC drive system. In our design, V_{dc} is 7 kV with 200 A rated load current in the amplitude, v_{com} amplitude is 80% of $V_{\text{dc}}/2$ (2800 V), and v_{oj} is negligible compared with v_{com} at extra low frequencies. For the traditional Si devices in the MV applications, the switching frequency is normally less than 1 kHz due to the switching losses and thermal concerns [4]. If the acceptable control accuracy ($<=$ 1/10 of carrier frequency f_c) is needed for v_{com} and i_z, the common-mode voltage frequency f_{com} is dramatically limited [15]. The SM capacitance is obtained when the capacitor voltage ripple is kept approximately 10%, and sine wave injection is used. The f_{com} with the conventional Si-based MMC is generally less than 200 Hz. For example, 45 Hz in [15], 100 Hz in [14] and [16], and 200 Hz in [17]. Thus, the capacitor size reduction will be limited by the f_{com} in the Si-based solution.

The MMC in this article takes advantage of the fast-switching characteristics of the SiC devices to reduce the SM capacitor size. By using much higher switching frequency (>2 kHz) and common-mode voltage frequency (>200 Hz), the capacitor size can be reduced significantly compared with Si-based MMC. This article uses 4 kHz switching frequency with the 400 Hz injection frequency. Thus, the required control accuracy ($f_{\text{com}} = 1/10\, f_c$) is still satisfied. In Fig. 3, the SM capacitance is reduced to 0.6 mF. It becomes one-fourth and half of Si-based MMCs with the f_{com} of 100 and 200 Hz, respectively. Thus, the overall MMC volume/weight can be reduced, resulting in dramatically improved power density than the traditional Si-based solution.

D. SM Design

To provide strong common-mode transient immunity (CMTI) and 7-kV differential mode insulation to the system, a custom gate drive topology was designed.

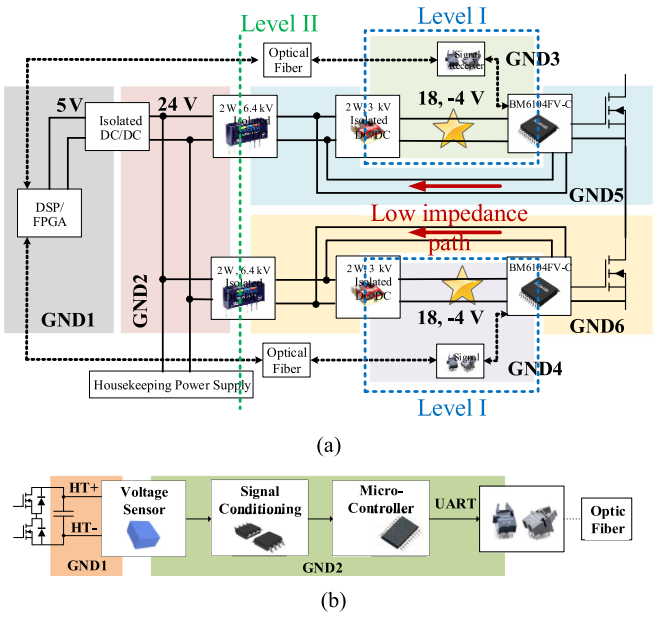


Fig. 4. Driving and sensing circuit design for the SM. (a) Gate driving circuit. (b) SM voltage sensing circuit.

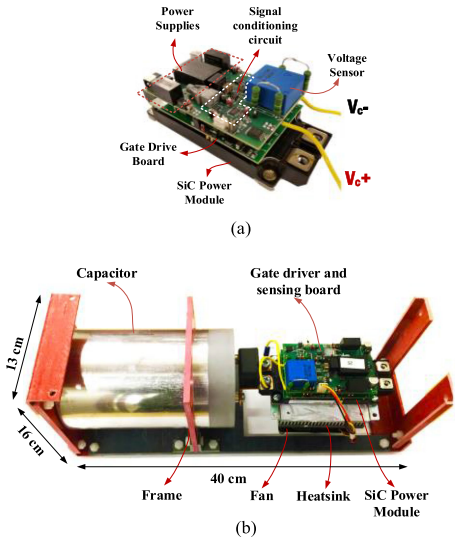


Fig. 5. SM physical structure. (a) SiC MOSFET with the driving and sensing boards. (b) Assembled SM.

The two-level gate drive is shown in Fig. 4(a). GND 3 and 4 (marked with a yellow star) are isolated from both SiC device and the signal source by the isolation components (level I). The gate drive BM6104FV has a CMTI larger than 100 V/ns with 2.5 kV isolation voltage, and the isolated dc/dc converter has 2 and 3 pF of isolation capacitance and 3 kV of isolation voltage. Considering their isolation impedances, a majority of the common-mode EMI current will flow through the low-impedance path back to the input power supplies. The critical ground GND 3 and 4 (gate drive chip primary sides) will be bypassed. By using this two-level gate drive topology with properly selected components, the clean and fast switching transients can be achieved.

For the insulation voltage of the gate driver, two 10-kV isolated dc/dc converters are used between the housekeeping power supply and GND 5/6 (level II); the required insulation value is half the dc bus, i.e., 3.5 kV. Optical fiber logic signals are adapted to transmit the gate signals. Thus, the strong insulation voltage between the high-voltage side of the gate driver connected with the power module and the low-voltage side with the housekeeping power supply is realized.

Fig. 4(b) shows the SM voltage measurement circuit with isolation between the measurement and the gate driver stage. An isolated closed-loop Hall effect sensor is used to measure the SM voltage. The output of the sensor is fed to a signal conditioning circuit and then read by a microcontroller. Finally, the SM voltage signal is transmitted via a universal asynchronous receiver/transmitter through optical fibers to the field-programmable gate array (FPGA).

The gate driver and sensing boards are shown in Fig. 5(a). The structure of the SM gate driver and measurement circuits is achieved using a two-printed circuit board (PCB) stack. The top PCB contains the power supplies, voltage sensor, and conditioning circuit. The power supplies are isolated to minimize the cross coupling within the module itself. The bottom PCB contains the gate driver circuits and protection circuits.

Fig. 5(b) illustrates the SM assembly with all the associated components installed. The SM capacitor is 0.6 mF with 1.6-kV voltage rating. Each power module has its own active cooling fan attached to the heat sink. The power module structure so designed allows very easy integration of the SM capacitor. Finally, all of these elements are installed in a high-insulation fiber-glass frame (13 cm $\times$ 16 cm $\times$ 40 cm) for side-by-side stacking to easily connect all SMs in each phase leg in series.

E. Arm Inductor Design

For the MMC-based VFD, a low arm inductance is preferred to minimize the size and cost of the arm inductors. However, the smaller arm inductance induces high control error and ripples in the circulating current. In our design, the allowable current ripple is set to 15% of the maximum circulating current magnitude as the boundary. We choose a relatively large current ripple (15%) to minimize the arm inductor size and the circulating current is still under good control. Besides, the circulating current error will not go the load side.

Fig. 6 shows the relationship between the circulating current ripple and the arm inductance. The maximum circulating current magnitude at low frequency is around 250 A. By repetitive running the simulation, the circulating current ripple is reduced from 100 to 8 A with the increase of the arm inductance from 0.05 to 0.35 mH. The minimized arm inductance is approximately 0.11 mH, which satisfies the 15% current ripple limitation. In the hardware implementation, a relatively larger arm inductance 0.13 mH is designed. It is realized by a coupled inductor for each phase, with the self-inductance 70 μH and the mutual-inductance 60 μH.

The coupled arm inductor is shown in Fig. 7(a). Coupled inductors provide around four times the self-inductance compared

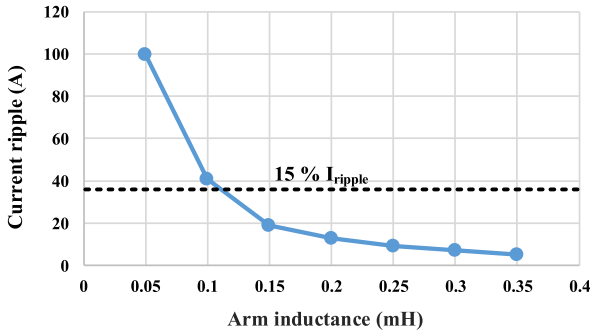


Fig. 6. Relationship of the circulating current ripple and the arm inductance.

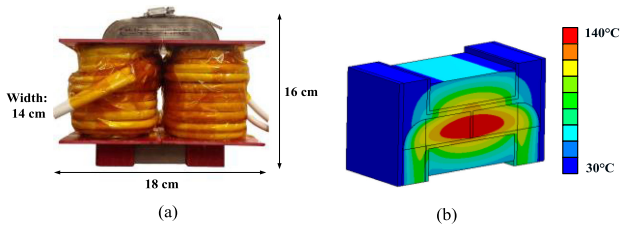


Fig. 7. Arm inductor design. (a) Physical structure. (b) FEA thermal anlaysis.

with none coupled one. Large inductance is needed for suppressing circulating currents in the high-frequency mode while simultaneously not affecting the three-phase currents through ac loads [20]. Moreover, appropriate core material should be selected; in [24], a comprehensive core materials comparison for the high-voltage high-frequency applications is presented. According to the comparison, amorphous core materials are selected due to their high saturation capability (up to 1.56 T), high permeability, and moderate core loss in high-frequency operation. To optimize the inductor loss as well as its power density, a parametric study was conducted. Then, a thermal model of an optimal candidate was built based on the experimental results. Using the results from finite-element analysis (FEA), a potting plus extruded fin heatsink cooling method was adopted to provide satisfactory cooling for the arm inductor. Fig. 7(b) shows the thermal analysis of the arm inductor. In the analysis, the ambient temperature is set to 30 °C, and the power losses on core and winding are set to be the maximum values in operation. The result shows that the maximum temperature of 140 °C occurs in the middle of the core, below the maximum allowable core temperature of 150 °C.

F. System Integration

For system integration, three critical aspects are considered.

1) Sufficient insulation is required due to the 7 kV MV operation condition.
2) The designed system provides sufficient cooling to ensure that all the components are operated in their safe thermal region.
3) The overall tower size is less than 1.5 $m^3$with the power density greater than 0.67 MVA/m^3, two times the power density compared with the traditional Si-based MV VFD [5].

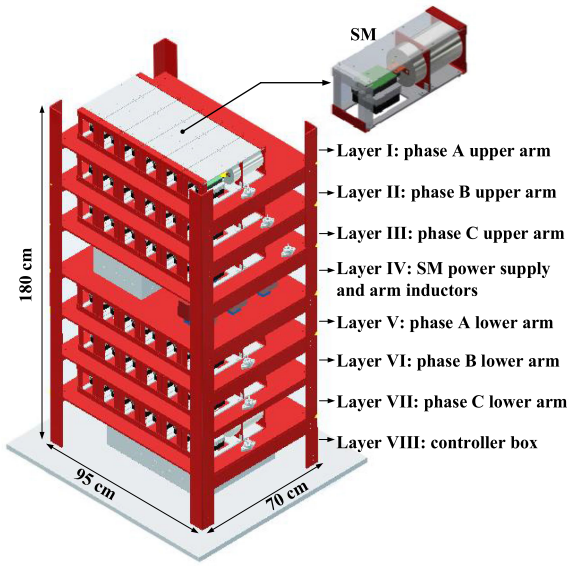


Fig. 8. Design of the three-phase seven-level MMC system integration.

A compact 95 cm × 70 cm × 180 cm MMC system frame is designed and built, as shown in Fig. 8. The overall volume is 1.2 m^3, 20% smaller than the design target. The designed frame integrates all the parts in eight layers. The upper-arm SMs are placed on the Layers I through III, while the lower-arm SMs on Layers V through VII. Each layer placement is a single-phase arm, containing six SMs placed side-by-side. The middle layer, Layer IV, holds the power distribution box and the three arm inductors. The power distribution box contains a 36-channel isolated power supply, providing power to the gate driver and sensing boards in each SM. Additionally, all the arm and load current sensors are placed on the middle layer. The bottom layer, Layer VIII, has the controller box. It contains the custom-designed control board containing a digital signal processor (DSP) and FPGA, and the fiber optic distribution board. SMs in each arm are connected electrically with the copper bus bar and each arm is connected using 400-A 10-kV isolated cables.

FEA thermal analysis is conducted to study the cooling effect of the designed system under the full-voltage and full-current condition [25]. Results show the proposed compact system design, containing all the SMs and arm inductors, can operate in the safe thermal region.

Four critical steps are taken to achieve sufficient insulation strength of the MMC prototype.

1) Both the system and the SM frames are made of fiberglass. The frames can provide strong mechanical strength and realize the insulation voltage strength >15 kV. Thus, the isolation between each SM and each layer is achieved.
2) For each SM, all the pulsewidth modulation (PWM) and fault signals are transmitted via optical fibers, resulting in the optical isolation between the controller board and the high-voltage SMs.
3) Power of the gate drivers and sensing boards of the SM is transferred via the 10-kV isolated dc–dc converter. Thus,

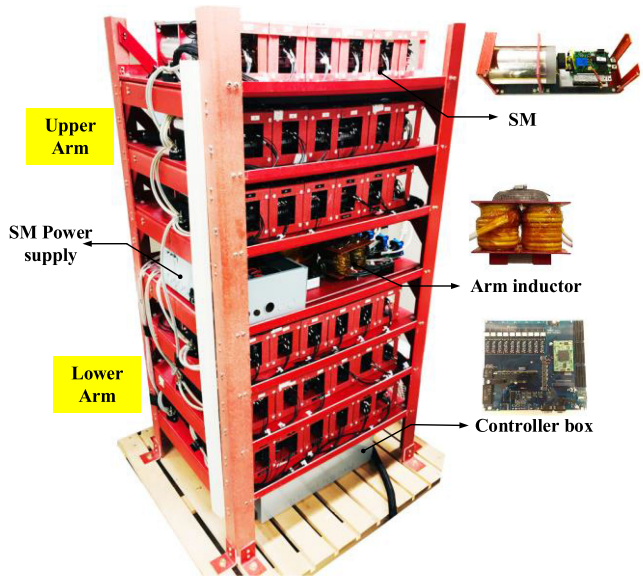


Fig. 9. Prototype of the three-phase seven-level SiC-based MMC.

the 10 kV isolation voltage of the drivers and sensing boards to the ground is realized.

4) For the arm inductors, they are designed and tested with the isolation strength at 10 kV without any partial discharge. Thus, the overall system is designed with the 10-kV isolation capability.

Fig. 9 shows the view of the full-scale SiC-based MMC prototype, with the one-to-one scale between the overall system and each individual component. The overall prototype consists of 36 SMs and 3 arm inductors, forming the three-phase seven-level MMC. The output terminals are connected to the high-voltage inductive load. When the MMC prototype is fed from a 7-kV input dc power supply, 4.16-kV rated line ac voltage can be generated. Thus, the 7-kV $V_{\rm dc}$/4.16-kV $V_{\rm ac}$ SiC-based MMC prototype is established.

III. Control Scheme and Controller Hardware

A. Proposed Control Scheme

The control scheme proposed needs to consider wide operational conditions, including the output ac voltages, currents, and frequency range from 0 to 1000 Hz. A fast and robust dynamic response is also required along with the robust and high-performance output currents in the steady state.

The proposed control scheme is illustrated in Fig. 10. The MMC controller has two closed current control loops: the load current loop to deal with the output load current and the circulating current loop for the purpose to balance the SM capacitor voltages and minimize the SM conduction losses. The voltage commands required by the load current and circulating current control determine the upper- and lower-arm voltages. Phase-shift PWM is used to determine the inserted SM numbers from each arm, while the optimized capacitor sorting algorithm is adopted to balance the capacitor voltages [6], [18].

In terms of the output frequency, the overall control scheme is divided into two control modes: low- and high-frequency modes (LF and HF mode). In the design, we define 15% of the base frequency (150 Hz) as the transition frequency between modes. In the LF mode, a 400 Hz common-mode current is controlled with a common-mode voltage to maintain a healthy voltage status on all of the SM capacitors [13]–[15]. The injected common-mode voltage and current are controlled in sine waveform for the smallest *di/dt* and *dv/dt* so that we can significantly reduce the EMI noise to the control hardware.

The injected common-mode voltage reference $v_{\rm com.ref}$ and circulating current reference $i_{Z.\rm ref}$ are derived in the following equations:

$$v_{\rm com.ref} = -\sqrt{2}V_{\rm com}\sin(\omega_{\rm com}t) \tag{3}$$

$$i_{Z.\rm ref} = \frac{1}{\sqrt{2}V_{\rm com}}\left(\frac{2v_{o.\rm ref}^2}{V_{\rm dc}} - \frac{V_{\rm dc}}{2}\right) i_o\sin(\omega_{\rm com}t) + \frac{v_{o.\rm ref}i_o}{V_{\rm dc}} \tag{4}$$

where $\omega_{\rm com}$ is the angular frequency of the common-mode voltage.

In the HF mode, a challenging issue identified and addressed is the circulating current oscillation [26]. Without proper control, a huge circulating current can occur when the MMC operates near the resonant frequency. Thus, we apply the circulating current suppressing control to minimize the unnecessary circulating current close to zero. Damping out the circulating current oscillation, the MMC VFD achieves much-improved reliability and reduced losses for the system.

In HF mode, the common-mode voltage and circulating current references are determined by

$$v_{\rm com.ref} = 0 \tag{5}$$

$$i_{Z.\rm ref} \approx i_{\rm dc}/3 \tag{6}$$

where $i_{\rm dc}$ is the input dc current.

The designed prototype MMC selects the common-mode voltage magnitude as 80% of $V_{\rm dc}$/2. This is because, based on the constant *V/f* control principle for the variable frequency motor drive applications, the required output voltage in low-frequency mode is <15% of the rated ac voltage. Thus, we have a sufficient voltage margin for the common-mode voltage generation at 400 Hz. A frequency of 400 Hz is chosen because the carrier frequency f_c is 4 kHz, so having a value that is one-tenth of f_c is reasonable [15]. To avoid transient while switching the modes, the transition mode is made gradual in a window from 150 to 200 Hz, during which the common-mode voltage and circulating current commands are smoothly transitioned.

B. Control Hardware Design and Implementation

To implement the proposed control scheme, a controller board is designed, as shown in Fig. 11, with the features of compact size, advanced functionalities, and very fast execution time.

As shown in the figure, the controller board consists of a DSP, an FPGA, conditional signal circuits, and an isolated communication interface. The DSP (TI TMS320F28379D) implements the load current control, circulating current control,

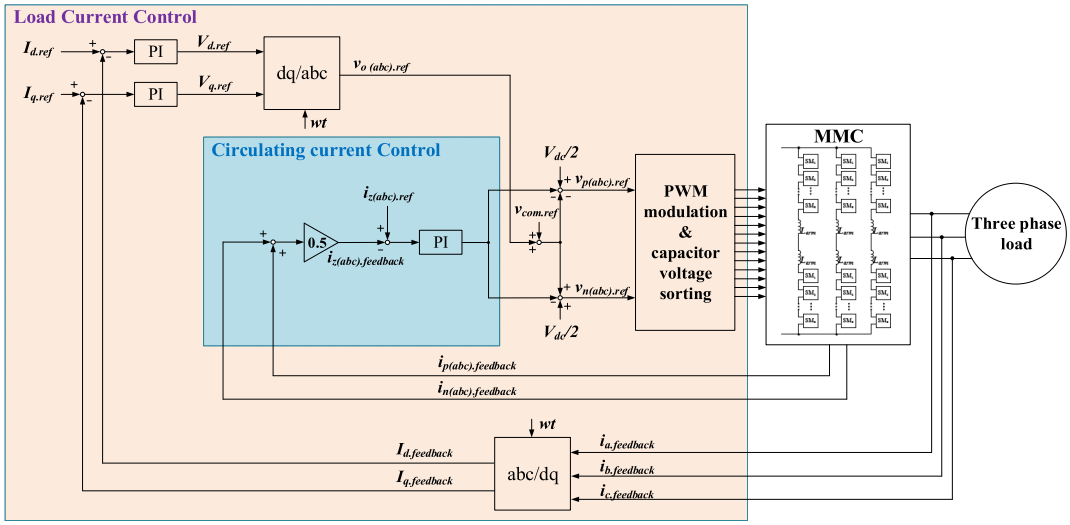


Fig. 10. Overall control scheme for the 7-kV SiC-based MMC prototype.

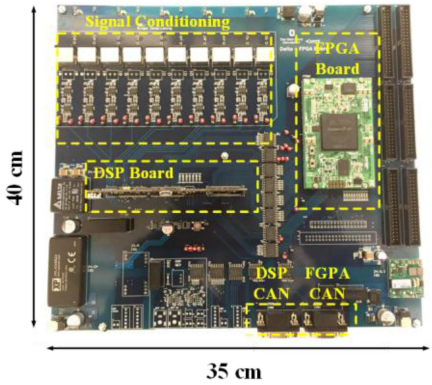


Fig. 11. DSP and FPGA controller board.

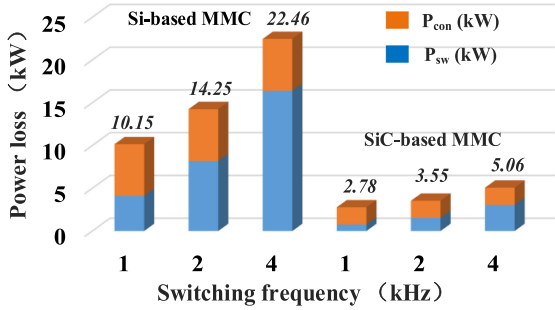


Fig. 12 Power loss analysis of the MMC based on Si and SiC devices.

arm voltage generation and human–machine interfacing. The FPGA (ALTERA Cyclone IV EP4CE40F29C8N) receives the arm voltage command from the DSP and implements the PWM algorithm and outputs 72 gate signals to the SMs via optical fibers. The FPGA also executes the SM voltage sorting and balancing algorithms by receiving the measured capacitor voltages and any fault signals from the SMs (36 total). The signal conditioning circuits are designed to receive the current sensor signals and send them to the DSP. The isolated communication interfaces are realized by a serial controller area network (CAN) interface port. The overall master control commands of the DSP are received from the operator's PC through the DSP CAN port. With the developed controller board, a control scheme for the MMC prototype is realized. The measured execution time for one cycle of the proposed control scheme is less than 20 μs or at a frequency of 50 kHz.

IV. Power Loss Analysis

Based on the proposed control scheme, the breakdown power loss of the full-scale MMC prototype is modeled and studied. The switch device considers the same voltage and current rating but with different materials: Rohm 1.7-kV 250-A SiC power module (BSM0015A) and the Infineon 1.7-kV 300-A Si power module (FF300R17KE4). The calculation method refers to the articles presented in [27] and [28]. The conduction loss of each device is computed from the current and the saturation voltage of the devices, and the average conduction loss is calculated for a fundamental cycle. The switching loss of the devices is calculated from the switching frequency and turn-ON/OFF energy. Finally, the total power loss of the inverter is obtained from adding the switching loss and the conduction loss of all devices.

Fig. 12 shows the breakdown power loss analysis for the Si-based and SiC-based MMCs. The calculated condition is based on the rated load current and rated frequency with the full dc bus voltage. $P_{\rm con}$ and P_{sw} represent the total conduction loss and switching loss, respectively. Three switching frequencies (1, 2, and 4 kHz) are studied and compared. As shown in Fig. 12, the total calculated power loss based on the SiC devices at 4 kHz is around 5.06 kW. By contrast, the Si-based MMC could be as high as 22.46 kW. The reason is that the high-voltage Si device has much larger turn-ON and turn-OFF energy and ON-state resistance. The increase of the switching frequency significantly induces higher switching loss for Si devices. Even Si-based MMC is operated at 1 kHz, and the total loss could be higher than that of Si-based MMC at 4 kHz. It is because the conduction loss of the Si-based MMC is dominant. Thus, MMC based on

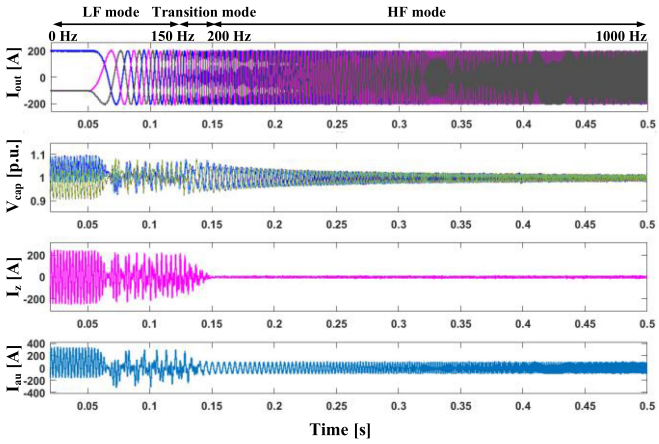


Fig. 13. Variable frequency operation from 0 to 1000 Hz with the rated output current.

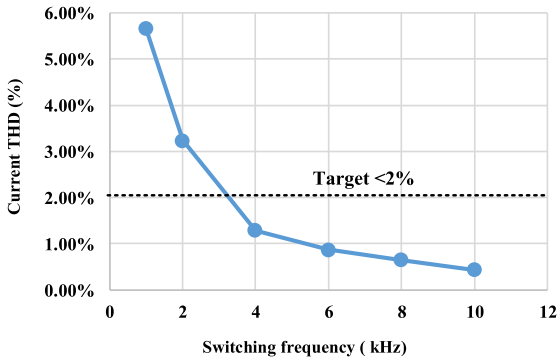


Fig. 14. Relationship of the switching frequency and output current THD at the rated frequency.

SiC devices present great potential to reduce the system power loss compared with the Si solution.

V. Simulation Analysis

To simulate the constant torque and variable speed operation condition as a motor drive, this article has tested the variable frequency operation of the control method from 0 to 1000 Hz with the full current. Fig. 13 shows the simulation results, starting from 0 Hz at 0.05 s and ramping up to 1000 Hz with a ramp rate of 2000 Hz/s. $I_{\rm out}$, $V_{\rm cap}$, I_z, and $I_{\rm au}$ represent three-phase output currents, Phase-A capacitor voltages, Phase-A circulating current, and Phase-A upper-arm current, respectively. It is evident that no instability issue is observed for the capacitor voltages and the arm currents for the full-frequency range and the load current is controlled to the rated value. In detail, all the capacitor voltages are stabilized, with fluctuations smaller than 10% of their nominal values. The injected circulating current is gradually reduced during the transition mode. Thus, the control method can be effectively applied in the developed MMC prototype for the full-frequency operation.

The load current total harmonic distortion (THD) theoretical analysis has been studied by the simulation. We consider the rated output frequency at 1000 Hz with 200 A rated current. The target is to keep the load current THD less than 2%. Thus, we can establish the converter prototype with a high-quality output current. Fig. 14 shows the relationship between the load current THD and switching frequencies. It is easy to observe that 4 kHz is the minimal frequency to satisfy 2% THD target. Although higher switching frequency (>4 kHz) can suppress THD more, it will induce high switching losses. That is why we do not use a higher switching frequency.

VI. Experimental Analysis

To examine the performance of the SiC-based MMC prototype with the proposed control scheme, extensive experimental tests are conducted on both the single SM and the full-scale MMC system. To be noted is that the reactive power and the inductive loads are used to test the prototype's full voltage and current capabilities, and frequency range from 0 to 1000 Hz. While being tested with the inductive loads, the MMC prototype will experience the equivalent voltage and current stress, resulting in the same 1-MVA apparent power. Meanwhile, no 1 MW real power will flow through the connected utility grid. The switching frequency is set to 4 kHz, resulting in the effective system PWM frequency of 24 kHz.

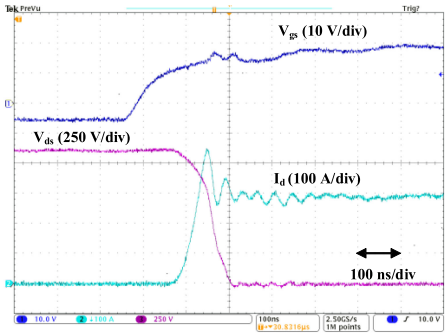
A. Single SM Test

The SiC MOSFET with the designed driving board in the SM is tested first to investigate its switching and current protection functions. Fig. 15(a) and (b) illustrates the turn-ON and -OFF transients under the full voltage (1.2 kV) and full current (300 A) conditions. $V_{\rm gs}$, $V_{\rm ds}$, and I_d represent the gate-to-source voltage, drain-to-source voltage, and drain current, respectively. It is easy to notice that the SiC MOSFET can be turned ON and OFF successfully at the full voltage and current. The rising and falling time is approximately 90 ns and 80 ns, respectively. The maximum *dv/dt* reaches approximately 15 kV/μs. Hence, the results in Fig. 15(a) and (b) validate the single SM controlled successfully with a very fast switching capability.

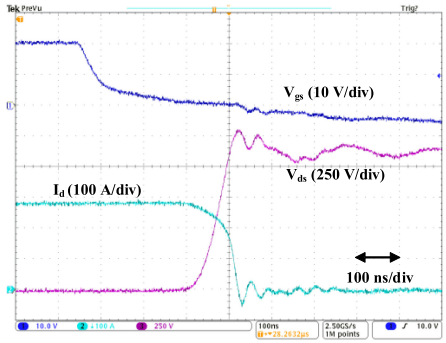
Fig. 15(c) demonstrates the functionality for short-circuit protection with the designed driving board. A short circuit is intentionally imposed for the tested device in the SM at 1200 V. As Fig. 15(c) displays, the SiC MOSFET is turned OFF and protected at 600 A within 1.2 μs. Thus, with the driving board design in the SM, the SiC power module has a strong over-current protection capability.

B. Full-Scale Three-Phase MMC Test

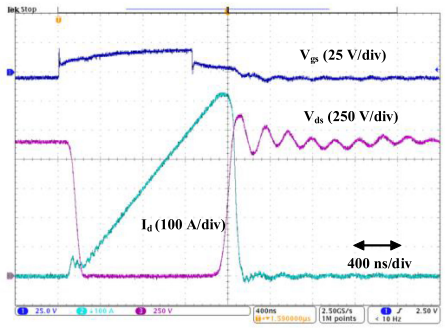
This section extensively examines and verifies the steady-state performance of the established prototype at the full dc voltage, full load current, and full-frequency range. The tested dc bus voltage is 7 kV and the load current 138 A rms. Fig. 16 illustrates the experimental results in low-frequency mode. Here, the examples used are 0, 10, and 50 Hz. Fig. 17 shows the results in the high-frequency mode; 400, 600, and 1000 Hz are the tested cases. Hence, the full-frequency range from 0 to 1000 Hz is covered. Results in Figs. 14 and 15 demonstrate that the established MMC prototype can successfully operate from 0 to 1000 Hz with the rated dc bus voltage and load currents



(a)



(b)



(c)

Fig. 15. Experimental results for the single SiC-based SM. (a) Turn-ON transient. (b) Turn-OFF transient. (c) Overcurrent protection.

required. Especially, the prototype can operate very well at 0 Hz condition without any instabilities.

Fig. 18 illustrates the detailed waveforms of the capacitor voltage and the arm current at low frequencies. The tested frequency is 10 Hz, with 400 Hz common-mode voltage injection. Results show that the capacitor voltage is stabilized around 1.15 kV with ripples less than $\pm 11.5\%$. The peak circulating current reaches around 350 A, but the RMS value is around 140 A, which is far less than the current limitation of the selected SiC devices. Similar waveforms can be observed for the rest of the frequencies in the LF mode, which is not repeated here. Thus, the experimental results in Fig. 18 validate the capacitor voltage, and the arm current is under well control at low frequencies.

Based on the steady-state results, the load current THD and the SM capacitor voltage ripples are further analyzed and results are shown in Fig. 19. The current THD for the full-range ac frequency is less than 2% for all cases tested, which matches the simulated result very well. At the base frequency (1000 Hz) is only 1.24%. The capacitor voltage ripple is within $\pm 12\%$ for the full-frequency range with 100% base load current. Due to the circulating current control, the excessive voltage fluctuations at low frequencies, such as 10 Hz, are minimized. Results in Fig. 19 verify that not only does the established MMC prototype has an excellent performance in the load current harmonics but also the strong balancing capability of SM voltages for the entire frequency range.

It is proven that the higher switching frequency enables a high injection frequency (400 Hz) to not only minimize the SM size but also the load current harmonics, even at the fundamental frequency (1000 Hz). Using the described topology and control scheme, the designed MMC meets successfully the targets of both load current THD and SM capacitor voltage ripple targets.

We also investigate the dynamic performance of the established MMC prototype. Fig. 20 shows the results when a large current step change is applied. The tested dynamic performance results are shown at 200 Hz in Fig. 20(a) and 1000 Hz in (b), where the commanded current step change is 50% of the base current, from 50 to 150 A peak. The results verify that the MMC prototype achieves a very fast dynamic response to the command, in less than 1 ms. During the transition, no stability issue is observed on the load voltage and current. Hence, the results in Fig. 20 demonstrate the fast and robust current dynamic capability of the MMC prototype.

C. *Tested Power Loss and System Efficiency*

The power loss of the semiconductors in SMs is calculated at the rated operation. The frequency is 1000 Hz with 200 A load current. The thermocouples are placed on the case surface of the power modules. Fig. 21 shows the temperature measurements for about 45 min. In the figure, the rated operation starts after 5 min, and lasts for 40 min until the thermal steady state is reached. The hottest SM is close to the arm inductors in the middle layer, which experiences a less-effective cooling effect. The coldest SM is located outside far away from the coupled inductors. The recorded temperature rise in the hottest and coldest SMs is 45.3 °C and 33.7 °C, respectively. The temperature inside the MMC tower rises by 7.1 °C.

The hottest SM is considered as the representative one in the power loss calculation. The power module loss is calculated from the temperature curves and the thermal resistance, as shown in the following equations [29]:

$$P_d = \frac{\Delta T_{\text{case}} - \Delta T_{\text{ambient}}}{R_{\text{th,c}\to\text{hs}} + R_{\text{th,hs}\to\text{a}}} = \frac{45.3\,^\circ\text{C} - 7.1\,^\circ\text{C}}{0.035\,^\circ\text{C/W} + 0.20\,^\circ\text{C/W}} = 162.5\,\text{W} \tag{7}$$

$$\Delta T_{\text{junction}} = \Delta T_{\text{ambient}} + (R_{\text{th,j}\to\text{c}} + R_{\text{th,c}\to\text{hs}} + R_{\text{th,hs}\to\text{a}})$$
$$P_d = 59.9\,^\circ\text{C} \tag{8}$$

where P_d is the power module loss, $R_{\text{th,j}\to\text{c}}$, $R_{\text{th,c}\to\text{hs}}$, and $R_{\text{th,hs}\to\text{a}}$ are the thermal resistances of the junction to case surface, case surface to heatsink, and heatsink to ambient,

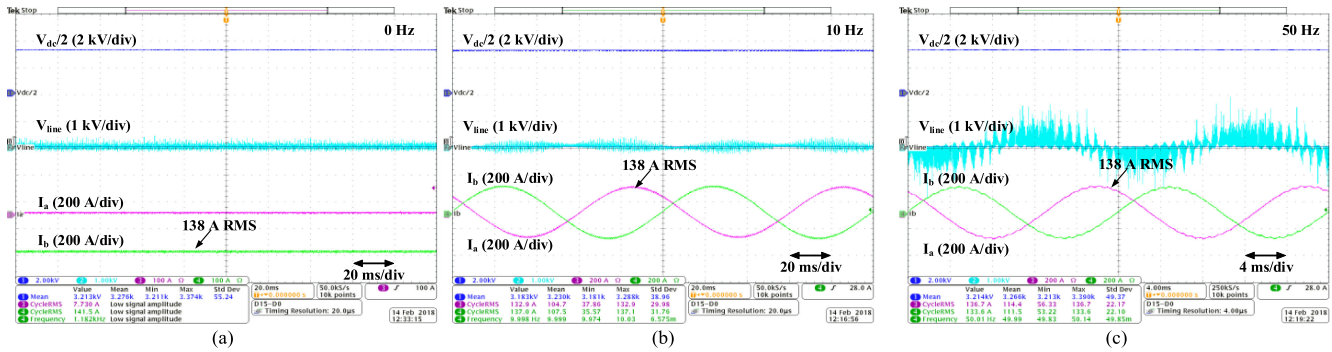


Fig. 16. Experimental results for the SiC-based MMC in low-frequency mode. (a) 0 Hz. (b) 10 Hz. (c) 50 Hz. Half dc bus voltage (2 kV/div), line voltage (1 kV/div), and phase-A and phase-B load currents (200 A/div).

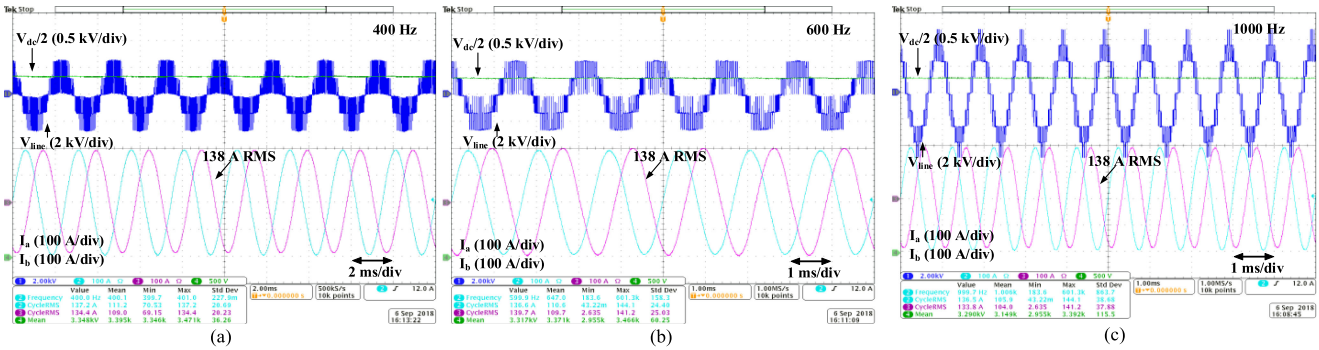


Fig. 17. Experimental results for the SiC-based MMC in high-frequency mode. (a) 400 Hz. (b) 600 Hz. (c) 1000 Hz. Half dc bus voltage (0.5 kV/div), line voltage (2 kV/div), and phase-A and phase-B load currents (100 A/div).

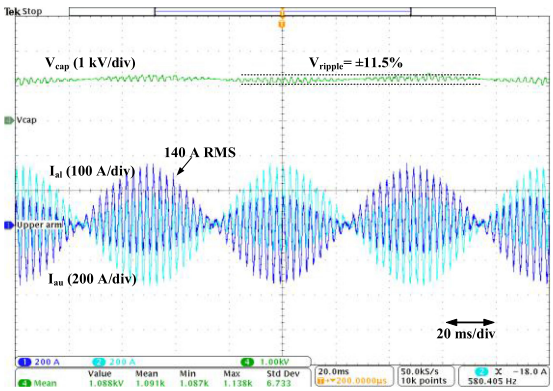


Fig. 18. Experimental results of capacitor voltage, upper-arm and lower-arm currents at low frequency (10 Hz). Capacitor voltage (1 kV/div), and phase-A upper- and lower-arm currents (200 A/div).

respectively. Their values are 0.09 °C/W, 0.035 °C/W, and 0.20 °C/W, respectively. ΔT_{case}, $\Delta T_{\text{ambient}}$, and $\Delta T_{\text{junction}}$ are the temperature rise in case, ambient, and junction temperature. Thus, the semiconductor loss for each SM is approximately 162.5 W, and the junction temperature of the SiC device is around 86 °C for the rated operation based on the calculation.

Table III lists the power loss distribution of semiconductors, capacitors, and arm inductors. The capacitor loss is calculated

TABLE III
LOSS CALCULATION OF THE 7-KV SiC-BASED MMC

	Single (W)	Number	Full-scale system (W)
Power modular loss	162.5	36	5850
Capacitor loss	10	36	360
Arm inductor loss	83.4	3	241
Total loss	/	/	6451

based on the equivalent series resistance (2.2 mΩ) and the bleeding resistor (400 kΩ), and the arm inductor loss is obtained from the FEA. Results in Table II show the estimated total power loss of the developed prototype is around 6.45 kW, resulting in 99.35% system efficiency for at the rated frequency and the output current condition. The tested power device loss matches well with the analyzed value in Section IV. For the equivalent 4.16-kV/1-MVA commercial motor drive systems, the reported peak efficiency is approximately 98% with 20 kW losses [5]. Thus, the developed MMC prototype can significantly reduce power losses and improve efficiency.

D. Volume and Power Density

For the next-generation MV megawatt VFD development, one critical aspect is the dramatic volume reduction compared with the existing traditional Si-based technology. For the designed

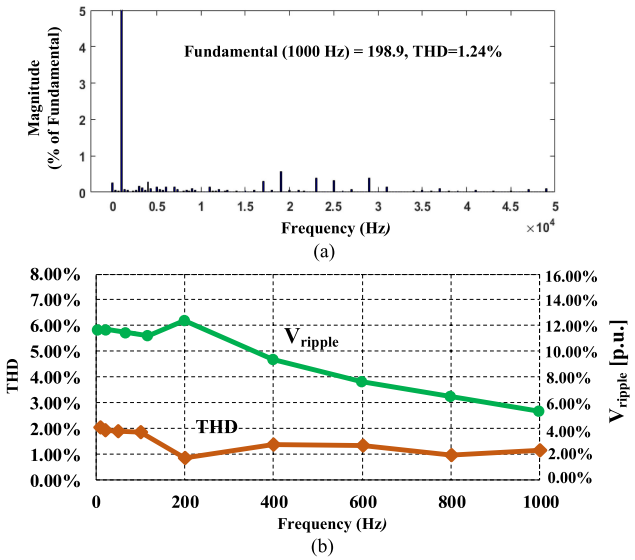


Fig. 19. Load current THD and SM capacitor voltage ripples. (a) FFT analysis of THD at 1000 Hz. (b) Distribution of THD and SM capacitor voltage ripples (V_{ripple}) from 0 to 1000 Hz.

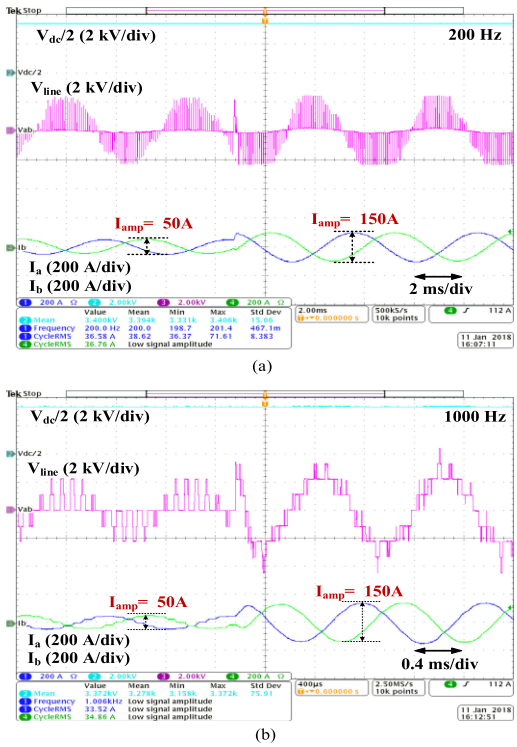


Fig. 20. Experimental results of the dynamic current response. (a) 50% current step change at 200 Hz. (b) 50% current step change at 1000 Hz. Half dc bus voltage (2 kV/div), line voltage (2 kV/div), and phase-A and phase-B load currents (200 A/div).

and tested 7-kV SiC-based MMC prototype, the total volume is only 1.19 m^3. Hence, the calculated power density and footprint are 0.85 MVA/m^3 and 0.75 m^2/MVA, respectively. Fig. 22 shows the comparison results with the baseline of the traditional MV Si VFD from the U.S Department of Energy [4], [5]. It is clear that the volume of the SiC-based VFD prototype can be 75%

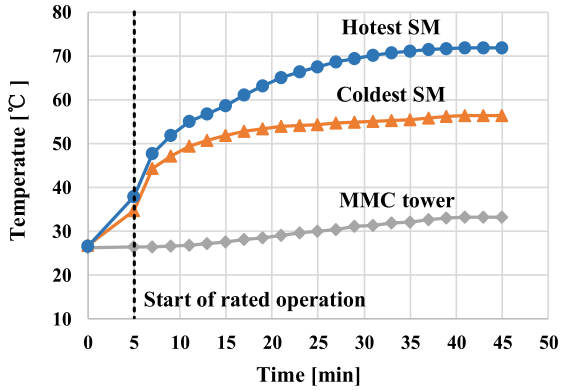


Fig. 21. Temperature measurement of the SiC power module at the rated voltage, current, and frequency.

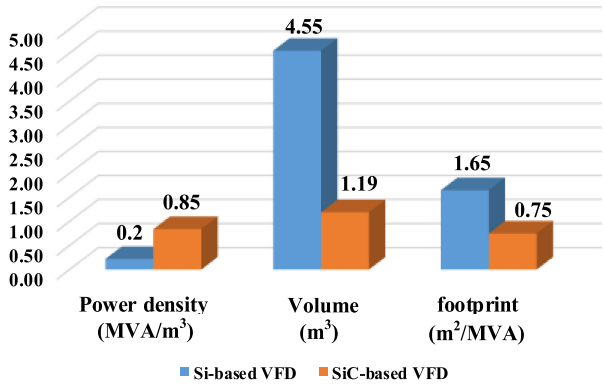


Fig. 22. Comparison of the SiC-based MMC prototype and the traditional Si-based VFD.

smaller, resulting in the 325% power density compared with the baseline. The footprint of the established VFD is also reduced by approximately 50%.

VII. Conclusion

This article presents the design and development of a 7-kV dc bus, 1-MVA MMC prototype using 1.7-kV SiC MOSFETs for high-speed MV VFDs. The implementation of the SiC devices can dramatically increase the common-mode voltage frequency, resulting in over 50% capacitor size reduction without compromising the system performance compared with the Si-based solution. Validated by the experimental results, the SM and MMC with the proposed design can successfully operate at MV high-power conditions. Especially, the single SM realizes fast switching and strong overcurrent protection effectively. The full-scale MMC prototype has a wide operation frequency from 0 to 1000 Hz, and extra low harmonic performance of $<$2%. Besides, the designed prototype can achieve a large and fast current dynamic demand without any instability issues.

The analyzed switch power loss is matched well with the tested result, and the tested system peak efficiency is approximately 99.35%. Compared with the traditional Si-based MV VFDs, the developed SiC-based MMC prototype achieves 75% volume reduction, resulting in 325% of the power density

compared with the baseline. Thus, with the proven excellent testing performance and reduced volume, the developed MMC prototype can significantly advance the next-generation MV VFD technology based on the up-to-date WBG devices.

REFERENCES

[1] H. Abu-Rub, S. Bayhan, S. Moinoddin, M. Malinowski, and J. Guzinski, "Medium-voltage drives: Challenges and existing technology," *IEEE Power Electron. Mag.*, vol. 3, no. 2, pp. 29–41, Jun. 2016.

[2] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, Jan. 2016.

[3] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[4] A. Morya, M. Moosavi, M. C. Gardner, and H. A. Toliyat, "Applications of wide bandgap (WBG) devices in ac electric drives: A technology status review," in *Proc. IEEE Int. Electr. Mach. Drives Conf.*, Miami, FL, USA, 2017, pp. 1–8.

[5] "Next generation electric machines: Megawatt class motors," Dept. Energy, Office Energy Efficiency Renewable Energy (EERE), DE-FOA-0001208. 2015. [Online]. Available: https://energy.gov/eere/amo/next-generation-electric-machines

[6] J. Kolb, F. Kammerer, and M. Braun, "Dimensioning and design of a modular multilevel converter for drive applications," in *Proc. 15th Int. Power Electron. Motion Control Conf.*, 2012, pp. LS1a-1.1-1-LS1a-1.1-8.

[7] J. Pan *et al.*, "Zero-cost closed-loop discharging method for modular multilevel converter submodules without external circuits," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 4846–4854, Sep./Oct. 2019.

[8] Z. Ke *et al.*, "Optimal submodule capacitor sizing for modular multilevel converters with common mode voltage injection and circulating current control," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 1802–1808.

[9] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[10] S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of 4-kV neutral-point-clamped, flying-capacitor, and series-connected H-Bridge multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1032–1040, Jul./Aug. 2007.

[11] R. Marquardt, A. Lesnicar, and J. Hildinger, "Modulares Stromrichterkonzept fur Netzkupplungsanwendungen bei hohen Spannungen," *presented at the ETG-Fachtagungen*, Bad Nauheim, Germany, 2002.

[12] M. Hiller, D. Krug, R. Sommer, and S. Rohner, "A new highly modular medium voltage converter topology for industrial drive applications," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–10.

[13] A. J. Korn, M. Winkelnkemper, and P. Steimer, "Low output frequency operation of the modular multilevel converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 3993–3997.

[14] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded control system of the modular multilevel converter for feeding variable-speed drives," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 349–357, Jan. 2015.

[15] M. Hagiwara, I. Hasegawa, and H. Akagi, "Start-up and low-speed operation of an electric motor driven by a modular multilevel cascade inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1556–1565, Jul./Aug. 2013.

[16] J.-J. Jung, H.-J. Lee, and S.-K. Sul, "Control strategy for improved dynamic performance of variable-speed drives with modular multilevel converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 2, pp. 371–380, Jun. 2015.

[17] B. Li *et al.*, "An improved circulating current injection method for modular multilevel converters in variable-speed drives," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7215–7225, Nov. 2016.

[18] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[19] A. Dekka, B. Wu, and N. R. Zargari, "A novel modulation scheme and voltage balancing algorithm for modular multilevel converter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 1, pp. 432–443, Jan./Feb. 2016.

[20] J. Salmon, J. Ewanchuk, and A. M. Knight, "PWM inverters using split-wound coupled inductors," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2001–2009, Nov./Dec. 2009.

[21] M. Glinka, "Prototype of multiphase modular-multilevel-converter with 2 MW power rating and 17-level-output-voltage," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, Aachen, Germany, 2004, vol. 4, pp. 2572–2576.

[22] D. Peftitsis *et al.*, "High-Power modular multilevel converters with SiC JFETs," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 28–36, Jan. 2012.

[23] J. Yu, R. Burgos, N. R. Mehrabadi, and D. Boroyevich, "Design of a SiC-based modular multilevel converter for medium voltage dc distriution system," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Tampa, FL, USA, 2017, pp. 467–473.

[24] Y. Du, S. Baek, S. Bhattacharya, and A. Q. Huang, "High-voltage high-frequency transformer design for a 7.2 kV to 120 V/240 V 20 kVA solid state transformer," in *Proc. 36th Annu. Conf. IEEE Ind. Electron. Soc.*, Glendale, AZ, USA, 2010, pp. 493–498.

[25] H. Li *et al.*, "Hardware design of a 1.7 kV SiC MOSFET based MMC for medium voltage motor drives," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 1649–1655.

[26] J. Pan *et al.*, "Circulating current resonant oscillation in modular multilevel converters for variable frequency operation and its suppression method," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 686–692.

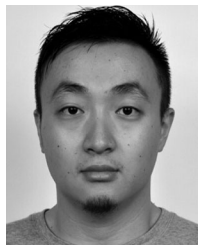
[27] Q. A. Le and D.-C. Lee, "A novel six-level inverter topology for medium-voltage applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7195–7203, Mar. 2016.

[28] D. Graovac and M. Pürschel, "IGBT power losses calculation using the data-sheet parameters," Infineon Technologies AG, Neubiberg, Germany, Jan. 2009.

[29] NXP, "Thermal Analysis of Semiconductor Systems," White Paper, 2012. [Online]. https://www.nxp.com/docs/en/white-paper/BasicThermalWP.pdf

Jianyu Pan (Member, IEEE) received the B.S. and M.S. degrees from Chongqing University, Chongqing, China, in 2011, and 2014, respectively, and the Ph.D. degree from The Ohio State University, Columbus, OH, USA, in 2019, all in electrical engineering.

He is currently an Assistant Professor with the School of Electrical Engineering, Chongqing University, Chongqing, China. His main research interests include power converters, electric machine control, wide-bandgap semiconductor applications, and high-voltage engineering.



Ziwei Ke (Member, IEEE) received the B.S. degree from the Zhejiang University of Technology, Hangzhou, China, in 2012, the M.S. degree from Oregon State University, Corvallis, OR, USA, in 2015, and Ph.D. degree from The Ohio State University, Columbus, OH, USA, in 2019, all in electrical engineering.

He is currently an Electrical Engineer with Wisk Aero, Mountain View, CA, USA. His research interests include electric machine control, power electronics, and firmware programming.

Muneer Al Sabbagh (Member, IEEE) was born in Sharjah, UAE, in 1987. He received the B.S. degree from the American University of Sharjah, Sharjah, UAE, in 2009, and the M.S. degree from RWTH Aachen University, Aachen, Germany, in 2012. He is currently working toward the Ph.D. degree with The Ohio State University, Columbus, OH, USA.

From 2012 to 2013, he was an R&D Control Software Engineer with ABB, Turgi, Switzerland. His research interests include the control of electric drives and power converters.

He Li (Member, IEEE) received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2012, and the Ph.D. degree from The Ohio State University, Columbus, OH, USA, in 2018.

He is currently a Senior Electronic Design Engineer with Tesla working on supercharger and energy storage system.

Dr. Li was a recipient of the IEEE IAS Will Portnoy Award in 2018.

Karun Arjun Potty (Member, IEEE) received the B.S degree in instrumentation and control systems engineering from the Manipal Institute of Technology, Manipal, India, in 2015. He is currently working toward the Ph.D. degree in electrical engineering with The Ohio State University, Columbus, OH, USA.

He was an intern with the Institute of Electrical Power Engineering, TU Dresden, Dresden, Germany, from June to August 2014. His research interests include ac–dc microgrids and their stability, wide-bandgap semiconductor applications, transportation electrification, and high-power motor drives.

Will Perdikakis received the MBA and M.S.E.E. degress from the University of Hartford, West Hartford, CT, USA, in 2013. He is currently working toward the Ph.D. degree with The Ohio State University (OSU), Columbus, OH, USA.

Before OSU, he worked on an inverter design team at Carrier (part of United Technologies) for ten years.

Risha Na (Member, IEEE) received the Ph.D. degree from the Harbin University of Science and Technology, Harbin, China, in 2013.

Since April 2013, he was an Assistant Professor with the Department of Electrical and Electronic Engineering, Harbin University of Science and Technology, Harbin, China. He is currently a Research Scientist with The Ohio State University, Columbus, OH, USA. His research interests include power electronics and applications of power electronics in medium-voltage drive systems.

Julia Zhang (Member, IEEE) received the Ph.D. degree in electrical engineering from The Ohio State University, Columbus, OH, USA, in 2010.

She is an Assistant Professor with the Center for High Performance Power Electronics, The Ohio State University, Columbus, OH, USA. From 2010 to 2012, she was a Control Engineer with Ford Motor Company, Dearborn, MI, USA. From 2012 to 2017, she was an Assistant Professor with Oregon State University. Her research interests include electric machines, drives, power electronics, and high-voltage engineering.

Jin Wang (Senior Member, IEEE) received the B.S. degree from Xi'an Jiaotong University, Xi'an, China, in 1998, the M.S. degree from Wuhan University, Wuhan, China, in 2001, and the Ph.D. degree from Michigan State University, East Lansing, MI, USA, in 2005, all in electrical engineering.

From September 2005 to August 2007, he was a Core Power Electronics Engineer with Ford Motor Company. He joined The Ohio State University in 2007 as an Assistant Professor and was promoted to Associate Professor in 2013 and as a Full Professor in 2017. His research interests include wide-bandgap power devices and their applications, high-voltage and high-power converter/inverters, integration of renewable energy sources, and electrification of transportation. He has more than 170 peer-reviewed journal and conference publications, and 8 patents.

Dr. Wang was a recipient of the IEEE Power Electronics Society Richard M. Bass Young Engineer Award in 2011, the National Science Foundation's CAREER Award in 2011, the Ralph L. Boyer Award for Excellence in Undergraduate Teaching Innovation at The Ohio State University, in 2012, the Lumley Research Award in 2013, and the Harrison Faculty Award for Excellence in Engineering Education in 2017. He served as the General Chair and the Steering Committee Chair for the IEEE Future Energy Challenge, in 2016 and 2017, respectively. From 2008 to 2014 he was an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. He is currently an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He initiated and served as the General Chair for the 1st IEEE Workshop on wide bandgap power devices and applications in 2013.

Longya Xu (Fellow, IEEE) received the M.S. and Ph.D. degrees from the University of Wisconsin-Madison, Madison, WI, USA, in 1986 and 1990, both in electrical engineering.

He is currently a Professor and Director of the Center for High Performance Power Electronics, The Ohio State University, Columbus, OH, USA. His research interests include the design and control of novel electric machines, power electronics, and digital technology for electrified transportation and renewable energy systems.

Dr. Xu was a recipient of several IEEE prestigious awards, including the First Prize Paper Award in 1992 from Industry Drive Committee IEEE/IAS, Best Transaction Paper Award in 2013, Outstanding Achievement Award in 2014, the highest society award, from the IEEE Industry Application Society and the Nikola Tesla Award for his outstanding contributions to the generation and utilization of electric power. He has served as the Chairperson of the Electric Machine Committee of IEEE/IAS and an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS over the past two decades. He was a Member-at-Large on IEEE/IAS Executive Board and the Conference Co-Chair for IEEE Transportation Electrification Conference and Expo, AP 2014, 2016, and 2019.