Letters

Three-Terminal Si/SiC Hybrid Switch

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***Abstract*—A Si/SiC hybrid switch is an innovative power semiconductor switch realized by paralleling a Si insulated-gate bipolar transistor (IGBT) and a SiC device (metal-oxide semiconductor field-effect transistor (MOSFET) or junction field-effect transistor). The Si/SiC hybrid switch combines advantages of Si IGBT's high conduction capability and SiC device's fast switching speed, and effectively addresses Si IGBT's high turn-OFF loss issue and SiC MOSFET's high cost concern. However, to control the hybrid switch, two separate gate drivers are usually needed, which increases the complexity and cost. In this letter, a simple and effective gate driver circuit is designed for the Si/SiC hybrid switch, which requires only one control signal and gate driver circuit to drive both Si IGBT and the SiC device, making the hybrid switch a typically three-terminal device. The operation principles and design guidelines are presented and analyzed. A three-terminal 1200-V, 200-A hybrid switch prototype in a half-bridge configuration is developed and experimental results verify its effectiveness.**

***Index Terms*—Gate driver circuit, hybrid switch, IGBT, junction field-effect transistor (JFET), metal-oxide semiconductor field-effect transistor (MOSFET), SiC.**

I. Introduction

SiC devices are increasingly popular in many emerging applications like electric vehicle (EV) chargers and powertrain, energy storage, etc., due to their superior performances compared to Si insulated-gate bipolar transistors (IGBTs). Thanks to the majority carrier conduction mechanism, SiC metal-oxide semiconductor field-effect transistors (MOSFETS) and junction field-effect transistors (JFETs) both have ultrafast switching speed and low switching losses over Si IGBT. However, the much higher cost, primarily due to more expensive SiC wafers and fabrication process, impedes its wide adoptions. Therefore, the Si IGBTs are still the workhorse for important high volume applications such as motor drives, photovoltaic (PV) inverters, etc. The Si IGBTs have the advantages of simple Metal-oxide Semiconductor (MOS) gate control, low forward voltage drop due to the conductivity modulation mechanism, and much lower cost compared to the SiC devices due to matured Si wafer and fabrication technologies. The main disadvantage of the IGBT is the large switching losses, especially the high turn-OFF losses, which limit its power conversion efficiency and allowable switching frequency.

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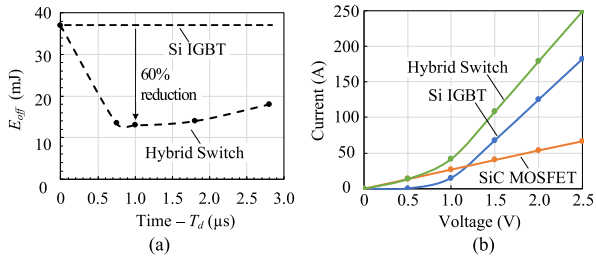

Fig. 1. Performances of the 1200-V, 150-A Si IGBT and 1200-V, 25-mΩ SiC MOSFET-based hybrid switch. (a) Measured turn-OFF loss (E_{off}) of the hybrid switch with different turn-OFF delay time (T_d). (b) *I*–*V* curves of the 150-A IGBT, 25-mΩ SiC MOSFET, and the hybrid switch at 125 °C [8].

Understanding the complementary properties of the Si IGBT and SiC devices, it is natural to consider the integration of the two devices together as one. We proposed the novel Si/SiC hybrid switch concept, known as FREEDM-Pair [1]–[3], by paralleling an Si IGBT with an SiC switch (e.g., MOSFET or JFET). One proven simple and advantaged gate control strategy for the Si/SiC hybrid switch is to fire the Si IGBT and the SiC device simultaneously during turn-ON and switch-OFF the SiC device with a special designed delay time after Si IGBT turns OFF [4]. Because of faster turn-ON speed of the SiC device (e.g., MOSFET), most of the current is turned ON by the SiC MOSFET and the IGBT is turned ON under the zero-voltage switching (ZVS) condition. During the turn-OFF, the Si IGBT is turned OFF first under ZVS condition and after a carefully selected delay time, the SiC MOSFET is turned OFF. In this way, the switching losses, especially the turn-OFF loss of the Si IGBT is significantly reduced due to the ZVS condition. In Fig. 1, a 1200-V, 200-A hybrid switch [8] is tested and demonstrated up to 60% turn-OFF loss reduction (from 37 to 14 mJ) compared to the Si IGBT with $\sim$1 μs optimal delay time (T_d). The Si/SiC hybrid switch also has better conduction characteristics compared to the Si IGBT by the combined current conduction capability of the unipolar and bipolar devices, as shown in Fig. 1(b).

Owing to the abovementioned advantages, the Si/SiC hybrid switch is the topic of a large number of publications. In [4], how to achieve the thermal balance between the Si IGBT and

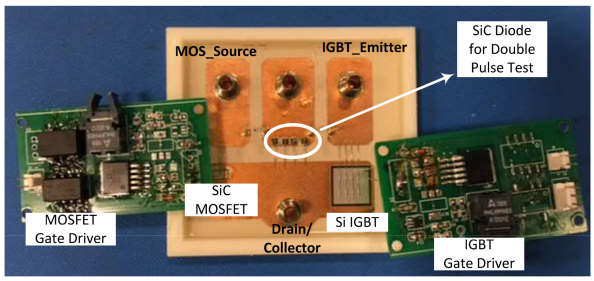

Fig. 2. One SiC MOSFET and Si IGBT-based hybrid switch example needing two separate gate drivers [3].

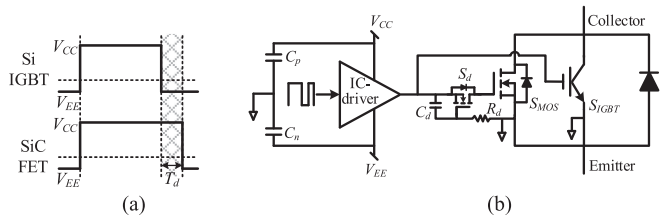

Fig. 3. (a) Gate control pattern to be realized by the proposed single gate driver circuit. (b) Proposed single gate driver circuit for the Si/SiC hybrid switch with turn-OFF delay time generation capability.

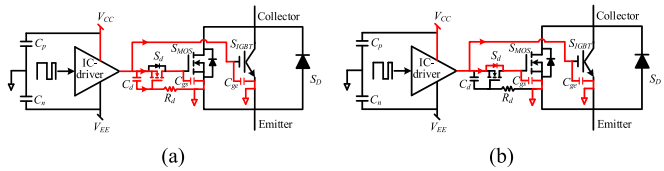

Fig. 4. Turn-ON current paths of the proposed single gate driver circuit. (a) Phase I: Gate current through LV MOSFET S_d channel. (b) Phase II: Gate current through LV MOSFET S_d body diode.

the SiC MOSFET was discussed, and Wang *et al.* [5] studies the short circuit ruggedness of the Si/SiC hybrid switch. In [6], we find the SiC MOSFET can reduce the IGBT losses even if the SiC MOSFET and the Si IGBT share the same gate signal. He *et al.* [7] introduces a current-dependent switching strategy, which is especially suitable for ac/dc inverters. Our group also proposed and verified various Si/SiC hybrid switch configurations [1]–[3] based on either SiC MOSFET or JFET. In [2] and [3], normally, a 6-kV OFF SiC JFET-based hybrid switch is developed and tested for the first time, and the SiC MOSFET-based hybrid switch is customized and experimentally verified in [3].

With the increasing popularity of the Si/SiC hybrid switch topic, there is still a need to optimize its performance. One significant improvement needed is the gate driver circuit design with delay time generation function for the hybrid switch. In most papers [1]–[7], two separate control signals and gate driver circuits are required to drive the two paralleled devices as shown in Fig. 2, especially when there is a turn-OFF delay between the Si IGBT and the SiC MOSFET. This is not preferred in a converter design, as this will double the control signal/channels needed, as well as double the driver circuits. In [8], Zhang *et al.* designed a single gate driver circuit with delay time generation capability for the Si/SiC hybrid switch and experimentally verified its functions in a 1200-V, 200-A hybrid switch for the first time. In the proposed gate driver circuit, only one control signal is needed to drive both the Si IGBT and the SiC MOSFET in the hybrid switch, and the specially designed gate driver circuit will turn ON the SiC MOSFET simultaneously with the Si IGBT and generate the turn-OFF delay time for the SiC MOSFET automatically. Compared to [8], the operation principles during the turn-ON and turn-OFF transient are more clearly analyzed with the help of the low voltage (LV) MOSFET and resistor capacitor (RC) circuit voltage waveforms, and the design guidelines of the proposed circuit is introduced for the first time in Part II, and the finalized parameters for the proposed circuit are summarized. The proposed circuit can be easily integrated and packaged inside the hybrid switch module, making the hybrid switch a typically three-terminal device (instead of four terminals including two gates).

II. Operation Principles and Design Guidelines of the Single Gate Driver Circuit

A. Operation Principles of the Single Gate Driver Circuit

In this section, the operation principles of the proposed single gate driver circuit are elaborated using a SiC MOSFET and Si IGBT-based hybrid switch as an example. As previously discussed, one proven simple and advantaged gate control strategy for the Si/SiC hybrid switch is to turn ON the Si IGBT and the SiC MOSFET simultaneously and turn OFF the SiC MOSFET with a carefully selected delay time after the Si IGBT turn-OFF, as shown in Fig. 3(a). V_{CC} is the positive gate voltage (typically +18 V) to turn ON the SiC MOSFET and Si IGBT, while V_{EE} is the negative gate voltage (typically –5 V) to guarantee the Si IGBT and SiC MOSFET are reliably turned OFF. T_d is the optimal turn-OFF delay time between the Si IGBT and the SiC MOSFET.

Fig. 3(b) shows the proposed single gate driver circuit to control the Si IGBT and SiC MOSFET's gate voltages according to the gate control pattern in Fig. 3(a). The single gate driver circuit consists of three major components: an LV (40∼100 V) MOSFET S_d connected to the SiC MOSFET gate terminal and an RC delay circuit (R_d and C_d) with time constant τ. The RC delay circuit time constant τ determines the turn-OFF delay time T_d between the Si IGBT and the SiC MOSFET, which will be elucidated later. How the proposed single gate driver circuit realizes the desired turn-ON and turn-OFF gate signals for the hybrid switch is explained respectively as following.

During the turn-ON transient, shown in Fig. 4, positive gate voltage V_{CC} is applied by the gate driver integrated circuit (IC). The gate to emitter capacitor (C_{ge}) of the Si IGBT is charged through a gate resistor or directly by the gate driver IC. The turn-ON of the SiC MOSFET is divided into two phases: Phase I in Fig. 4(a), the current from the gate driver IC conducts through the channel of the LV MOSFET S_d (as the initial voltage $V_{gs,Sd}$ of the delay capacitor C_d is $-V_{EE}$, and S_d is in ON state); Phase II in Fig. 4(b): the current conducts through the body diode of S_d (as $V_{gs,Sd}$ falls and S_d turns OFF). Although there are two phases for the SiC MOSFET turn-ON, the Si IGBT and the SiC MOSFET are turned ON simultaneously, as shown in Fig. 6(a), where the blue line is the gate voltage $(V_{gs,Si})$ of the Si IGBT and the yellow line is the gate voltage $(V_{gs,\mathrm{SiC}})$ of the SiC MOSFET. The

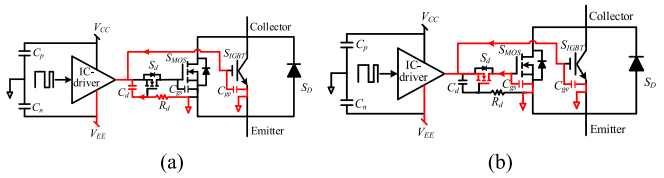

Fig. 5. Turn-OFF current paths of the proposed single gate driver circuit. (a) Phase I: Delay period. (b) Phase II: Turn-OFF period.

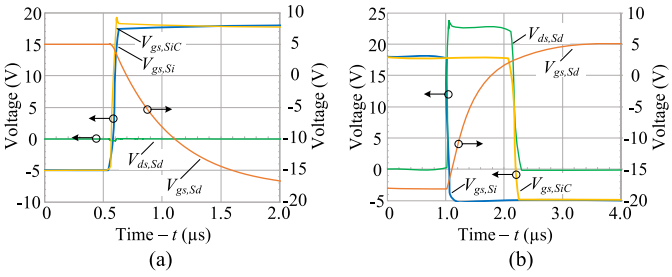

Fig. 6. Voltage waveforms of the single gate driver circuit. (a) During turn-ON process. (b) During turn-OFF process.

only concern is in Phase II, the body diode of S_d could introduce an LV drop (∼0.7 V) for the gate of the SiC MOSFET. However, this can be easily mitigated by slightly increase the positive gate voltage V_{CC}.

Fig. 5 shows the turn-OFF process of the proposed single gate driver circuit, which includes two phases: Phase I, delay period, as in Fig. 5(a), and Phase II, turn-OFF period, as in Fig. 5(b). Similarly, the negative gate voltage V_{EE} is applied directly or through a gate resistor to the gate of the Si IGBT by the gate driver IC. In Phase I, the initial voltage [$V_{gs,Sd}$, orange line in Fig. 6(b)] of the delay capacitor C_d is $-V_{CC}$, and S_d is turned OFF (green line in Fig. 6(b) shows S_d drain-to-source voltage $V_{ds,Sd}$), impeding the gate driver IC current discharge the gate capacitor C_{gs} of the SiC MOSFET. The SiC MOSFET gate voltage [$V_{gs,\mathrm{SiC}}$, yellow line in Fig. 6(b)] maintains high before S_d is turned ON. As the current from the gate driver IC charges the delay capacitor C_d through the resistor R_d, as shown in Fig. 5(a), the gate voltage ($V_{gs,Sd}$) of S_d reaches its threshold voltage (V_{th}) and S_d is turned ON [happening at $t = 2$ μs in Fig. 6(b)]. After S_d is turned ON, the turn-OFF process enters Phase II in Fig. 5(b), and the current from the gate driver IC discharges the gate capacitor of the SiC MOSFET through S_d, and the gate voltage of the SiC MOSFET starts to fall. Therefore, the SiC MOSFET is turned OFF after a delay time T_d. The RC delay circuit (C_d and R_d) and the threshold voltage (V_{th}) of S_d determine the turn-OFF delay time T_d, which is derived later.

B. Design Guidelines of the Single Gate Driver Circuit

The proposed gate driver circuit contains three key components: the LV MOSFET S_d, and the RC delay circuit (C_d and R_d). In this section, the guidelines to select S_d, C_d, and R_d are elucidated.

The RC delay circuit time constant τ determines the turn-OFF delay time T_d between the Si IGBT and the SiC MOSFET. Fig. 7(a)

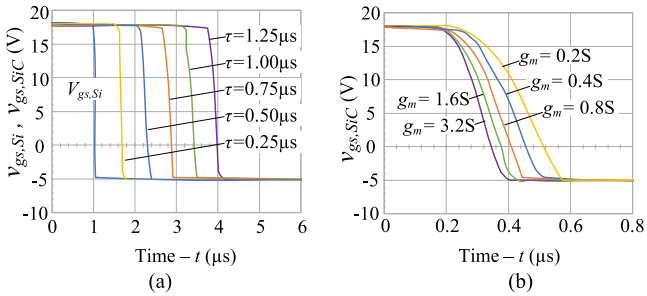

Fig. 7. (a) Simulated turn-OFF waveforms of the SiC MOSFET with different RC time constant τ. (b) Turn-OFF waveforms of the SiC MOSFET with different transconductance g_m of the LV MOSFET S_d.

shows the simulated turn-OFF waveforms of the SiC MOSFET with different RC time constant τ. The light blue line is the gate voltage $V_{gs,Si}$ of the Si IGBT during turn-OFF transient, and the other lines are the SiC MOSFET's gate voltage $V_{gs,\mathrm{SiC}}$ tested with different RC delay circuit time constant τ. The higher time constant τ leads to a longer turn-OFF delay time T_d. For example, when $\tau = 0.5$ μs, the SiC MOSFET is turned OFF 1 μs ($T_d = 1$ μs) after the Si IGBT turn-OFF. The relationship between T_d and τ can be derived from (1) and (2) as

$$v_{gs,S_d}(t) = (V_{CC} - V_{EE})(1 - e^{-t/\tau}) \tag{1}$$

where $v_{gs,Sd}(t)$ is the gate voltage of the LV MOSFET S_d; V_{CC}, and V_{EE} are the positive gate voltage and negative gate voltage, respectively; and τ is the RC delay circuit time constant. Based on the analysis in previous section, the SiC MOSFET starts to turn OFF when $v_{gs,S_d}(t) = V_{th}$ (V_{th} is S_d threshold voltage). Then, the delay time can be derived as

$$T_d = -\tau \ln\left(1 - \frac{V_{th} + V_{CC}}{V_{CC} - V_{EE}}\right). \tag{2}$$

From (2), the required time constant τ can be calculated based on the desired turn-OFF delay time T_d. It can also be found that the delay time is related to S_d's threshold voltage V_{th}. As the turn-ON gate voltage for S_d is $-V_{EE}$ (usually 5 V), a relative low threshold voltage LV MOSFET S_d is preferred to guarantee its full turn-ON.

Usually, higher (more negative) *dv/dt* of the gate voltage is preferred for SiC MOSFET to speed up its turn-OFF and reduce its losses. The *dv/dt* of the SiC MOSFET's gate voltage [$V_{gs,\mathrm{SiC}}$, yellow line in Fig. 6(b)] depends on the turn-ON speed or the *dv/dt* of the LV MOSFET's (S_d's) drain-to-source voltage [$V_{ds,Sd}$, green line in Fig. 6(b)]. The turn-ON *dv/dt* of the LV MOSFET's drain-to-source voltage can be derived as [9]

$$\frac{dv_{gs,SiC}(t)}{dt} = \frac{dv_{ds,S_d}(t)}{dt} = \frac{V_{EE}+V_{th}}{R_d C_{gd,S_d}} + \frac{I_{ds,S_d}}{g_m R_d C_{gd,S_d}} \tag{3}$$

where V_{EE} is the negative gate voltage (usually –5 V), V_{th} is the threshold voltage (2∼4 V) of S_d, $C_{gd,Sd}$ is S_d's gate-to-drain parasitic capacitance, $I_{ds,Sd}$ is S_d's drain-to-source current, and g_m is the S_d's transconductance. From (3), it can be concluded that to achieve high (more negative) gate voltage *dv/dt* of the SiC MOSFET, an LV MOSFET S_d with low parasitic capacitance

TABLE I
SPECIFICATIONS OF THE GATE DRIVER CIRCUIT

Components	Symbol	Value
LV MOSFET	S_d	NVR5198NL (60 V, 0.2 Ω, g_m=3 S, V_{th}=2.1 V)
Delay capacitor	C_d	2.5 nF
Delay resistor	R_d	200 Ω
RC time constant	τ	0.5 μs
Positive gate voltage	V_{CC}	18 V
Negative gate voltage	V_{EE}	-5 V

$C_{gd,Sd}$, low threshold voltage V_{th} and high transconductance g_m is preferred. Fig. 7(b) shows the SiC MOSFET gate voltages during turn-OFF transient with different transconductance g_m of the LV MOSFET S_d. It verifies that high transconductance g_m leads to faster SiC MOSFET gate voltage *dv/dt*, but once the transconductance g_m of the LV MOSFET is high enough ($g_m > 3$ S), it will not be the key limiter for high *dv/dt*. In the later prototype development, an LV MOSFET with $g_m = 3$ S is selected, as shown in Table I.

Based on the above derivations, the following components are selected and listed in Table I to achieve 1 μs optimal turn-OFF delay time [based on Fig. 1(a)] between the Si IGBT and the SiC MOSFET. A 60 V, 0.2 Ω MOSFET (NVR5198NL) [10] from ONsemi is selected as S_d because of its high transconductance g_m and relative low threshold voltage V_{th}. The needed RC delay circuit time constant τ should be 0.5 μs according to (2) and the RC delay circuit value is selected as 200 Ω and 2.5 nF, respectively, to avoid the influences on T_d from the gate resistances and parasitic capacitances (typically 20 ∼300 pF) of the LV MOSFET S_d.

C. Switching Frequency and Dead Time Limitations From Single Gate Driver Circuit

In this section, the power converter switching frequency limitation from the single gate driver circuit and how to set the dead time for the three-terminal Si/SiC hybrid switch are discussed. In the proposed single gate driver circuit, the RC delay circuit needs to be fully charged and discharged before the next switching cycle, which could limit the maximum switching frequency of the three-terminal Si/SiC hybrid-switch-based power converter. For example, the charging and discharging time of the delay capacitor, respectively, is about 1.5 μs (about 3 times of the RC time constant τ) from Fig. 6, which means the maximum switching frequency limit from the delay capacitor should be $f_{sw,\max} = 1/(3\tau + 3\tau) = 333.3$ kHz. If the switching frequency of two hybrid switches in a half bridge is too high, short circuit could happen and the devices could get damaged.

It also needs to be mentioned that the switching frequency of most high-power converters cannot reach the maximum switching frequency limit from the single gate driver circuit. For example, most IGBT-based power converter's switching frequency varies from a few kilohertz to tens of kilohertz, far below the maximum switching frequency limit from the delay capacitor [14]. Even the SiC-based high-power converters (e.g., a 20 kW buck/boost converter for EVs [15]) demonstrate only

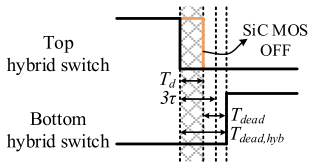

Fig. 8. Dead time setting for the hybrid-switch-based converter.

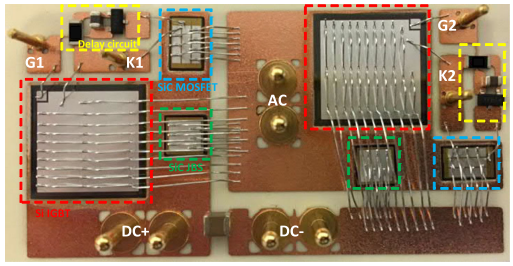

Fig. 9. Packaged 1200 V, 200 A Si/SiC hybrid switch half-bridge module with the turn-OFF delay gate driver circuit integrated.

up to 100 kHz switching frequency, still below the maximum switching frequency limit, although some SiC-based power converters demonstrated a ∼MHz switching frequency performances. The three-terminal Si/SiC hybrid switch is not suitable for that type of ultrahigh switching frequency applications.

The dead time setting for the hybrid-switch-based converter could be a little more complicated than conventional pure IGBT or SiC MOSFET-based power converters. To address this, the dead time ($T_{\text{dead},hyb}$) for the proposed three-phase hybrid switch can be set based on the following two equations:

$$T_{\text{dead},hyb} = T_{\text{dead}} + T_d \tag{4}$$

$$T_{\text{dead},hyb} > 3\tau. \tag{5}$$

In (4), T_{dead} is the power converter needed dead time, T_d is the SiC MOSFET turn-OFF delay time in the hybrid switch, and τ is the time constant of the RC delay circuit. As the SiC MOSFET is turned OFF after the gate driver signal with delay time T_d, as shown in Fig. 8, the turn-OFF delay time T_d should be added to the needed power converter dead time T_{dead}. For example, the dead time needed between the top switch and the bottom switch, is $T_{\text{dead}} = 2$ μs. The dead time for the hybrid-switch-based converter should be set to $T_{\text{dead},hyb} = T_{\text{dead}} + T_d = 3$ μs ($T_d = 1$ μs). In (5), τ is the time constant of the RC delay circuit. Before the next switching cycle, the delay capacitor needs to be fully charged and discharged (which takes about 3τ), which poses a minimum dead time requirement for the hybrid switch as shown in (5). Fortunately, the delay capacitor time constant τ is short ($\tau = 0.5$ μs in this letter), the minimum dead time requirement is easy to meet.

III. EXPERIMENTAL VALIDATION

To verify the proposed single gate driver circuit, a 1200 V, 200 A hybrid switch power module is developed and packaged based on Cree's SiC MOSFET [11] (C2M0025120D) and ABB's Si IGBT [12] (ABB, 5SMY12M1280), as shown in Fig. 9. The hybrid switch power module is a half-bridge module and the

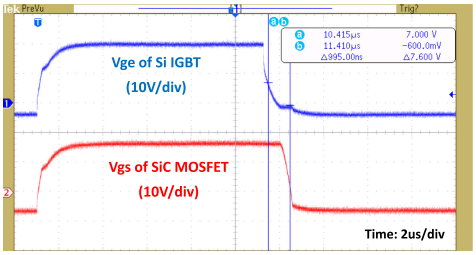

Fig. 10. Gate voltages of the Si IGBT and SiC MOSFET showing simultaneous turn-ON and 1.0 μs turn-OFF delay.

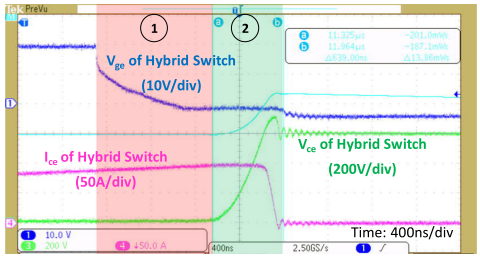

Fig. 11. Si/SiC hybrid switch 600 V, 100 A turn-OFF waveforms with 1.0 μs turn-OFF delay and ~14 mJ turn-OFF losses (compared to Si IGBT's 37 mJ turn-OFF losses under same conditions).

gate driver circuit for simultaneous turn-ON and 1 μs delayed turn-OFF is integrated inside the power module as shown in the dashed yellow box in Fig. 9. The specifications of the single gate driver circuit are enumerated in Table I. With the help of the designed gate driver circuit, the hybrid switch becomes a typically three-terminal switch, making it easy to use and cost-effective to realize.

Fig. 10 shows the gate voltages of the Si IGBT and the SiC MOSFET. The proposed single gate driver circuit successfully achieves the design goal: the Si IGBT and the SiC MOSFET are turned ON simultaneously, and the SiC MOSFET is turned OFF with 1.0 μs delay time after the Si IGBT. Fig. 11 shows 600 V, 100 A turn-OFF waveforms of the Si/SiC hybrid switch with the designed gate driver circuit. It shows clearly that the turn-OFF process contains two phases. Phase I (pink area) is the 1.0 μs delay time for the SiC MOSFET, and Phase II (green area) is the turn-OFF period for the SiC MOSFET. The experimental results show up to 60% turn-OFF loss reduction when compared to the Si IGBT.

The proposed gate driver circuit is also verified in a buck converter, built based on the half-bridge module in Fig. 9. The buck converter is operated with 600 V input voltage and 0.25 duty cycle at 22.5 kHz switching frequency. At 7.5 kW output power, the efficiency of the hybrid-switch-based buck converter is ~3% (from 91.4% to 94.2%) higher compared to that of the Si IGBT-based buck converter.

IV. Summary

In this letter, a novel gate driver circuit with simultaneous turn-ON and delayed turn-OFF capability is designed for the Si/SiC hybrid switch, which reduces the required number of control signals and gate driver circuits to drive the hybrid switch, leading to a lower bill of materials. The proposed gate driver circuit consists of an LV MOSFET and RC delay circuit, which can be easily integrated and packaged inside the hybrid switch module, making the hybrid switch the same as a typically three-terminal device (gate, emitter, and collector). The operation principles and design guidelines are provided, and the concept is experimentally verified in a 1200 V, 200 A hybrid switch half-bridge power module.

The three-terminal Si/SiC hybrid switch is more suitable for fixed load applications. In load variable conditions, the three-terminal Si/SiC hybrid-switch-based converter may have lower efficiency compared to the variable delay time control method, and the hybrid switch needs to be designed based on the maximum load to avoid the SiC MOSFET exceeds its junction temperature.

The reliability of the integrated LV MOSFET and RC circuits are not thoroughly studied yet. Some existing commercial power modules like the IGBT intelligent power modules prove the reliability of the integrated LV MOSFET and RC circuit is not an obvious concern, but their reliability still could be a good future research topic.

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