Three-Phase Split-Source Inverter-Fed PV Systems: Analysis and Mitigation of Common-Mode Voltage

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***Abstract*—Common-mode voltage (CMV), caused by standard high-frequency pulsewidth modulated (PWM) voltage source inverters (VSIs), is a major area of interest in various applications, such as electric motor drives, transformerless photovoltaic systems, and grid-tied inverters. Since VSIs have only the buck capability during the inversion mode, an additional boosting stage either in the dc side or in the ac side has to be utilized for low-voltage-fed applications. On the other hand, single-stage solutions, with buck and boost capabilities, represent an interesting alternative with reduced cost, complexity, and converter volume. Among the possible single-stage solutions, split-source inverter (SSI), which has been recently proposed, has several merits over its counterparts. One of the questionable aspects concerning this topology is the CMV, which has not been investigated yet. This article examines the induced CMV with the SSI. This is done by examining the CMV waveforms for VSI and SSI topologies, and then, comparing each other under different PWM schemes. Furthermore, this article proposes the use of the discontinuous space vector PWM scheme with the SSI to mitigate the CMV, where the analysis shows a significant reduction in the CMV compared to the other schemes. In order to validate the introduced analysis, simulation model has been designed using MATLAB/Simulink environment, and simulation results are presented. Moreover, a prototype has been built-up for testing the proposed concepts and the obtained experimental results are provided.**

***Index Terms*—Boost inverter, common-mode voltage (CMV), low-voltage application, photovoltaic (PV) systems, pulsewidth modulation, single-stage converter, split-source inverter (SSI).**

I. Introduction

COMMON-MODE voltage (CMV), caused by prevalent high-frequency pulsewidth modulated (PWM) inverters, is a significant issue for many applications, such as motor drives, transformerless photovoltaic (PV) systems, and grid-tied inverters. For example, the induced high amplitude, high frequency, and large step change of the CMV induces motor bearing currents, which significantly influence the aging rate of the bearing and lead to bearing failure, and as a consequence affects the overall system reliability. Moreover, it brings undesirable conducted and radiated electromagnetic interference (EMI) issues, motor insulation breakdown, common mode (CM) leakage current, mechanical vibration, and also malfunction of surrounded electronic equipment [1]–[3]. In addition to that, PV modules with an integrated metallic backside and thin-films on flexible laminates may possess very large parasitic capacitance, even when they are dry. Thus, in combination with transformerless inverters, quite large capacitive discharge currents may be generated due to the lack of galvanic isolation. The high switching speeds also bring on voltage fluctuations in the load neutral point. Therefore, a high-frequency CMV appears, resulting in a high level of CM leakage current that may exceed the permissible levels [4]. The induced leakage current circulates through the PV panel's parasitic capacitance can also cause grid voltage and current distortion, EMI issues, additional losses, and a potential safety risk [4]–[7]. Therefore, the CMV issue is seen as a striking area of research, especially in the aforementioned applications.

The integration of PV systems into the grid is usually implemented through a voltage source inverter (VSI), where a boosting stage might be mandatory if the dc input voltage is not sufficient under all the operating conditions. Such added boosting stage results in a two-stage architecture, as depicted in Fig. 1, and this architecture is usually characterized by being bulky and costly solution [8]. On the other hand, single-stage solutions have recently gained higher attention due to the seen merits, in terms of the system volume and cost [9]–[13]. Among the possible single-stage solutions, split-source inverter (SSI), which has been recently proposed in [13], is seen as an interesting and competitive solution due to the gained merits compared to its counterparts. SSI has the merit of lower number of passive elements with reference to the classical impedance source inverter, requiring only three extra diodes with the similar number of complementary switching devices as the VSI [13].

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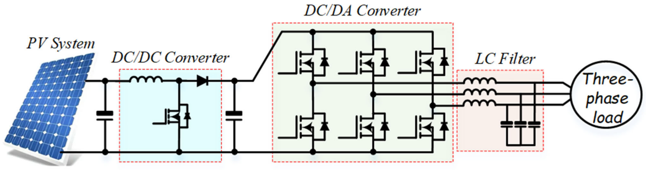


Fig. 1. Two-stage PV system architecture.

Furthermore, no special pulses are required for its basic operation compared to the conventional modulation schemes of the VSI. However, SSI has some demerits, such as high-frequency commutations of the input diodes, unequal current stresses, and increased voltage stresses at lower voltage gains [14].

Recently, several research activities have been conducted on the SSI considering its single-phase structure, as discussed in [9]–[12] and its three-phase one, as discussed in [13]–[16]. It is worth noting that the previous studies have mainly focused on the boosting capability gained from SSI through either conventional inductor [13] or coupled inductor concept [10]. In addition to that, multilevel configurations of SSI such as diode-clamped [14] and flying-capacitor structures [16] have been investigated as well. Furthermore, closed-loop grid-connected operation through decoupled control strategy [17], high-speed commutation issue of SSI extra diodes [9], and recently, the switch count reduction for the simplified version of the SSI [11] have been also considered. However, so far, research has yet to systematically examine the CMV behavior of the SSI. Therefore, output CMV issue of the SSI topology is investigated in this article under different PWM schemes. Then, a discontinuous space vector PWM (DSVPWM) strategy is proposed in order to mitigate such CMV issue.

This article is organized as follows. Section II elucidates the CMV problem in VSI and SSI topologies using converters' equivalent circuits. After that, the proposed DSVPWM strategy is discussed in Section III. Then, the simulation results and discussion, which verify the effectiveness of the suggested modulation strategy, are presented in Section IV, where the experimental validation is introduced in Section V. Finally, the conclusion is drawn in Section VI.

II. ANALYSIS OF COMMON-MODE VOLTAGE

The CMV generated by the inverter-based PV systems, along with parasitic capacitive couplings, may cause undesirable issues in various applications as mentioned before. This CMV (u_{cm}) can be obtained by averaging the voltages of the three-phase-legs with reference to (O), as shown in Fig. 2, considering the traditional three-phase VSI. Thus, u_{cm} can be expressed as follows:

$$u_{\mathrm{cm}} = \frac{u_{\mathrm{AO}} + u_{\mathrm{BO}} + u_{\mathrm{CO}}}{3} \tag{1}$$

where u_{AO}, u_{BO}, and u_{CO} are the three-phase-legs voltages of the inverter, as illustrated in Fig. 2. In this section, the intrinsic properties of the CMV in VSI and SSI topologies are thoroughly analyzed and compared.

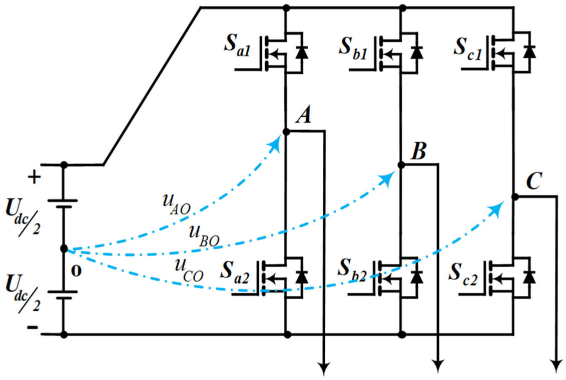


Fig. 2. VSI topology converters' equivalent circuit.

TABLE I
SWITCHING STATES AND RESULTANT CMV VALUES

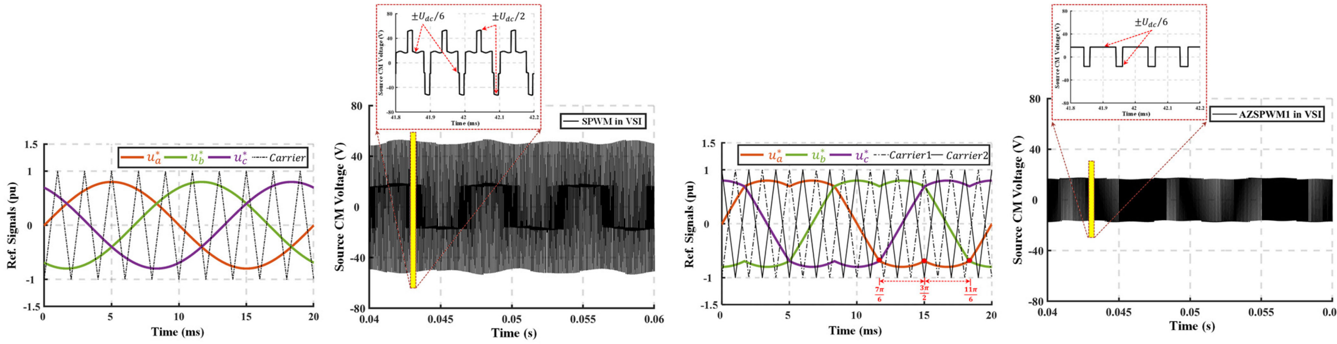
Switching state	u_{AO}	u_{BO}	u_{CO}	u_{cm}
NNN	$-U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$
NNP	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/6$
NPN	$-U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/6$
NPP	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$U_{dc}/6$
PNN	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/6$
PNP	$U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/6$
PPN	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/6$
PPP	$U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$

A. *VSI CMV Analysis*

Before proceeding to analyze the consequent CMV issue produced by the SSI topology, it is essential to review the CMV of the conventional VSI as a reference case.

The typical three-phase VSI, in which a B6-bridge is fed from a dc-link voltage (U_{dc}), is shown in Fig. 2. In this B6-bridge, each pair of switches are switched in a complementary manner, where Table I lists the permissible eight switching states and their relevant phase-legs voltages with reference to point (O), and the presumed CMV values. Note that "P" or "N" indicate either the load is tied to the positive or to the negative dc-bus terminals, respectively. From this table, it can be noted that the CMV has four different values, which are $\pm U_{\mathrm{dc}}/6$ and $\pm U_{\mathrm{dc}}/2$. The six active states induce a voltage level of $\pm U_{\mathrm{dc}}/6$ compared to $\pm U_{\mathrm{dc}}/2$ from the two zero switching states.

Different approaches have been investigated in [18]–[21] to mitigate the CMV issue in the conventional VSIs. These approaches can be classified into software-based approaches as discussed in [7], [18]–[21] and hardware-based ones as discussed in [3] and [4], in which the CM filters are the commonly used solution. Although hardware-based approaches give an effective reduction in the CMV impacts, it greatly influences the system cost, losses, and complexity. In addition to its weight and size that depends on the magnetic saturation of the utilized core, which is thoroughly impacted by the induced CMV. On the other hand, software-based approaches are seen as cost-effective



(a) (b) (c) (d)

Fig. 3. Modulating signals and their induced CMV in VSI under different modulation schemes, where $m_i = 0.8$ and $m_f = 10$. Note that $U_{\mathrm{dc}} = 100$ V. (a) SPWM. (b) CMV using SPWM. (c) AZSPWM1. (d) CMV using AZSPWM1.

and easy to test and implement. One of the most common software-based approaches to limit the CMV level is to use the reduced CMV PWM (RCMV-PWM) techniques [18], [20]–[22]. These techniques are based on pulse pattern adaptation to remove the zero vector states, and keeps only the active vector states such as active zero state PWM (AZSPWM) [18], [23], remote-state PWM (RSPWM) [18] and near-state PWM [18], [19]. Various versions of the AZSPWM schemes are available, where the AZSPWM1, shown in Fig. 3(c), replaces the zero state vectors with two opposing active vectors to establish a null vector through phase-opposite carrier waves. It is worth to note that the induced CMV levels due to AZSPWM1 utilization are reduced to only $\pm U_{\mathrm{dc}}/6$ [see Fig. 3(d)] compared to $\pm U_{\mathrm{dc}}/2$ in case of SPWM [see Fig. 3(a) and (b)] or conventional space vector PWM (SVPWM) [18]. For the RSPWM scheme, only a three active vector states, either the odd active vectors or the even active vectors, are utilized to synthesize the output voltage. However, RSPWM suffers from reduced dc-link voltage utilization where the maximum magnitude of the phase to neutral voltages only represent a 57.7% of the voltage achieved by SVPWM [7]. Another insightful approach of RCMV-PWM methods is presented in [20], where a constrained nonlinear programming models are considered. This approach aims at optimizing the three-phase current ripples by minimizing the mean-square values of the ripples, and minimizing the switching loss over a wide range of load power factor. However, so far, none of these approaches can be applied to the SSI topology due to inductor/capacitor charging/discharging concept, which will be discussed and verified in the remaining part of this article. Moreover, all the RCMV-PWM approaches produce bipolar line-to-line voltage pulses, which lead to serious overvoltage at the motor terminals [19].

B. SSI CMV Analysis

A schematic diagram of the SSI is described in Fig. 4. It has the same structure as the VSI but with three extra diodes, in which the boosting feature can be obtained through inductor/capacitor set (L_{SSI} and C_{SSI}). In this section, the modulation techniques applied to the SSI will be analyzed in terms of the induced CMV to deeply understand the problem and then suggest a solution to curtail the peak-to-peak (pk-pk) level of the induced CMV.

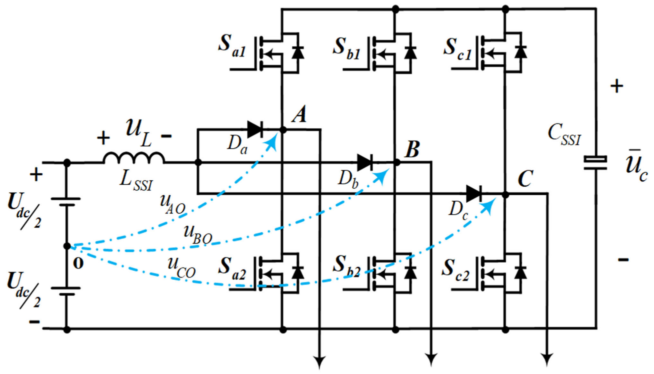


Fig. 4. Equivalent circuit of the three-phase SSI.

Detailed analysis and illustrations of the feasible switching states for the SSI topology are shown in Figs. 5 and 6, where the red lines are dedicated to the inductor charging and discharging paths. Note that the active states are shown in Fig. 5. Based on the same CMV signature, the active states can be classified into odd and even states, where the odd states are illustrated in Fig. 5(a)–(c) and the even states are depicted in Fig. 5(d)–(f). From these figures, in contrast to the VSI topology, it is revealed that the CMV of the SSI primarily depends on the average capacitor voltage. Furthermore, it is confirmed that all the active states are considered as charging states for the inductor L_{SSI}, as stated in [13]. On the other hand, Fig. 6 shows the zero states. Meanwhile, this figure provides a deep insight into the phase-legs voltages when the upper or lower switches are connected. One interesting finding is that, in contrast to the phase-legs voltages with respect to a reference point in the VSI, the inductor voltage in the SSI contributes to the phase-legs voltages when the upper semiconductor devices are ON. This contribution forms asymmetrical configuration of the induced CMV in case of SSI inconsistent to that produced by VSI.

Table II gives a recap of the CMV generated by the SSI. From this table, one can notice that the inductor charging state occurs

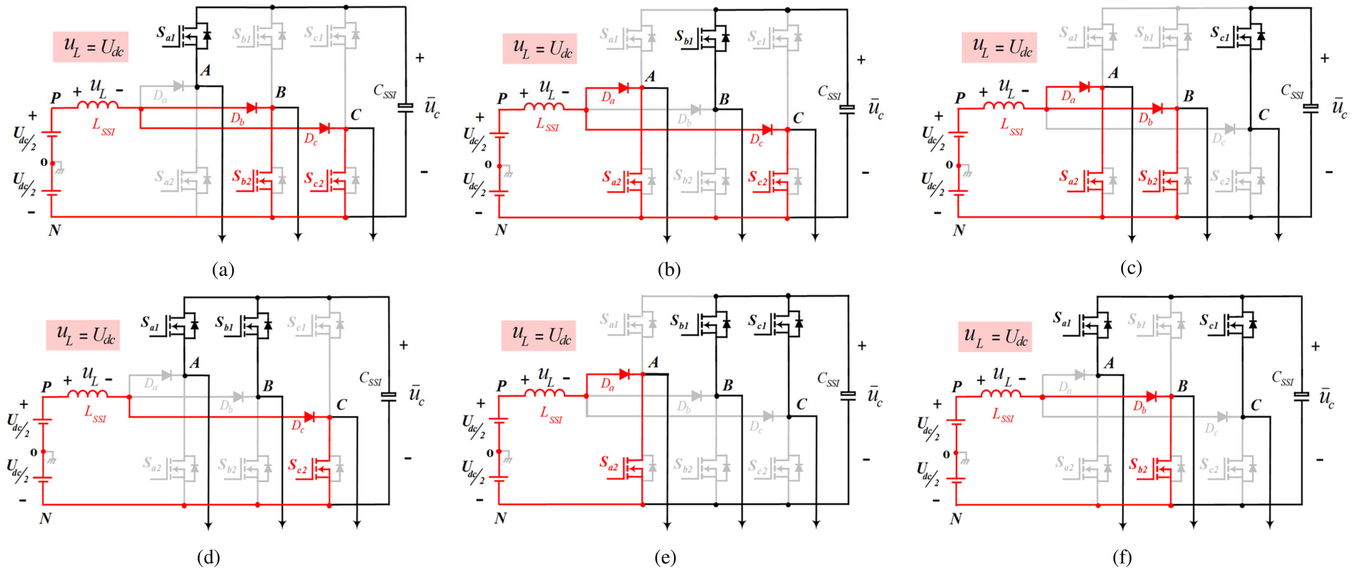


Fig. 5. SSI active states equivalent circuits. (a) PNN. (b) NPN. (c) NNP. (d) PPN. (e) NPP. (f) PNP.

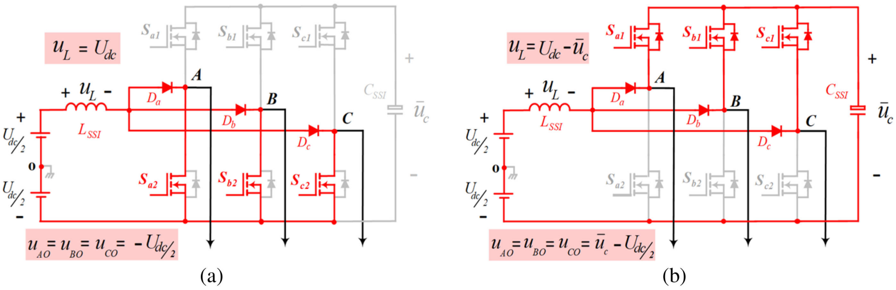


Fig. 6. SSI zero states' equivalent circuits and phase-leg voltages. (a) NNN. (b) PPP.

TABLE II
DIFFERENT SWITCHING STATES AND THEIR CMV ESTIMATION

Switching State	Inductor		Line voltages			u_{cm}	CMV level
	u_L	Charging	u_{AB}	u_{BC}	u_{CA}		
NNN	U_{dc}	Yes	0	0	0	$-U_{dc}/2$	①
PNN	U_{dc}	Yes	$\bar{u}_C$	0	$-\bar{u}_C$	$(2\bar{u}_C - 3U_{dc})/6$	②
PPN	U_{dc}	Yes	0	$\bar{u}_C$	$-\bar{u}_C$	$(4\bar{u}_C - 3U_{dc})/6$	③
NPN	U_{dc}	Yes	$-\bar{u}_C$	$\bar{u}_C$	0	$(2\bar{u}_C - 3U_{dc})/6$	②
NPP	U_{dc}	Yes	$-\bar{u}_C$	0	$\bar{u}_C$	$(4\bar{u}_C - 3U_{dc})/6$	③
NNP	U_{dc}	Yes	0	$-\bar{u}_C$	$\bar{u}_C$	$(2\bar{u}_C - 3U_{dc})/6$	②
PNP	U_{dc}	Yes	$\bar{u}_C$	$-\bar{u}_C$	0	$(4\bar{u}_C - 3U_{dc})/6$	③
PPP	$U_{\mathrm{dc}} - \bar{u}_C$	No	0	0	0	$\bar{u}_C - U_{dc}/2$	④

in seven switching states (six active states in addition to one of the two zero states, NNN, where all the three-phases are clamped to the negative terminal of the dc-link). On the other hand, the inductor is discharging (in other words the capacitor is charging) during one switching state, PPP, where the three legs are clamped to the positive terminal of the dc-link. In case of SSI, it is not possible to remove the positive zero state for the shown configuration in Fig. 4. Furthermore, as indicated in the last two columns, the odd states, PNN, NPN, and NNP have the same CMV level of $[(2\bar{u}_C - 3U_{\mathrm{dc}})/6]$, and the even states, PPN, NPP, and PNP have the same CMV level with a value of $[(4\bar{u}_C - 3U_{\mathrm{dc}})/6]$. On the other hand, the zero states, NNN and PPP, have the lowest and highest CMV levels with values of $(-U_{\mathrm{dc}}/2)$ and $[\bar{u}_C - U_{\mathrm{dc}}/2]$, respectively, in contrast to $(-U_{\mathrm{dc}}/2)$ and $(+U_{\mathrm{dc}}/2)$ in case of VSI. In order to well examine the CMV issue with the SSI, different modulation schemes are investigated as follows.

1) Sinusoidal PWM (SPWM): The normalized sinusoidal modulating signals indicating the inductor charging periods, illustrated in Fig. 7, during a complete fundamental cycle of

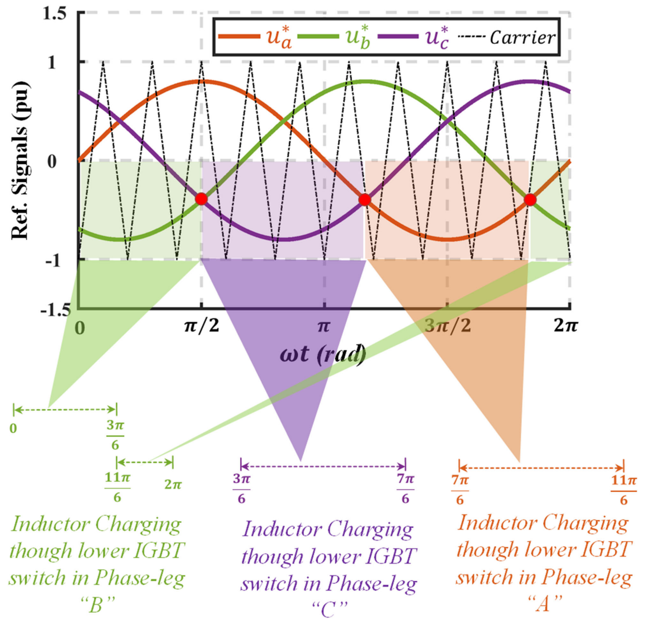


Fig. 7. Reference modulating waveforms of SPWM indicating the inductor charging periods through certain phase leg.

$0 < \omega t \leq 2\pi$ can be expressed by the following equation:

$$\begin{bmatrix} u_a^*(\omega t) \\ u_b^*(\omega t) \\ u_c^*(\omega t) \end{bmatrix} = \begin{bmatrix} m_i \sin(\omega t) \\ m_i \sin\left(\omega t - \frac{2\pi}{3}\right) \\ m_i \sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix}. \tag{2}$$

It is worth mentioning that the charging process is achieved with the help of lower switches through their insulated-gate bipolar transistors (IGBTs), whereas the upper antiparallel diodes are used to discharge the inductor's stored energy. Based on the implemented modulation strategy in SSI, the SSI inductor charged at a variable duty ratio. In SPWM, this variable duty ratio $D_{aL}(\omega t)$ of the boosting action phase "a" can be determined by the following equation:

$$D_{aL}(\omega t) = \frac{1}{2}\left[1 - m_i \sin(\omega t)\right] \rightarrow \left(\frac{7\pi}{6} \leq \omega t \leq \frac{11\pi}{6}\right). \tag{3}$$

As mentioned earlier, the CMV depends on the capacitor voltage. Therefore, the average capacitor voltage must be considered. This capacitor voltage depends mainly on the duty ratio, which is time varying over the fundamental period. The average capacitor voltage, $\bar{u}_C$, can be calculated from

$$\bar{u}_C = \frac{4\pi U_{\mathrm{dc}}}{2\pi - 3\sqrt{3}m_i}. \tag{4}$$

According to [13], an average duty ratio of $[0.5 + 3\sqrt{3}m_i/4\pi]$ used for inductor charging, where the duty ratio is defined with a maximum value of $[0.5 + 0.5m_i]$ at $\omega t = 3\pi/2$ and a minimum value of $[0.5 + 0.25m_i]$ at $\omega t = 7\pi/6$ and $11\pi/6$. The simulated CMV of the SSI employed with traditional SPWM is shown in Fig. 8. This figure also introduces the inductor, capacitor voltages related to the CMV. From this figure, it can be seen that the pk-pk CMV has a value of $\bar{u}_C$. The difference between the average capacitor voltage and the upper limit of the CMV is $U_{\mathrm{dc}}/2$, since the CMV in these simulation results is considered between the phase-legs midpoint and a reference point (O), as shown in Fig. 4. Furthermore, from the enlarged version, it is worth noting that the CMV has four different levels in accordance to the CMV level column in Table II that comprises six transitions in each switching cycle, which also contributes to the CM noise behavior.

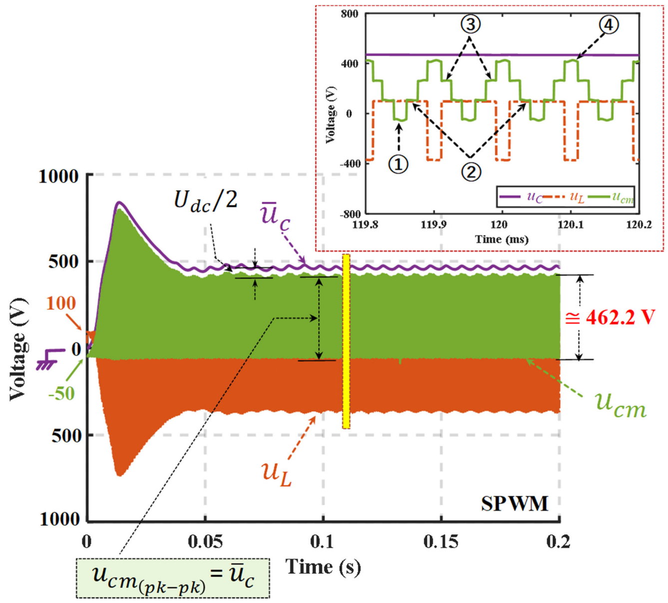


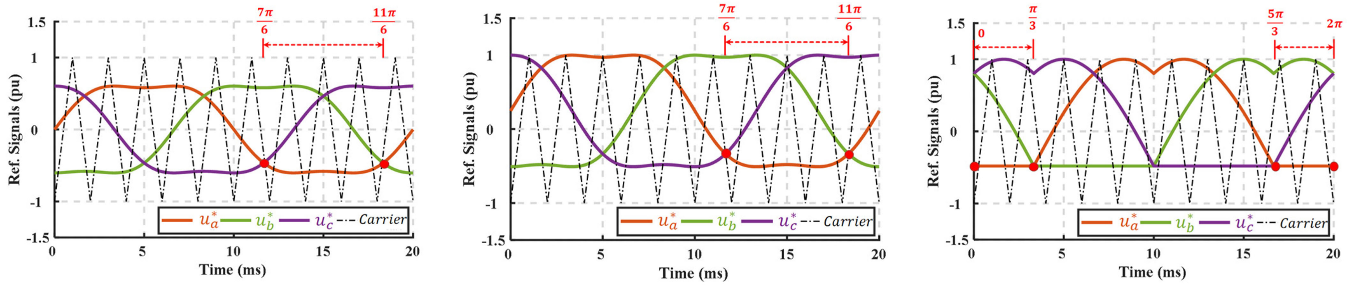
Fig. 8. Relationship between SSI CMV and voltages of the inductor and capacitor with $U_{\mathrm{dc}} = 100$ V, $L_{\mathrm{SSI}} = 5$ mH, $C_{\mathrm{SSI}} = 168$ μF, and $\bar{D} = 0.7812$.

2) Third-Harmonic Injection PWM (THIPWM): A considerable limitation with the SPWM is the limited feasible peak of the fundamental output voltage compared to the available dc-bus voltage. Moreover, based on the carrier-based implementation of the continuous PWM schemes, the zero states distribution can be controlled through the addition of the third harmonic component to the reference modulating signals. The modulating signals of the classical third-harmonic injection PWM (THIPWM) scheme are illustrated in Fig. 9(a), where the THIPWM scheme features higher modulation index of $1.15 = (2/\sqrt{3})$ compared to unity in SPWM scheme with 15% increase in the dc-link utilization. The THIPWM reference signal of phase "a" $(u_a^*(\omega t))$ is given by the following equation:

$$u_a^*(\omega t) = \frac{2m_i}{\sqrt{3}}\left[\sin(\omega t) + K \sin(3\omega t)\right] \tag{5}$$

where $K = 1/6$ that used to maximize the utilization of the dc-bus voltage and gain higher fundamental voltage. Similar to the SPWM scheme, the expressions for duty ratio of lower switch used for inductor charging and average capacitor voltage must be established, which are given in Table III.

3) SVPWM: One approach to produce SVPWM switching pulses is to use the digital way of implementation. Another approach is to use carrier-based equivalent modulation, where a zero-sequence signal (ZSS) component can be added to the reference modulation signals to further enhance the voltage



(a) (b) (c)

Fig. 9. Reference and carrier signals of different modulation schemes used for the SSI [13]. The frequency modulation ratio $m_f = 10$ which is very low compared to the actual carrier frequency for illustration. (a) THIPWM. (b) BTHIPWM. (c) MSVPWM.

TABLE III
SUMMARY OF THE SSI RELATIONSHIPS UNDER DIFFERENT MODULATION SCHEMES USED IN THE ANALYSIS

Parameter		Modulation schemes			
		THIPWM	BTHIPWM	SVPWM	
$D_a(\omega t)$	Value	$\frac{1}{2}-\frac{m_i}{\sqrt{3}}\left(\sin(\omega t)+\frac{\sin(3\omega t)}{6}\right)$	$\frac{m_i}{2}-\frac{m_i}{\sqrt{3}}\left(\sin(\omega t)+\frac{\sin(3\omega t)}{6}\right)$	$\frac{1}{2}-\frac{m_i}{2}\sin\left(\omega t+\frac{\pi}{6}\right)$	$\frac{1}{2}+\frac{m_i}{2}\cos\left(\omega t+\frac{\pi}{3}\right)$
	Range	during $(7\pi/6 \le \omega t < 11\pi/6)$	during $(7\pi/6 \le \omega t < 11\pi/6)$	during $(7\pi/6 \le \omega t < 3\pi/2)$	during $(3\pi/2 \le \omega t < 11\pi/6)$
$\overline{D}$		$\frac{1}{2}+\frac{3m_i}{2\pi}$	$\left(\frac{1}{2}+\frac{3}{2\pi}\right)m_i$	$\frac{1}{2}+\frac{3m_i}{2\pi}$	
$\bar{u}_c$		$\frac{2\pi U_{dc}}{\pi-3m_i}$	$\frac{2\pi U_{dc}}{2\pi-(\pi+3)m_i}$	$\frac{2\pi U_{dc}}{\pi-3m_i}$	

linearity range of the SPWM scheme [24]. This ZSS also has a substantial impact on the switching loss of the converter [25], where its value is produced by the following [26]:

$$u_{\text{zss}}(\omega t) = \frac{1}{2}\left[(1-u_{\max}^*)-(1+u_{\min}^*)\right] \tag{6}$$

where $u_{\min}^*$ and $u_{\max}^*$ represent the minimum and maximum instantaneous reference waveforms given by the following:

$$\begin{cases} u_{\min}^* = \min(u_a, u_b, u_c) \\ u_{\max}^* = \max(u_a, u_b, u_c). \end{cases} \tag{7}$$

The ZSS injected to the reference modulating signals to obtain the SVPWM modulating signals is in the form of

$$u_{\text{zss}}(\omega t) = \begin{cases} -\frac{m_i}{\sqrt{3}}\sin\left(\omega t-\frac{\pi}{3}\right) \rightarrow \begin{cases} \left(\frac{\pi}{6} \le \omega t \le \frac{\pi}{2}\right) \\ \left(\frac{7\pi}{6} \le \omega t \le \frac{3\pi}{2}\right) \end{cases} \\ -\frac{m_i}{\sqrt{3}}\sin\left(\omega t+\frac{\pi}{3}\right) \rightarrow \begin{cases} \left(\frac{\pi}{2} \le \omega t \le \frac{5\pi}{6}\right) \\ \left(\frac{3\pi}{2} \le \omega t \le \frac{11\pi}{6}\right) \end{cases} \\ \frac{m_i}{\sqrt{3}}\sin(\omega t) \rightarrow \begin{cases} \left(\frac{5\pi}{6} \le \omega t \le \frac{7\pi}{6}\right) \\ \left(\frac{11\pi}{6} \le \omega t \le \frac{13\pi}{6}\right). \end{cases} \end{cases} \tag{8}$$

Similar to the other modulation schemes, an expression for the average capacitor voltage must be defined which are also provided in Table III.

4) Biased THIPWM (BTHIPWM): Due to the increased voltage stresses using the prior modulation schemes, the biased THIPWM (BTHIPWM) is proposed in [13] as a manipulation of the conventional THIPWM to reduce the voltage stresses. The modulating signals of the BTHIPWM are illustrated in Fig. 9(b), where modulating signal of phase "a" is given by the following:

$$u_a^*(\omega t) = \frac{2m_i}{\sqrt{3}}\left[\sin(\omega t)+\frac{1}{6}\sin(3\omega t)+\frac{\sqrt{3}}{2m_i}-\frac{\sqrt{3}}{2}\right]. \tag{9}$$

The expressions for the duty ratio and the resultant capacitor voltage due to the application of the BTHIPWM scheme are further given in Table III.

5) Modified SVPWM (MSVPWM): The modified SVPWM (MSVPWM) has been proposed in [13] as a strategy for the reduction of low-frequency component either in the inverter voltage or the inductor current. Such reduction can be achieved by fixing the duty ratio instead of being variable as in the aforementioned modulation schemes. The approach is based on the zero state periods redistribution without affecting the active state times. It is noteworthy that the inductor discharging period is settled at the minimum zero state time, as illustrated in Fig. 9(c) by the lower virtual envelop. Therefore, a fixed duty cycle of m_i is obtained. In this case, the capacitor voltage can be determined from the following:

$$\bar{u}_C = \frac{U_{\text{dc}}}{1-m_i}. \tag{10}$$

III. PROPOSED DISCONTINUOUS SVPWM (DSVPWM) FOR CMV REDUCTION IN THE SSI

An alternative approach, widely used in VSI, to control the zero states distribution is the utilization of the DSVPWM

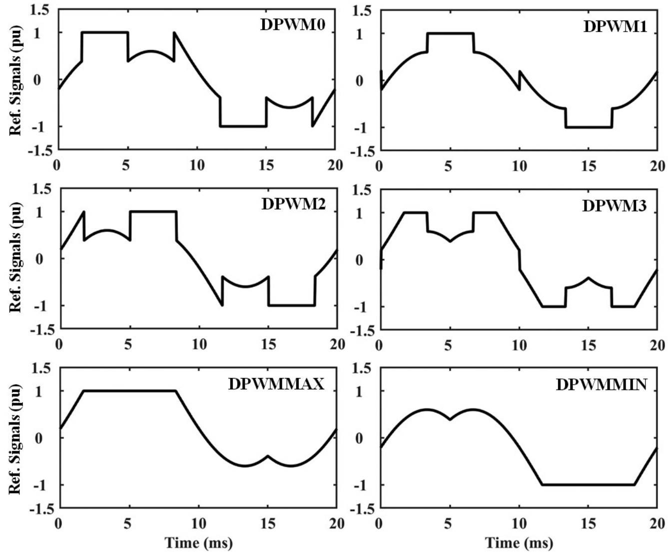


Fig. 10. Discontinuous SVPWM (DSVPWM) schemes.

schemes. Recently, these strategies have gained higher attention due to the reduced switching loss [27], [28], compared to the traditional SVPWM. The average switching frequency of these discontinuous schemes is only two-third of the switching frequency. A comprehensive review of different PWM techniques including DSVPWM is discussed in [25]. Most common DSVPWM schemes, used in various applications such as electric motor drives, are DPWM0, DPWM1, DPWM2, DPWM3, DPWMMAX, and DPWMMIN [24], [28] as shown in Fig. 10. In the DPWM1, each phase-leg is connected to the negative or the positive dc-link terminals alternately within the middle 60° interval in each half of its fundamental cycle. Where DPWM0 and DPWM2 have phase-shit of –30°, and +30°, respectively, with respect to DPWM1. Meanwhile, every phase-leg is locked to the positive or negative dc-link terminals for 30° interval every quarter cycle in the DPWM3 scheme. Alternatively, within the positive half cycles of the DPWMMAX, each phase-leg is connected to the positive dc-link for 120° of the fundamental cycle. Besides, each phase-leg is connected to the negative dc-link for one-third period of the fundamental cycle during the negative half cycles under the DPWMMIN. It is worth to mention that the DPWMMAX and DPWMMIN methods have nonuniform thermal stress distribution on the semiconductor switching devices, where, in DPWMMAX, the upper switching devices could experience further conduction losses than the lower ones. However, under each of the DPWMMAX and the DPWMMIN schemes, one of the two zero states is eliminated during the entire fundamental period, which results in a reduced CMV shape in case of VSI. Moreover, in case of the SSI topology, it is worth to mention that only one zero state can be eliminated; which is the state of NNN [shown in Fig. 6(a)] to keep the discharging/charging process of the dc-side.

In this article, the DPWMMAX modulation technique is employed with the SSI for the CMV mitigation by eliminating one of the two zero switching states. A novelty behind selecting the modulation technique proposed in this article is that it has a reverse envelope shape (i.e., inverted configuration) of the MSVPWM introduced in [13], as illustrated in Fig. 11. Such MSVPWM technique can be considered as a manipulation of the DPWMMIN, shown in Fig. 10, which cannot be applied to the SSI in its original form due to the absence of the “PPP” zero state that is necessary for inductor discharging. Furthermore, the proposed modulation scheme has an aspect of variable duty cycle, which does not exist in [13]. This is obviously illustrated in Fig. 11. The modulating sinusoidal signals, in a three-phase symmetrical system considering the extended voltage range of the modulation index, can be defined as follows:

$$\begin{bmatrix} u_a(\omega t) \\ u_b(\omega t) \\ u_c(\omega t) \end{bmatrix} = \begin{cases} \frac{2m_i}{\sqrt{3}} \sin(\omega t) \\ \frac{2m_i}{\sqrt{3}} \sin\left(\omega t - \frac{2\pi}{3}\right) \\ \frac{2m_i}{\sqrt{3}} \sin\left(\omega t + \frac{2\pi}{3}\right). \end{cases} \tag{11}$$

Referring to Fig. 11, by assuming each phase leg is continuously clamped to the positive dc rail for one-third of the fundamental period, the normalized reference modulating signals of the proposed DPWMMAX can be expressed by the following:

$$u_a^*(\omega t) = \begin{cases} 1 \rightarrow \left(\frac{\pi}{6} \le \omega t \le \frac{5\pi}{6}\right) \\ 1 + 2m_i \cos\left(\omega t - \frac{\pi}{3}\right) \rightarrow \left(\frac{5\pi}{6} \le \omega t \le \frac{3\pi}{2}\right) \\ 1 - 2m_i \cos\left(\omega t + \frac{\pi}{3}\right) \rightarrow \left(\frac{3\pi}{2} \le \omega t \le \frac{13\pi}{6}\right) \end{cases} \tag{12}$$

$$u_b^*(\omega t) = \begin{cases} 1 - 2m_i \cos\left(\omega t - \frac{\pi}{3}\right) \rightarrow \left(\frac{\pi}{6} \le \omega t \le \frac{5\pi}{6}\right) \\ 1 \rightarrow \left(\frac{5\pi}{6} \le \omega t \le \frac{3\pi}{2}\right) \\ 1 - 2m_i \cos(\omega t) \rightarrow \left(\frac{3\pi}{2} \le \omega t \le \frac{13\pi}{6}\right) \end{cases} \tag{13}$$

$$u_c^*(\omega t) = \begin{cases} 1 + 2m_i \cos\left(\omega t + \frac{\pi}{3}\right) \rightarrow \left(\frac{\pi}{6} \le \omega t \le \frac{5\pi}{6}\right) \\ 1 + 2m_i \cos(\omega t) \rightarrow \left(\frac{5\pi}{6} \le \omega t \le \frac{3\pi}{2}\right) \\ 1 \rightarrow \left(\frac{3\pi}{2} \le \omega t \le \frac{13\pi}{6}\right). \end{cases} \tag{14}$$

The clamped effect is realized by the addition of a ZSS component, which produces no intersection between the clamped phase leg and the high-frequency carrier. This prevents the three phases from being connected to the negative dc rail simultaneously, hence the NNN zero state is eliminated. In this case, the ZSS component is given by the following:

$$u_{\text{zss}}(\omega t) = \begin{cases} 1 - \frac{2m_i}{\sqrt{3}} \sin(\omega t) & \left(\frac{\pi}{6} \le \omega t \le \frac{5\pi}{6}\right) \\ 1 + \frac{m_i}{\sqrt{3}} \sin(\omega t) + m_i \cos(\omega t) & \left(\frac{5\pi}{6} \le \omega t \le \frac{3\pi}{2}\right) \\ 1 - \frac{2m_i}{\sqrt{3}} \sin\left(\omega t + \frac{2\pi}{3}\right) & \left(\frac{3\pi}{2} \le \omega t \le \frac{13\pi}{6}\right). \end{cases} \tag{15}$$

The duty cycles of the dc-side can be determined from the following:

$$d_{aL}^*(\omega t) = \begin{cases} -m_i \cos\left(\omega t - \frac{\pi}{3}\right) \rightarrow \left(\frac{7\pi}{6} \le \omega t \le \frac{3\pi}{2}\right) \\ m_i \cos\left(\omega t + \frac{\pi}{6}\right) \rightarrow \left(\frac{3\pi}{2} \le \omega t \le \frac{11\pi}{6}\right) \end{cases} \tag{16}$$

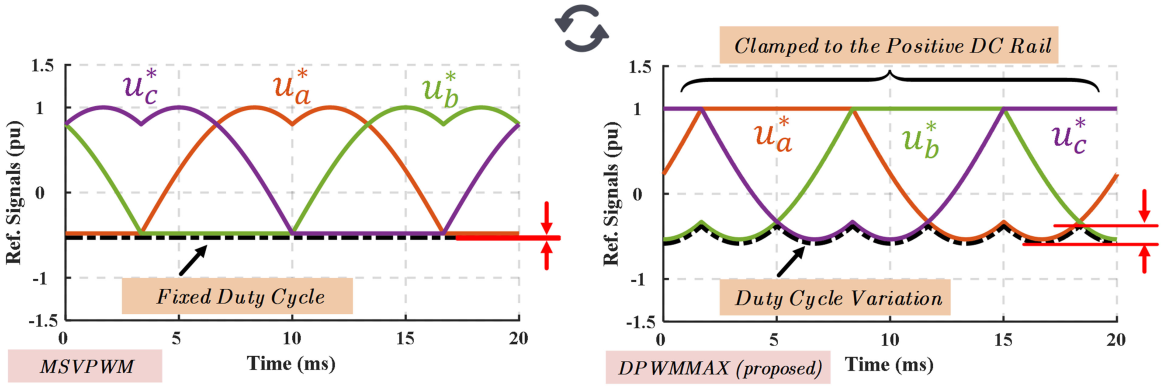


Fig. 11. Novelty behind selecting the proposed modulation scheme.

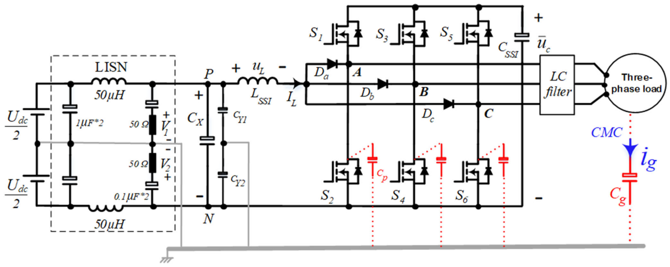


Fig. 12. Schematic diagram of the overall system for simulation and experimental set-up for SSI CMV evaluation.

$$d_{bL}^*(\omega t) = \begin{cases} m_i\cos\left(\omega t - \frac{\pi}{3}\right) \to \left(\frac{\pi}{6} \le \omega t \le \frac{\pi}{2}\right) \\ m_i\cos(\omega t), \to \left(\frac{11\pi}{6} \le \omega t \le \frac{13\pi}{6}\right) \end{cases} \tag{17}$$

$$d_{cL}^*(\omega t) = \begin{cases} -m_i\cos\left(\omega t + \frac{\pi}{3}\right) \to \left(\frac{\pi}{2} \le \omega t \le \frac{5\pi}{6}\right) \\ -m_i\cos(\omega t) \to \left(\frac{5\pi}{6} \le \omega t \le \frac{7\pi}{6}\right). \end{cases} \tag{18}$$

Then, the average duty cycle of the dc-side under the DPWM-MAX can be calculated from the following:

$$\bar{d}_{aL} = \frac{3m_i}{\pi} \to \begin{cases} \left(\frac{7\pi}{6} \le \omega t \le \frac{3\pi}{2}\right) \\ \left(\frac{3\pi}{2} \le \omega t \le \frac{11\pi}{6}\right) \end{cases} \tag{19}$$

where the duty ratios have minimum and maximum limits of (m_i) and $(\sqrt{3}m_i/2)$. In addition to that, the average capacitor voltage can be estimated by the following:

$$\bar{u}_C = \frac{\pi U_{\mathrm{dc}}}{\pi - 3m_i}. \tag{20}$$

The outlines of the key findings corresponding to the CMV from the SSI, and the resultant conducted noise including the proposed modulation scheme, are introduced in the next section.

IV. SIMULATION RESULTS

In order to validate the behavior of the SSI in terms of CMV mitigation and related quantities, a 1-kW system with the schematic circuit shown in Fig. 12 is designed, where the system parameters are summarized in Table IV. For quantitative analysis, a 10-nF capacitor is attached between the load frame and the ground to emulate the stray capacitance [26]. Due to the fact that real mains supplies provide a variable CM and differential-mode impedances based on the environmental circumstances, it is necessary to use a stable and well-defined impedance transducer for conducted noise measurement.

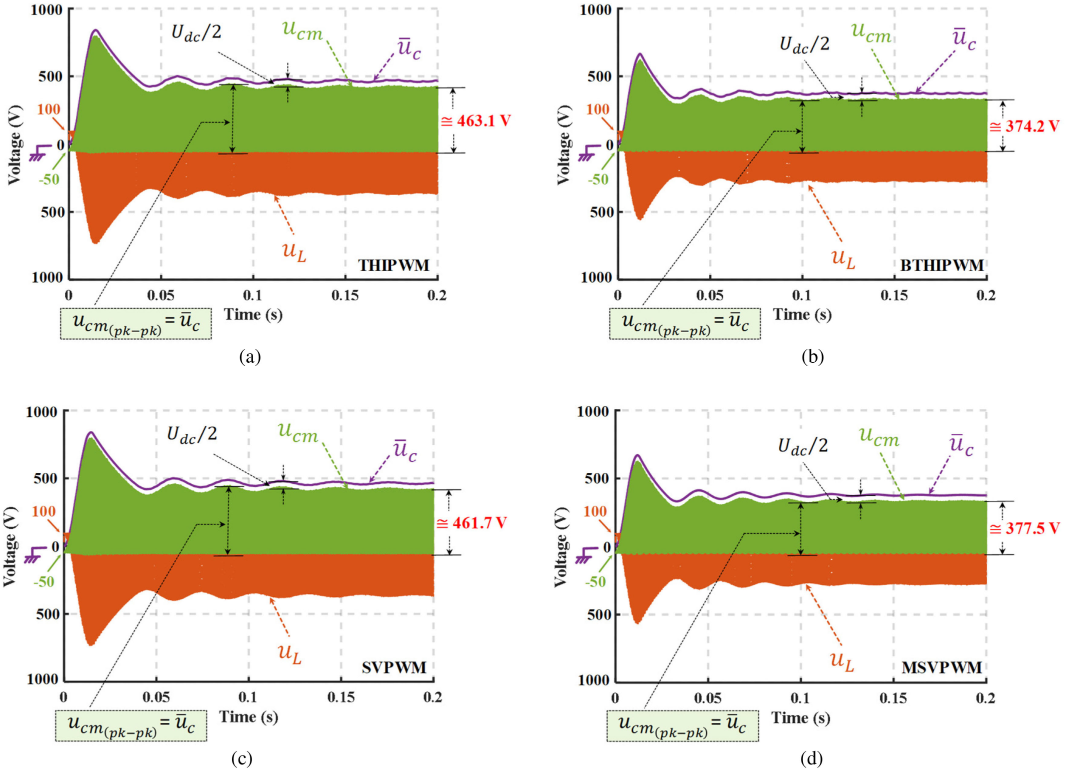
TABLE IV
PARAMETERS OF THE SIMULATED SYSTEM FOR CMV INVESTIGATION

Symbol	Parameters	Value
U_{dc}	DC input voltage	100 V
I_{dc}	DC input current	10 A
f_o	Fundamental frequency	50 Hz
f_S	Switching frequency	10 kHz
L_{SSI}	SSI inductance	5 mH
C_{SSI}	SSI capacitance	168 μF
C_X	Class-X capacitance	41 μF
C_{Y1}, C_{Y2}	Class-Y capacitance	2.2 nF
L_f	Filter inductance	2.5 mH
C_f	Filter capacitance	12 μF
R_{load}	Load resistance	40 Ω

Therefore, the noise voltage is measured by a line impedance stabilization network (LISN), in which a repeatable measurement can be obtained in a wide range of frequencies (conducted noise range of 150 kHz–30 MHz).

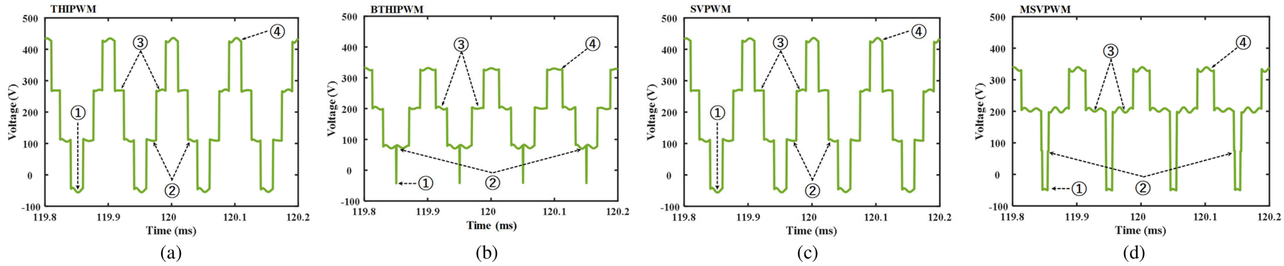
A. Analysis of CMV Results

Simulation results of the SSI, shown in Fig. 13, reveal that all the investigated modulation techniques give a pk-pk value of $\bar{u}_C$ for the CMV. The CMV deviates between $[-U_{\mathrm{dc}}/2]$ and $[\bar{u}_C - U_{\mathrm{dc}}/2]$ as negative and positive peaks, respectively. This is similar to the CMV limits produced by the SPWM strategy shown in Fig. 8. However, the average capacitor voltage differs from a scheme to another one depending on the average duty ratios given in Table III. Moreover, from Table III, it can be stated that the THIPWM and SVPWM schemes have the same average duty cycles of $[0.5 + (3m_i/2\pi)]$. Therefore, the same modulation index is used in the simulation for both schemes, as given in Table III, which gives the same CMV pattern as shown in Fig. 13(a) and (c) with pk-pk voltage of 463.1 and 461.7 V at an average duty ratio of 0.7881. On the other hand, CMVs for the BTHPWM and MSVPWM, illustrated in Fig. 13(b) and (d), have comparable values of 374.2 and 377.5 V at average duty ratios of 0.7371 and 0.74, respectively. The main difference, clarified in the enlarged CMV profiles shown in Fig. 14, is related to the inductor charging states that includes the first



(a) (b) (c) (d)

Fig. 13. Simulated CMV of the SSI under the conventional modulation strategies, showing the voltage across the inductor (u_L) and average voltage across the dc-link capacitor $(\bar{u}_C)$. Note that the starting of the converter is also shown. (a) THIPWM. (b) BTHIPWM. (c) SVPWM. (d) MSVPWM.



(a) (b) (c) (d)

Fig. 14. Zoomed-in view of the simulated CMV of SSI under the conventional modulation schemes. (a) THIPWM. (b) BTHIPWM. (c) SVPWM. (d) MSVPWM.

three levels, according to Table II, while keeping the discharging state approximately without appreciable change. Hence, the fourth level of the CMV does not make a significant change. This is further clarified in Fig. 14(b) and (d).

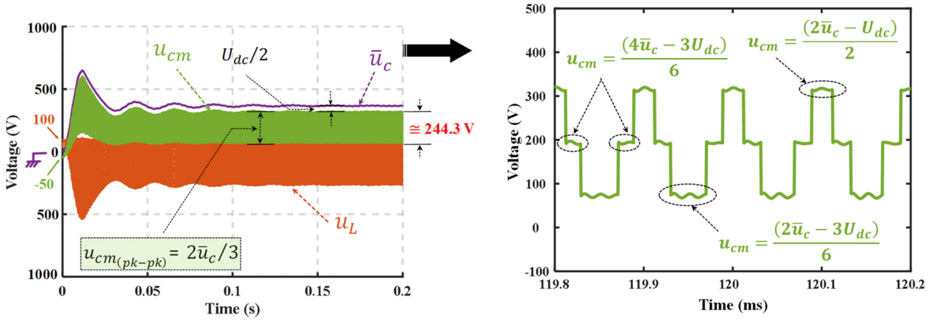
A related point to consider is the number of transitions in the CMV pulse pattern in each switching cycle, which have an effect on the CM noise spectra, from the EMI point of view, especially in the high-frequency region. From Figs. 8 and 14, it is obviously seen that all the CMV waveforms of the five modulation techniques, i.e., SPWM, THIPWM, BTHIPWM, SVPWM, and MSVPWM have six transition actions per switching cycle with four different CMV levels as described in Table II. The simulated CMV of the proposed modulation scheme is given in Fig. 15. It can be seen that the proposed modulation scheme has an average capacitor voltage of 366.6 V from (20) at $\bar{D} = 0.7325$, which is comparable to the average capacitor voltage that results from BTHIPWM and MSVPWM. However, the pk-pk CMV level of the proposed modulation strategy, shown in Fig. 15, has a value of only two-thirds of the average capacitor voltage $(2\bar{u}_C/3 = 244.3\ \text{V})$, compared to $\bar{u}_C$, induced from BTHIPWM or MSVPWM, at values of 374.2 and 377.5 V, respectively. In other words, the proposed modulation eliminates one of the two zero states; NNN that represents the first CMV level according to Table II, while keeping the other three levels with minimum and maximum levels of $[(2\bar{u}_C - 3U_{\text{dc}})/6]$ and $[\,(2\bar{u}_C - U_{\text{dc}})/2]$, respectively, as illustrated in Fig. 15(b).

B. Analysis of Total Harmonic Distortion (THD) Results

The harmonic content is an important aspect that should be considered when comparing different modulation schemes for both switched output voltage and/or current. The sideband harmonic number for each modulation scheme can be determined from the following [29]:

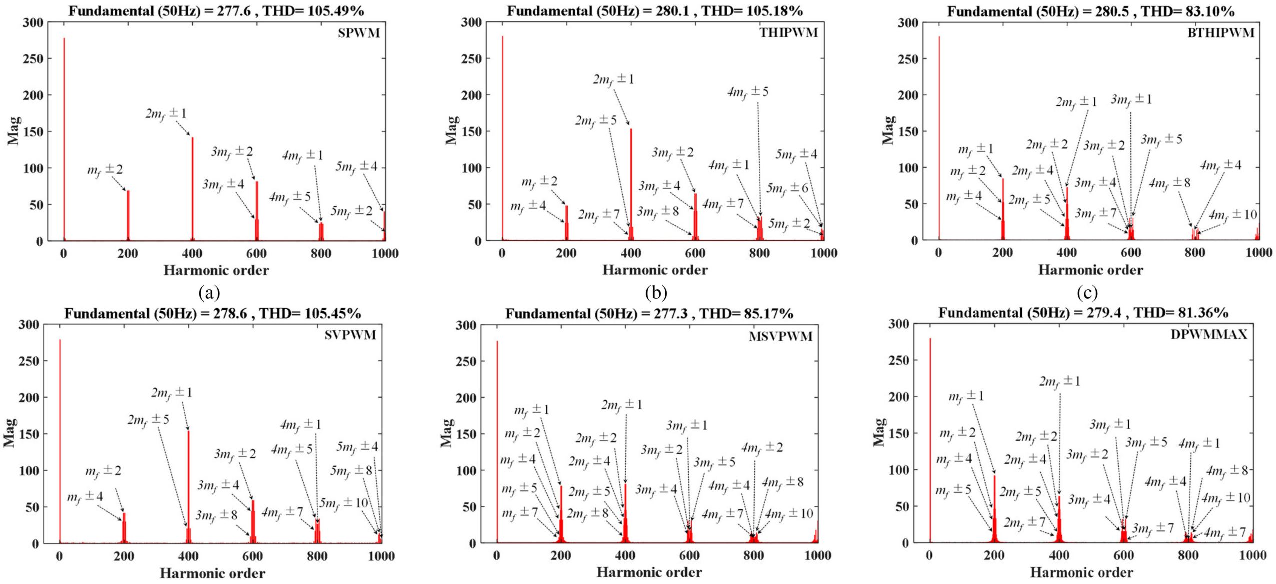
$$h = pm_f + q \tag{21}$$

where p and q are integers. This harmonic index is always used to characterize the harmonic content in the output voltage or



(a) (b)

Fig. 15. Obtained simulation results of the CMV for the SSI under the proposed modulation strategy. Note that (b) is a zoomed-in view of (a).



(a) (b) (c)

(d) (e) (f)

Fig. 16. Simulated THD content of line-to-line voltage of SSI. (a) SPWM. (b) THIPWM. (c) BTHIPWM. (d) SVPWM. (e) MSVPWM. (f) Proposed DPWMMAX.

current. The THD of the line voltage is used as a performance index of the investigated modulation techniques. The simulated fast Fourier transform (FFT) analysis from Simulink powergui of the line voltage is presented in Fig. 16. From this figure, one important point to note is that all the modulation schemes have the same fundamental voltage with different THD distribution. The THD of the line voltage for the SPWM, THIPWM, and SVPWM schemes approximately have the same values. In case of odd numbers of p, the sidebands exist only for even values of q. On the contrary, for even values of p, the sidebands exist only for odd values of q, as clearly shown in Fig. 16(a), (b), and (d). In fact, this is due to the symmetrical configuration of their modulating signals shown in Figs. 3(a) and (b), and 9(a). On the other hand, the line voltage for the BTHIPWM, MSVPWM, and DPWMMAX schemes, has a comparable THD values, yet the proposed modulation technique has the lowest THD content. In contrast to SPWM, THIPWM, and SVPWM schemes, the harmonic sidebands for BTHIPWM, MSVPWM, and DPWMMAX schemes exist for most values of q whatever value the p has, even or odd, as pointed out in Fig. 16(c), (e), and (f), respectively, but at much lower amplitudes. In other words, BTHIPWM, MSVPWM, and DPWMMAX have a widespread harmonic signal distribution that reduce the harmonic content of the line voltages instead of concentrating the harmonic components at a specific harmonic order. This is due to the asymmetrical configuration around the time-axis of the modulation signals, as illustrated in Figs. 9(b) and (c), and 11.

C. *Analysis of CM Noise Source Spectra*

A reduced EMI noise can be obtained through manipulation of the noise source voltage using modification either in the topology [30] or in the modulation scheme [19], which is one of the aims of this research, or by using extra CM chokes. In this section, the effect of the achieved CMV reduction on the CM noise spectra produced by the SSI is studied. The SVPWM scheme is considered as a reference one for comparison between modulation schemes, where Hou *et al.* in [18] proved that SVPWM scheme has the worst case in terms of the CM noise due to the null vector states utilization. Fig. 17 shows a simulated comparative analysis of the noise source spectra for the investigated modulation schemes. The frequency range is limited to 1 MHz due to the insufficient number of points obtained from simulation results for performing the FFT algorithm. From this figure, it is

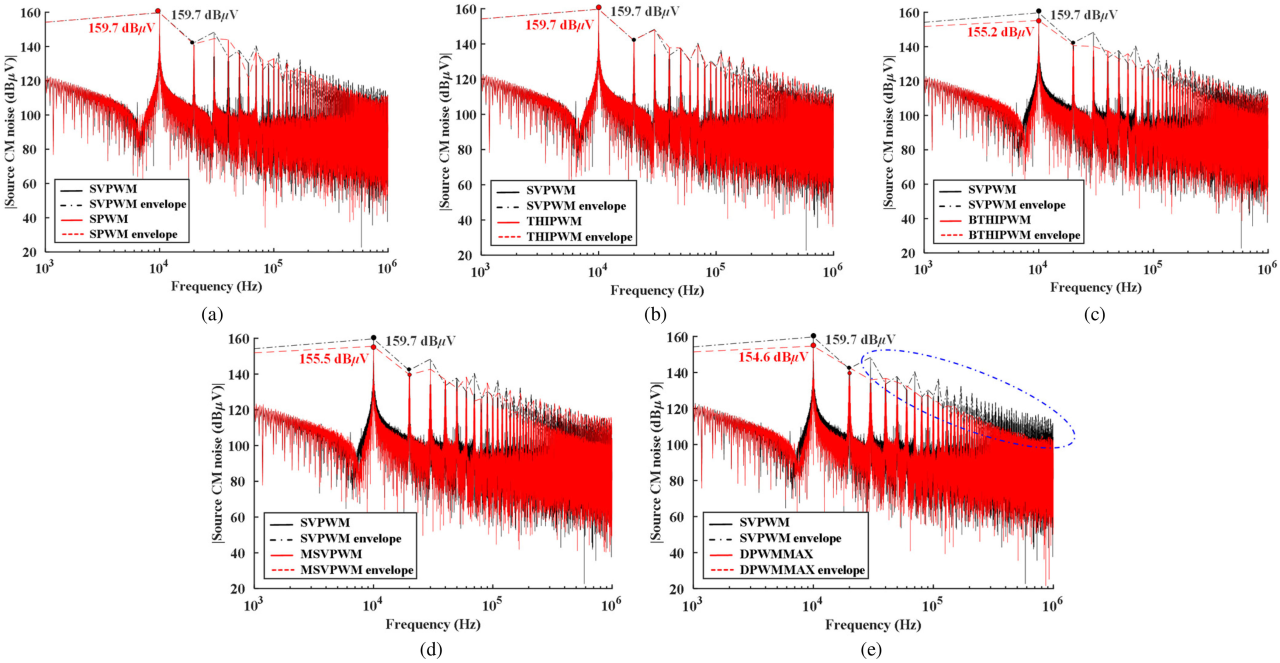


Fig. 17. Simulated results of CM noise source spectra for the SSI under different modulation strategies. (a) SVPWM versus SPWM. (b) SVPWM versus THIPWM. (c) SVPWM versus BTHIPWM. (d) SVPWM versus MSVPWM. (e) SVPWM versus DPWMMAX.

worth noting that noise source spectra of the SPWM, THIPWM, and SVPWM have the same characteristics, as described in Fig. 17(a) and (b). On the other hand, the peak magnitudes of the noise source spectra of BTHIPWM and MSVPWM schemes decreased by about 4.5 dB and 4.2 dB μV, respectively, at the switching frequency of 10 kHz compared with that of SVPWM, as illustrated in Fig. 17(c) and (d), respectively. On the other hand, the application of the proposed modulation scheme not only achieves some reduction in the peaks of the CM noise source spectra in the low-frequency range, but also achieves some peaks' attenuation at higher frequencies. For instance, at the switching frequency of 10 kHz, an approximate reduction of 5.1 dBμV is achieved, shown in Fig. 17(e), which is higher than the reduction attained by BTHIPWM and MSVPWM strategies. It is supposed that this reduction in the peak value at the switching frequency is due to the reduction achieved in the rms value of the CMV. In particular, for the system parameters given in Table IV, it has been found that the SPWM, THIPWM, and SVPWM schemes have CMV rms values of 243.19, 244.88, and 244.29 V, respectively, which seems to be comparable. On the other hand, modulation techniques of BTHIPWM, MSVPWM, and DPWMMAX have CMV rms values of 210.04, 210.98, and 206.92 V, respectively, which are also comparable. So far, the proposed one has the lowest CMV rms value. Moreover, by comparing both groups of CMV rms values, it can be seen that a much reduction in the CMV rms values can be achieved by using the BTHIPWM, MSVPWM, and DPWMMAX control schemes.

D. Analysis of CM Current (CMC) Results

Reducing the CMV magnitude and number of transitions per-switching cycle are the key factors for the CM current (CMC) reduction. In this framework, the simulated CMC (i_g) values, measured as indicated in Fig. 12 with blue color, for the different modulation schemes are plotted in Fig. 18. Out of all the modulation schemes, THIPWM and SVPWM schemes experience the same (highest) CMC values. This similarity is contributed to the duty ratios, which have the same expressions and values as given in Table III. For the SPWM and BTHIWPM, comparable CMC values are induced. Finally, the proposed modulation scheme has by far the lowest CMC behavior due to the lower number of transition actions.

V. EXPERIMENTAL VALIDATION

A typical CM conducted emission test setup is described in Fig. 19. The system components and measurement are based on the complete equivalent system shown in Fig. 12. A programmable ac/dc power supply (KP3000S) with 3 kVA rating is used as a power supply. This power supply is connected to the device under test (DUT) through a commercially available LISN (ESH2-Z5) manufactured by Rohde & Schwarz. An EMI test receiver of (ESCI 1166.5950.03) is attached to the LISN that is used for measuring accurate frequency spectrum from the diverted noise. A postprocessing computer-based procedures are carried out to obtain the resultant noise spectrum. A separation distance of 40 cm is necessary between the bottom of the DUT and the ground reference plain (GRP), with at least 80-cm clearance from all other conducting surfaces. The GRP of the test setup is connected to the LISN's ground terminal.

The experimental platform of the presented study, used for performing CMV reduction verification and CM conducted noise emissions measurements, is depicted in Fig. 20. The SSI power circuit comprises the conventional B6-bridge with inductor/capacitor set (L_{SSI} and C_{SSI}) and additional three diodes

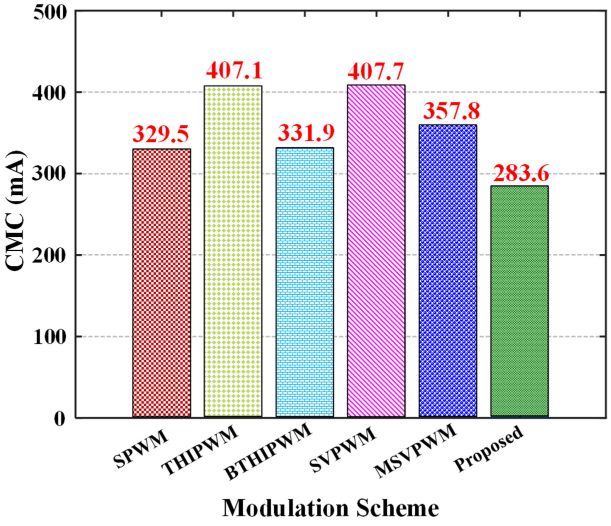


Fig. 18. Simulated CMC at different modulation strategies for the same power rating.

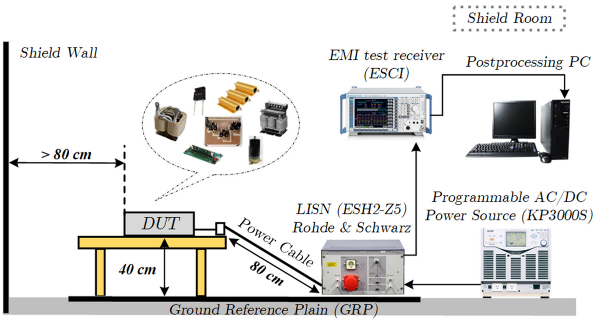


Fig. 19. Typical CM conducted noise emission test setup.

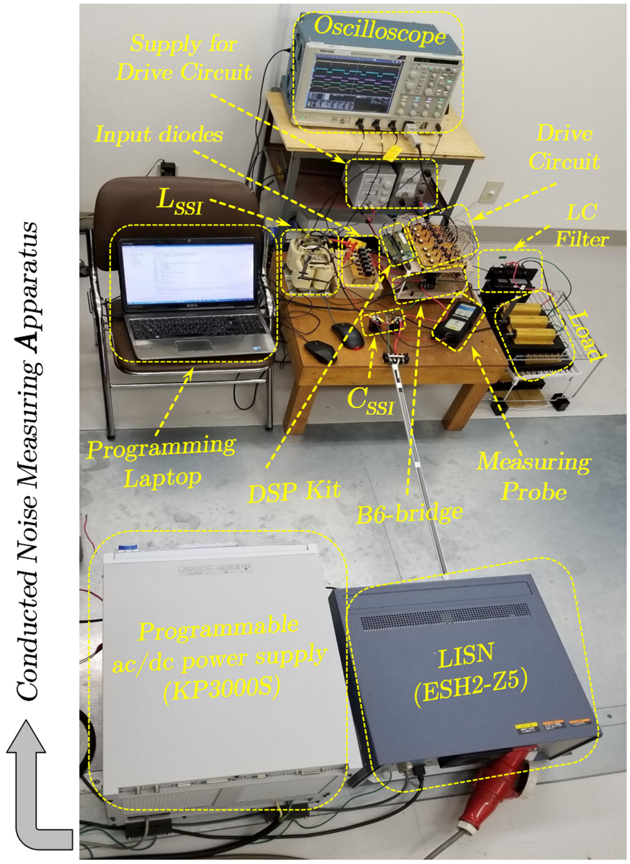
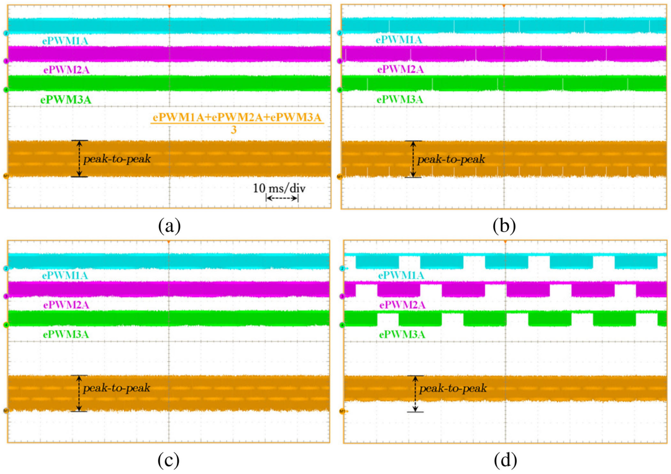


Fig. 20. Experimental platform for complete system.



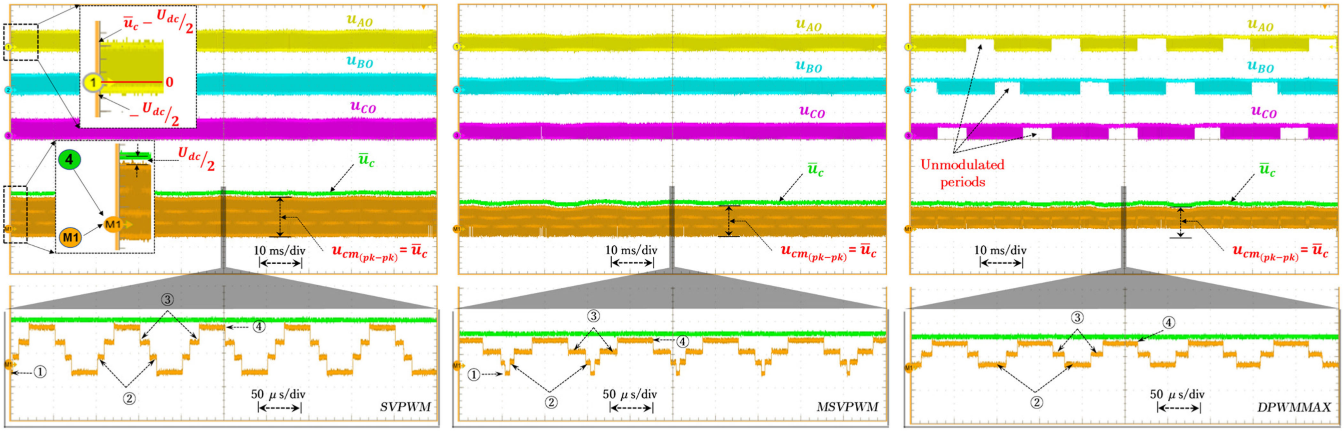
(a) (b)

(c) (d)

Fig. 21. Experimental validation of the conducted modulation techniques in terms of gating signals and their expected CMV waveform (5 V/div for the vertical axis). (a) SPWM, SVPWM, and THIPWM. (b) BTHIPWM. (c) MSVPWM. (d) DPWMMAX.

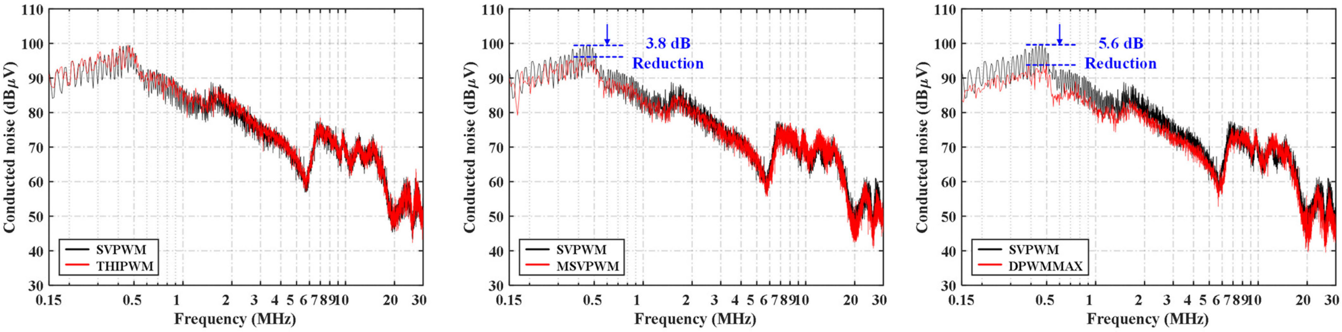
in the input side of the three-phase inverter. The conventional B6-bridge consists of three-pairs of complementary SiC semiconductor power MOSFET (C3M0065090D) from Wolfspeed (A CREE company) with voltage and current ratings of 900 V and 36 A, respectively. The inductor and capacitor values are 5 mH (LC32AM-2.5M28A) and 168 μF, respectively. A high-performance fast recovery diode with low loss (DHG30I600HA from IXYS) is used for the extra diode. It has a maximum repetitive reverse voltage of 600 V and average forward current of 30 A. The three-phase load consists of a set of power resistances with an average value of 40 Ω per phase and *LC* filter with 2.5 mH and 12 μF, respectively. The experimental results have been recorded using a digital phosphor oscilloscope (DPO7104C-G3) from Tektronix. For gate driver, IR2110 driver chip, from International Rectifier, is used as high side and low side MOSFET driver circuitry. It has a floating circuit to handle a bootstrap operation, which is cost effective in driving two switches (i.e., upper and lower) with only one driver chip. The gate voltage is controllable from a digital signal processor (DSP) output pins, which is normally referenced to ground. The real-time modulation techniques are realized through programming a TMS320F28069 DSP from Texas Instruments. This control card features a high-efficiency 32-Bit CPU and single-precision floating-point operations. The implementation of the conducted modulation schemes is done through Code Composer Studio programming.

In this article, six modulations schemes were studied, programmed, analyzed, and experimentally investigated. Fig. 21 illustrates the experimental validation of the conducted schemes



(a) (b) (c)

Fig. 22. Experimental relationship between phase-legs voltages, CMV pulse shape and average capacitor voltage where (Ch1—Ch3 have 200 V/div) and (Ch4 and M1 have 100 V/div) for the vertical axis. (a) SVPWM. (b) MSVPWM. (c) DPWMMAX (Proposed).



(a) (b) (c)

Fig. 23. Experimental comparison for the conducted noise spectra from LISN. (a) SVPWM versus THIPWM. (b) SVPWM versus MSVPWM. (c) SVPWM versus DPWMMAX.

in terms of gating signals and their expected CMV pulses by simply averaging the three gating signals. From these figures, it is worth noting that the main difference between these results is the clamping periods to the positive dc rail occurred in the DPWMMAX scheme, in which the switches exhibit nonswitching actions. This effect has a reflection on the CMV pulse shapes thereby eliminating one pulse during each switching cycle. By using the same simulation parameters listed in Table IV except the dc supply is downscaled to 50 V. Fig. 22 shows the actual phase-legs voltages with respect to reference point (O), as described earlier in Fig. 11, in which the asymmetrical configurations of the phase-leg voltages and CMV are verified as illustrated in Fig. 22(a). Meanwhile, the relationship between the CMV and the average capacitor voltage is confirmed, as described in Figs. 8 and 15. Furthermore, it can be seen that the pk-pk level of the resultant CMV is reduced due to the proposed modulation scheme, as shown in Fig. 22(c). The comparison indicates that a good agreement between the simulated results and experiments is attained in terms of CMV pulse shape and number of CMV levels along with the number of switching actions as listed in Table II.

The verification of the EMI conducted noise reduction is obtained from LISN measurements through EMI test receiver, as clearly demonstrated in Fig. 23. From this figure, it can be observed that the THIPWM scheme has the same noise spectra as SVPWM scheme, as described previously in Fig. 17(b), in which no reduction in the noise spectra can be achieved. The same effect is available for SPWM scheme. On the other hand, an attenuation in the peaks of the EMI noise spectra can be attained using both of the MSVPWM and DPWMMAX schemes, in which the highest reduction is achieved using the proposed control scheme, as shown in Fig. 23(c). It is worth mentioning that the BTHIPWM has approximately the same attenuation in the noise spectra as that achieved using MSVPWM.

VI. CONCLUSION

The CMV behavior of the conventional VSI using the RCMV-PWM techniques is briefly reviewed and limitation of applying such techniques in SSI is also investigated which is not yet considered in the existing literature. Considering the inherent constraint of the SSI, which is preserving the discharging state of the SSI inductor, this article proposed and deeply investigated the use of a DSVPWM scheme to operate the SSI and mitigate the instantaneous peak value of the induced CMV as well. The simulated and experimental results indicate that the SPWM, SVPWM, and THIPWM schemes experience the same characteristics in terms of the investigated parameters in SSI. Similarly, the BTHIPWM and MSVPWM schemes provide similar performance. Though the DPWMMAX control scheme is not newly developed here, its implementation to the SSI provided several attractive merits compared to counterparts which are as follows.

1) The achieved reduction in the dc-link voltage applied to the dc-link capacitors when using the BTHIPWM and MSVPWM schemes compared to other modulation schemes is also attained using the proposed DPWMMAX scheme. Accordingly, the dc-link ripple current can be reduced, which means less loss and lower operating temperature. Hence, the dc-link capacitor's life expectancy can be extended.
2) Reducing the voltage stress on the semiconductor switching devices due to the reduction achieved in the dc-link voltage. Though this reduction can also be obtained using the BTHIPWM and MSVPWM schemes due to the reduced dc-link voltage. However, a further reduction can be achieved using the proposed modulation scheme especially for the lower IGBTs due to the unmodulated periods.
3) Reducing around one-third of the switching power loss in the semiconductor switching devices due to the one-third unmodulated (nonswitching) periods of the switching devices.
4) Reducing the instantaneous pk-pk CMV with approximately 33.33% (due to the elimination of one-zero state vector), compared to that obtained using BTHIPWM and MSVPWM schemes.
5) Reducing the switching transitions to four transition actions within one switching cycle using the proposed DPWMMAX scheme, compared to six transition actions using counterparts. Therefore, further attenuation in the CM noise spectra is achieved.
6) Reducing the leakage CMC that flows through the stray capacitance existing between the load frame and GRP.

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