Recovering Partial Three-Level Operation in a T-Type Inverter With Fault Management Redundant Unit

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***Abstract*—A redundant unit has been utilized in prior work for a T-type three-level inverter to handle multiple open-circuit faults, but the output was limited to two levels. In this article, equivalent switching state and improved virtual vector methods are proposed to complement switching states and provide better fault-tolerant performance. Under fault scenarios, equivalent replacement of unreachable switching states can be used to generate the target line-to-line voltages. If the replacement cannot be achieved by equivalent switching states, a virtual vector with redundant capability is employed to support two- and three-level modulations at the output. The rearranged switching sequences can be formed by employing virtual vectors and existing vectors. In addition, by reconstructing the virtual vectors, a balancing method is adopted to eliminate neutral point voltage offset in cases of multiple faults. Experimental tests verify the effectiveness and feasibility of the proposed method.**

***Index Terms*—Fault-tolerant control, multiple open-circuit faults, redundant topology, space vector modulation (SVM), T-type inverters.**

I. Introduction

MULTILEVEL inverters have advantages over conventional two-level inverters in various industrial applications, such as a high effective switching frequency, low total harmonic distortion (THD), and high efficiency [1]–[3]. Among multilevel inverters, the T-type three-level ($T^2$3L) inverter, shown in Fig. 1, has the highest efficiency in low-voltage and medium switching frequency (4–30 kHz) applications [4], [5].

Power semiconductor devices are relatively vulnerable, limiting system reliability [6]. Devices such as insulated-gate bipolar transistors (IGBTs) may suffer from short-circuit (SC) or open-circuit (OC) faults. Catastrophic damage can happen quickly following SC faults [7]–[9]. OC faults can cause output distortion and problems in other parts, which will degrade system performance [10]–[12]. Here, power device redundancies and fault-tolerant strategies are explored to provide continuous operation in OC fault scenarios [13], [14].

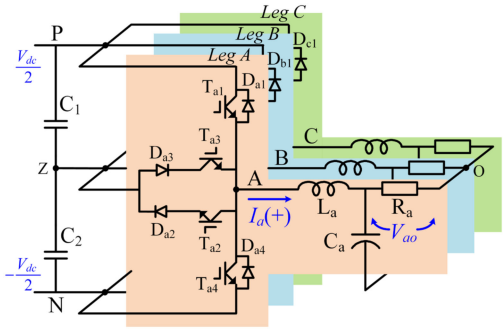

Fig. 1. Diagram of a three-phase $T^2$3L inverter system.

Fault-tolerant capability is essential for system reliability improvement, especially for applications with high availability requirements. Multilevel converters with redundant switching states manage OC faults in [15]–[18]. Redundant strategies based on space vector modulation (SVM) for T-type inverters were proposed in [17] and [18] to mitigate OC faults without additional hardware. In those cases, continuous operation is possible, but the maximum modulation index reduces in some scenarios due to asymmetry of switching states.

The fault-tolerant schemes based on hardware circuits proposed in [19]–[23] avoid modulation index reduction. In [19] and [20], a quasi-Z-source $T^2$3L inverter addresses OC faults in a half-bridge switch. The circuit can operate with no decrease in output voltage because this topology can boost as needed, but devices must be rated for the boosted dc-link voltage. An additional leg is added in [21]–[23] to expand fault tolerance. The added leg can be used to improve the performance of power converter during normal operation, although power loss in the redundant leg may compromise reliability improvements. When an OC fault occurs, redundant devices can take over for the failed parts and maintain rated output voltage, although only one faulty leg can be managed.

In practice, considering the high number of power switches in multilevel inverters, faults are likely to occur simultaneously

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TABLE I
OVERVIEW OF DIFFERENT T-TYPE INVERTER TOPOLOGIES WITH FAULT-TOLERANT CAPABILITIES

Topology		Conventional T^{2}3L	[19]	[21]	[22]	[23]	Proposed topology
Extra components	Capacitor	0	2	0	2	0	0
	Inductor	0	4	0	1	0	0
	Fuse	0	0	0	11	0	0
	Diode	0	2	0	0	0	6
	Switch device	0	0	4	17	11	2
Device blocking voltages	$1.73V_{dc}$	0	6 switches 6 diodes	0	0	0	0
	V_{dc}	6 switches 6 diodes	0	8 switches 8 diodes	16 switches 8 diodes	11 switches 8 diodes	14 switches 12 diodes
	$0.87V_{dc}$	0	6 switches 8 diodes	0	0	0	0
	$0.5V_{dc}$	6 switches 6 diodes	0	8 switches 8 diodes	13 switches 6 diodes	12 switches 12 diodes	6 diodes
Fault tolerant types and multiple faults allowed simultaneously	SC faults in RS	0	—	2	2	2	2
	OC faults in RS	0	—	2	0	0	0
	SC faults in HS	0	0	0	2	2	0
	OC faults in HS	0	2	2	2	2	6
	SC faults in MS	0	0	2	2	2	0
	OC faults in MS	6	6	6	6	6	6
Output derating		no	no	no	no	no	no

Note: "$V_{\rm dc}$" means "input dc voltage." "HS" means "half-bridge switch," "MS" means "middle switch," and "RS" means "redundant switch."

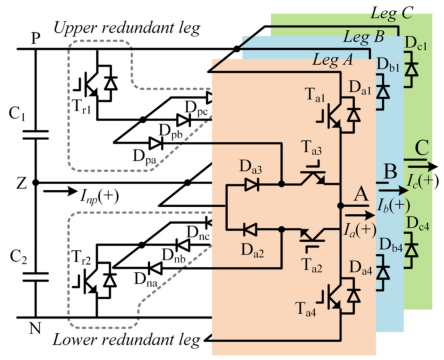

Fig. 2. T^{2}3L inverter topology with shared redundant unit.

in multiple devices connected to the same branch. Due to failure rates and similar operating conditions in each leg, faults may also occur sequentially in different legs during fault-tolerant operation. The occurrence of multiple switch failures as a possible situation in inverter systems has been analyzed in [24]–[26], where corresponding diagnosis methods were also introduced. However, effective schemes for supporting sustained operation with multiple faults are rarely covered. A redundant control strategy for a three-phase neutral point (NP) clamped active rectifier is presented in [27], which can handle multiple OC faults in its inner switches. However, half-bridge switch OC faults in the T-type inverter will increase output distortion [18]. Enhancing system capability to tolerate single and multiple faults is necessary for reliable operation and to avoid harmful consequences.

A T^{2}3L inverter with a shared redundant unit (SRU-T^{2}3LI) was proposed in [28] to handle multiple OC faults in half-bridge switches (T_{x1} and T_{x4}), as shown in Fig. 2. The redundant unit includes two switches and six diodes, with the active switches (T_{r1} and T_{r2}) connected by diodes to middle switches (T_{x3} and T_{x2}, $x =$ a, b, c) of each phase. The redundant unit can be shared by all three main legs. The added unit is idle during normal operation, with no extra power loss. The characteristics of existing and proposed T-type topologies, and their fault-tolerant performance, are summarized in Table I.

In Table I, tolerable fault scenarios, cost (extra components necessary to implement redundancy), and the blocking voltages of devices, including antiparallel diodes of power switches are listed. The conventional T^{2}3L inverter is adopted as a reference. The main advantage of the proposed circuit compared to previous redundant leg topologies is the ability to tolerate OC faults in multiple phases with full use of healthy devices in faulty legs. More redundant legs can be added to existing schemes to address multiple fault scenarios, but the number of devices and gate drivers must increase proportionally. Compared to conventional T^{2}3L inverters, middle switches in the proposed topology need to be overdesigned because their maximum blocking voltages change from 0.5 $V_{\rm dc}$ to $V_{\rm dc}$. The added devices should also be rated for $V_{\rm dc}$.

In this article, a fault-tolerant control strategy extends the results in [28], employing SVM to recover three-level operation under many fault scenarios. By applying the proposed strategy, switching states rendered unreachable by faults can be replaced with equivalent switching states or virtual vectors. The duration of switching states used to synthesize a virtual vector can be calculated based on constant average output voltages over each switching cycle. A voltage balancing method is adopted to eliminate NP deviation. Experimental results are presented to validate the proposed fault-tolerant strategy at various modulation indices.

II. ANALYSIS OF FAULT-TOLERANT T-TYPE INVERTERS

The proposed SRU-T^{2}3LI can address OC faults in multiple half-bridge switches and isolate SC faults in redundant switches.

TABLE II
TOLERABLE FAULT SCENARIOS

Fault location	Fault device
OC faults in half-bridge switches	T_{x1}, T_{y1} (T_{x4}, T_{y4}) (T_{x1}, T_{y4})
SC faults in redundant legs	T_{r1}, T_{r2}
OC faults in upper half-bridge switches and SC fault in the lower redundant leg	T_{x1}, T_{r2}
OC faults in lower half-bridge switches and SC fault in the upper redundant leg	T_{r1}, T_{x2}

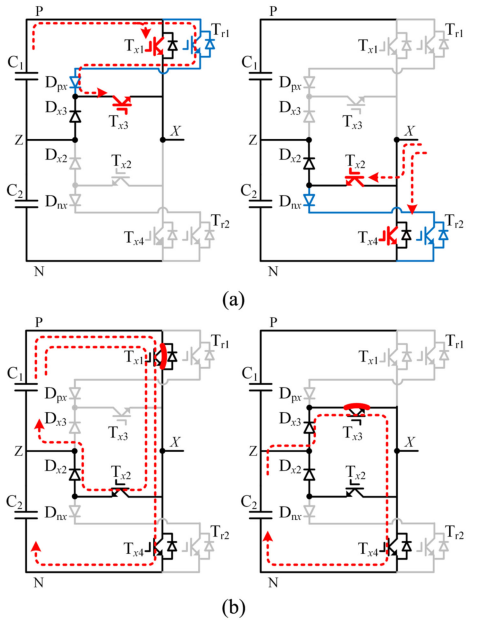

Fig. 3. Abnormal current paths (the devices in grey are OFF) in phase X (X = A, B, C) when (a) OC faults in half-bridge switches and middle switches occur simultaneously and (b) SC fault occurs in half-bridge switches or middle switches.

When various types of failures occur simultaneously, the tolerable scenarios are listed in Table II.

OC faults in middle switches are not included in this table since continuous operation can be ensured through degraded output levels without additional redundant devices [17], [18]. However, if OC faults occur simultaneously in both half-bridge switches and middle switches, such as T_{x1} (T_{x4}) and T_{x3} (T_{x2}), as shown in Fig. 3(a), this topology cannot remain in operation, since the faulty leg cannot connect to one side of the dc bus. Fig. 3(b) shows an SC loop formed around the dc-link capacitors. Redundant legs cannot open the abnormal current path, and SC faults in the main leg should be isolated immediately.

In [28], control approaches for fault management in the SRU-T^{2}3LI were presented. All three phases can output two-level voltages by disabling middle switches if the redundant switches have SC faults. Similarly, redundant switch SC faults have no adverse impact on redundant operation. Fig. 4 depicts circuit operation to isolate redundant device SC failure and tolerate an OC fault in a half-bridge switch. When OC faults occur in multiple half-bridge switches, a standby current path consisting of the redundant leg and middle switches can be formed. Positive and negative outputs are still possible. Without a connection to the NP, the circuit reverts to two-level modulation. In contrast, here, it is shown that switching states can generate three output levels in many fault cases.

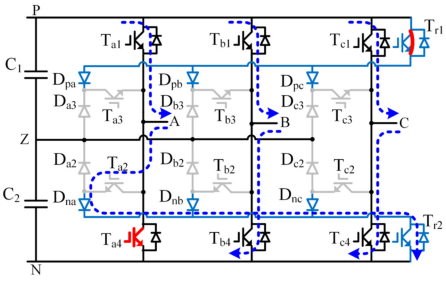

Fig. 4. Current path with T_{r1} SC fault and T_{a4} OC fault.

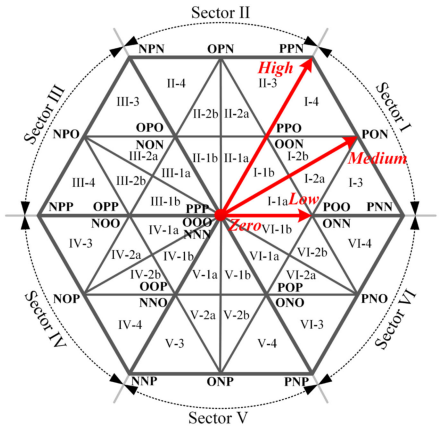

Fig. 5. Space voltage vector diagram of a three-level T-type inverter.

In the space vector diagram of Fig. 5, 27 switching state combinations are distributed across six sectors, where states [P], [O], and [N] indicate that the output pole voltage V_{XZ} is positive, zero, or negative, respectively. Each sector contains six regions, shown as regions 1a, 1b, 2a, 2b, 3, and 4 in Fig. 5. Switching states are represented by zero, low, medium, and high-voltage vectors, based on their magnitudes. In accordance with the direction of the NP current ($I_{\rm np}$), two switching states are involved in each low-voltage vector. These can be designated with states [P] (such as [PPO]) and [N] (such as [OON]). After implementing redundant devices, lost switching states are analyzed for representative cases to analyze manageable fault cases given structural symmetry. Current flowing from the input to loads is defined as positive $I(+)$. Positive and negative $I_{\rm np}$ can be represented by states [O+] and [O−], respectively.

A. Case I: OC Faults in T_{a1} and T_{b1}

Once faults occur, T_{r1} should be turned ON to provide a connection to the dc bus, and fault phases can still deliver positive output through T_{a3} or T_{b3}. As shown in Fig. 6(a), when the circuit operates during [POO] and $I_a > 0$, T_{r1} is ON and diodes D_{x3} are reverse biased. In this case, T_{a3} is turned ON, and T_{b3} and T_{c3} should be turned OFF to avoid forming an SC ($T_{r1} - D_{px} - T_{x3} - T_{x2} - D_{x2}$) around C_1. Thus, if I_b

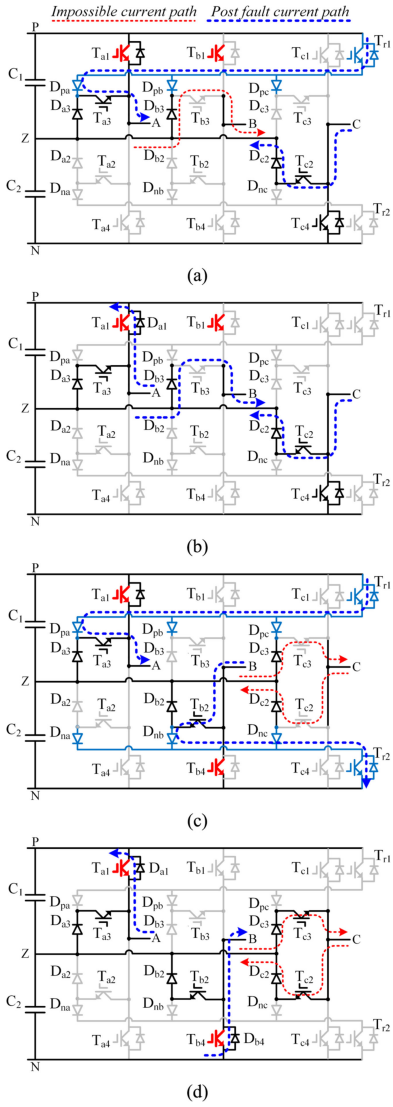

Fig. 6. Current paths during fault-tolerant operation. (a) OC faults occur in T_{a1} and T_{b1} during [POO] when $I_a > 0$. (b) OC faults occur in T_{a1} and T_{b1} during [POO] when $I_a < 0$. (c) OC faults occur in T_{a1} and T_{b4} during [PNO] when $I_a > 0$ and $I_b < 0$. (d) OC faults occur in T_{a1} and T_{b4} during [PNO] when $I_a < 0$ and $I_b > 0$.

is positive, state [O] in phase B is unreachable. Hence, when T_{r1} is ON, low- and medium-voltage vectors that contain [O+], such as [POO] and [PON], become invalid, but high-voltage vectors will not be affected. The loss of state [O] in a given phase due to redundant legs involved in fault-tolerant operation is defined here as a "state-loss" phase. During normal operation, the blocking voltage of T_{a3} is $0.5V_{\rm dc}$. When T_{r1} is switched ON, T_{a3} will be connected to the dc bus, so it needs to be rated for $V_{\rm dc}$. In this case, the voltage across T_{c3} is $0.5V_{\rm dc}$ when I_c flows through the NP, which will increase to $V_{\rm dc}$ if phase C operates during state [N].

Since IGBTs with antiparallel diodes (D_{x1} and D_{x4}) are employed for the half-bridge switches, when T_{a1} fails, the post fault reverse current I_a can still flow through the parallel diode D_{a1} even though D_{pa} is reverse biased, as shown in Fig. 6(b). The redundant leg is not involved in fault-tolerant operation in this case. The circuit will no longer operate properly if both D_{a1} and T_{a1} fail.

B. Case II: OC Faults in T_{a1} and T_{b4}

When T_{a1} and T_{b4} fail, T_{r1} and T_{a3} are turned ON to provide a positive current path during state [P] in phase A, and T_{r2} and T_{b2} should be turned ON to provide a negative current path during state [N] in phase B. High-voltage vectors can still be achieved. However, state [O+] is not available in phases B and C if T_{r1} is ON, and state [O−] is unreachable in phases A and C when T_{r2} is ON. Fig. 6(c) shows the current path during switching state [PNO]. Under this condition, both T_{c2} and T_{c3} are OFF. State loss has occurred in phase C since I_c cannot flow through NP and state [O] is unreachable. The middle switches must be rated for $V_{\rm dc}$ in this case.

If $I_a < 0$ or $I_b > 0$, the post fault current path can be formed through D_{a1} or D_{b4}, as depicted in Fig. 6(d). OC failures have no adverse impacts on operation, provided that antiparallel diodes D_{a1} and D_{b4} are working.

As analyzed earlier, when faults occur in half-bridge switches, T_{r1} (T_{r2}) can provide a positive (negative) current path connected to the dc bus, which will cause the loss of state [O+] (state [O−]) in a phase. Reverse current can flow through the antiparallel diodes in faulty legs. In the following section, scenarios are considered in which post fault current cannot flow through corresponding failed switches.

III. Fault-Tolerant Control Strategy for Recovering Three-Level Operation

To mitigate unreachable switching states during faults, a control strategy is proposed here for the SRU-T^{2}3LI. The explanation will be divided into low and high modulation index regimes, shown, respectively, as regions 1a and 1b, and as regions 2a, 2b, 3, and 4 in Fig. 5.

A. Low Modulation Index

At low modulation index, only zero- and low-voltage vectors compose the switching sequence. If an upper half-bridge switch (T_{x1}) fails, unreachable [P] switching states can be changed to equivalent [N] switching states. If a low-side switch (T_{x4}) fails, [P] switching states can substitute for [N] switching states. These replacements will not affect the three-phase output, since equivalent [P] and [N] switching states can generate the same line-to-line voltages.

1) *Case I. OC fault in T_{a1} and T_{b1}:* To tolerate a T_{a1} OC fault, T_{r1} are turned ON, and T_{b3} and T_{c3} should be turned OFF when phase A operates during state [P]. The low-voltage vectors in sectors I and VI, such as [POO], become unreachable if I_b or I_c is positive. Similarly, [OPO] is no longer reachable due to a T_{b1} OC fault if I_a or I_c is positive.
2) *Case II. OC fault in T_{a1} and T_{b4}:* When a fault occurs in T_{b4}, [N] switching states in sectors V and VI, such as [ONO], become unreachable if I_a or I_c is negative since T_{r2} is ON. Considering a fault in T_{a1}, [P] switching states

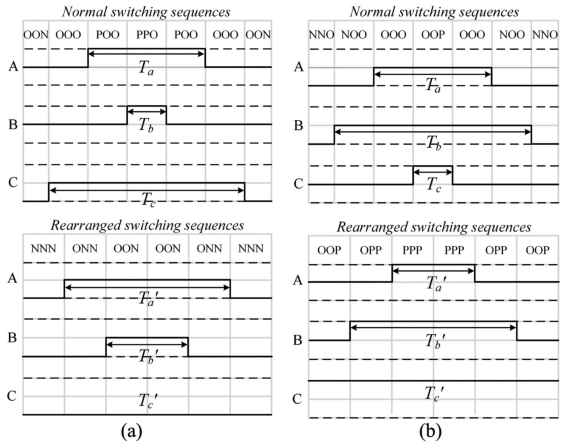

Fig. 7. Arrangement of switching sequence to tolerate T_{a1} and T_{b1} OC faults in (a) region 1b of sector I, and (b) region 1b of sector IV.

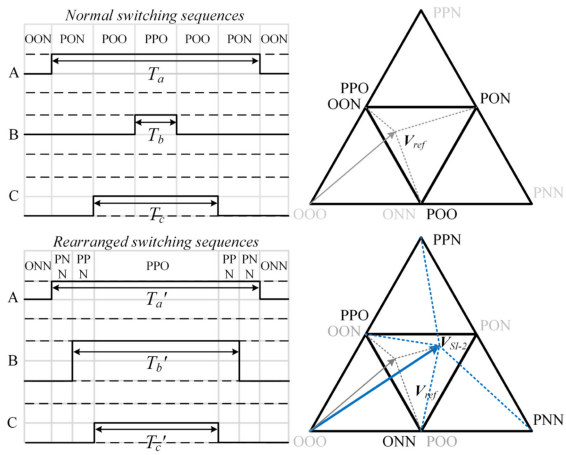

Fig. 8. Arrangement of switching sequence to tolerate T_{a1} and T_{b1} OC faults in region 2b of sector I (unused states are represented in grey color).

TABLE III
RECONFIGURED TURN-ON TIMES AT LOW MODULATION INDEX

Sector and region	Current	Fault cases	Redefined T_{on}
I-1b	$I_b>0$	Case I Case II	$T'_{a,b}=T_{a,b}+T_{min}$ $T'_c=0$
II-1a	$I_a>0$	Case I	$T'_{a,b}=T_{a,b}+T_{min}$
	—	Case II*	$T'_c=0$
III-1a	$I_{a,c}<0$	Case I*	$T'_{a,c}=T_{a,c}-T_{min}$
	—	Case II*	$T'_b=T_s$
III-1b	$I_c>0$	Case I	$T'_a=0$
	—	Case II*	$T'_{b,c}=T_{b,c}+T_{min}$
IV-1b	$I_a<0$	Case I*	$T'_{a,b}=T_{a,b}-T_{min}$
	—	Case II*	$T_c'=T_s$
V-1a	$I_b<0$	Case I* Case II	$T'_{a,b}=T_{a,b}-T_{min}$ $T'_c=T_s$
VI-1a	$I_c>0$	Case I Case II	$T'_{a,c}=T_{a,c}+T_{min}$ $T'_b=0$
VI-1b	$I_{b,c}<0$	Case I*	$T'_a=T_s$
	$I_c<0$	Case II	$T'_{b,c}=T_{b,c}-T_{min}$

in sectors I and VI, such as [POO], are unreachable if I_b or I_c is positive.

To illustrate the general time action, Fig. 7(a) shows the change of switching sequence while $V_{\rm ref}$ is in region 1b of sector I with T_{a1} and T_{b1} OC faults. When $I_b > 0$, [POO] can be changed to [ONN]. In order to minimize the number of switch actions, [OON] and [NNN] are adopted to replace [PPO] and [OOO]. The dwell times of equivalent switching states are

$$\begin{cases} T'_{[\rm OON]} = T_{[\rm OON]} + T_{[\rm PPO]} = 2T_b \\ T'_{[\rm ONN]} = T_{[\rm POO]} = T_a - T_b \\ T'_{[\rm NNN]} = T_{[\rm OOO]} = T_c - T_a. \end{cases} \tag{1}$$

The new turn-ON times for each phase can be obtained by adding the minimum turn-ON times $T_{\rm min}$

$$\begin{cases} T'_a = T_a + T_{\rm min} = T_a + T_b \\ T'_b = T_b + T_{\rm min} = 2T_b \\ T'_c = 0. \end{cases} \tag{2}$$

In Fig. 7(a), there is no state [P] in the rearranged switching sequence. Hence, the arrangement is effective in any single or multiple upper half-bridge switch OC fault cases.

After arrangement, dc bias results, since only [N] switching states are implemented and I_c cannot flow through the NP. To obviate dc deviation, [N] switching states should be replaced with equivalent [P] switching states in opposite regions (region 1b of sector IV) to complement $I_{\rm np}$. The average of $I_{\rm np}$ over a fundamental period can be driven to zero.

Rearranged switching sequences in region 1b of sector IV are shown in Fig. 7(b). By employing [P] switching states in place of [N] switching states, turn-ON times in each switching cycle (T_s) are redefined by subtracting $T_{\rm min}$

$$\begin{cases} T'_a = T_a - T_{\rm min} = T_a - T_c \\ T'_b = T_b - T_{\rm min} = T_b - T_c \\ T'_c = T_s. \end{cases} \tag{3}$$

Table III lists redefined turn-ON times for two fault cases. The asterisks show cases with rearranged switching sequences to balance the NP voltage.

B. High Modulation Index

At high modulation index, low-, medium-, and high-voltage vectors are employed in the switching sequences. Considering there are no equivalent switching states in medium-voltage vectors, a virtual vector is established instead of unreachable medium-voltage vectors. To avoid output distortion caused by a change in line-to-line voltages, the duty ratios of half-bridge switches should remain the same to ensure that the average of pole voltages is unchanged over each switching cycle. Taking the region 2b of sector I in Fig. 8 for instance, the duty ratio is

$$\begin{cases} d_{a,b(+)} = \frac{T_{[P]}}{T_s} = \frac{T_{a,b}}{T_s} \\ d_{c(-)} = -\frac{T_{[N]}}{T_s} = -\frac{T_s - T_c}{T_s}. \end{cases} \tag{4}$$

Here, $d_{x(+)}$ refers to the duty ratio of state [P], and $d_{x(-)}$ refers to the duty ratio of state [N]. $T_{[\mathrm{P}]}$ and $T_{[\mathrm{N}]}$ refer to the duration of states [P] and [N] during a switching cycle.

1) Case I. OC Faults in T_{a1} and T_{b1}: To tolerate T_{a1} and T_{b1} OC faults, T_{r1} is turned ON. Both low- and medium-voltage vectors that contain state [O] should be considered. Except for [POO] and [OPO], mentioned for low modulation index, medium-voltage vectors [PON], [OPN], [NPO], and [PNO] become unreachable if I_{np} is positive. When V_{ref} is in sector I and $I_b > 0$, state loss occurs in phase B, and switching states [PON] and [POO] become unreachable. [POO] can be replaced with [ONN], but no available vectors can replace medium-voltage vector [PON]. To avoid output distortion due to the loss of [PON], a new virtual vector is defined as

$$\begin{cases} \boldsymbol{V}_{SI-2(I)} = k_{I1}\boldsymbol{V}_{[\mathrm{PPN}]} + k_{I2}\boldsymbol{V}_{[\mathrm{PNN}]} \\ \qquad\qquad + k_{I3}\boldsymbol{V}_{[\mathrm{PPO}]} + k_{I4}\boldsymbol{V}_{[\mathrm{ONN}]} \\ k_{I1} + k_{I2} + k_{I3} + k_{I4} = 1. \end{cases} \tag{5}$$

Here, $k_{I1} \sim k_{I4}$ are weighting coefficients ($-1 \le k \le 1$), $\boldsymbol{V}_{SI-2(I)}$ refers to the virtual vector in region 2 of sector I for case I. $\boldsymbol{V}_{\mathrm{ref}}$ in region 1b of sector I can be represented utilizing $\boldsymbol{V}_{SI-2(I)}$

$$\begin{aligned} \boldsymbol{V}_{\mathrm{ref}} T_s = {} & \boldsymbol{V}_{[\mathrm{PPO}]}(T_{[\mathrm{PPO}]} + T_{[\mathrm{OON}]}) + \boldsymbol{V}_{[\mathrm{ONN}]} T_{[\mathrm{POO}]} \\ & + \boldsymbol{V}_{SI-2(I)} T_{[\mathrm{PON}]}. \end{aligned} \tag{6}$$

In order to minimize the number of switch actions, equivalent switching state [PPO] can substitute for [OON]. The new switching sequence is ONN—PNN—PPN—PPO— PPN—PNN—ONN, where the dwell times can be derived as

$$\begin{cases} T'_{[\mathrm{PPO}]} = T_{[\mathrm{PPO}]} + T_{[\mathrm{OON}]} + k_{I3} T_{[\mathrm{PON}]} = 2T_b + k_{I3}(T_a - T_c) \\ T'_{[\mathrm{ONN}]} = T_{[\mathrm{POO}]} + k_{I4} T_{[\mathrm{PON}]} = T_c - T_b + k_{I4}(T_a - T_c) \\ T_{[\mathrm{PPN}]} = k_{I1} T_{[\mathrm{PON}]} = k_{I1}(T_a - T_c) \\ T_{[\mathrm{PNN}]} = k_{I2} T_{[\mathrm{PON}]} = k_{I2}(T_a - T_c). \end{cases} \tag{7}$$

In Fig. 8, state [O] is reachable in phases A and C after arrangement, but not in phase B. Since the duty ratios in each phase remain the same, $k_{I1} \sim k_{I4}$ can be obtained from

$$\begin{cases} d_{a(+)} = d'_{a(+)} = \frac{T_a}{T_s} = \frac{T'_a}{T_s} \\ d_{b(+)} = d'_{b(+)} + d'_{b(-)} = \frac{T_b}{T_s} = \frac{T'_b}{T_s} - \frac{T_s - T'_b}{T_s} \\ d_{c(-)} = d'_{c(-)} = -\frac{T_s - T_c}{T_s} = -\frac{T_s - T'_c}{T_s} \end{cases} \tag{8}$$

$$\begin{cases} k_{I1} = \frac{0.5T_a + T_b - T_c}{T_a - T_c} \\ k_{I2} = \frac{0.5T_a - T_b}{T_a - T_c} \\ k_{I3} = -k_{I4} = \frac{T_c - 2T_b}{T_a - T_c}. \end{cases} \tag{9}$$

Based on (7)∼(9), the redefined turn-ON times can be expressed as

$$\begin{cases} T'_{a,c} = T_{a,c} \\ T'_b = 0.5T_b + 0.5T_s. \end{cases} \tag{10}$$

In addition, $\boldsymbol{V}_{SI-2(I)}$ can be used to balance the NP voltage since coefficients k_{I3} and k_{I4} are opposite, as explained in the following.

It is worth mentioning that if current is reversed relative to the output pole voltage, such as $I_c > 0$, low-voltage vectors ([PPO] and [POO]) in this region become unreachable since I_c is positive and T_{r1} is turned ON. Thus, phases A and C cannot connect to the NP. [PPP] is used in the rearranged switching sequence to replace [PPO]. The switching sequence ONN—PNN—PPN—PPO—PPN—PNN—ONN will be changed to ONN—PNN—PPN—PPP—PPN—PNN—ONN. Both phases A and C are modulated for two-level operation, and the output voltage levels are reduced. This case is not described here in detail.

If V_{ref} is in region 4 of sector I or region 3 of sector II, phases A and B operate during states [P] and [O]. If I_a and I_b are positive, state loss occurs in phases A and B since T_{r1} is ON and state [O+] is unreachable.

When V_{ref} is in region 4 of sector I, [NNN] is used in the switching sequence to replace [OON]. Virtual vector $\boldsymbol{V}_{SI-4(I)}$ consisting of [PPN], [PNN], [PPO], and [NNN] is used instead of unreachable vector [PON]. The switching sequence OON—PON—PPN—PPO—PPN—PON—OON is rearranged to NNN—PNN—PPN—PPO—PPN—PNN—NNN. Weighting coefficients in the synthesized virtual vector are given as

$$\begin{aligned} \boldsymbol{V}_{SI-4(I)} = {} & k_{I1}\boldsymbol{V}_{[\mathrm{PPN}]} + k_{I2}\boldsymbol{V}_{[\mathrm{PNN}]} \\ & + k_{I3}\boldsymbol{V}_{[\mathrm{PPO}]} + k_{I5}\boldsymbol{V}_{[\mathrm{NNN}]} \end{aligned} \tag{11}$$

$$\begin{cases} k_{I1} = \frac{T_a - T_b + T_c}{2(T_a - T_b)} \\ k_{I2} = \frac{1}{2} \\ k_{I3} = -2k_{15} = \frac{T_c}{T_b - T_a}. \end{cases} \tag{12}$$

The turn-ON times for rearrangement are

$$\begin{cases} T'_{a,b} = 0.5T_{a,b} + T_s \\ T'_c = T_c. \end{cases} \tag{13}$$

2) Case II. OC Faults in T_{a1} and T_{b4}: If OC faults occur in T_{a1} and T_{b4} simultaneously, medium-voltage vectors [PON], [ONP], and [PNO] become invalid in addition to low-voltage vectors from the low-index cases. Taking sector VI as an example, if phase A operates during state [P] and phase B operates during state [N], phase C cannot operate during state [O] since T_{r1} and T_{r2} are turned ON.

Fig. 9 shows the switching sequence in region 2b of sector VI. Vectors [ONO] and [PNO] are unreachable. Equivalent replacement of [ONO] can be achieved by employing [POP], and a suitable virtual vector $\boldsymbol{V}_{\mathrm{SV}I-2(II)}$ is used to replace [PNO]

$$\begin{aligned} \boldsymbol{V}_{SVI-2(II)} = {} & k_{VI1}\boldsymbol{V}_{[\mathrm{PNP}]} + k_{VI2}\boldsymbol{V}_{[\mathrm{PNN}]} \\ & + k_{VI3}\boldsymbol{V}_{[\mathrm{POP}]} + k_{VI4}\boldsymbol{V}_{[\mathrm{ONN}]}. \end{aligned} \tag{14}$$

To minimize the number of switch actions, [ONN] replaces [POO]. After rearrangement, phase C operates during states [P] and [N] instead of states [O] and [N]. Thus, the duty ratio of

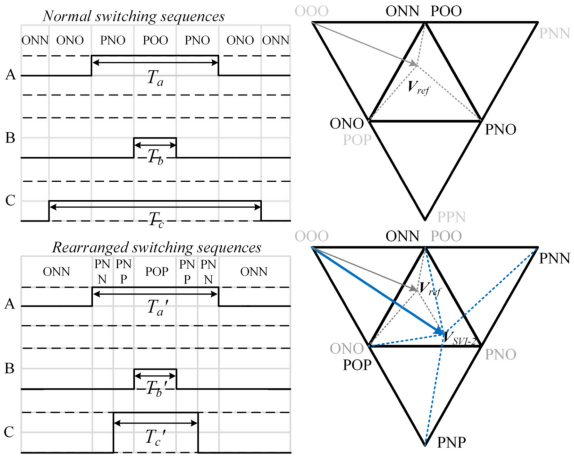

Fig. 9. Arrangement of switching sequence to tolerate T_{a1} and T_{b4} OC faults in region 2b of sector VI.

phase C should remain the same

$$d_{c(-)} = d'_{c(+)} + d'_{c(-)} = -\frac{T_s - T_c}{T_s} = \frac{T'_c}{T_s} - \frac{T_s - T'_c}{T_s}. \quad (15)$$

The redefined turn-ON times can be calculated based on (16)

$$\begin{cases} T'_{[\mathrm{POP}]} = T_{[\mathrm{ONO}]} + k_{VI3} T_{[\mathrm{PNO}]} = T_b \\ T'_{[\mathrm{ONN}]} = T_{[\mathrm{ONN}]} + T_{[\mathrm{POO}]} + k_{VI4} T_{[\mathrm{PNO}]} = T_c + T_b - T_a \\ T_{[\mathrm{PNP}]} = k_{VI1} T_{[\mathrm{PNO}]} = 0.5T_c - T_b \\ T_{[\mathrm{PNN}]} = k_{VI2} T_{[\mathrm{PNO}]} = T_a - 0.5T_c \end{cases} \quad (16)$$

$$\begin{cases} T'_{a,b} = T_{a,b} \\ T'_c = 0.5T_c. \end{cases} \quad (17)$$

At high modulation index, redefined turn-ON times for two cases are listed in Table IV. Based on current directions and states of fault phases, virtual vectors are established to replace unreachable vectors. After rearrangement, phases, except for state-loss phases, can output three-level voltages. However, the NP voltage will be unbalanced due to the loss of medium-voltage vectors, and a method is needed to restore balance.

C. NP Voltage Modulation for Balancing

Taking T_{a1} and T_{b1} OC faults as an instance, there is potential dc deviation in the NP voltage since [PON] is unreachable and i_{np} is not equal to 0 over a switching cycle. If V_{ref} is in region 2b of sector I, and V_{C1} is larger than V_{C2}, k_{I3} can be increased and k_{I4} is decreased to change the dwell times of [PPO] and [ONN] during fault-tolerant operation when $I_a > 0$ and $I_c < 0$.

In [29], an offset time Δt was obtained to minimize NP voltage oscillations and balance the NP voltage under normal conditions. However, in rearranged switching sequences, only low-voltage vectors will cause current to flow through the NP, and their effect on NP voltage deviation cannot be counteracted. Thus, the magnitude of NP voltage deviations ($\Delta V_C = V_{C1} - V_{C2}$) caused by [PPO] and [ONN] should be made equal using Δt,

TABLE IV
RECONFIGURED TURN-ON TIMES AT HIGH MODULATION INDEX

Sector and region	Current	Fault cases	Redefined T_{on}
I-2a I-3	$I_b>0$	Case I Case II	$T'_{a,c}=T_{a,c}$ $T'_b=0.5T_b$
I-2b	$I_b>0$	Case I Case II	$T'_{a,c}=T_{a,c}$ $T'_b=0.5T_b+0.5T_s$
I-4	$I_b>0$	Case II	$T'_{a,c}=T_{a,c}$ $T'_b=0.5T_b+0.5T_s$
	$I_b>0$	Case I	$T'_{a,b}=0.5T_{a,b}+0.5T_s$ $T'_c=T_c$
II-2a	$I_a>0$	Case I	$T'_a=0.5T_a$ $T'_{b,c}=T_{b,c}$
II-3	$I_a>0$	Case I	$T'_{a,b}=0.5T_{a,b}+0.5T_s$ $T'_c=T_c$
II-2b II-4	$I_a>0$	Case I	$T'_a=0.5T_a+0.5T_s$ $T'_{b,c}=T_{b,c}$
III-2a III-3	$I_c>0$	Case I	$T'_{a,b}=T_{a,b}$ $T'_c=0.5T_c$
III-2b III-4	$I_c>0$	Case I	$T'_{a,b}=T_{a,b}$ $T'_c=0.5T_c+0.5T_s$
V-2a V-3	$I_a<0$	Case II	$T'_a=0.5T_a$ $T'_{b,c}=T_{b,c}$
V-2b V-4	$I_a<0$	Case II	$T'_a=0.5T_a+0.5T_s$ $T'_{b,c}=T_{b,c}$
VI-2a	$I_c>0$	Case I	$T'_{a,b}=T_{a,b}$
VI-3	—	Case II	$T'_c=0.5T_c+0.5T_s$
VI-2b	$I_c>0$	Case I	$T'_{a,b}=T_{a,b}$
VI-4	—	Case II	$T'_c=0.5T_c$

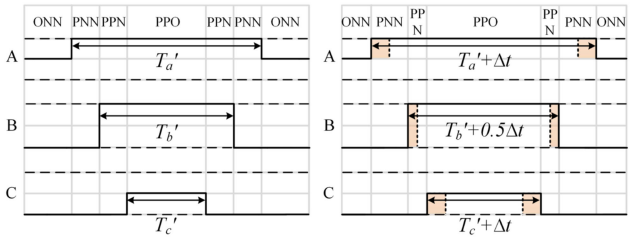

Fig. 10. Tolerant switching sequence in region I-2b before adding Δt and after adding Δt.

and

$$\Delta V_C = -\frac{1}{C}(T'_{[\mathrm{PPO}]} + \Delta t) I_c = \frac{1}{C}(T'_{[\mathrm{ONN}]} - \Delta t) I_a \quad (18)$$

where C is the dc-link capacitor value.

In (18), Δt adjusts the durations of [PPO] and [ONN]. The dwell times of phases A and B in state [P] increase, and the dwell time of phase C in state [N] decreases, as shown in Fig. 10. Based on duty ratios, redefined turn-ON times (T_a^*, T_b^*, T_c^*) can be obtained as

$$\begin{cases} T_a^* = (d'_{a(+)} + \frac{\Delta t}{T_s}) T_s = T'_a + \Delta t \\ T_b^* = \frac{1}{2}[(d'_{b(+)} + \frac{\Delta t}{T_s}) + (1 + d'_{b(-)})] T_s = T'_b + \frac{1}{2}\Delta t \\ T_c^* = (1 + d'_{c(-)} + \frac{\Delta t}{T_s}) T_s = T'_c + \Delta t. \end{cases} \quad (19)$$

TABLE V
OFFSET TIME ADDED TO REDEFINED TURN-ON TIMES

Sector and region	Offset time Δt
I-2,3	$[(T_s - T'_a)I_a + T'_cI_c] / (I_a - I_c)$
II-2,4	$[(T_s - T'_b)I_b + T'_cI_c] / (I_b - I_c)$
I-4, II-3	$-T'_c$
III-2,3,4	$[(T_s - T'_b)I_b + T'_aI_a] / (I_b - I_a)$
VI-2,3,4	$[(T_s - T'_a)I_a + T'_bI_b] / (I_a - I_b)$

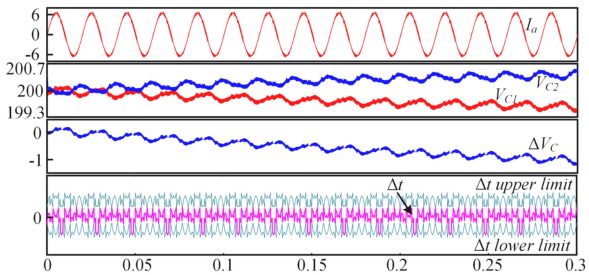

Fig. 11. Simulation results of ΔV_C by using Δt modulation in case of T_{a1} and T_{b1} faults.

Since turn-ON times have changed, virtual vector $\boldsymbol{V}_{SI-2(I)}$ should be reconstructed using bias coefficient Δk ($\Delta k = \Delta t/T_{[\mathrm{PON}]}$)

$$\boldsymbol{V}_{SI-2(I)} = (k_{I1} - 0.5\Delta k)\boldsymbol{V}_{[\mathrm{PPN}]} + (k_{I2} + 0.5\Delta k)\boldsymbol{V}_{[\mathrm{PNN}]} + (k_{I3} + \Delta k)\boldsymbol{V}_{[\mathrm{PPO}]} + (k_{I4} - \Delta k)\boldsymbol{V}_{[\mathrm{ONN}]}. \tag{20}$$

At low modulation index, Δt is not considered since only [P] or [N] switching states of low-voltage vectors are adopted in the switching sequences. Voltage balance at the NP can be achieved by replacement with equivalent switching states.

In accordance with Table IV, the values of Δt are shown in Table V, which should satisfy

$$-T_{\min} < \Delta t \le T_s - T_{\max} \tag{21}$$

to avoid output distortion. However, under multiple OC faults, more vectors that include state [O+] become unreachable in asymmetric regions. As shown in Fig. 11, deviation appears in every fundamental period during fault-tolerant operation due to the lower limit on Δt. To further improve NP voltage balance, a deviation compensation method can be applied.

In Fig. 11, due to the lower limit on Δt, V_{C2} increases and V_{C1} decreases as voltage deviation accumulates. To obviate the dc bias, the accumulated voltage deviation $\Delta V'_C$ should be considered when calculating the offset time Δt. In accordance with (18), Δt is changed by adding a time adjustment factor ε

$$[T'_{[\mathrm{PPO}]} + (1+\varepsilon)\Delta t]I_c + [T'_{[\mathrm{ONN}]} - (1+\varepsilon)\Delta t]I_a = -C\Delta V'_C. \tag{22}$$

The redefined offset time $\Delta t'$ is given by

$$\Delta t' = (1+\varepsilon)\Delta t \tag{23}$$

$$\varepsilon = \frac{C\Delta V'_c}{(I_a - I_c)\Delta t}. \tag{24}$$

TABLE VI
OFFSET TIME BY ADDING A TIME ADJUSTMENT FACTOR

Sector and region	$(1+\varepsilon)\Delta t$
I-2,3	$[C\Delta V'_C + (T_s - T'_a)I_a + T'_cI_c] / (I_a - I_c)$
II-2,4	$[C\Delta V'_C + (T_s - T'_b)I_b + T'_cI_c] / (I_b - I_c)$
I-4, II-3	$[C\Delta V'_C + T'_cI_c] / (-I_c)$
III-2,3,4	$[C\Delta V'_C + (T_s - T'_b)I_b + T'_aI_a] / (I_b - I_a)$
VI-2,3,4	$[C\Delta V'_C + (T_s - T'_a)I_a + T'_bI_b] / (I_a - I_b)$

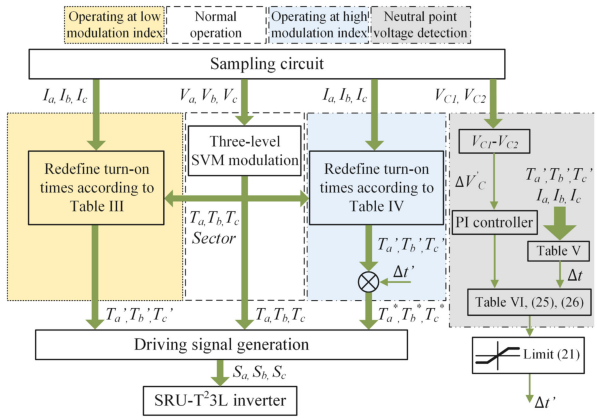

Fig. 12. Block diagram of the proposed fault-tolerant strategy.

In region 2 of sector I, if $I_a > 0 > I_c$, the redefined offset time $\Delta t'$ can be expressed as

$$\Delta t' = \begin{cases} (1+\varepsilon)\Delta t & (\Delta V'_c > 0, \Delta t > 0) \\ T_s - T_{\max} & (\Delta V'_c > 0, \Delta t < 0) \\ -T_{\min} & (\Delta V'_c < 0, \Delta t > 0) \\ (1+\varepsilon)\Delta t & (\Delta V'_c < 0, \Delta t < 0). \end{cases} \tag{25}$$

In (25), $\Delta t'$ should be positive to increase the duration of state [O−] when $\Delta V'_C > 0$. However, if $\Delta t < 0$, it is difficult to determine whether $\Delta t'$ is positive or negative in accordance with (23). To avoid further increase of voltage deviation, $\Delta t'$ should be set to the upper limit (T_s–$T_{\max}$). Similarly, when $\Delta V'_C < 0$ and $\Delta t > 0$, $\Delta t'$ should be set to the lower limit (–$T_{\min}$). If $I_c < I_a < 0$, $\Delta t'$ can be rewritten as

$$\Delta t' = \begin{cases} -T_{\min} & (\Delta V'_c > 0, \Delta t > 0) \\ (1+\varepsilon)\Delta t & (\Delta V'_c > 0, \Delta t < 0) \\ (1+\varepsilon)\Delta t & (\Delta V'_c < 0, \Delta t > 0) \\ T_s - T_{\max} & (\Delta V'_c < 0, \Delta t < 0). \end{cases} \tag{26}$$

It should be noted that if both I_a and I_c are negative, I_{np} always flows into the NP during [PPO] and [ONN]. When $\Delta V'_C < 0$, $\Delta t'$ can only restrain further deterioration of NP imbalance. In this case, the circuit should revert to two-level operation.

Adjustments in all sectors are listed in Table VI. A block diagram of the fault-tolerant strategy for cases I and II is given in Fig. 12. Based on (25) and (26), $\Delta t'$ for other sectors can be obtained by comparing phase currents and calculating $\Delta V'_C$ and Δt.

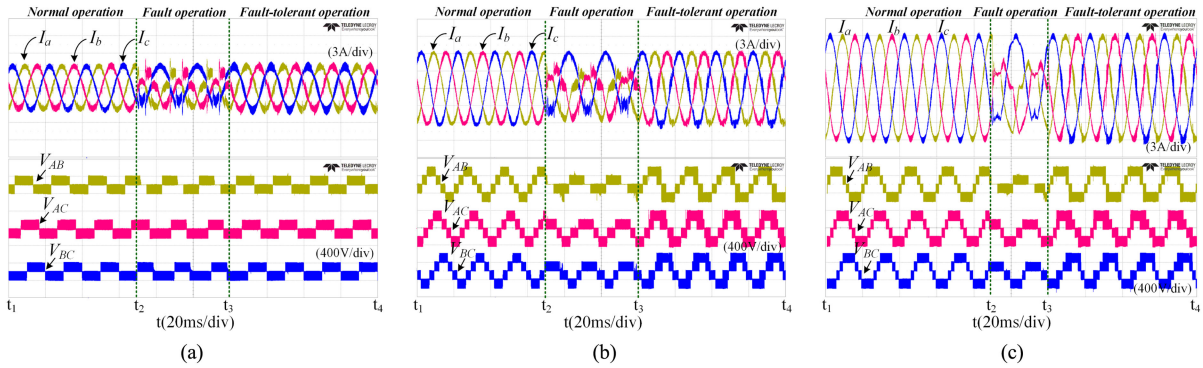

Fig. 13. Phase currents (I_a, I_b, I_c) and line-to-line voltages (V_{AB}, V_{AC}, V_{BC}) during normal operation, T_{a1} and T_{b1} OC fault operation, and fault-tolerant operation ($pf = 1$) when (a) $m = 0.5$, (b) $m = 0.8$, and (c) $m = 1.15$.

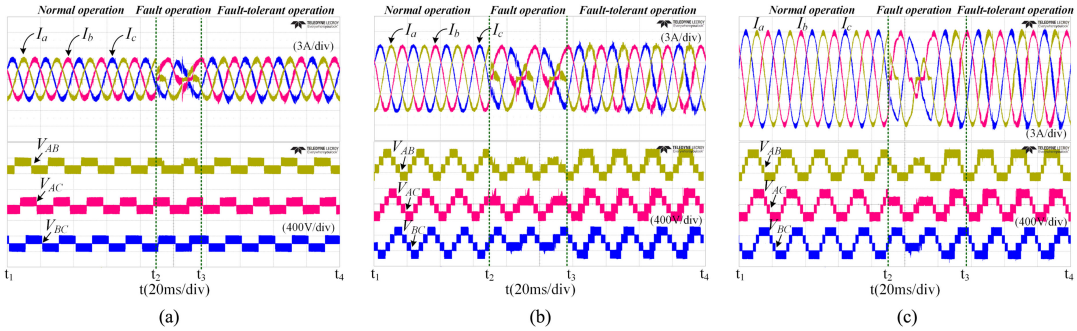

Fig. 14. Phase currents (I_a, I_b, I_c) and line-to-line voltages (V_{AB}, V_{AC}, V_{BC}) during normal operation, T_{a1} and T_{b4} OC fault operation, and fault-tolerant operation ($pf = 1$) when (a) $m = 0.5$, (b) $m = 0.8$, and (c) $m = 1.15$.

TABLE VII
SPECIFICATIONS OF THE EXPERIMENTAL PLATFORM

Parameters	Symbols	Values
Input dc link voltage	V_{dc}	400 V
Filter inductances	L_a, L_b, L_c	4 mH
Filter capacitors	C_a, C_b, C_c	4.7 μF
Switching frequency	f_s	10 kHz
Rated output frequency	f	50 Hz
Load resistances	R_a, R_b, R_c	25 Ω

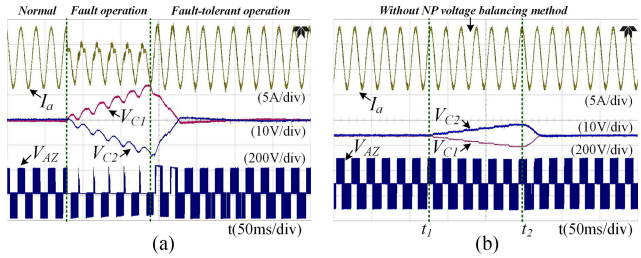

Fig. 15. Response of NP voltage when faults occur in T_{a1} and T_{b1} ($m = 0.8$, $pf = 1$): (a) when faults occur; and (b) during fault-tolerant operation.

IV. EXPERIMENTAL RESULTS

To verify the operating performance of the proposed method, experiments have been performed using an inverter with specifications given in Table VII. The control employs a TMS320F28335 processor. OC faults in IGBTs are simulated by disabling the corresponding gate drive signals. The experimental results for fault cases mentioned in Section III are presented in this section. Although fault diagnosis is beyond the scope of this article, it should be considered to provide effective information for redundant operation. Multiple IGBT OC faults in the proposed T-type inverter can be detected and located with the fast diagnosis method proposed in [30], and fault tolerant strategies can be applied based on corresponding diagnosis results.

Fig. 13 shows three-phase currents (I_a, I_b, I_c) and line-to-line voltages (V_{AB}, V_{AC}, V_{BC}) during normal operation, T_{a1} and T_{b1} faults, and fault-tolerant operation. Line-to-line voltages show three levels at low modulation index ($m = 0.5$) and five levels at high modulation index ($m = 0.8$ and 1.15) under normal conditions. When T_{a1} and T_{b1} fail, missing state [P] will distort the phase currents I_a and I_b. During fault-tolerant operation, line-to-line voltages show three levels by applying equivalent switching states ($m = 0.5$). If modulation index $m = 0.8$ and 1.15, line-to-line voltages are asymmetrical since two-level modulation appears in sectors I, II, III, and VI, which is consistent with the analysis in Section III.

Fig. 14 shows experimental results for T_{a1} and T_{b4} OC faults. When faults occur, phases A and B cannot operate during respective positive and negative half cycles of output currents. By implementing the proposed extended state and virtual vector

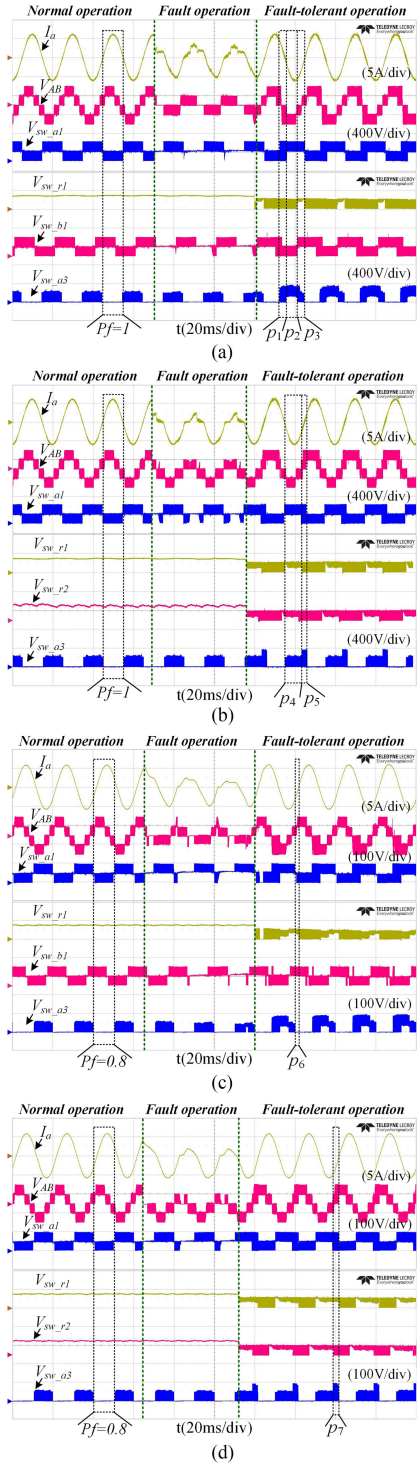

Fig. 16. Blocking voltages during normal, fault, and fault-tolerant operation ($m = 0.8$). (a) T_{a1} and T_{b1} faults, $pf = 1$. (b) T_{a1} and T_{b4} faults, $pf = 1$. (c) T_{a1} and T_{b1} faults, $pf = 0.8$. (d) T_{a1} and T_{b4} faults, $pf = 0.8$.

methods, output distortion is eliminated. In Fig. 14(a), three-level line-to-line voltages are recovered during fault-tolerant operation at low modulation index. Fig. 14(b) and (c) shows post-fault performance with the fault-tolerant strategy at high modulation index. Compared to normal operation, line-to-line voltages are asymmetrical since three phases operate with two- and three-level modulations simultaneously. This verifies the performance of proposed method.

TABLE VIII
CURRENT THD IN DIFFERENT SCENARIOS (pf = 1)

OC faults scenario		m=0.5	m=0.8	m=1.15
Normal	Three-level operation	1.77%	1.38%	0.86%
T_{a1} & T_{b1}	Proposed method	3.31%	1.97%	1.29%
	Tolerant two-level operation	3.71%	2.49%	1.85%
T_{a1} & T_{b4}	Proposed method	3.24%	1.59%	1.04%
	Tolerant two-level operation	3.59%	2.37%	1.76%

Experimental results in Fig. 15 show that the method can maintain NP voltage balance. In Fig. 15(a), the NP voltage is balanced under normal conditions. When T_{a1} and T_{b1} fail simultaneously, V_{C1} increases and V_{C2} decreases since state [P] is missing. After applying the fault-tolerant strategy, output distortion can be eliminated and the capacitor voltages converge. In Fig. 15(b), the circuit operates during fault-tolerant operation and the NP voltage is balanced. At t_1, the balancing control is removed and voltage deviation begins to grow. At t_2, the balancing control method is restored and capacitor voltages converge. It can be seen that the proposed balancing method can suppress dc bias in the NP voltage.

Experimental results in terms of the voltage across power devices based on *pf* and *m* are shown in Fig. 16. Under normal conditions, the T^{2}3L inverter outputs three-level voltages. The voltages across half-bridge switches ($V_{\mathrm{sw_}a1}$ and $V_{\mathrm{sw\_}b1}$) and middle switch ($V_{\mathrm{sw\_}a3}$) are V_{dc} and $0.5V_{\mathrm{dc}}$, respectively. $V_{\mathrm{sw\_}a1}$ and $V_{\mathrm{sw\_}b1}$ represent the variation of V_{AZ} and V_{BZ}, considering that the dc-link voltage is constant. In Fig. 16(a), phase A is modulated for two-level operation, and $I_a > 0$, during period p_1. When T_{r1} is switched ON and T_{a3} connects to the dc bus, the voltage across T_{r1} ($V_{\mathrm{sw\_}r1}$) reduces to 0, and $V_{\mathrm{sw\_}a3}$ changes to V_{dc}. During p_2, I_a is negative, and phase B operates during the positive half cycle. Thus, $V_{\mathrm{sw\_}a3}$ becomes $0.5V_{\mathrm{dc}}$ or V_{dc} when phase A is in states [O−] or [N], since T_{r1} is still ON. During p_3, phases A and B revert to three-level operation, and the blocking voltage of T_{a3} reduces to $0.5V_{\mathrm{dc}}$. In Fig. 16(b), $V_{\mathrm{sw\_}a3}$ is still $0.5V_{\mathrm{dc}}$ during p_4, and $V_{\mathrm{sw\_}a3}$ increases to V_{dc} when phase A is modulated for two-level operation during p_5. In Fig. 16(c) and (d), the load is changed to 10 mH and 6 Ω ($m = 0.8$, $pf = 0.8$). During p_6, the operating state of phase A is [P] or [O] and $I_a < 0$. $V_{\mathrm{sw\_}a1}$ is 0 when current flows through D_{a1} and T_{r1} is not involved in the operation. During p_7, V_{AZ} has two levels, and $I_a < 0$. The negative current path will form through D_{a1} instead of T_{r1}, based on the values of $V_{\mathrm{sw\_}a1}$ and $V_{\mathrm{sw\_}r1}$. These results are consistent with the analysis in Section II.

Table VIII lists the measured phase current THD for various operating scenarios, given resistive loads. The THD values with the proposed method increase compared to normal three-level operation, but are less than those during two-level fault-tolerant operation, due to two- and three-level combined modulation. Cases with multiple upper half-bridge switch faults contribute to a higher THD value, since two-level modulation is implemented in more regions.

V. Conclusion

This article proposes a fault-tolerant control strategy for a $T^2$3L inverter with a shared redundant unit to handle OC faults in multiple half-bridge switches. Since the added unit is shared among all three phases, the few additional power devices can make the circuit more reliable. In prior work, fault-tolerant operation reverts to two-level modulation. To improve post-fault operation performance, an extended switch state method has been used to replace unreachable switching states at low modulation index. At high modulation index, an improved virtual voltage vector method is adopted, and output distortion is eliminated by using virtual vectors instead of unreachable medium-voltage vectors. After rearrangement, the duty ratios of states [P] and [N] in the switching sequences remain the same to ensure that the moving average two-level and three-level output voltages are unchanged. An offset time is added to turn-ON times to balance the NP voltage by adjusting the duration of virtual vectors and calculating the magnitude of capacitor voltages. Under fault-tolerant conditions, full output power capacity is supported, and three-level operation can be recovered although two-level modulation is required during some portions of each fundamental cycle. Even though phase current THD becomes higher owing to the shift to partial two-level modulation, the proposed method can improve operating performance compared to two-level fault-tolerant operation.

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