Reconfigurable Nonisolated DC–DC Converter With Fault-Tolerant Capability

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***Abstract*—Malfunction of power semiconductor switches is the dominant cause of failure in power electronic converters. This article proposes a novel dual-switch dc–dc topology for high-reliability applications. The proposed converter is fault tolerant and supports operation under both step-down and step-up modes. The proposed topology can be reconfigured automatically under various switch-fault conditions in order to maintain normal operation. This is enabled by an affine-parametrization-based control design, which minimizes the transient impact of the faults. The reliability performance of the proposed converter is evaluated theoretically using a Markov model, demonstrating its superiority over conventional topologies. Finally, a laboratory prototype is developed and tested to verify the proposed design and control performance under switch faults.**

***Index Terms*—DC/DC converters, fault tolerance, reliability evaluation, seamless reconfiguration, switch fault.**

I. Introduction

RELIABILITY of power electronic converters is one of the highest importance in mission-critical applications such as aerospace devices, medical equipment, electric vehicles, and distributed generation units [1]–[4]. Therefore, it becomes essential to incorporate fault-tolerant (FT) techniques in the design stage and eventually improve system resilience against unpredictable failures [5]–[8]. The demand for dc–dc conversion—both step-up and step-down—has been increasing in the recent past due to its use in photovoltaic generation, battery systems, and dc-based loads for instance [9], [10]. Therefore, in this article, we focus on increasing the reliability of dc–dc converters using a FT design.

An FT scheme generally entails two stages: fault detection (FD), and remedial action. The former identifies and isolates the existence of a fault, while the latter reconfigures the converter to ensure service continuity. The ideal FT solution should be cost-effective and minimal additional power losses. Studies in the past have shown that the malfunction of power semiconductors is the main cause of converter faults [11], [12]. A sudden malfunction of the power switches can trigger a catastrophic and unrecoverable system failure [7], [13]–[15].

Hardware redundancy is an effective way to improve the reliability of converters by avoiding disruptions arising from a single-point failure for the instance of a switch fault [16], [17]. Various approaches have been proposed in the past addressing this issue [6], [7], [13]–[15]. A number of classical converter topologies with an FT design have been proposed, such as those with $N + M$, $2N$, and $3N$ redundancies [5], [18]–[20]. Here, the variable N denotes the minimum number of working converter modules (either in parallel or cascaded form), and M is the required number of backup devices associated with each converter module. Jamshidpoure *et al.* [5] proposed a redundant switch in-series with a triode for alternating current (TRIAC), which is in-parallel with the active switch to provide redundancy for a conventional boost converter. This allows the converter to reconfigure by creating an alternative current path when the main switch experiences either a short-circuit fault (SCF) or an open-circuit fault (OCF). Similarly, FT in a multilevel boost converter can be achieved using a controlled TRIAC as proposed in [4]. For high step-up gain applications involving a cascaded-level quasi boost converter, the FT design can be achieved using a complex and costly structure, as proposed in [19]. In this study, a $3N + 9$ redundancy is formed by three cascaded converters along with nine additional relays in order to bypass switch failures. Furthermore, a cascaded buck and buck-boost converter using two synchronous switches has also been proposed for step-down applications in [8]. The presented FT design consists of one redundant switch, which provides an alternative path when either one of the synchronous switches fails. Another study in [20] presents a dc–dc converter combining a number of resonant switched-capacitor cells to form a voltage multiplier circuit. This topology enables the selection of a variable output voltage gain along with the FT feature. If one of the active cells fail, the faulty switch is bypassed, and the converter reconfigures to retain the desired voltage regulation. Furthermore, FT design has been applied in four-leg interleaved dc–dc converters [21]–[23]. In this context, FT operation is achieved by modifying the multiphase pulsewidth modulation (PWM) control technique based on an OCF detection algorithm. Hence, the interleaved

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converter is able to maintain service continuity and ensure low current ripples when one of the switch-legs fail, albeit at the cost of a higher number of components.

The focus of this article is to address the weakness of a single-switch failure in conventional dc–dc converters. This is achieved through modification of the buck topology by utilizing a single redundant switch, which is both cost effective and achieves high reliability. It extends the work in [24] to demonstrate the superior lifetime and reliability as compared to conventional dc–dc converters. In addition, an advanced control technique based on affine parameterization is proposed to systematically tune the feedback controller to improve the speed of postfault reconfiguration and minimize overshoots. As a result, a seamless and smooth reconfiguration can be attained. A laboratory prototype of the proposed converter has been constructed, and experimental results highlighting the effectiveness of the proposed topology design as well as the control technique are subsequently presented. Finally, a Markov chain approach is used to assess the reliability of the proposed FT converter when compared to other conventional converters. Theoretical and numerical analyses show that the proposed FT converter has a longer operational lifespan than the conventional designs.

This article is organized as follows. In Section II, the design and operation principles of the proposed FT converter under step-down and step-up modes are presented. Section III presents the theoretical Markov model-based procedure used for assessing the reliability of the proposed FT converter and the conventional converter. Section IV presents the numerical evaluation of the converters' reliabilities. Section V presents the affine parameterization technique for tuning the control of the proposed FT converter. Section VI illustrates the effectiveness of the proposed FT converter using experimental results under various fault conditions, and finally, Section VII concludes this article.

II. Operational Principles of the Proposed FT Converter

The proposed FT topology is derived from the conventional buck converter illustrated in Fig. 1(a). The proposed design shifts the inductor L_1 to the bottom rail, between the anode side of the freewheeling diode D_1 and the negative polarity of the output capacitor C_L, as shown in Fig. 1(b). The switch, S_2 is added to interact with the interlinking inductor and provide an alternative current path to form a $(N+1)$ converter structure. As a result, the proposed converter is designed based on a floating output. Such design is more suitable for standalone applications, including battery energy storage, solid-state lighting, dc motor, and cascaded/interleaved converters.

In a SCF event, the fuses F_1 and F_2 in-series with the power MOSFETs S_1 and S_2 will isolate the fault, respectively. The reader is referred to our previous study in [24] for details on the selection of the fuse rating. Besides the FT capability, the proposed design also supports the functionality of step-down and step-up, as illustrated in Fig. 1(c) and (d), respectively. This allows the FT converter to adapt to a wide range of input and output voltages, as explained in the following.

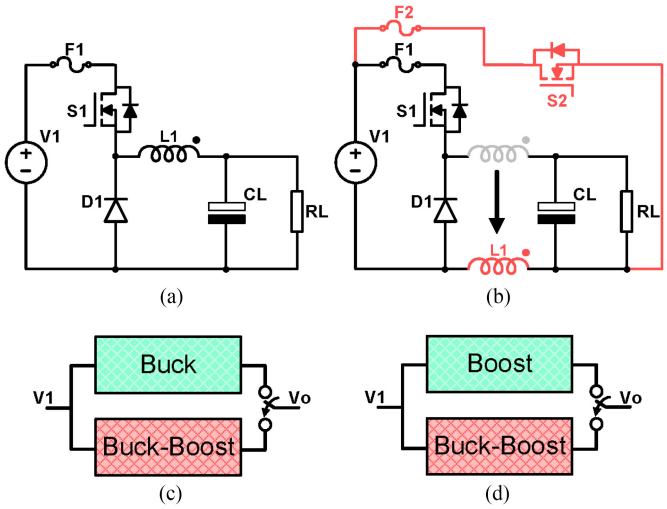


Fig. 1. Overview of the proposed converter structure. (a) Conventional buck converter. (b) Proposed FT converter with 1-level redundancy. (c) Step-down operation of the FT converter. (d) Step-up operation of the FT converter.

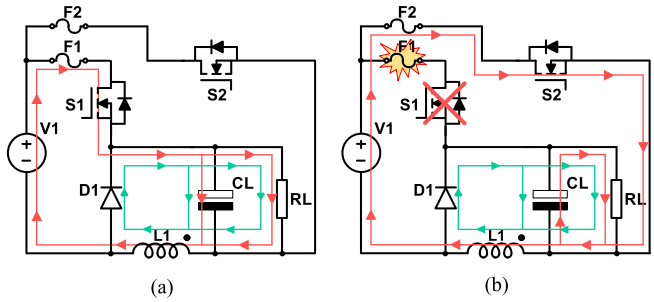


Fig. 2. Step-down fault-tolerant operation (Red: Charge and Green: discharge). (a) Buck (S_1-active, S_2-idle, and D_1-active). (b) Buck–boost: (S_1-faulty, S_2-active, and D_1-active).

A. Step-Down Mode

In Fig. 1(c), the proposed topology enables both the operational modes of buck and buck–boost. The step-down operation is illustrated by the circuit analysis in Fig. 2. The current path indicates when S_1 turns ON for charging the output capacitor C_L and storing the energy in the inductor L_1. In the next cycle, when S_1 is turned OFF, D_1 conducts as it is forward biased. This is represented as the freewheeling current path shown in Fig. 1(c), where C_L and L_1 discharge the remaining energy during this cycle. In the case of S_1 failure, e.g., due to SCF, S_2 will bypass the fault and continue the charging process of L_1, as shown in Fig. 2(b). The proposed FT converter will, then, operate as a buck–boost converter through the switching action of S_2, while sharing the same diode D_1 during the discharging state. Even though the reconfigured circuit is capable of supporting the boost operation, it is continued to be operated in the step-down mode in order to maintain the steady-state output. Note that, to achieve the abovementioned operation, an FD circuit is required to detect a fault occurring in S_1. Such a design is presented in Section VI.

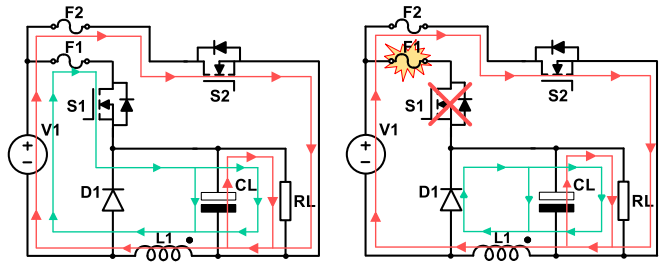


Fig. 3. Step-up fault-tolerant operation (Red: Charge and Green: discharge). (a) Boost (S_1-active, S_2-active, and D_1-OFF). (b) Buck–boost: (S_1-faulty, S_2-active, and D_1-active).

The inductor volt-seconds balance under the continuous conduction mode (CCM) can be derived as

$$\int_0^t V_L \cdot dt = (V_1 - V_o)DT - V_o(1-D)T = 0 \tag{1}$$

$$\int_0^t V_L \cdot dt = V_1(DT) - V_o(1-D)T = 0 \tag{2}$$

where (1) to (2) determines the transition from faulty S_1 to healthy S_2 at ON-state period. As seen in Fig. 2, both circuits share the same diode D_1 for the discharging state. Hence, the volt seconds in both of the abovementioned equations during the OFF-state period can be written as $V_o(1\text{-}D)T$.

By manipulating (1) and (2), the output voltage conversion of the proposed FT converter can be written as

$$V_{\text{bc}} = DV_1, \text{ and} \tag{3}$$

$$V_{\text{bbc}} = \frac{D}{1-D}V_1 \tag{4}$$

where V_{bc} and V_{bbc} represent the output voltage of the buck and buck–boost configurations, respectively. To enter the step-down region of buck–boost operating mode, the switching duty cycle should be $D \leq 0.5$.

B. Step-Up Mode

The proposed topology can also operate in the boost and buck–boost modes, as shown in Fig. 1(d). Both active switches, S_1 and S_2, are utilized to form a synchronous boost converter illustrated in Fig. 3(a). Therefore, S_1 and S_2 operate in complementary mode, i.e., they should never be turned ON for conduction at the same time. The charging state of L_1 is activated when S_2 is turned ON. The discharging state of L_1 is through the switching action of S_1, as indicated in Fig. 3(a). Note that the step-up conversion will not function if the backup switch S_2 fails to operate.

Referring to the volt-seconds balance when S_1 and S_2 is healthy, the steady-state inductor current in the CCM for the boost converter can be derived as

$$\int_0^t V_L \cdot dt = V_1(DT) - (V_1 - V_o)(1-D)(T) = 0. \tag{5}$$

Note that both the circuits, shown in Fig. 3(a) and (b), utilize S_2 during the charging state, whose volt seconds can be defined as $V_1(DT)$. Therefore, using (5), the voltage conversion ratio can be expressed by

$$V_{\text{boc}} = \frac{1}{1-D}V_1 \tag{6}$$

where V_{boc} represents the output voltage of the boost converter.

In the event of S_1 failure, the converter will operate in buck–boost mode, as shown in Fig. 3(b). The operation principle is the same as described in Section II-A and illustrated in Fig. 2(b). The step-up region of the buck–boost operating mode is $D \geq 0.5$.

III. Reliability Evaluation

This section presents the reliability assessment using the Markov reliability approach for the conventional and proposed FT converter structures based on different levels of redundancy.

A Markov chain uses directed graphs to visualize the probability of transitioning from one state to another within a finite number of possible states. In the literature, various FT converter topologies have been extensively studied using Markov models to evaluate the operational lifetime versus system reliability based on the mean-time-to-failure (MTTF) profile [19], [25]. MTTF is the mean time to the first failure of a component under specified experimental conditions. It is assessed by integrating the reliability function during the time interval $[0, \infty]$ as follows:

$$\text{MTTF} = \int_0^\infty R(t) \cdot dt. \tag{7}$$

A. Conventional Buck Converter

The states and their transition paths for a single-switch conventional buck converter are shown in Fig. 4(a). The states considered, here, are defined as follows. State 1 refers to the condition when the converter is "Healthy," State 2 refers to the presence of a "Partial fault" in the converter, while State 3 refers to a "Complete Fault" in the converter. The transition path λ_{12} indicates when the converter is transitioning from a healthy state to a partial fault condition. This could be the consequence when either C_i or C_L fail, and the failed component is removed from the input or output sides, respectively. Although the converter may still be able to achieve an acceptable operation under this situation, the removal of a parallel capacitor will increase the magnitude of the voltage ripples at the steady state. Note that State 3 is the end of the Markov chain, where the converter suffers a complete failure. Therefore, λ_{13} and λ_{23} represent a system-level breakdown caused by a failure of components including S_1, F_1, D_1, L_1, and C_L.

A summary of all possible transition paths is shown in Table I. Note that λ_{S1}, λ_{D1}, λ_{L1}, λ_{CL}, and λ_{F1} represent the lambda failure rates of the MOSFET, diode, inductor, output capacitor, and fuse, respectively. λ_{C_ip} and λ_{C_Lp} determine when an input and output capacitor will suffer from a partial fault, respectively. In addition, the relative terms λ_{S1k}, λ_{D1k}, λ_{L1k}, λ_{CLk}, and λ_{F1k} can be considered as the lambda failure rates caused by degradation faults of C_i or C_o.

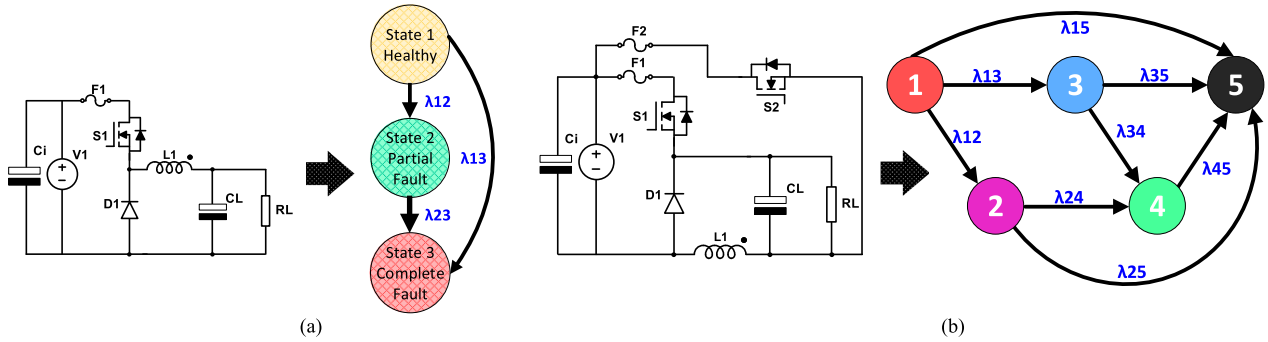


Fig. 4. Reliability model of power converters based on a Markov chain. (a) Conventional buck converter consisting of three possible states and three transition paths. (b) TProposed FT converter with 1-level redundancy, consisting of five possible states and eight transition paths.

TABLE I
TRANSITION PATHS OF THE CONVENTIONAL AND PROPOSED FT CONVERTERS

Converter topologies	Markov transition chain of converter reliability
Conventional Converter	$\lambda_{12} = \lambda_{Cip} + \lambda_{CLp}$, $\lambda_{13} = \lambda_{S1} + \lambda_{D1} + \lambda_{L1} + \lambda_{CL} + \lambda_{F1}$ $\lambda_{23} = \lambda_{S1k} + \lambda_{D1k} + \lambda_{L1k} + \lambda_{CLk} + \lambda_{F1k}$
Proposed FT Converter with 1-Level redundancy	$\lambda_{12} = \lambda_{34} = \lambda_{Cip} + \lambda_{CLp}$, $\lambda_{13} = \lambda_{S1} + \lambda_{F1}$, $\lambda_{24} = \lambda_{S1k} + \lambda_{F1k}$ $\lambda_{15} = \lambda_{D1} + \lambda_{CL} + \lambda_{L1}$, $\lambda_{25} = \lambda_{D1k} + \lambda_{CLk} + \lambda_{L1k}$ $\lambda_{35} = \lambda_{S2} + \lambda_{D1} + \lambda_{CL} + \lambda_{L1} + \lambda_{F2}$, $\lambda_{45} = \lambda_{S2k} + \lambda_{D1k} + \lambda_{CLk} + \lambda_{L1k} + \lambda_{F2k}$

A transition matrix defines the probability of a state transition from one state to another, for all possible combinations of starting and ending states. The dimensions of the transition matrix correspond to the number of possible states, which is three in this case. Let the probability state function be defined as $P_n(t), n \in \{1, 2, 3\}$, and failure rate of the transition path be λ_{ij}. The derivative of the probability function is then

$$\frac{d}{dt}\begin{bmatrix} P_1(t) & P_2(t) & P_3(t) \end{bmatrix} = \begin{bmatrix} P_1(t) & P_2(t) & P_3(t) \end{bmatrix} \times \begin{bmatrix} -(\lambda_{13}+\lambda_{12}) & \lambda_{12} & \lambda_{13} \\ 0 & -\lambda_{23} & \lambda_{23} \\ 0 & 0 & 0 \end{bmatrix} \tag{8}$$

$$\frac{dp_1(t)}{dt} = -(\lambda_{13}+\lambda_{12}) \cdot p_1(t) \tag{9}$$

$$\frac{dp_2(t)}{dt} = \lambda_{12} \cdot p_1(t) - \lambda_{23} \cdot p_2(t). \tag{10}$$

The converter is initially assumed to be healthy, and the probability $P_1(0)$ is assigned as "1". The initial probability of all n states can, then, be written as

$$P_n(0) = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}. \tag{11}$$

Solving the differential equation from (9) and (10) using the initial probability vector given by (11), the probability distribution for each state is obtained as follows:

$$P_1(t) = e^{-(\lambda_{13}+\lambda_{12})t}, \text{ and} \tag{12}$$

$$P_2(t) = e^{-\lambda_{23}(t)} - e^{-(\lambda_{13}+\lambda_{12})t}. \tag{13}$$

Subsequently, the operational lifetime of the conventional converters can be obtained. This is shown by the exponential distribution curve presented in Fig. 5. Now, MTTF can be

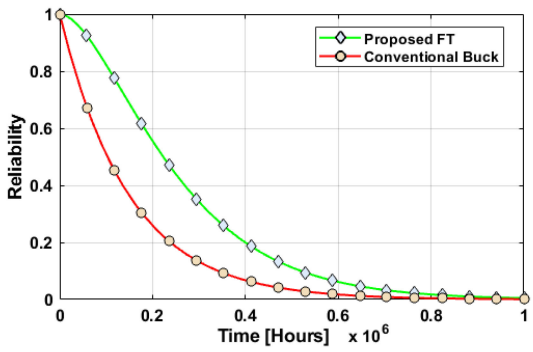


Fig. 5. Reliability comparison between the conventional and the proposed fault-tolerant converters.

calculated by summing the probabilities of (12) and (13), and, then, substituting it in (7). The abovementioned expressions are similarly extended to derive the Markov chain model for the proposed FT converter.

B. Proposed FT Converter Equipped With 1-Level Redundant Switch

In Fig. 4(b), the corresponding Markov chain can be expanded into five possible states and eight transition paths. The converter is operating under step-down mode, as illustrated in Fig. 2. The transition path λ_{13} represents the scenario when the proposed FT converter reconfigures from buck to buck–boost operation when S_1 fails to operate and F_1 blows. Note that this particular switch failure will not force the converter to the absorption State 5 due to the presence of the redundant switch S_2. Next, the transition paths with λ_{12} and λ_{34} indicate the transition of the converter under buck and buck–boost modes from a healthy to a degradation state, respectively. Furthermore, λ_{24} is when

TABLE II
COMPONENT FAILURE RATE [26]–[28]

Element	Failure Rate	Temperature Factor	Power Losses
MOSFET	$\lambda_S = \lambda_b \cdot \pi_T \cdot \pi_A \cdot \pi_Q \cdot \pi_E$	$\pi_t = exp\big[-1925\big(\frac{1}{T_j+273}-\frac{1}{298}\big)\big]$	$P_S = \frac{1}{T}\left[\int_0^T \left(R_{\mathrm{DS,on}} i_S^2(t) + V_T i_S(t)\right) dt\right]$
Diode	$\lambda_D = \lambda_b \cdot \pi_T \cdot \pi_S \cdot \pi_C \cdot \pi_Q \cdot \pi_E$	$\pi_t = exp\big[-3091\big(\frac{1}{T_j+273}-\frac{1}{298}\big)\big]$	$P_D = \frac{1}{T}\left[\int_0^T \left(R_d i_S^2(t) + V_f i_D(t)\right) dt\right]$
Capacitor	$\lambda_C = \lambda_b \cdot \pi_T \cdot \pi_C \cdot \pi_V \cdot \pi_Q \cdot \pi_E$	$\pi_t = exp\big[5.09\big(\frac{T_a+273}{358}\big)^5\big]$	$P_C = \frac{1}{T}\left[\int_0^T R_{esr} i_{rms}^2(t) dt\right]$
Inductor	$\lambda_L = \lambda_b \cdot \pi_T \cdot \pi_Q \cdot \pi_E$	$\pi_t = exp\big[\frac{0.11}{8.617\times 10^{-5}}\big(\frac{1}{T_{HS}+273}-\frac{1}{298}\big)\big]$	$P_L = \frac{1}{T}\left[\int_0^T R_{dcr} i_{rms}^2(t) dt\right]$

the converter reconfigures from S_1 (buck) to S_2 (buck–boost), while the converter still suffers from a partial fault. The absorption state can happen through the following four transition paths; λ_{15}, λ_{25}, λ_{35}, and λ_{45}. In this case, λ_{35} and λ_{45} refer to the failure of the last redundant switch S_2 from healthy and degradation conditions, respectively. In Fig. 4(b), λ_{15} and λ_{25} are when the switches are intact while the converter experienced a single-point-failure from D_1, L_1, and C_L. The transition paths along with component failure factors are summarized in Table I.

The transition matrix of the proposed FT converter with 1-level redundancy can be modeled as

$$\frac{d}{dt}\left[P_1(t)\cdots P_5(t)\right] = \left[P_1(t)\cdots P_5(t)\right]\left[\begin{array}{c|c} A & B \\ \hline C & D \end{array}\right] \tag{14}$$

where

$$A = \begin{bmatrix} -(\lambda_{12}+\lambda_{13}+\lambda_{15}) & \lambda_{12} \\ 0 & -(\lambda_{24}+\lambda_{25}) \\ 0 & 0 \end{bmatrix} \tag{15}$$

$$B = \begin{bmatrix} \lambda_{13} & 0 & \lambda_{15} \\ 0 & \lambda_{24} & \lambda_{25} \\ -(\lambda_{34}+\lambda_{35}) & \lambda_{34} & \lambda_{35} \end{bmatrix} \tag{16}$$

$$C = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad D = \begin{bmatrix} 0 & -\lambda_{45} & \lambda_{45} \\ 0 & 0 & 0 \end{bmatrix}. \tag{17}$$

The initial probability vector of the n states can be written as

$$P_n(0) = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}. \tag{18}$$

The reliability function of the proposed FT converter with 1-level redundancy can, then, be written as

$$R_{1-\mathrm{level}} = P_1(t) + P_2(t) + P_3(t) + P_4(t). \tag{19}$$

IV. NUMERICAL RELIABILITY ASSESSMENT

This section presents a numerical reliability assessment of the proposed FT converter and the conventional converter based on the typical failure rates observed for the various components. The probabilities of each of the transition paths in the Markov chain model are derived based on the military handbook MIL-HDBK-217 [26]

$$\lambda_{\mathrm{component}} = \lambda_b \prod_{i=1}^{n} \pi_i \tag{20}$$

where λb is the base failure rate, which depends on factors such as the packaging type and ambient temperature conditions. Note that n is the number of π_i failure factors including the temperature effect π_T, voltage stress π_S, application type π_A, quality factor π_Q, and capacitance factor π_C. Other considered factors are listed in Table II. The details are presented as follows.

1) π_E is an environmental effect that is a function of the operating temperature conditions.
2) π_a is an application factor of the transistor (MOSFET, bipolar junction transistor (BJT), and junction gate field-effect transistor (JFET)). It depends on the rated output power.
3) π_s is the voltage stress factor considered in the diode element, which is calculated by
$$\pi_s = (V_d/V_r)^{Ts} \tag{21}$$
where V_d is the forward voltage of the diode and V_r is the rating of its reverse voltage. T_s is the transient suppressor, which is fully dependent on the calculated ratio of V_d/V_r.
4) π_V is the voltage stress factor considered in the capacitor element
$$\pi_V = \left(\frac{V_{\mathrm{OC}}/V_{\mathrm{RC}}}{0.5}\right)^{17} + 1 \tag{22}$$
where V_{oc} and V_{rc} are the applied operating voltage and rated voltage of a capacitor, respectively. π_C is the capacitor factor of an electrolytic capacitor, which is given by
$$\pi_C = 0.34\, C^{0.18}. \tag{23}$$
5) π_Q is the quality factor defined as screening level of power semiconductor prefix (JANTXV, JANTX, JAN, D, C, S, R, B, P, M, lower).
6) π_T is the temperature factor, which considers the device junction temperature T_j of the MOSFET and the diode. Alternatively, for inductors and transformers, the hotspot temperature T_{HS} is considered.

Based on these factors, the junction temperatures of MOSFET and diode induced by their respective power losses can be calculated as

$$T_C = T_a + \theta_{\mathrm{CA}} P_{\mathrm{DS}} \tag{24}$$

TABLE III
CONVERTER RELIABILITY PROFILE

Converter	Normal mode (Buck)	FT mode (Buck-Boost)	Transition path	MTTF (hour/failure)
Conventional	λ_{Cip} = 0.00001 , λ_{CLp} = 0.0449 λ_{S1} = 6.566 , λ_{D1} = 0.0633 λ_{L1} = 0.0012 , λ_{CL} = 0.0371 λ_{F1} = 0.08 , λ_{S1k} = 6.912 λ_{Dk1} = 0.0594 , λ_{L1k} = 0.0013 λ_{CLk} = 0.0449 , λ_{F1k} = 0.08	None	$\lambda_{12} = 0.0449$, $\lambda_{13} = 6.7476$ $\lambda_{23} = 7.0975$	$MTTF = \int_0^\infty R(t)\,dt$ = 0.1482 $\times 10^6$
Proposed	λ_{Cip} = 0.00001 , λ_{CLp} = 0.0449 λ_{S1} = 6.566 , λ_{D1} = 0.0633 λ_{L1} = 0.0012 , λ_{CL} = 0.0371 λ_{F1} = 0.08 , λ_{S1k} = 6.912 λ_{Dk1} = 0.0594 , λ_{L1k} = 0.0013 λ_{CLk} = 0.0449 , λ_{F1k} = 0.08	λ_{Cip} = 0.00001 , λ_{CLp} = 0.0489 λ_{S2} = 7.2576 , λ_{D1} = 0.0673 λ_{L1} = 0.0014 , λ_{CL} = 0.0489 λ_{F2} = 0.08 , λ_{S2k} = 7.430 λ_{Dk1} = 0.0693 , λ_{L1k} = 0.0015 λ_{CLk} = 0.0531 , λ_{F2k} = 0.08	$\lambda_{12} = \lambda_{34} = 0.0489$, $\lambda_{13} = 7.3376$ $\lambda_{24} = 7.510$, $\lambda_{15} = 0.1176$, $\lambda_{25} = 0.1238$, $\lambda_{35} = 7.4552$, $\lambda_{45} = 7.6338$	$MTTF = \int_0^\infty R_{1-level}(t)\,dt$ = 0.2661 $\times 10^6$

TABLE IV
LIST OF COMPONENTS USED IN THE FT CONVERTER

Parameters	Values
Input Voltage V_i	24 V
Switching frequency F_s	100 kHz
MOSFET S_1, S_2 (I_d, R_{ds}, $\theta_{\rm JC}$)	33 A, 44 mΩ, 1.15 $^\circ C/W$
Diode D_1 (V_F, I_F, $\theta_{\rm JC}$)	0.5 V, 20 A, 2.00 $^\circ C/W$
Resistor load R_L	11Ω
Inductor L_1,R_{DCR}	80 μH, 0.15 Ω
Input Capacitor C_i, R_{ESR}	100 μF, 20 $m\Omega$
Output Capacitor C_L, R_{ESR}	220 μF, 10 $m\Omega$

$$T_j = T_C + \theta_{\rm JC} P_{\rm DS} \tag{25}$$

where $P_{\rm DS}$ represents the maximum power dissipation of the MOSFET or diode shown in Table II. $\theta_{\rm CA}$ and $\theta_{\rm JC}$ determine the thermal resistance of the electronic devices between the case-to-ambience and junction-to-case temperatures, respectively. These two parameters can be found in the SPICE model libraries or datasheets [29], [30].

The hotspot temperature depends on the power loss of the inductor, and can be calculated as follows:

$$T_{\rm HS} = T_a + 1.1\,\Delta T, \text{ and} \tag{26}$$

$$\Delta T = 125\,\frac{P_{\rm L}}{A} \tag{27}$$

where ΔT defines the average temperature swing of the inductor, and is defined as the power loss divided by the area of the inductor core. Additional information associated with the reliability assessment of various components can be referred from [26].

Table III lists the numerical values regarding the converter reliability profile. These are computed based on the components outlined in Table IV and the experimental conditions discussed in Section VI. Fig. 5 illustrates the reliability comparison between a conventional buck converter and the proposed FT converter under different redundancy levels. The exponential distribution curve shown in this figure demonstrates that the proposed FT converter has a longer lifetime than the conventional converter. Furthermore, increasing the level of redundancy will guarantee higher reliability, which may be suitable for critical industrial applications.

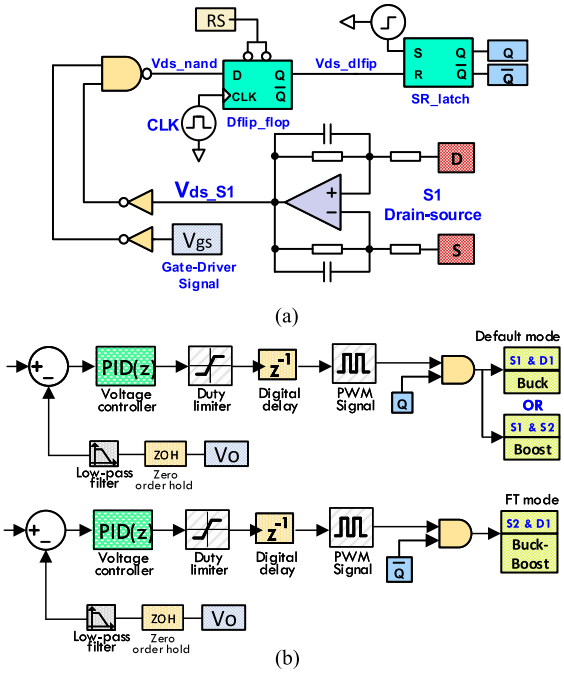


Fig. 6. Simplified FT control diagram showing the proposed. (a) FD scheme. (b) Reconfiguration of the feedback controller.

V. PROPOSED CONTROL SCHEME

Fig. 6 presents the proposed digital control scheme including the functions of FD and voltage regulation. The FT control structure is coordinated by the microcontroller for reconfiguring the redundant switch when an S_1 fault occurs. A feedback controller of the proposed converter (with one-level redundancy) is designed for the buck–boost mode in this case study. Based on the CCM of the buck–boost converter, the small signal model in the state-space notation can be derived as

$$\begin{cases} \frac{d}{dt}\begin{bmatrix}\hat{i}_L \\ \hat{v}_o\end{bmatrix} = \begin{bmatrix} 0 & \frac{D'}{L} \\ -\frac{D'}{C_L} & \frac{1}{R_L C_L}\end{bmatrix}\begin{bmatrix}\hat{i}_L \\ \hat{v}_o\end{bmatrix} + \begin{bmatrix}\frac{V_i+V_0}{L} \\ -\frac{i_L}{C_L}\end{bmatrix}\hat{d} \\ y = \begin{bmatrix}0 & 1\end{bmatrix}\begin{bmatrix}\hat{i}_L \\ \hat{v}_0\end{bmatrix},\ D' = 1 - D. \end{cases} \tag{28}$$

TABLE V
PARAMETERS OF THE PID CONTROLLER FOR THE RECONFIGURED FT CONVERTER

Status	ω_{cl}	ζ_{CL}	P	I	D	T_d
Overshoot	1.65	0.70	6.10e-03	952.69	7.32e-10	9.92e-06
Undershoot	0.25	0.85	4.80e-03	97.89	7.93e-10	6.54e-05
Affine	0.90	0.85	6.41e-04	352.43	7.34e-10	1.82e-05

From (28), the control-to-output transfer function can be obtained as

$$\frac{V_o(s)}{d(s)} = \frac{K_o(-b_o \cdot S + 1)}{s^2 + 2\zeta_o\omega_o \cdot S + \omega_o^2} \tag{29}$$

where

$$K_o = \frac{V_i}{L_1 C_L}, \quad \zeta_o = \frac{\sqrt{LC}}{2D' R_L C_L}$$
$$\omega_o = \frac{D'}{\sqrt{L_1 C_L}}, \quad \text{and} \quad b_o = \frac{DL_1}{D'^2 R_L}.$$

The affine parameterization can, now, be utilized to synthesize the PID controller. The controller, $C_{\text{pid}}(s)$, is represented as follows:

$$C_{\text{PID}}(s) = K_P + \frac{K_I}{s} + \frac{K_D s}{\tau_D s + 1} \tag{30}$$

where

$$K_P = \frac{2\zeta_o\omega_o a_1 - \omega_o^2 a_2}{K_o a_1^2}, \quad K_I = \frac{\omega_o^2}{K_o a_1}$$
$$K_D = \frac{a_1^2 - 2\zeta_o\omega_o a_2 a_1 + a_2^2\omega_o^2}{K_c a_1^2}, \quad \tau_D = \frac{a_2}{a_1}$$
$$\omega_{CL} = K_G \frac{\omega_o}{4\zeta_o\zeta_{CL}}, \quad a_1 = \frac{2\zeta_{cl}}{\omega_{CL}}, \quad a_2 = \frac{1}{\omega_{CL}^2}. \tag{31}$$

Here, ζ_{cl} is the damping ratio closely related to the overshoot performance, It can usually be assigned a value from 0.7 to 1 for obtaining the desired closed-loop performance [31]. K_G is the scaling factor to adjust the gain of ω_{cl}, which impacts the response speed of the closed-loop system [31]. Table V shows that the parameters of the PID controller are varied by the two variables ζ_{cl} and ω_{cl}. With this design, the performance of the controller is practically tested in Section VI for illustrating the effectiveness of the control tuning approach.

VI. EXPERIMENTAL VERIFICATION

The performance of the proposed FT converter, transitioning from a healthy state to various faulty conditions, was evaluated using the prototype FD and converter circuit shown in Fig. 7. The circuit parameters are listed in Table IV. The filter parameters are rated for 5% voltage ripple at rated load. The FD circuit shown in Fig. 6(a) measures the drain-source voltage V_{ds} of the switch S_1 to detect a fault. The simplified feedback control structure for FT reconfiguration illustrated in Fig. 6(b) was implemented in the DSP controller TMS320F28335.

Initially, a SCF between the drain source $V_{\text{ds}-S1}$ terminals of S_1 was triggered at 500 μs, as shown in Fig. 8. Consequently, the F_1 fuse blew, and the S_1 fault was detected by comparing the

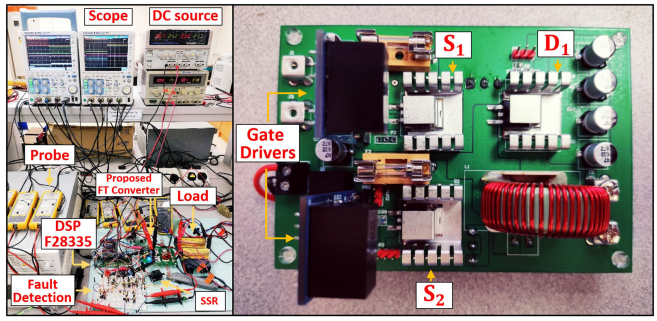


Fig. 7. Experimental setup of the proposed FT converter.

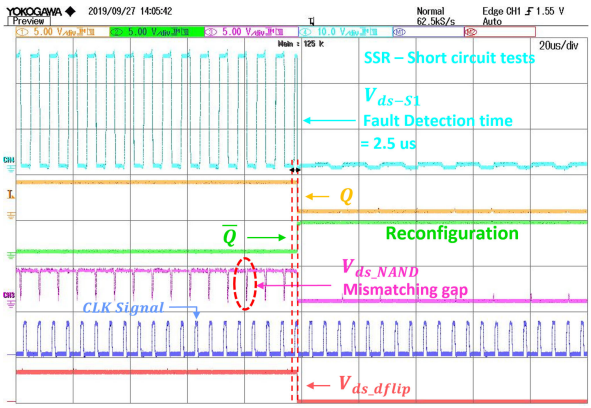


Fig. 8. Short-circuit fault is triggered at 500 μs, and the FD time is around 2.5 μs. A clock signal is added to the D flip-flop gate to prevent mis-triggering of the reconfiguration signal between Q and $\overline{Q}$.

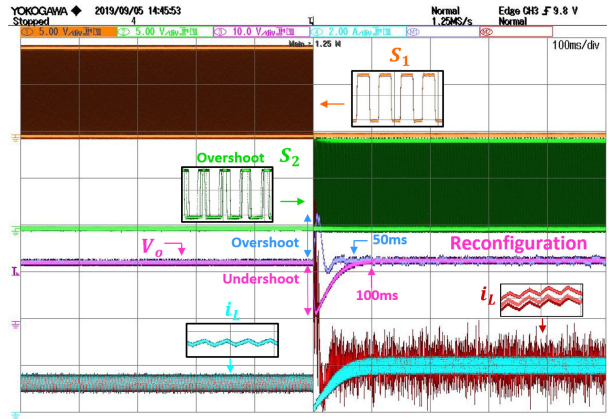


Fig. 9. Waveforms of the proposed FT converter when transitioning from the buck mode to the buck–boost mode after an SCF at 500 μs. Output voltage (blue and pink) and inductor current (red and cyan) are for two separate cases one with an overshoot and another with an undershoot, respectively.

PWM signal of the gate driver V_{gs} with V_{ds}. The propagation delay of the gate driver and inverter gate caused a mismatch $V_{\text{ds}-\text{nand}}$ signal. In this case, the $V_{\text{ds}-\text{flip}}$ is compensated through the D-flip flop [see Fig. 6(a)] by injecting the input clock signal to fill the mismatching signal gap. This ensured that the S-R latch could properly activate the FT reconfiguration when S_1 failed. Subsequently, the signal $\overline{Q}$ became 1 and triggered the

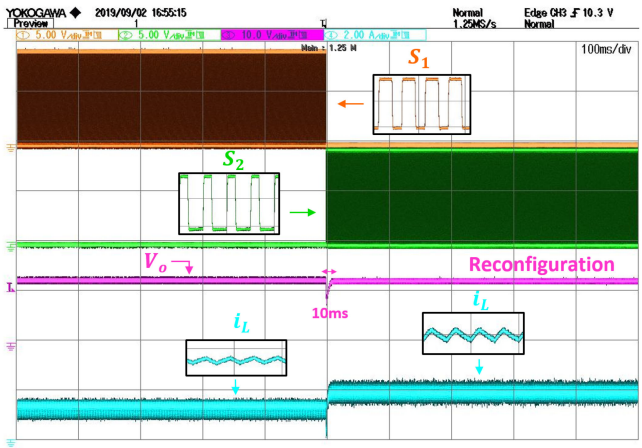


Fig. 10. Waveforms of the proposed FT converter transitioning from the buck mode to the buck-boost mode after an SCF at 500 μs using affine parameters.

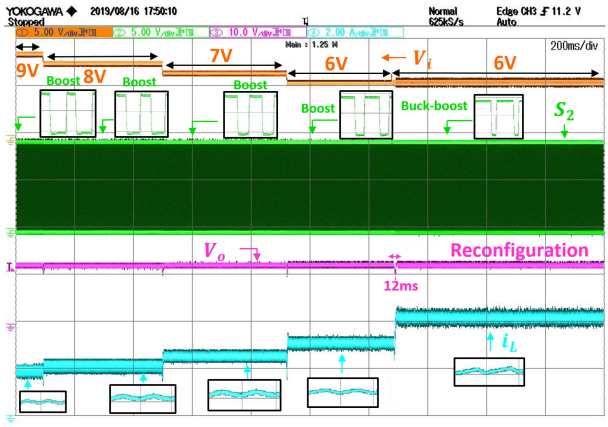
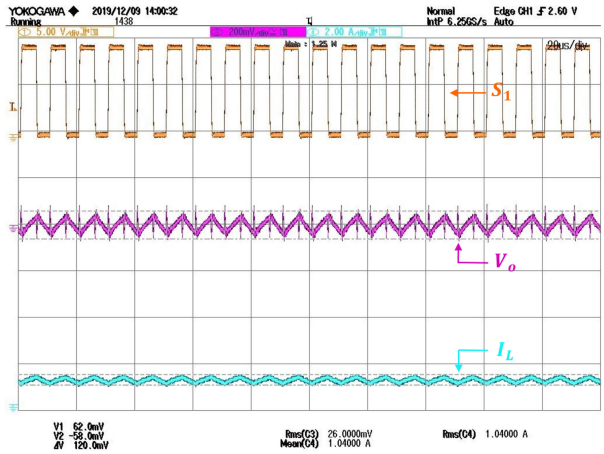
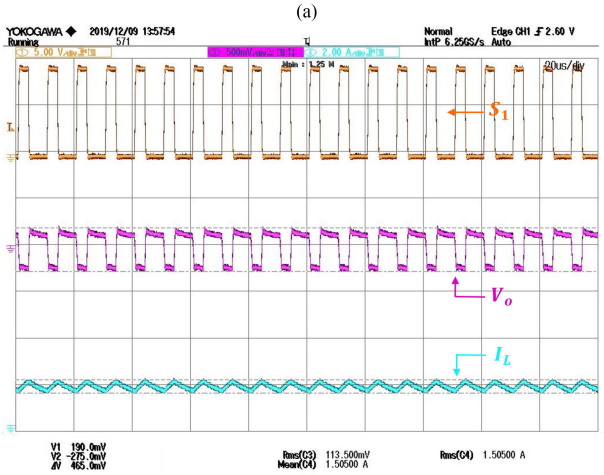


Fig. 12. Waveforms of the proposed FT converter transitioning from the boost mode to the buck–boost mode after an SCF at 1.3 s. The converter experienced multiple input step changes.

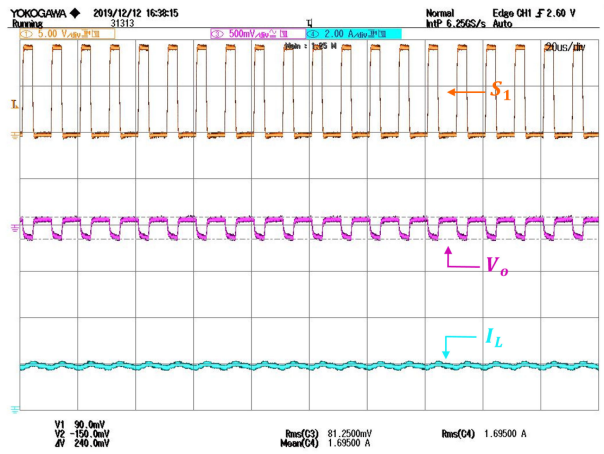


(a)

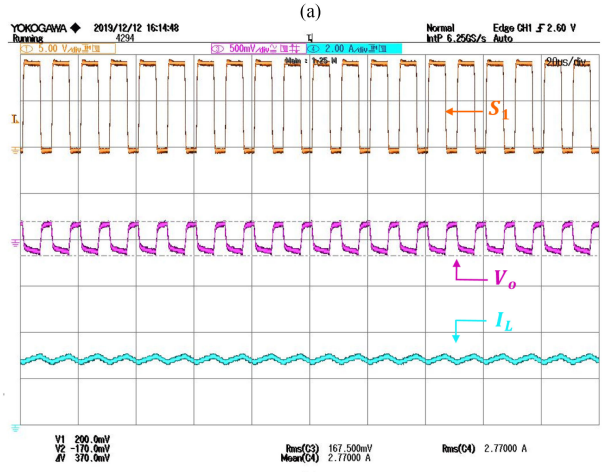


(b)

Fig. 11. Waveforms of the proposed FT converter in step-down mode during the steady-state condition. (a) Buck converter. (b) Buck–boost converter.



(a)



(b)

Fig. 13. Waveforms of the proposed FT converter in step-up mode during the steady-state condition. (a) Boost converter. (b) Buck–boost converter.

buck–boost mode, i.e., the SCF was detected. Note that the FD time was around 2.5 μs, which was less than the switching period.

The output performance of the step-down mode of the reconfigured FT converter is illustrated in Fig. 9. The large overshoots observed in V_o and i_L during the transition period were the outcome of using the *overshoot* parameters listed in Table V. In addition, the zoomed-in waveforms of the S_2 PWM signal and i_L exhibited time-varying duty cycles and fluctuating currents, respectively. These fluctuating dynamics led to additional power losses induced by the switching noise. Furthermore, overshoots (voltage and current spikes) could cause physical damages to

other electronic components, and consequently reduce the overall lifespan of the converter. In contrast, for the *undershoot* control parameters, the smoother i_L and V_o waveforms after the reconfiguration reduced the component stress. However, the reconfiguration speed was slower than the *overshoot* counterpart. The larger corresponding voltage dip of V_o may also cause a downtime to the connected load. This demonstrates the need for affine parameterization to achieve the desired transition dynamics.

The corresponding scopes of the *affine* controller are shown in Fig. 10. This controller was able to achieve a more seamless and smoother reconfiguration. Specifically, the transitioning time was around 10 ms compared to the *overshoot* and *undershoot* controllers of 50 ms and 100 ms, respectively. As a result, the lifetime reliability of the power converter is enhanced. Note that Fig. 11(a) and (b) shows the proposed FT converter between buck and buck–boost operation modes under steady-state conditions. The waveform results illustrate the inductor current and output voltage ripples based on Table IV.

The proposed converter was further demonstrated for a transition from the synchronous boost mode to the buck–boost mode in step-up FT operation. In this case, an SCF was triggered after 1.3 s, and the corresponding reconfiguration time was around 12 ms, as shown in Fig. 12. In this scenario, the affine controller also maintained V_o at 12 V when the input voltage was varied between 9 and 6 V, and i_L was ramped up at different time intervals. The steady-state operational waveforms for the boost mode (for 9 V input) are shown in Fig. 13(a) and (b).

VII. Conclusion

This article presented a new dc/dc topology to achieve not only the function of FT, but also flexible voltage conversion for either step-down or step-up operation after a switch fault. Both objectives were achieved by simply adding one additional switch to the conventional buck converter. Thus, the overall component count is low in the proposed design in comparison with other FT approaches. Reliability assessment was performed using Markov chains, which indicated an improved reliability index and fault tolerant capability for the proposed design in response to switch failures. Furthermore, to enhance the performance during steady state and while transitioning between healthy and reconfigured states (after a fault), affine parameterization was adopted. An experimental study was performed to illustrate the effectiveness of the proposed FT converter topology and control design.

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