Optimized Design of Multi-MHz Frequency Isolated Auxiliary Power Supply for Gate Drivers in Medium-Voltage Converters

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***Abstract*—This article presents the design and optimization of a suitable topology for an isolated dc–dc auxiliary power supply with high isolation voltage and low coupling capacitance. The converter consists of a GaN HEMT inverter operating at 6.78 MHz, an *LCC* resonance tank, and a class-E low d*v*/d*t* rectifier. Furthermore, the galvanic isolation is implemented using a coreless planar transformer that enables higher insulation voltage with similar or better converter efficiency compared to designs using a magnetic material. An analytical design methodology is developed, however, SPICE investigations show that optimal designs might lie outside the validity of the design equations. Consequently, a virtual prototyping tool is developed based on a genetic algorithm with numerical simulations, and in turn, is used to optimize the converter. The optimization algorithm maximizes the converter efficiency while minimizing the transformer size. Prototypes are constructed based on the resulting Pareto front. Experimental results show the validity of the simulated results. Prototypes transferring power up to 15 W with a peak efficiency of 81% are shown. The selected topology enables insulating voltages exceeding 40 kV and coupling capacitances below 10 pF.**

***Index Terms*—Gate drivers, inductive power transmission, medium voltage, resonant power conversion, virtual prototyping.**

I. Introduction

With the continuous development of high-voltage power semiconductors, medium-voltage converters can obtain lower power losses and increased efficiency. Main applications for medium voltage (up to 36 kV_{RMS}) converters include industrial drives (e.g., fans, mills, and pumps), wind turbines with fully rated converters, medium-voltage dc distribution grids for marine vessels, urban transportation or other applications, and flexible ac transmission systems used in medium-voltage grids [1]–[7]. Such converters operate with dc links of up to a few tens of kilovolts, which necessitates the use of either modular multilevel converter (MMC) topologies, or two-level or three-level voltage source converters (VSCs) using valves with series-connected power semiconductor switches [see Fig. 1(a) and (b)]. The characteristics and current development of high-voltage SiC devices make them especially attractive for medium-voltage applications.

Regardless of the specific medium-voltage converter topology, an auxiliary power supply is always required for energizing control and gate circuitry. In particular, the auxiliary power supply provides power to a switching unit that consists either of a submodule in an MMC converter or several series-connected switches in two-level VSCs (see Fig. 1). The typical output power requirement of the auxiliary power supply is approximately 10 W [8, pp. 121–132].

One way to supply this power is through the local medium voltage dc link by using a dc–dc step-down converter, such as the tapped inductor buck converter [8], [9]. However, to improve system safety and provide better diagnostics, it is more beneficial to supply auxiliary circuits via an external power source [10]. The latter requires the design of sophisticated isolated power supplies with high-voltage insulation and low coupling capacitance. The insulation requirement is related to the operating voltage of the medium-voltage converter, requiring an isolation voltage of at least the full dc-link voltage. A crucial challenge is to simultaneously minimize the coupling capacitance of the auxiliary power supply, as this capacitor constitutes a path for the noise current generated during d*v*/d*t* events and possibly affecting control circuitry [11]. Moreover, the fast switching capabilities of SiC MOSFETs increase the importance of this requirement.

A. Isolated Power Supplies

Isolated power supplies feeding gate drivers in medium-voltage converters are targeted in several publications. In general, these works can be categorized along two dimensions; a single converter feeding a single load or multiple loads, and

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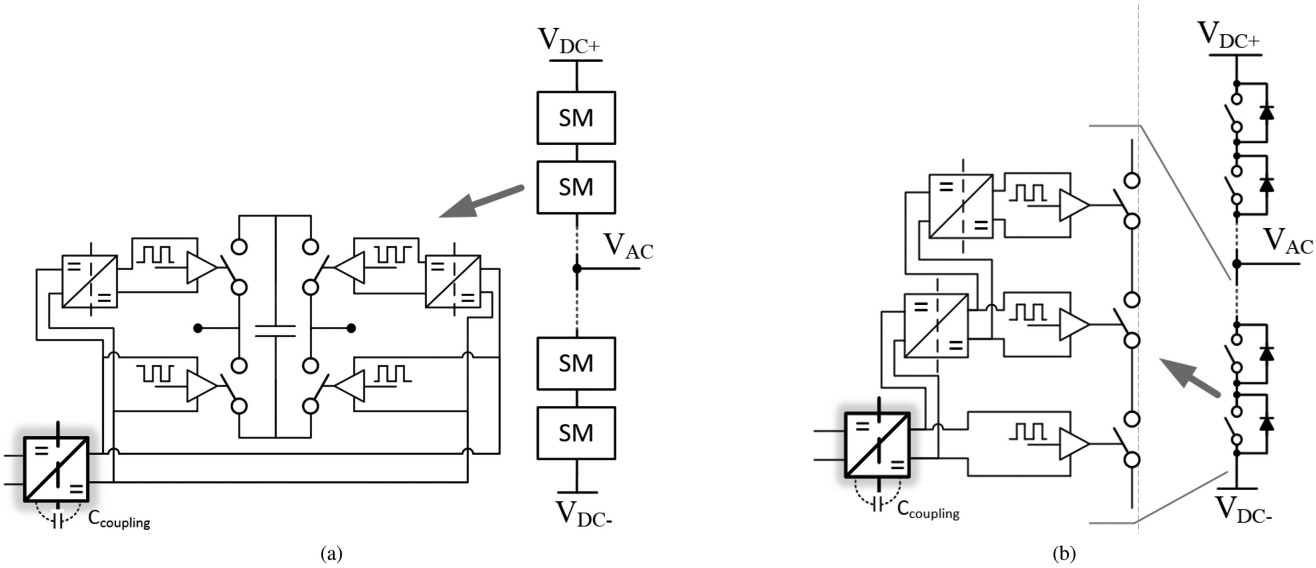


Fig. 1. Conceptual diagrams of the application—supplying power to the gate drivers in a medium-voltage converter arm. The arms of the medium-voltage converter consist of either (a) submodules (SM) in a multilevel converter or (b) series-connected switches. The auxiliary power supply targeted in this article is shown in bold.

transformer design with or without magnetic material. For most of the concepts, a resonant or quasi-resonant converter structure is used. Within resonant converter topologies, the series–series compensated (SS) resonant converter structure is usually preferred due to its simple design. An established architecture consists of a single converter feeding multiple loads using a single primary winding that goes through several toroidal magnetic cores on which the secondary turns are winded and supplies the loads separately [12]–[14]. The reported coupling capacitance is in the range of 1–2 pF [13], which is very low. The disadvantage with a single to multiple load system is that the medium-voltage converter system is dependent on the reliability of the single feeding converter. Furthermore, the previously mentioned feature of better diagnostics is lost.

An alternative architecture consists of separate feeding converters, each with its own transformer and supplying each load separately [10], [15]–[17]. A compact transformer concept designed for up to 36 kV_{RMS} application has been shown using a magnetic material and a dielectric design using potting gel and conductive paint [10]. Although the withstand voltage and small system size are impressive, the transformer concept is complex to manufacture. In comparison, a transformer concept that is easier to fabricate with a breakdown voltage higher than 40 kV is demonstrated in [15] and [16]. Here, the transformer with a magnetic core has an airgap of 1 mm in which a nonmagnetic insulating material is placed. However, it is reported that any increase in the gap distance, and hence, the insulation voltage, drastically decreases the converter efficiency [15].

A more traditional transformer design consisting of insulated wires with different magnetic core materials and shapes has been proposed in [17] and [18]. Additionally, an insulating material is wrapped around the core to increase the insulation voltage. Such schemes have been shown to provide an insulation voltage above 20 kV with low coupling capacitances of less than 5 pF. Yet, such layering of dielectric material must be designed carefully to avoid partial discharges in air pockets between layers. Furthermore, such systems have to comply with several criteria in the standards of the International Electrotechnical Commission (IEC) governing insulation schemes that may result in derating of the insulation voltage [18].

The auxiliary power supply with galvanic isolation can also be established by using power-over-fiber technology [19]–[21]. Although a very low coupling capacitance can be achieved, this technology faces power transmission limitations and low efficiency.

Several publications have also investigated the use of inductive power transfer (IPT) systems as a method of fulfilling the insulation requirements [22]–[25]. Both single converter to single load [22], [25] and single converter to multiple loads [23], [24] have been demonstrated. IPT systems use resonant converters to transfer power by coreless transformers that have poor coupling coefficients. The gap between the primary and secondary sides of the transformer is used to establish an insulation barrier by using either air or another nonmagnetic material as the insulation material. Intrinsically, large gap distances result in low coupling capacitance. IPT systems should operate at high frequency to limit the physical size of the transformer and passive components.

B. Contribution of This Article

This article presents an isolated auxiliary power supply, which is based on the insulation scheme reported by *Am et al.* [15]. By using GaN devices together with a coreless planar transformer, the presented converter can improve the efficiency while simultaneously increasing the achievable insulation voltage compared to the published work. The proposed topology in this article is shown in Fig. 2. It consists of a half-bridge inverter, an *LCC* resonant tank, a coreless transformer, and a class-E rectifier

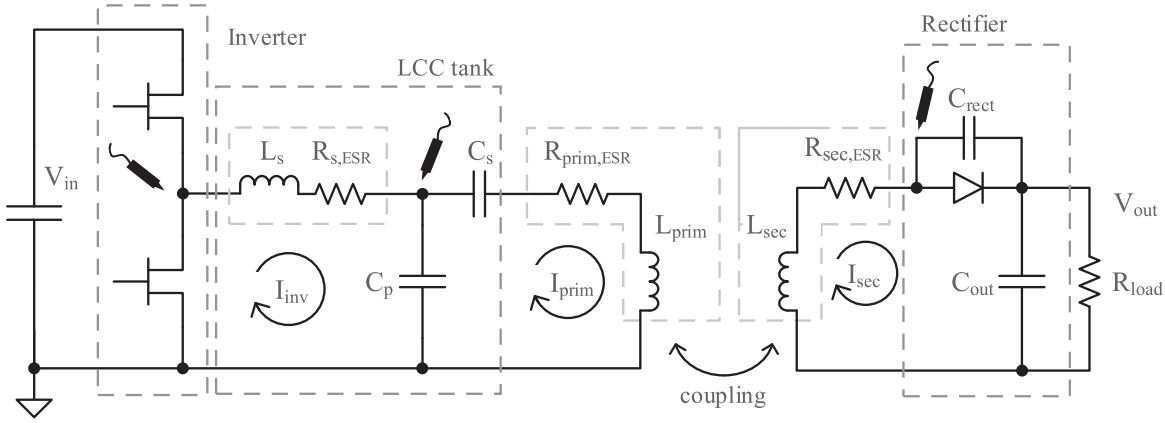


Fig. 2. Schematic diagram of the converter topology consisting of a half-bridge inverter, an *LCC* resonance tank, coreless transformer, and a class-E rectifier. The probe signals indicate the voltage measurement points in the experimental setup for time-domain comparison.

designed for an operating frequency of 6.78 MHz. The proposed topology results in a simple system that can operate in open loop with large variations in load.

Furthermore, an analytical design method is proposed for the topology. In addition, further investigations using SPICE simulations reveal that the rectifier performance improves when designed for frequencies beyond that of the resonance converter. Above-resonance operation is found to be beneficial for the efficiency, however, this necessitates simulation-based design. Thus, this article demonstrates the feasibility of using a virtual prototyping tool for the converter design, which is used to optimize the converter efficiency while minimizing the transformer coupling capacitance. The optimization results are coherent with the presented design theory and investigations. Three potential candidates for the nonmagnetic insulation material are explored in this article and the insulation performance is evaluated in terms of insulation voltage and coupling capacitance.

This article is organized as follows. Section II describes the converter topology and implementation choices. In addition, arguments for the use of a computer-assisted design method are given. In Section III, the converter modeling is analyzed, and then, verified experimentally. The optimization tool and results are presented in Section IV. Section V presents experimental results of four prototypes taken from the optimized designs obtained in Section IV. Finally, the conclusion is drawn in Section VI.

II. Converter Structure for the Auxiliary Power Supply

A. Proposed Converter Structure

In the literature, an SS resonant converter structure is usually preferred due to the simple design procedure and that the phase angle for the converter does not change with load resistance [26]. The output voltage of the resonant system is rectified using a full-bridge diode rectifier consisting of four diodes. In comparison, the class-E low dv/dt rectifier consists of a single diode. While the rectifier topology is known in the literature for several decades [27, ch. 4], [28], it has gained interest in recent years for use in IPT systems [29], [30]. For this topology, the transformer secondary-side coil, L_{sec}, and the parasitic capacitance of the diode are used as part of the passive elements needed to form a resonant soft switching circuit. This results in a very compact and efficient rectifier for multimegahertz (multi-MHz) systems. The diode losses are lower than for the full-bridge diode rectifier solutions that are reported as a significant contribution to total losses [25], especially for low output-power designs.

TABLE I
Component Comparison Between the SS Topology and the Proposed Topology

	Capacitors	Discrete inductors	Diodes	Switches
SS	2	0	4	2
Proposed	3	1	1	2

There are several inverter topologies available for multi-MHz (i.e., 6.78 MHz and beyond) frequency applications. Due to the high switching frequency, the inverter must operate with soft switching in order to eliminate the excessive switching losses. The class-E inverter [27, ch. 13], [31], [32] and the class Φ_2 [33] are often used, both consisting of a single switch. Main drawbacks of these converters are low switch utilization and sensitivity to load variation and tuning issues. In this work, a half-bridge structure is used in combination with an *LCC* resonant tank [34], which results in a total component count that is similar to the SS topology (summarized in Table I). The main difference is the need for a discrete inductor, while only a single diode is needed. In a half bridge, the switch voltage is equal to the dc-link voltage, leading to high switch utilization. This allows for using an integrated half-bridge module with GaN high-electron-mobility transistors (HEMT) that is available for low power applications [35]. Using GaN HEMT devices operating at high frequency keeps the converter size small while ensuring low driving losses. The characteristic capacitances of GaN HEMTs are lower than for Si and SiC counterparts with similar rating [36]. In this regard, GaN HEMT is an enabling technology as using Si or SiC devices at megahertz frequency would result in driver losses comparable to the output power

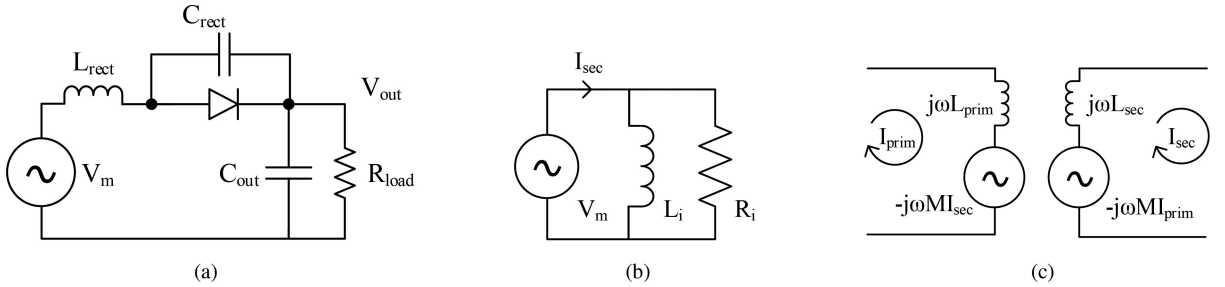


Fig. 3. Schematic diagrams of (a) rectifier model, (b) equivalent input impedance of the rectifier, and (c) coupled inductor model.

of the auxiliary power supply. This is critical for low power applications. However, a concern regarding GaN devices is the effect of dynamic ON-resistance [37], [38] and losses related to the charging and discharging of the output capacitance [39].

B. Analytical Design Method

The design method for the converter is developed based on the fundamental harmonic approximation [27]. The rectifier is modeled, as shown in Fig. 3(a). The load resistance is set as

$$R_{\text{load,min}} = \frac{V_{\text{out}}^2}{P_{\text{nom}}} \tag{1}$$

where V_{out} is the output voltage at the nominal power, P_{nom}. Next, the required inductance and capacitance of the rectifier, L_{sec} and C_{rect}, are found by

$$L_{\text{sec}} = \frac{R_{\text{load,min}}}{\omega_{\text{sec}} Q_r} \tag{2}$$

$$C_{\text{rect}} = \frac{1}{\omega_{\text{sec}}^2 L_{\text{sec}}} \tag{3}$$

where Q_r is the loaded quality factor [27]. ω_{sec} is often set equal to the operating frequency, ω_0. Furthermore, the voltage transfer function between the rectifier input voltage and the dc output voltage of the rectifier is defined as

$$M_V = \frac{V_{\text{out}}}{V_m} \tag{4}$$

where V_m is the amplitude of the voltage source at the rectifier input [27]. Furthermore, the coupled inductors of the primary and secondary side are modeled as [see Fig. 3(c)]

$$V_{\text{prim}} = -j\omega_0 \, M I_{\text{sec}} \tag{5}$$

$$V_{\text{sec}} = -j\omega_0 \, M I_{\text{prim}} \tag{6}$$

where the mutual inductance is defined as

$$M = k\sqrt{L_{\text{prim}} L_{\text{sec}}} \tag{7}$$

where k is the transformer coupling factor. The transformer efficiency depends on the coupling coefficient and the quality factor of the coils. For two spiral coils, the coupling coefficient is at its highest when the coils are of the same size with identical winding number [40]. Consequentially, the coil inductance is chosen as $L_{\text{prim}} = L_{\text{sec}} = L$.

Starting from (6), the current in the primary side of the transformer is dimensioned to satisfy the required input voltage of the rectifier, V_m, as defined in (4)

$$I_{\text{prim}} = \frac{V_m}{\omega_0 \, M} = \frac{V_m}{\omega_0 \, kL}. \tag{8}$$

Next, the equations for the primary-side circuit are developed by using Kirchhoff's voltage law for the fundamental frequency

$$\frac{\sqrt{2}}{\pi} V_{in} = \left(j\omega L_s - j\frac{1}{\omega C_p} \right) I_{\text{inv}} + j\frac{1}{\omega C_p} I_{\text{prim}} \tag{9}$$

$$0 = j\frac{1}{\omega C_p} I_{\text{inv}} + I_{\text{prim}} \left(j\omega L_{\text{prim}} - j\frac{1}{\omega C_p} + Z_{\text{load}} \right) \tag{10}$$

where $Z_{\text{load}} = R_{\text{load}} + jX_{\text{load}}$ is the rectifier impedance reflected to the primary side, V_{in} is the dc input voltage, C_p is the parallel capacitor, L_s is the series inductance, L_{prim} is the transformer primary-side inductance, and I_{inv} and I_{prim} are the currents, as indicated in Fig. 2. Next, we set the resonance of L_s and C_p according to the following criteria:

$$\omega_0^2 = \frac{1}{L_s C_p} = (2\pi f_{\text{sw}})^2 \tag{11}$$

where ω_0 is the series resonance of L_s and C_p, and f_{sw} is the switching frequency of the inverter. With (11) fulfilled, the part containing I_{inv} in (9) equals zero and the expression for the current I_{prim} becomes

$$I_{\text{prim}} = -j\omega_0 C_p \frac{\sqrt{2}}{\pi} V_{\text{in}}. \tag{12}$$

Hence, the current in the primary side of the transformer can be dimensioned by C_p for a given dc-link voltage and is approximately constant over the converter operating range. Combining (8) and (12), the value of C_p is found as

$$C_p = \frac{\pi V_m}{\sqrt{2}\omega_0^2 \, kL V_{\text{in}}}. \tag{13}$$

In the next step, the series capacitor, C_s, is used to tune the switching current. The switching current, $I_{\text{inv,sw}}$, is defined as the current amplitude of I_{inv} at the moment of switching in the half bridge. This current is the sum of the fundamental and higher order harmonics of current resulting from the square wave voltage output of the inverter [34]. At the moment of switching,

the switching current equals

$$I_{\mathrm{inv,sw}} = \frac{\sqrt{2}V_{\mathrm{in}}}{\pi Z_c}\left(\frac{L_{\mathrm{prim}}}{L_s} - \frac{C_p}{C_s} + \frac{X_{\mathrm{load}}}{Z_c} - \frac{\pi^2}{8}\right) \tag{14}$$

where Z_c is the characteristic impedance of the primary resonance circuit ($Z_c = \sqrt{L_s/C_p}$), and X_{load} is the reactance of the rectifier reflected to the primary side. As described in [34], zero current switching (ZCS) can be achieved by setting this expression equal to zero. However, ZCS entails loss of the C_{oss} energy for every switching transition, which is substantial at multi-MHz frequencies. If $I_{\mathrm{inv,sw}}$ is set to a negative value, then ZVS can be obtained. Thus, for a given transformer design, C_s governs the size of the current at the switching instant. C_s is chosen so that the impedance seen from the inverter stays inductive, and with a small switching current that allows for soft switching within the set dead time of the half bridge. Since R_{load} does not appear in (14), this switching current is not dependent on the active power transfer to the secondary side. However, (14) contains the term X_{load}. The equivalent impedance of the class-E rectifier used in this article has shown to change with duty cycle, and hence, with the operating point [28]. This is countered by setting a margin for the switching current.

From (5) and using Fig. 3(b), the rectifier impedance reflected to the primary side is found as

$$Z_{\mathrm{load}} = -\frac{w_0^2\, M^2}{R_i} - \frac{jw_0\, M^2}{L_i} \tag{15}$$

where R_i and L_i are the equivalent input resistance and inductance, respectively, as defined in [27]. The switching current is set according to the output capacitance of the inverter and the target dead time

$$I_{\mathrm{inv,sw}} = -\frac{C_{\mathrm{oss}}V_{\mathrm{in}}}{t_{\mathrm{commutation}}} \tag{16}$$

where C_{oss} is the output capacitance of the inverter switches, and $t_{\mathrm{commutation}}$ is the time required to complete a switching transient, which is equal or smaller than the deadtime. Finally, the value of C_s is found by combining (14)–(16) as

$$C_s = \frac{C_p}{-\frac{\pi Z_c I_{\mathrm{inv,sw}}}{\sqrt{2}V_{in}} + \frac{L_{\mathrm{prim}}}{L_s} + \frac{X_{\mathrm{load}}}{Z_c} - \frac{\pi^2}{8}}. \tag{17}$$

An example of dimensioning the converter is given in the Appendix. The SPICE simulation of the converter shows that the output voltage is within 2.6% of the ideal case.

C. Design of an Above-Resonance Rectifier

The converter is further investigated by changing the resonance frequency of the rectifier, ω_{sec}. In [29], many class-E rectifiers are compared according to their design parameters. It is shown that designing the rectifier OFF-resonance might give advantageous characteristics for the system. An example of a benefit is a smaller output voltage variation with a varying load current if the rectifier resonance frequency is higher than operating frequency, ω_0 [29]. The rectifier circuit, shown in Fig. 3(a), is evaluated through SPICE simulations using ideal components. The relation between the resonance frequency of the rectifier and the voltage source frequency is defined as

$$A_r = \frac{\omega_{\mathrm{sec}}}{\omega_0}. \tag{18}$$

The rectifier is dimensioned using (1)–(3), for which Q_r is set so that the diode duty cycle is 50% [27], [29]. A_r is varied in this article from 1.5 to 2.0 since this has been found to be the most promising design space in terms of high efficiency and lowest output voltage variation [29]. With the component values set, the load resistor is varied from $R_{L,\mathrm{min}}$ and toward open circuit (a decreasing load). M_V is shown in Fig. 4(a). The trend in M_V for nominal output power is consistent with the findings in [29]. For A_r equal to 1.5 (and below), the rectifier output is closer to a current source behavior. For higher A_r, the output behaves like a voltage source until approximately 10% load. In Fig. 4(b) the M_V is used to investigate the expected variation in the output voltage with changing load. Low-voltage variation is observed for a higher A_r. On the other hand, this lower variation comes at a price of lower efficiency since M_V decreases. Additionally, the second harmonic of the rectifier circuit increases drastically, as shown in Fig. 4(c). Nevertheless, an added benefit of increasing A_r is that the required inductor value decreases. Fig. 4(d) shows the passive component values for varying A_r. The inductance value decreases from 2.41 to 0.164 μH, which makes the converter size smaller. The increase in the capacitance value has a softer impact on the practical implementation.

However, for the optimization problem, it is paramount that the model used in the optimization method is coherent with the final experimental results. Fig. 4(c) shows that there is substantial content of harmonics, and in consequence, the fundamental harmonic approximation can no longer be assumed accurate. In this article, it is rather argued for choosing a computer-assisted design process due to the complexity and interactions between design parameters. A high fidelity simulation model serves as the basis for the optimization algorithm. Although this approach requires more time due to the development time of exact models and long simulation times, the benefit is that the inverter, transformer, and rectifier are optimized holistically. The converter topology contains many components resulting in many degrees of freedom. Moreover, even the resonance frequency could be chosen different from the switching frequency, adding to the design problem complexity. To globally answer the design problem, a virtual prototyping tool is used that is based on a genetic algorithm that is suitable for a mixed integer programming problem. However, since the output of the optimization process is dependent on the fidelity of the simulation results, accurate simulation models must be first established.

III. Modeling, Simulation Procedure, and Verification of Converter Operation

A simulation model of the converter structure was established in a SPICE simulation software (LTspice), as such simulators are suitable for detailed component behavior of the semiconductor devices. The electrical simulation model is used to investigate

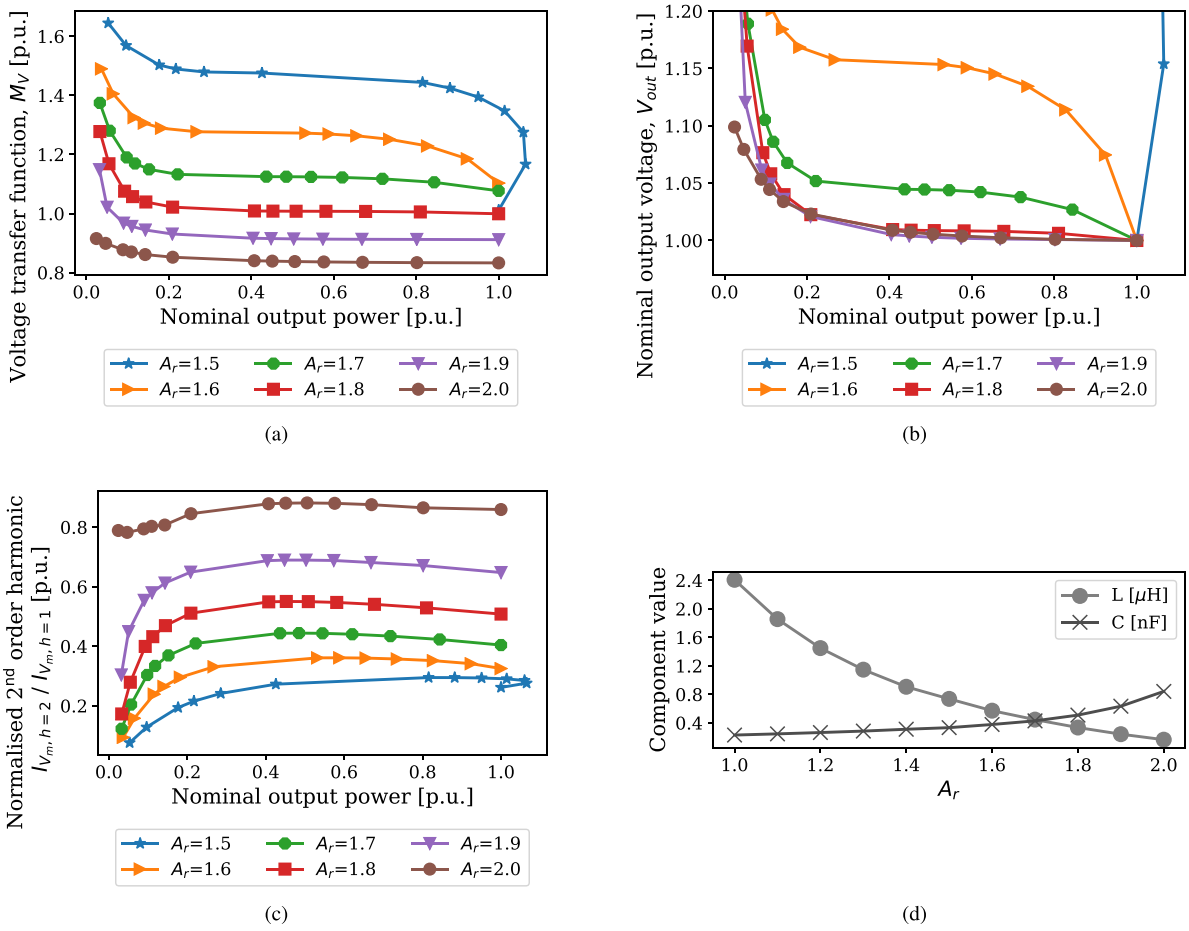


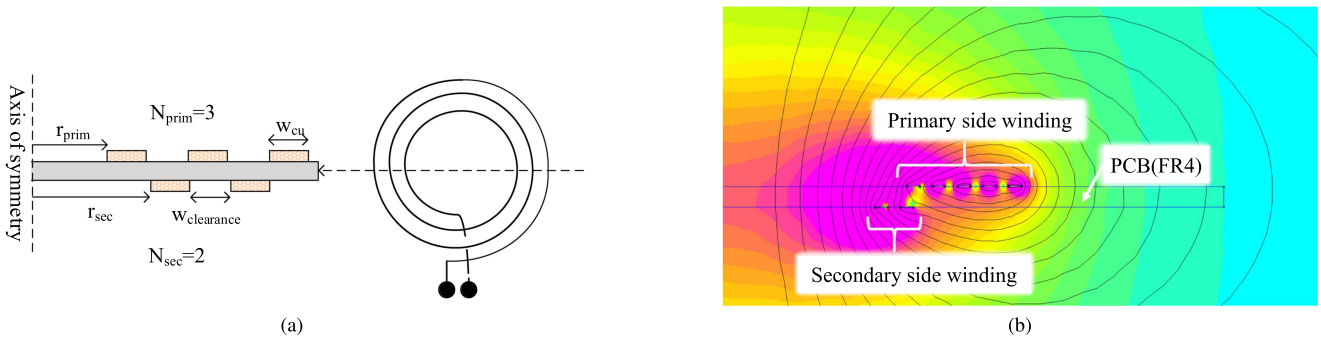
Fig. 4. Results from SPICE simulations of the rectifier circuit assuming ideal components. (a) Voltage transfer function as a function of the output power. (b) Output voltage variation as a function of the output power. (c) Relative second harmonic in the current are plotted as a function of the output power. (d) Values for the resonance components with increasing resonance frequency.

the converter behavior in time domain when steady-state operation has been established. Appropriate semiconductor components for the application are selected among commercially available components, and their SPICE models are included in the simulation. Furthermore, all passive components are added, as shown in Fig. 2. For all capacitors, the equivalent series resistance is set according to the manufacturer data for the chosen operating frequency. For the inductances, the calculated or measured value for the series resistance was used.

The coreless transformer was modeled using finite-element software as a magneto-static problem. From this model, lumped parameter model of the transformer can be extracted to be used in the electrical simulation in time domain. A free software for solving electromagnetic problems using finite-element method, *FEMM*, was used [41]. The transformer is designed as spiral inductors, thus simplifying the electromagnetic problem to a two-dimensional geometry with axisymmetrical properties. Additionally, the transformer can be accurately reproduced by printing windings on a printed circuit board (PCB). Fig. 5(a) shows the geometry of the transformer windings and the magneto-static problem. An example simulation result showing the lines of the magnetic field distribution using FEMM is shown in Fig. 5(b).

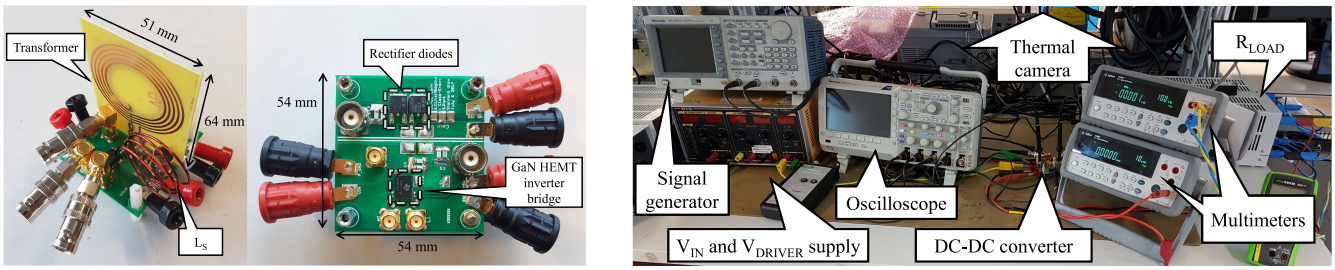
An initial prototype is constructed to verify the results obtained in simulation. Both the converter prototype and the measurement setup are seen in Fig. 6. The prototype is designed to be able to handle the resulting currents when operating with an input voltage of 48 V, resulting in the prototype component values that are given in Table II. The inverter is realized using a GaN HEMT half-bridge module (TI LMG5200). As source for the logic input signals for the lower and upper switch, a signal generator is used (Tektronix AFG3052C). C_p is chosen to obtain a circulating current of approximately 2 A at 48 V input voltage. The transformer was designed with a 5:2 turn ratio, which results in an output voltage of approximately 20 V. On the rectifier side, a SiC Schottky diode is used in the rectifier (STPSC406B, 600 V/4A).

To be able to evaluate the accuracy of the simulation model of the inverter, a loss estimation for the inverter is obtained thermally using a thermal camera (Fluke Ti25). The loss estimate takes into account the ambient temperature and is compensated for the driving losses. All prototype component values are measured with an impedance analyzer (Agilent E4990). The estimated lumped parameters of the prototype PCB transformer are extracted and presented in Table III where they are compared



(a) (b)

Fig. 5. Modeling of a coreless transformer printed on the PCB. (a) Axisymmetric geometry and FEM modeling of the PCB transformer cross section. (b) Example view of magnetic field density calculation for the transformer in FEMM.



(a) (b)

Fig. 6. (a) Initial prototype featuring a coreless transformer made on a PCB. (b) Test setup.

TABLE II
PARAMETERS OF THE PROTOTYPE CONVERTER USED FOR VALIDATION OF THE SIMULATION MODEL

Component	$Inverter$	L_s	C_p	C_s	L_{prim}	L_{sec}	coupling	C_{rect}	C_{out}	Diode
	–	nH	pF	pF	nH	nH	–	pF	nF	–
Value	LMG5200	473	981	330	1379	240	0.48	330	100	STPSC406B

TABLE III
COMPARISON OF TRANSFORMER CHARACTERISTICS BETWEEN FEMM SIMULATION AND THE ESTIMATED VALUES FOUND THROUGH IMPEDANCE MEASUREMENT

Parameter	Value FEM design	Value experimental	Error
L_{prim}	1369 nH	1379 nH	1%
L_{sec}	210 nH	240 nH	15%
coupling	0.48	0.48	-

to the transformer parameters from the FEMM simulation. As can be seen, the transformer inductance values are close to the values obtained from the simulation study. The additional inductance in the developed transformer design is hypothesized to originate from the connecting wires that are not accounted for in FEMM [see Fig. 5(a)]. Hence, the measurements verify that simulated inductance values in FEMM can be realized in an experimental setup with high accuracy.

The converter is simulated and tested in the lab for several input voltages and load resistances. Fig. 7(a) shows the total system efficiency, the output power, and inverter losses for an input voltage of 48 V, while the load resistance varies from 15 to 1000 Ω. The peak measured efficiency is 67% and the converter obtains a peak output power of approximately 8 W. The difference in the maximum efficiency between simulation and experimental values is approximately 5%. Part of this error is due to the thermal and electrical model of the inverter used in the simulation. The comparison of the simulated and measured inverter losses in Fig. 7(a) shows that the inverter losses are underestimated in simulation. It is the hypothesis of the authors that these losses are related to two phenomena in the GaN HEMTs. One is the loss related to charging and discharging of the output capacitance, C_{oss}. The second loss factor is dynamic ON-state resistance, resulting in a higher effective ON-resistance than stated in the device datasheet. Experimental data on hysteresis losses has been published recently [39], [42]. Depending on which manufacturer data from [39] is used for estimating the losses, a range in losses of 0.4 to 1 W is obtained per device. However, this is for 650-V devices. In [42], measurements of the output capacitance losses are performed for a 100-V device, indicating a loss factor of approximately 5–10% of the C_{oss} energy per

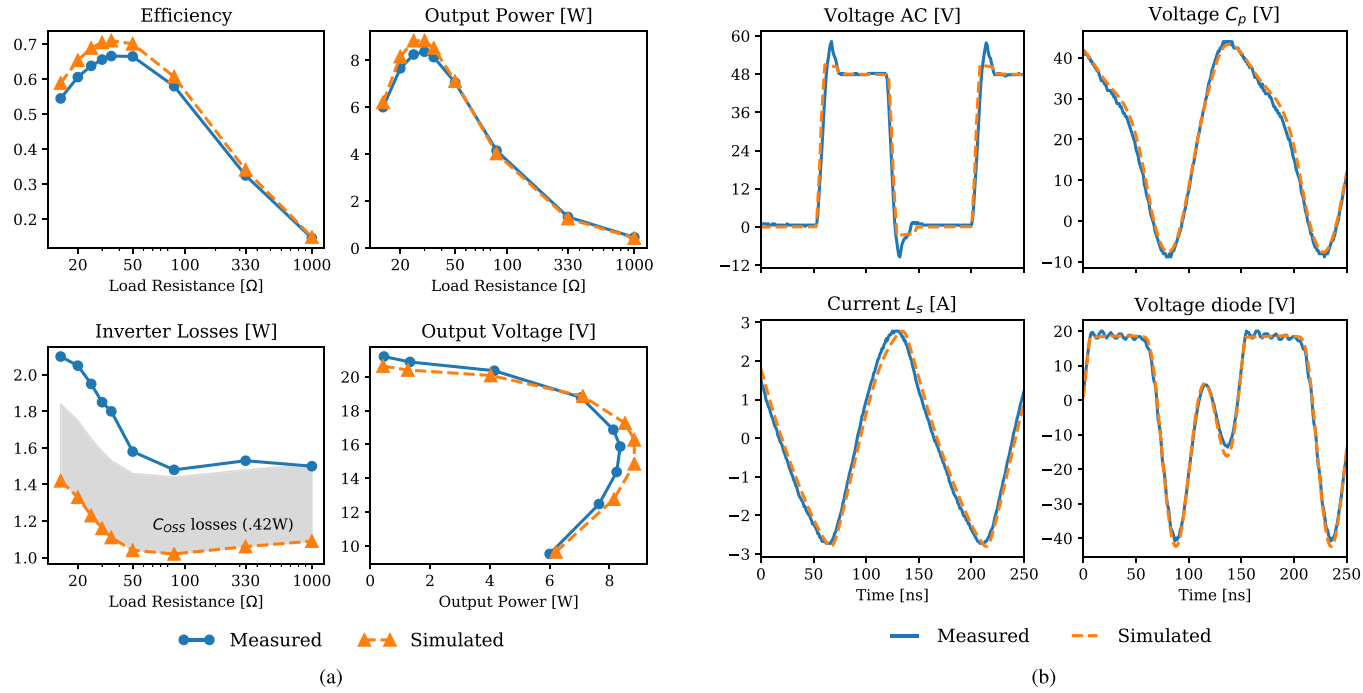


Fig. 7. Comparison of simulated and experimental results of the initial prototype operating with 48 V input voltage. The solid lines are the measured signals and the dashed lines are the simulated signals. (a) DC–DC efficiency, output power, and inverter losses with varying load resistance. Additionally, variation in the output voltage with output power is also shown. (b) Waveforms in time domain from the prototype operating with a 35-Ω load.

cycle [42]. Using this relationship, the output capacitor loss for the two devices in the half bridge then evaluates to

$$P_{C_{\text{oss}}} = 2 \cdot \%_{\text{per cycle}} \cdot E_{\text{oss}} \cdot f = \%_{\text{per cycle}} \cdot C_{\text{oss}} \cdot V_{DS}^2 \cdot f. \quad (19)$$

Using a conservative $\%_{\text{per cycle}} = 10\%$, $C_{\text{oss}} = 266$ pF from the datasheet and $V_{\text{dc}} = 48$ V, $P_{C_{\text{oss}}}$ evaluates to approximately 0.42 W. This power loss is added to the simulated inverter loss as a shaded area in Fig. 7(a). Consequently, the gap between simulated and experimentally measured losses in the inverter is partly explained by the C_{oss} loss mechanism. Moreover, part of the additional losses are hypothesized to be due to dynamic ON-resistance. This effect has been shown to affect GaN HEMTs. The magnitude of the increased effective resistance depends on the operating parameters. At 6.78 MHz and 50% duty cycle, the ON-period for each switch in the inverter is approximately 70 ns, which is below the time frame of published work investigating the transient dynamic ON-state resistance of commercially available devices. Yet, two recent works have investigated the effect on the average ON-resistance in the megahertz range and with soft switching condition [43], [44]. The results from these works indicate that the effective resistance can be increased up to a factor of 7. In conclusion, the experimental results are expected to show higher losses, and hence, lower efficiency than the simulated results.

The simulated versus experimental performance of the converter is also investigated in time domain by four measurements. Three voltages are measured (shown in Fig. 2 by probe symbols) using passive probes (TPP0200)—the output voltage of the half bridge, the voltage over C_p and the voltage at the anode of the diode. The probe tip capacitance is added in the simulation model to account for probe loading. In addition, the current in L_s is measured with a Rogowski coil (PEM CWT015). An example of the waveform comparison is shown in Fig. 7(b). A good accordance is observed between the simulation and the measured signals. A difference is seen at the edges related to the reverse conduction of the half bridge. In addition to the measured overshoot, a slight difference in the reverse conduction voltage drop of the simulation model and the GaN chip can be observed. For the three other waveforms, the voltages and the current deviate slightly during transients containing harmonics. Yet, the simulation is deemed well within the needed accuracy, knowing that some increased losses should be expected. The goal is to identify the potential of the selected topology. Using the simulation model as input, an optimization method can be utilized to obtain designs with maximized efficiency. The resulting converter design could then be tested experimentally to establish an expectation of the final converter performance.

IV. Converter Optimization

This section describes the optimization procedure and the simulation results. The goal of the optimization algorithm is defined through the objective functions. For this article, two such functions are defined. The first function maximizes the converter efficiency, while the second one minimizes the size of the transformer. The transformer size is defined as the radius of the outer circumference of the transformer windings. The largest value of either the primary or secondary side is selected.

Minimizing the transformer size is an indirect method of minimizing the transformer coupling capacitance without adding additional simulation steps to quantify the capacitance value. Furthermore, a constraint for the output voltage is added. The optimization problem is thus formulated as follows:

$$\begin{aligned} \underset{\mathbf{x}}{\text{maximize}} \quad & \text{Obj}_1(\mathbf{x}) = \eta_{\text{dc-dc}} \\ \underset{\mathbf{x}}{\text{minimize}} \quad & \text{Obj}_2(\mathbf{x}) = \max(r_{\text{prim}}, r_{\text{sec}}) \\ \text{subject to} \quad & \mathbf{x} \geq \mathbf{x}_{\text{lowerbound}} \\ & \mathbf{x} \leq \mathbf{x}_{\text{upperbound}} \\ & V_{\text{out,min}} \leq V_{\text{out}}(\mathbf{x}) \leq V_{\text{out,max}} \end{aligned} \tag{20}$$

where $\mathbf{x}$ is a vector of variables of the optimization with minimum and maximum values, as defined by $\mathbf{x}_{\text{lowerbound}}$ and $\mathbf{x}_{\text{upperbound}}$; $\eta_{\text{dc-dc}}$ is the converter efficiency; r_{prim} and r_{sec} are the outer radii of the transformer's primary and secondary sides, respectively; and V_{out} is the converter output voltage.

The optimization algorithm can vary the geometry of the transformer and the remaining passive elements of the converter. Changes to the transformer geometry results in variation in the lumped parameters, which in turn are used in the circuit simulation. In total, the multiobjective optimization has ten variables. The variable vector, $\mathbf{x}$, is hence defined as

$$\mathbf{x} = (N_{\text{prim}}, N_{\text{sec}}, w_{\text{cu}}, r_{\text{prim}}, r_{\text{sec}}, L_s, C_p, C_s, C_{\text{rect}}, R_{\text{load}})$$

where N_{prim} and N_{sec} are the number of turns on the primary and secondary side, respectively; w_{cu} is the width of the copper track and $L_s, C_p, C_s, C_{\text{rect}}$, and R_{load} are the component values of the circuit, as indicated in Fig. 2. The load resistance is defined as an optimization variable to ensure that an optimal efficiency point is found for any given combination of values for the other passive elements.

A genetic algorithm is chosen to identify the Pareto front of the converter. The algorithm, NSGA-II, is suitable for the multiobjective, mixed integer programming problem [45]. Fig. 8 shows the algorithm flow chart. Initialization of the population is done using random sampling of all variables. During the evaluation step, each individual is evaluated in terms of efficiency and transformer size. First, the lumped parameters of the transformer are found by FEM simulation, as described in the previous section. Following the FEM simulation, an LTspice simulation is run with the circuit parameters of the individual to find the converter efficiency. The time-domain simulation runs for a sufficiently long time period so that steady-state conditions are reached. Since convergence cannot be guaranteed for all SPICE simulations, a time-out is set for each simulation. If the simulation does not finish in time, the individual is rejected by the algorithm. When both of the simulations are finished, the individuals are evaluated based on the objective functions. In addition, violation of the given constraints influences the evaluation of the individuals. The best individuals are chosen among the parents and the children to form the new generation. The algorithm continues to run until the generation number exceeds the maximum number set by the user.

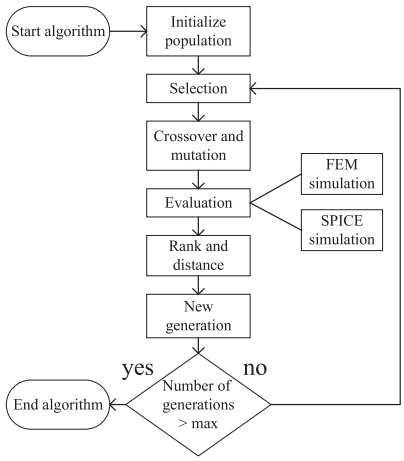


Fig. 8. Flow chart for the genetic algorithm used for the design optimization.

TABLE IV
USE CASE FOR THE OPTIMIZATION ALGORITHM

V_{IN}	$V_{out,min}$	$V_{out,max}$	$P_{out,max}$	Insulation
48 V	20 V	25 V	$\geq$10 W	1.6 mm FR4

For the optimization procedure, a suitable use case is constructed that is based on the schematic diagram shown in Fig. 1 and which is summarized in Table IV. An auxiliary power supply provides power to a switching unit that consists either of a module in an MMC converter or several series-connected switches. Regardless of the switching unit, the power required would be similar at approximately 10 W [8, pp. 121–132]. The input voltage is set to a common dc bus voltage of 48 V, while the output voltage constraint is set according to the driving voltage needed for the switches. For SiC MOSFETs, typical driving voltages are in the range of -5 to 0 V negative driving voltage to 15 to 20 V positive driving voltage. Hence, the output voltage constraint is set between 20 and 25 V. As insulation material, FR4 material is used with a thickness of 1.5 mm. This criterion is set to facilitate the production of the simulated transformers for prototyping. Future optimizations could include further details regarding the insulation scheme. The algorithm is launched with 100 individuals that are developed over 125 generations. Using a single processor, the simulation is carried out and the simulation time is approximately 3.5 days. The development of the optimization with increasing generation number and the final generation are shown in Fig. 9(a) and (b).

The 100 individuals forming the Pareto front achieves a peak system efficiency ranging from 78% to above 87% with a transformer radius of approximately 10 to 17 mm. It is observed that the efficiency obtained by the optimization algorithm give substantially higher values than that for the initial prototype reported in Section III. The individuals are investigated in terms of average values of key parameters to identify the design trends that result in high efficiency. These values are presented in Table V. Common for all individuals is a transformer turns ratio of 4:4, which maximizes transformer coupling as discussed in Section II. Hence, the voltage conversion from 48 V input to

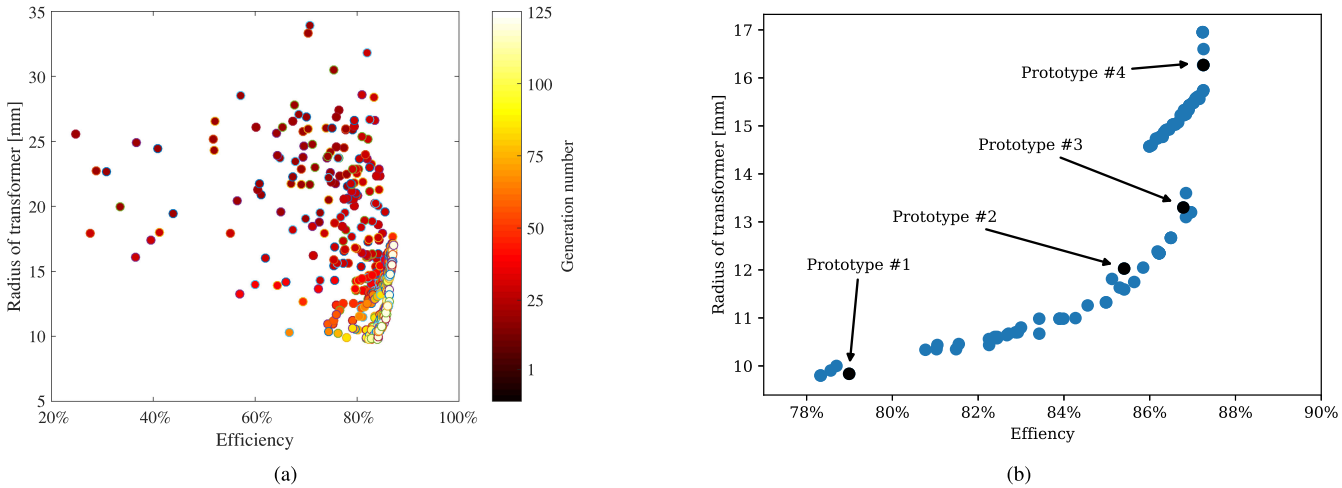


Fig. 9. Developed and identified Pareto front using the genetic algorithm. (a) Development over several generations. The later generations move down right and form a Pareto front. (b) Last generation showing the Pareto front and the realized prototypes.

TABLE V
AVERAGE VALUES OF KEY PARAMETERS OF THE PARETO FRONT THAT IS PLOTTED IN Fig. 9(b)

$N_{prim} : N_{sec}$	w_0 MHz	w_{sec} MHz	L_s nH	L_{prim} nH	L_{sec} nH	C_p pF	C_s pF	C_{rect} pF	coupling
4 : 4	7.28	10.64	460	419	431	1049	1310	540	0.62

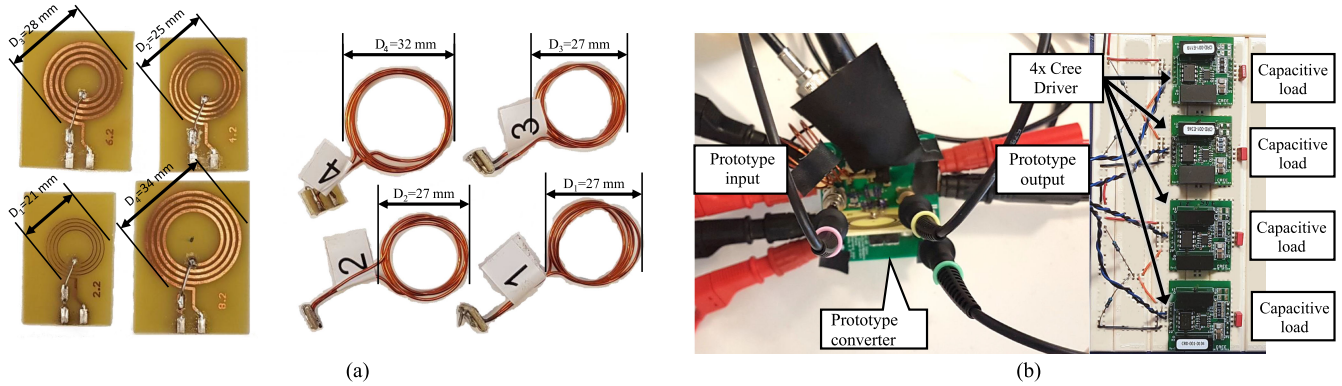


Fig. 10. (a) Transformers and series inductors for the four prototypes used in the experimental validation. (b) Photo of prototype 4 and the load on the output consisting of four Cree SiC MOSFET drivers (CRD-001).

20–25 V output is achieved by different characteristics. It can be seen that the average resonance frequency of the rectifier, ω_{sec}, is approximately 1.5 times higher than the operating frequency, thus increasing the voltage transfer function toward the peak value. Again, this is in line with the investigations in Section II. Since the turns ratio is the same for all individuals, the increased transformer size is mainly due to wider windings that result in lowered track resistance. In turn, the transformer and system efficiency increases. Moreover, the average resonance frequency of the primary-side series resonance, ω_0, is slightly higher than the operating frequency. This is contrary to the circuit design derived from the analytic approach, where the resonance frequency is set to the operating frequency. An important finding that effects the converter implementation is that the inductance of the transformer can be decreased compared to the existing design method in the literature [27].

V. EXPERIMENTAL VALIDATION

From the final generation, several individuals are chosen to verify the simulation results. A multitude of prototypes serves to show that the simulation model is in fact a good representation for the actual circuit behavior. Four individuals are chosen based on their total distance from all other individuals, excluding the outliers on each side. Similarly to the initial prototype, the air transformers are made on PCBs which are seen, together with the series inductors, L_s, in Fig. 10(a). Each series inductor was manually tuned to obtain the targeted inductance value.

TABLE VI
COMPARISON OF COMPONENT VALUES BETWEEN SIMULATION AND THE EXPERIMENTAL SETUP

	Experimental value (error %)							
Prototype	#1		#2		#3		#4	
L_s $[nH]$	468	(1%)	501	(1%)	502	(2%)	469	(2%)
L_{prim} $[nH]$	395	(3%)	392	(5%)	388	(6%)	561	(4%)
L_{sec} $[nH]$	395	(4%)	380	(6%)	377	(6%)	573	(5%)
coupling	0.57	(1%)	0.64	(-1%)	0.68	(<1%)	0.71	(-1%)
C_p $[pF]$	724	(<1%)	1036	(<1%)	1075	(4%)	1170	(3%)
C_s $[pF]$	1347	(<1%)	1379	(-1%)	1376	(-1%)	1199	(-1%)
C_{rect} $[pF]$	859	(2%)	808	(<1%)	813	(1%)	232	(-1%)
$C_{coupling}[pF]$ (sim / exp)	4.5 / 7.6		8.1 / 11.8		10.7 / 14.8		13.8 / 18.3	

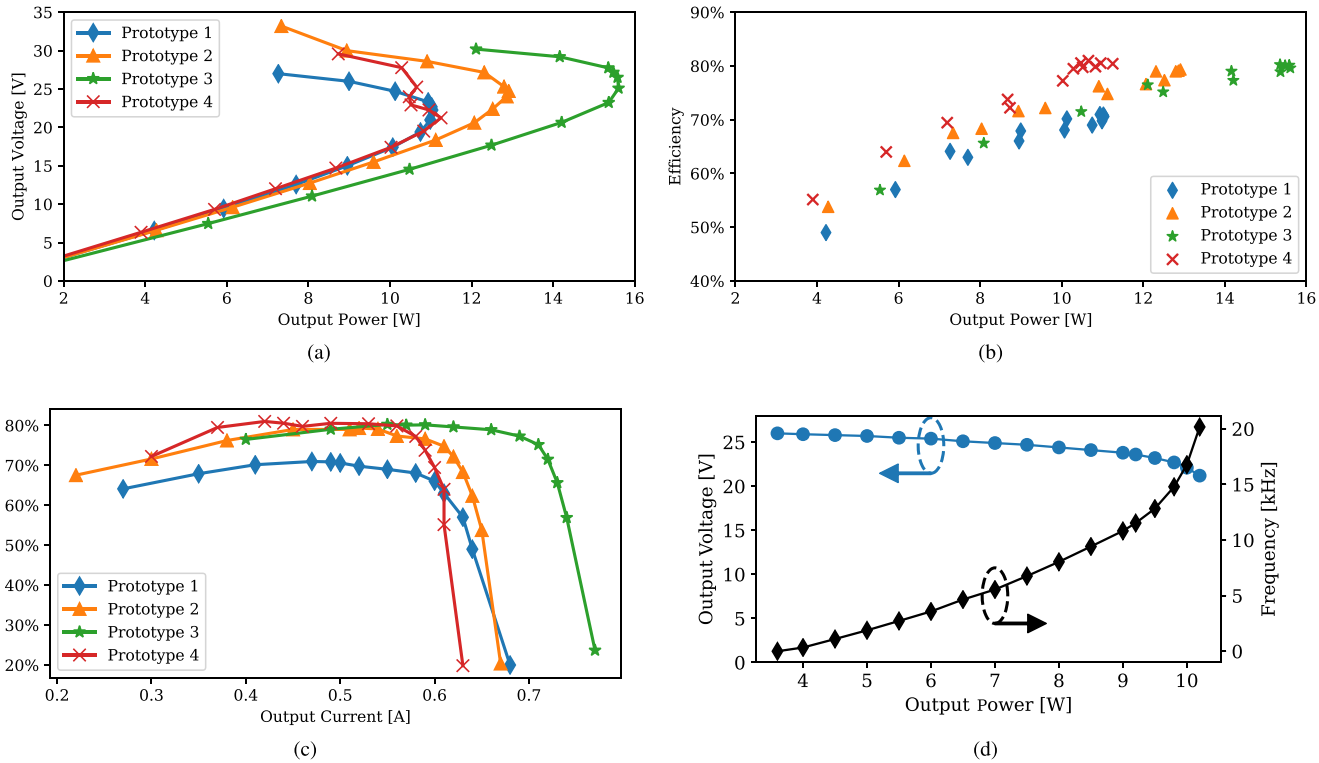


Fig. 11. Experimental results from the four prototypes. (a) Efficiency as a function of output power for varying load resistance. (b) Output voltage variation as a function of output power. (c) Efficiency as a function of the output current. (d) Load line of the prototype #4 while powering four Cree SiC MOSFET drivers with capacitive loads, where the output power varies with the driver switching frequency.

This method is time consuming, however, a more industrial product could use PCB printed or three-dimensional printed toroids [46], [47]. An added benefit of the toroid structure will be the containment of the field inside the structure. The measured component values and the error compared to the simulated values are shown for all four prototypes in Table VI. The inductance values are within 6% deviation from the simulated value, while the coupling coefficient is within $\pm 1\%$. The capacitance values of the prototypes have little deviation compared to simulation as the capacitors are selected based on their measured capacitance value using the impedance analyzer.

The efficiency and output voltage of the four prototypes are shown in Fig. 11. Fig. 11(a) shows the change in the output voltage as a function of the output power and the characteristic nose curve is observed. The minimum output power or current is limited thermally during testing as the inverter case temperature comes close to its maximum allowable value when operating without a heatsink. Fig. 11(b) shows the efficiency as a function of the output power. However, this way of presenting the efficiency leads to double points per output power. To present the data without double points, the efficiency is plotted as a function of the output current in Fig. 11(c), where zero current

TABLE VII
EVALUATION OF THE ISOLATION VOLTAGE AND TRANSFORMER GEOMETRY COMPARED TO OTHER PUBLISHED WORK

Publication	Gap distance [mm]	Radius - ferrite or winding [mm]	Radius - dielectric [mm]	Peak efficiency	Insulation voltage [kV_{peak}]	Insulation material
[16]	1.0	7	50	70 %	40	Teflon
[10]	13	40	86	90 %	95	Polyurethane
This work	1.5	10–17	-	71–81 %	*32 *48 *80	FR4 Polyesterimide Teflon

* Peak insulation voltage is estimated using the experimental data on breakdown voltages for different materials and material thicknesses found in [16].

equals an open-circuit condition and the maximum value equals a short-circuit condition.

The maximum efficiency is measured to be 71.0%, 79.3%, 80.3%, and 81.0%, ordered according to the prototype number, and hence, with increasing transformer size. All prototypes are able to supply over 10 W, with prototype #3 being able to supply more than 15 W. This fits well with the previously discussed application of the auxiliary power supply. Compared to [15] and [16], the proposed designs have the same or better efficiency while increasing both the output power and the air gap height. The latter results in an increased insulating voltage of the isolated auxiliary power supply. The measured efficiency of the prototypes are lower than the values found in simulation (79.0%, 85.4%, 86.8%, and 87.3%). The difference in efficiency between simulation and measured for prototypes #2–4 is approximately 6–7%. As shown with the initial prototype, increased losses should be expected for the experimental setup due to the modeling of the inverter. As discussed in Section III, the simulation model consistently underestimated the losses in the inverter due to the phenomena of dynamic ON-resistance of GaN HEMTs. The additional inverter losses measured for all prototypes accounts for the missing percentage points in the measured efficiency compared to the simulated efficiency. The larger efficiency gap of the prototype #1 is likely related to the thin track width of the prototype #1. The track width of this individual is only 0.2 mm, making the performance sensitive to small variations in track width due to the manufacturing resolution of the in-house etching technique. This is verified as the measured resistance values of the PCB transformer are found to be 15% higher than simulated. The converters appear to loose their soft switching operation when the load goes toward an open circuit. Other practical converter constraints like nose curve shape, inverter temperature, and soft switching operation should be included in future optimizations either as separate simulations or by simplified analytic expressions.

The main difference between prototypes #1–3 is the track width, which only slightly decreases the transformer inductance and winding resistance while the coupling slightly increases. Prototype #1 differs from the other prototypes by having a resonance of the primary side higher than the operating frequency (8.65 MHz), whereas prototypes #2–4 are close to the operating frequency (6.99, 6.85, and 6.79 MHz, respectively). For the secondary side, prototypes #1–3 are similar (8.18, 8.57, 8.58 MHz, respectively), whereas the prototype #4 has a larger resonance frequency of 11.54 MHz. The maximum output power and variations in the output voltage with load resistance are observed to change for different design configurations. Desired converter characteristics could be added to the optimization algorithm to further develop the design space in the desired direction. It is hypothesized that the shapes of the nose curves of prototypes #1–3 are similar due to similar impedance values on the rectifier side. Their differences in resistance and coupling give the premise for the maximum power output and efficiency.

The coupling capacitance of the transformer is indirectly included in the optimization algorithm since the transformer area is minimized. The coupling capacitance was modeled using FEMM and measured experimentally for the four prototypes. Simulated and measured values are given in Table VII. From measurements, it is found that the coupling capacitances are in the range of 8–14 pF, which is higher than compared to the literature [15], [16]. Part of this capacitance is related to the higher value of ϵ_r of FR4 that is used as the dielectric material in this work. All measured values are 3–5 pF higher than the simulated values due to the simplified geometry of the simulation model and possibly the exact value of ϵ_r for the prototypes. In view of these aspects, the measured values correspond well to the simulation. The coupling capacitance appears to be proportional to the area of the transformer windings, as can be expected. The optimization algorithm could be modified by adding a simulation of the coupling capacitance to calculate this value directly. Although, minimization of the transformer size, in particular, the surface area, also minimizes the coupling capacitance. Similarly, increasing the distance between the primary and secondary side also decreases the coupling capacitance.

The prototype 4 is tested in a setup that is similar to the target application. The setup is shown in Fig. 10(b), where the prototype power supply provides power to four Cree SiC MOSFET drivers (CRD-001). Each driver is loaded with a 220 nF capacitor, which is equivalent to the gate capacitance of a modern 3.3 kV SiC MOSFET high power module. The switching frequency of the driver load is varied from 1 to 20 kHz to vary the loading of the prototype converter. The resulting load line of the prototype converter is shown in Fig. 11(d). A drop in the output voltage from 26 to 21.2 V is observed over the whole power range. However, the output voltage at 9 W is only 23.8 V, a voltage drop of less than 10%.

Based on the transformer geometry of the experimental prototypes, a comparison is made with similar works regarding the insulation voltage. The comparison is summarized in Table VII. For this work, the breakdown voltage of the insulation barrier is estimated using published experimental data for different materials and material thicknesses combined with the gap distances between the primary and secondary side [16]. For the prototypes, the insulating material is FR4, which results in a breakdown voltage of 32 $\mathrm{kV_{peak}}$. If polyesterimide or Teflon material of 1.5-mm thickness is used instead, breakdown voltages of approximately 48 and 80 kV are obtained. Furthermore, the dielectric constant of these materials, 3.5 [48] and 2.0 [49], respectively, would result in a decreased coupling capacitance down to a half with respect to the case of FR4. This results in coupling capacitances in the range of 4–9 pF for the prototypes in this article.

VI. Conclusion

This article presented the design and optimization of a suitable topology for an isolated dc–dc auxiliary power supply with high isolation voltage and low coupling capacitance. The converter consisted of a GaN HEMT inverter operating at 6.78 MHz, an *LCC* resonance tank, a coreless transformer, and a class-E low dv/dt rectifier. In regard to the application, the converter was suitable for supplying gate drivers in medium-voltage converters. A design methodology was developed, however, SPICE investigations showed that optimal designs might lie outside the validity of the design equations. In particular, the rectifier showed preferential characteristics when designed with a resonance frequency higher than the operating frequency ($\omega_{\mathrm{res}} \geq 1.6$); the output voltage regulation improved and the inductor size was reduced. A virtual prototyping tool was developed based on a genetic algorithm that was used in an holistic optimization of the converter. The optimization algorithm maximized the converter efficiency while minimizing the coupling capacitance. Using the developed Pareto front, the best performing prototype exhibited a peak efficiency of 81% when supplying 15 W of power. The prototypes all had smaller transformer sizes, and hence, lower coupling capacitance compared to the existing design method in the literature [27]. Moreover, the coupling capacitances of the prototypes were found through measurement in the range of 7–18 pF. However, if a more suitable dielectric material like Teflon was used, the coupling capacitance was halved and coupling capacitances below 10 pF could be obtained. At the same time, using Teflon as insulation material could increase the insulation breakdown voltage up to 80 kV.

Appendix

This section shows a numerical example using the analytical design method given in Section II. For the example, the input voltage is set to 48 V, while the desired output voltage is chosen to 20 V for the maximum load requirement of 10 W. First, the rectifier passive components are found according to (1)–(3)

$$R_{\mathrm{load,min}} = \frac{(20\ \mathrm{V})^2}{10\ \mathrm{W}} = 40\ \Omega$$

$$L_{\mathrm{sec}} = \frac{40\ \Omega}{\omega_0 \cdot 0.3884} = 2.418\ \mu\mathrm{H}$$

$$C_{\mathrm{rect}} = \frac{1}{\omega_0^2 L_{\mathrm{sec}}} = 0.2279\ \mathrm{nF}$$

where ω_0 equals $2\pi \cdot 6.78\mathrm{MHz}$ and the values of Q_r and M_V are given as 0.3884 and 0.3684, respectively, in [27] for the maximum output-power capability of the rectifier. Then, the input voltage is found using (4) as

$$V_m = \frac{20\ \mathrm{V}}{0.3684} = 54.29\ \mathrm{V}.$$

In the following step, C_p is found. However, this requires that the coupling factor of the transformer is known. For the example, it is assumed that the factor is 0.6. Furthermore, L_{prim} is assumed equal to L_{sec}. From (13), C_p becomes

$$C_p = \frac{\pi \cdot 54.29\ \mathrm{V}}{\sqrt{2} \cdot \omega_0^2 \cdot 0.6 \cdot 2.418\ \mu\mathrm{H} \cdot 48\ \mathrm{V}} = 0.9545\ \mathrm{nF}.$$

The corresponding I_{prim} is found to be 0.88 A. Using (11), L_s evaluates to

$$L_s = \frac{1}{\omega_0^2 \cdot 0.9545\ \mathrm{nF}} = 0.577\ \mu\mathrm{H}.$$

The values of L_i is set as $0.814 \cdot L$ [27]. With a target switching current of -1.25 A, the series capacitor is calculated according to (17) as

$$C_s = \frac{0.9545\ \mathrm{nF}}{\frac{\pi \cdot 24.59\ \Omega \cdot (-1.25\ \mathrm{A})}{\sqrt{2} \cdot 48\ \mathrm{V}} + \frac{2.418\ \mu\mathrm{H}}{0.577\ \mu\mathrm{H}} + \frac{-46.27\ \Omega}{24.59\ \Omega} - \frac{\pi^2}{8}} = 0.471\ \mathrm{nF}.$$

The component values are evaluated using SPICE simulations for modeling the reference circuit [27]. Moreover:

1) the input source, V_{in}, is a trapezoidal voltage that changes between 0 and 48 V with rise and fall times of 10 ns;
2) the diode has no junction capacitance, and is modeled with R_{on} and R_{off} of 50 and 10 MΩ, respectively;
3) all passive components have zero resistance.

For the design case, the output voltage of the full circuit evaluates to 21.11 V compared to 20.57 V for the reference circuit, an error of 2.6%. The error for changing transformer coupling is shown in Fig. 12. The error in the output voltage is small for a coupling factors up to approximately 0.7. Above this value, the second harmonic generated by the rectifier influences the converter behavior and the calculations become less accurate. Nevertheless, the coupling factor of coreless transformers are usually lower than 0.7. Additionally, it is seen that the switching current also has a slight offset meaning that tweaking of the C_s value is likely needed for the final converter design. Moreover, the error between the positive and negative current is asymmetric due to the second harmonic content in the inverter current.

Fig. 13 shows the behavior of the rectifier output with changing load condition. The increasing voltage and power with increasing load resistance are characteristics of a current source. In many cases, a voltage source behavior is preferred over the current source behavior.

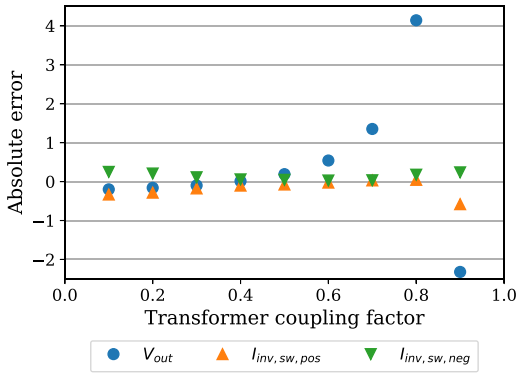


Fig. 12. Absolute error between the proposed topology and the reference circuit for the output voltage and the inverter current at the switching instant, $I_{\mathrm{inv,sw}}$, for either falling (*pos*) or rising (*neg*) edge of the inverter output voltage.

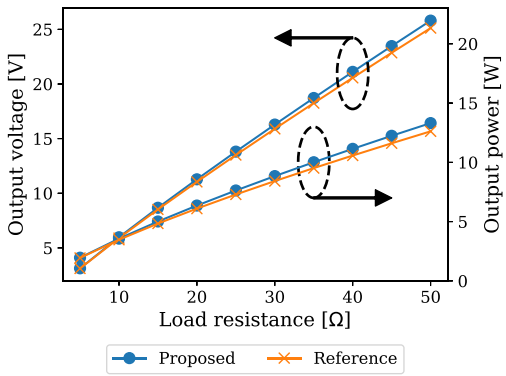


Fig. 13. Inverter output voltage and power as a function of load resistance.

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