# Novel High Step-Up Soft-Switching DC–DC Converter Based on Switched Capacitor and Coupled Inductor

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***Abstract*—A novel high step-up dc–dc converter with coupled inductor and switched capacitor is proposed in this article. The proposed converter adopts capacitors charged in parallel and discharged in series with a coupled inductor to achieve high step-up voltage gain. By utilizing the energy stored in the leakage of the coupled inductor, both of the switches can realize zero-voltage switching, which can reduce switching loss and improve efficiency. In addition, the voltage stress of the switches and diodes are also reduced. Therefore, low voltage components can be utilized and the input current is continuous. The operating principle, steady-state, and parameter design are shown in details, and a 100-W experimental prototype with 25-V input voltage and 380-V output voltage is established in the laboratory to verify the feasibility of the proposed converter, and the highest efficiency is 96.21%.**

***Index Terms*—Coupled inductor, dc–dc converter, high voltage gain, switched capacitor, zero voltage switching (ZVS).**

## I. Introduction

TRADITIONAL fossil energy such as coal and oil is no longer able to meet growing demand due to its non-renewability. Moreover, excessive use of fossil energy has caused great pollution to the environment [1], [2]. Therefore, high efficiency especially renewable energy systems are more and more widely utilized to provide electric energy [3]–[5]. However, the solar photovoltaics (PV) and fuel cells sources and are both low-voltage sources, which need high step-up dc–dc converter as the front-stage to boost low voltage to the high bus voltage.

Isolated converters can achieve a high voltage gain by adjusting the transformer ratio. However, a large turn ratio results in a complex transformer structure and a large transformer volume. Meanwhile, the efficiency of the converter is greatly affected by the voltage spikes caused by leakage inductor and high switch voltage stress [6]–[8]. Thus, non-isolated step-up converters are widely adopted.

Among the non-isolated dc–dc converters, conventional boost converters can step-up voltage by increasing the duty ratio of the switch. However, the step-up ability is greatly limited by parasitic resistor of switch and inductor. Meanwhile, the high duty ratio leads to a large current ripple of the inductor, a large turn-off current and high voltage stress of the switch, which results in large conduction loss and switching loss. Meanwhile, the reverse recovery problem of the output diode is also serious due to a large current of the output diode [9], [10]. The converter based on coupled inductor is also a very popular choice for a high-voltage gain converter. They can achieve high voltage gain by adjusting the ratio of the coupled inductor. However, the leakage inductor of the coupled inductor causes serious power loss and voltage spike during switching transition. In order to overcome the problems, a passive clamp coupled inductor converter in [11] is proposed. Although a simple diode-capacitor clamp circuit is adopted to recycle the energy stored in the leakage inductor, the voltage stress of the output diode is very high. In [12], a coupled inductor converter with an active clamp circuit is proposed. However, the number of the components greatly increases.

For the switched capacitor converters, the high voltage gain can be achieved by charging the switched capacitors in parallel and discharging in series. However, the voltage gain of the switched capacitor converter is closely related to the circuit structure. When the required voltage gain is high, a large number of cascaded switched capacitor units are required, which undoubtedly increases the complexity of the circuit [13]–[15]. To get a high voltage gain with less components, the switched capacitor converters combined with a coupled inductor are presented in [16] and [17]. These converters can realize high voltage gain and the voltage stress of the switch is low. However, these converters cannot achieve soft switching. In [18], a passive snubber circuit is given, which provides zero voltage switching (ZVS) and zero curent switching (ZCS) for the switches. In the snubber circuit, additional coupled inductor, capacitor, and diode are required, which significantly increases the number of components.

In this article, a novel soft-switching, high voltage gain, and high efficient converter with low voltage stress is proposed, as

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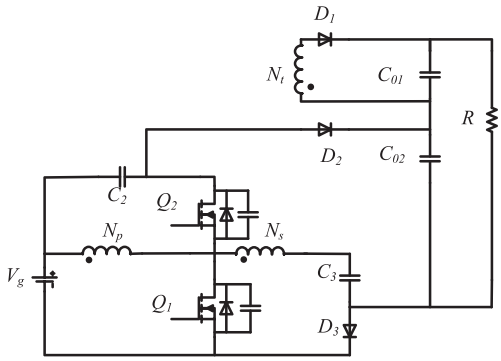


Fig. 1. Circuit diagram of the proposed converter.

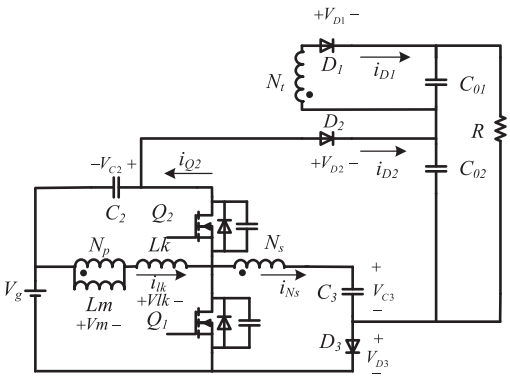


Fig. 2. Equivalent diagram of the proposed converter circuit.

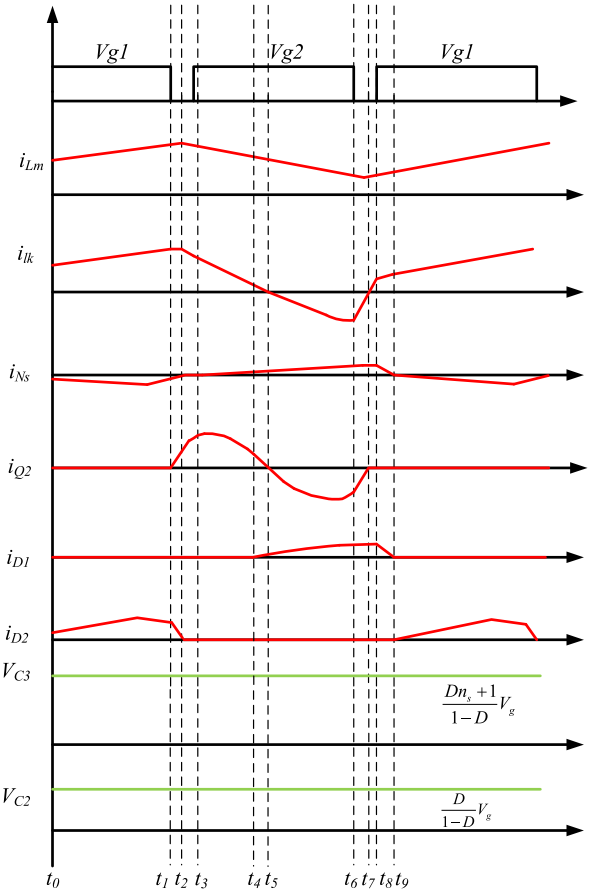


Fig. 3. Waveform diagram of the main devices.

shown in Fig. 1. Thus, low ON-state resister MOSFETs can be selected, which results in a reduced conduction loss and the efficiency can be significantly improved. In this converter, the leakage inductor energy of the coupled inductor is not used to improve the voltage gain as in [19], but is used to provide the ZVS energy for the switches. Thus, both of the switches are able to achieve ZVS. This helps to reduce the switching loss and work at a higher switching frequency with high efficiency. A high operating frequency is conductive to improve the power density by reducing the size of magnetic components. In addition, the capacitor $C_2$ and the switch $Q_2$ can also work as an active clamp circuit to suppress voltage spike of $Q_1$. Then, the input current of the proposed converter is continuous, which is very important for PV applications.

This article is organized as follows: Section II analyzes the operation modes of the proposed converter. Section III presents a steady-state analysis, voltage stress calculation, and characteristics comparison. The experimental results of the prototype are given and discussed in Section IV. Finally, Section V concludes this article.

## II. Operation of the Proposed Converter

The equivalent circuit of the proposed converter is shown in Fig. 2, where the coupled inductor is represented by an ideal transformer with a turn ratio of $N_p : N_s : N_t$ and a magnetizing inductor $L_m$ as well as the primary leakage inductor $L_{lk}$. The converter consists of two switches, three diodes, and four capacitors. The body diode of the switch $Q_2$ conducts before $Q_2$ turning ON, therefore, $Q_2$ can realize ZVS naturally. The energy stored in the leakage inductor is used to realize ZVS for the switch $Q_1$. Both of the switches can realize ZVS, which help to reduce the switching loss and ensure operating at a higher switching frequency with high efficiency. In addition, the capacitor $C_2$ and the switch $Q_2$ can also work as active clamp suppressing the turn-OFF voltage spike of $Q_1$.

In order to simplify the analysis of the circuit, some assumptions are made as follows.

1) All the capacitors are large enough, hence, their voltages can be seen as constant during one switching period.
2) All the power devices are ideal and the ON-resistance and forward conduction voltage are ignored.
3) The turn ratio of the coupled inductor 1: $n_s : n_t$ is defined as $N_p$:$N_s : N_t$ and the coupled coefficient $k$ is equal to $L_m/(L_m + L_k)$.

### A. Operating Principle

The theoretical waveform diagram of the converter is shown in Fig. 3 based on the aforementioned assumptions. In the waveform, $V_{g1}$ and $V_{g2}$ are the gate signals of the switch $Q_1$ and $Q_2$, respectively. There are nine operating modes during one switching period and simplified equivalent circuits for each

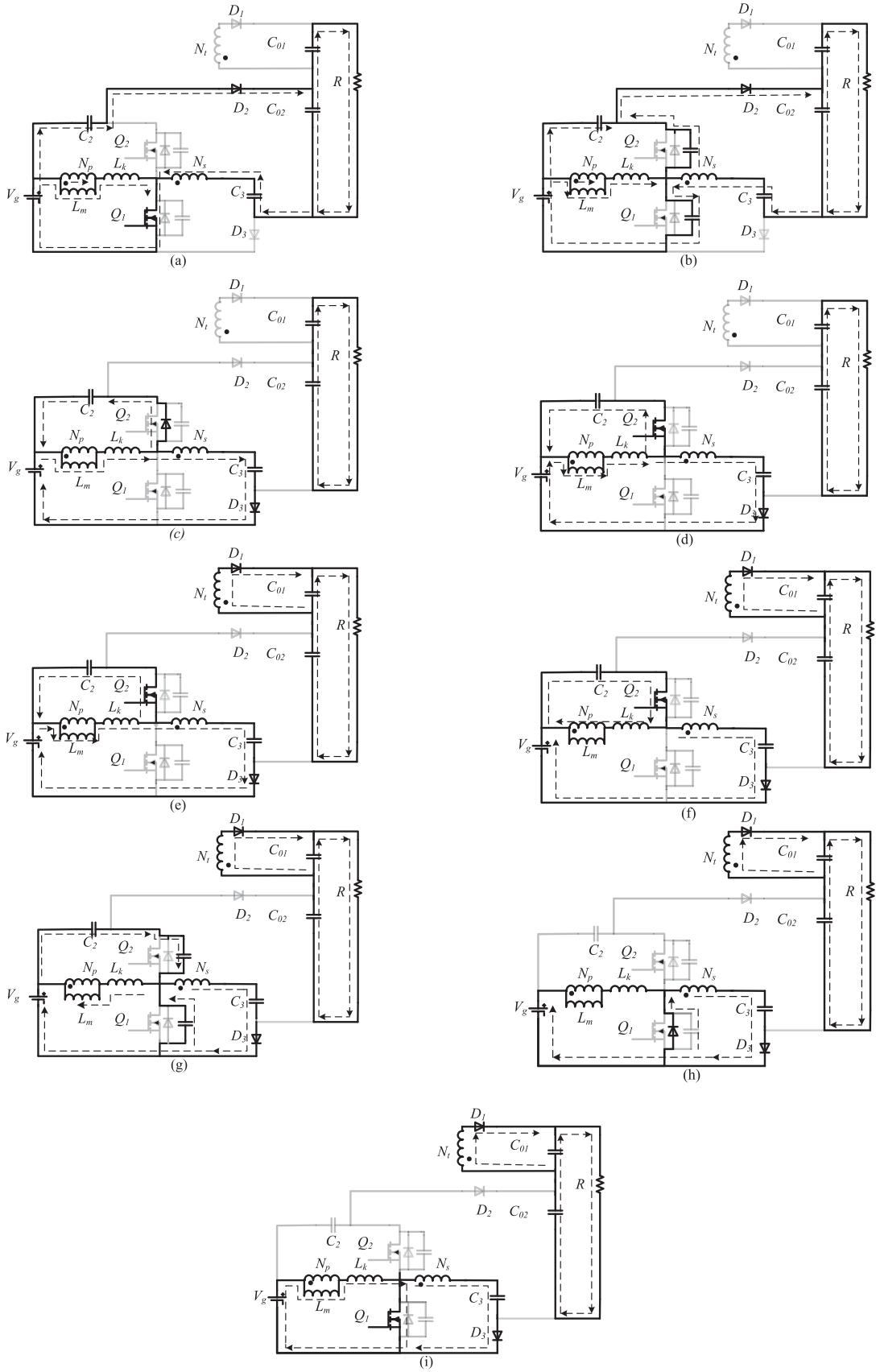


Fig. 4. Different modes of the proposed converter during one switching period. (a) Mode 1 ($t_0$ – $t_1$). (b) Mode 2 ($t_1$ – $t_2$). (c) Mode 3 ($t_2$ – $t_3$). (d) Mode 4 ($t_3$ – $t_4$). (e) Mode 5 ($t_4$ – $t_5$). (f) Mode 6 ($t_5$ – $t_6$). (g) Mode 7 ($t_6$ – $t_7$). (h) Mode 8 ($t_7$ – $t_8$). (i) Mode 9 ($t_8$ – $t_9$).

mode are given in Fig. 4(a)–(i). The operating modes are described as follows.

*Mode 1 ($t_0$ – $t_1$):* In this mode, the switch $Q_1$ is turned ON while the switch $Q_2$ is turned OFF. Diode $D_2$ is in conduction while $D_1$ and $D_3$ remain OFF. The current-flow path is shown in Fig. 4(a). The input voltage source $V_g$ charges the magnetizing inductor $L_m$ and leakage inductor $L_{lk}$. The current $i_{Lm}$ of magnetizing and current $i_{lk}$ of leakage inductor increase linearly. Meanwhile, the input voltage source $V_g$, $C_2$, $C_3$, and the secondary winding are in series to charge the output capacitor $C_{02}$.The output capacitor $C_{01}$ supplies energy to the load. The current of magnetizing inductor and current of leakage inductor can be expressed as

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_{Lm}}{L_m}(t - t_0) \tag{1}$$

where

$$V_{Lm} = \frac{L_m}{L_m + L_k} V_g = kV_g \tag{2}$$

$$i_{Lk}(t) = i_{Lk}(t_0) + \frac{V_g - V_{lm}}{L_k}(t - t_0). \tag{3}$$

The voltage of output capacitor $C_{02}$ can be derived as follows:

$$V_{C02}(t) = V_{C3}(t) + V_{Ns}(t) + V_g(t) + V_{C2}(t). \tag{4}$$

*Mode 2 ($t_1$ – $t_2$):* This mode starts at $t = t_1$, when the switch $Q_1$ is turned OFF. The current of leakage inductor start to charge and discharge the parasitic capacitors of $Q_1$ and $Q_2$, respectively. The drain–source voltage of $Q_1$ increases from 0 to $V_g + V_{C2}$ and the drain–source voltage of $Q_2$ drops from $V_g + V_{C2}$ to 0. The drain–source voltage $V_{ds.Q1}$ and leakage inductor current $i_{lk}$ are given by

$$V_{ds.Q1} = V_g(1 - \cos(\omega_1(t - t_1))) + i_{lk}(t_1) Z_1 \sin(\omega_1(t - t_1)) \tag{5}$$

$$i_{lk}(t) \approx i_{lk}(t_1) \cos(\omega_1(t - t_1)) + \frac{V_g - V_{\text{ds.}Q1}}{Z_1} \sin(\omega_1(t - t_1)) \tag{6}$$

where $\omega_1 = 1/\sqrt{2C_{\text{oss}}(L_m + L_k)}$ and $Z_1 = 1/\sqrt{(L_m + L_k)/2C_{\text{oss}}}$.

The input voltage source, $C_2$, $C_3$, and the secondary winding continue to charge the output capacitor $C_{02}$ in series. The output capacitor $C_{01}$ supplies energy to the load. At the end of the mode, $D_2$ turns OFF naturally.

*Mode 3 ($t_2$ – $t_3$):* While the current $i_{D2}$ achieve zero, this mode starts. At the same time, the drain–source voltage of $Q_1$ reaches to $V_g + V_{C2}$ and the body diode of the switch $Q_2$ start to conduct. The voltage spike of the switch $Q_1$ can be absorbed by the capacitor $C_2$. The magnetizing inductor $L_m$, leakage inductor $L_{lk}$, and the switched capacitor $C_2$ form a resonant circuit and the switched capacitor $C_2$ start to charge, at the same time, the switched capacitor $C_3$ also starts to charge, as shown in Fig. 4(c). Charging current of the switched capacitor $C_2$ can be calculated as follows:

$$i_{C2}(t) \approx i_{lk}(t_2) \cos(\omega_2(t - t_2)) + \frac{V_{Lk}(t)}{Z_2} \sin(\omega_2(t - t_2)) \tag{7}$$

where $\omega_2 = 1/\sqrt{C_2(L_m + L_k)}$ and $Z_2 = 1/\sqrt{(L_m + L_k)/C_2}$. In order to achieve ZVS for the switch $Q_2$, it should be turned ON before the direction of resonant current $i_{c2}(t)$ reverses.

*Mode 4 ($t_3$ – $t_4$):* At $t_3$, the gate signal for $Q_2$ is high. Before $t_3$, the body diode of the switch $Q_2$ has conducted. Therefore, the switch $Q_2$ turns ON under the ZVS condition. The paths of the currents are shown in Fig. 4(d). The input voltage source, the magnetizing inductor $L_m$, leakage inductor $L_{lk}$, and the secondary winding are in series to charge $C_3$. Meanwhile, the magnetizing inductor $L_m$ and leakage inductor $L_{lk}$ charge $C_2$. The output capacitor $C_{01}$ and $C_{02}$ supply energy to the load.

*Mode 5 ($t_4$ – $t_5$):* While the diode $D_1$ conducts, this mode starts. The input voltage source, the magnetizing inductor $L_m$, leakage inductor $L_{lk}$, and the secondary winding continue to charge $C_3$ in series. At the same time, the magnetizing inductor $L_m$ and leakage inductor $L_{lk}$ charge $C_2$.

*Mode 6 ($t_5$ – $t_6$):* While $i_{lk}$ crosses zero, this mode starts. $D_1$ and $D_3$ remain ON. During this interval, the current direction of $i_{lk}$ changes. The energy stored in the switched capacitor $C_2$ charges the magnetizing inductor $L_m$, leakage inductor $L_{lk}$. At the same time, the winding $N_s$ and $N_t$ charge the switched capacitor $C_3$ and the output capacitor $C_{01}$, respectively. This mode ends when the switch $Q_2$ is turned OFF.

*Mode 7 ($t_6$ – $t_7$):* The mode starts at $t_6$, when the switch $Q_2$ is turned OFF. At this point, the leakage inductor $L_{lk}$ and the parasitic capacitors of the switch $Q_1$ and $Q_2$ form a new resonant circuit and the parasitic capacitor of the switch $Q_1$ starts to discharge, as shown in Fig. 4(g). At the same time, the parasitic capacitor of the switch $Q_2$ starts to charge. Due to the parasitic capacitor of the switch is very small, the drain–source voltage of $Q_1$ decreases rapidly. The drain–source voltage of $Q_1$ can be derived as follows:

$$V_{ds.Q1}(t) \approx V_d - (V_d - V_{ds.Q1}(t)) \cos(\omega_3(t - t_6)) + i_{lk}(t_6) Z_3 \sin(\omega_3(t - t_6)) \tag{8}$$

where $V_d = V_g + ((V_g - V_{C3}(t))/(1 + n_s))$, $\omega_3 = 1/\sqrt{2C_{\text{oss}}L_k}$ and $Z_3 = 1/\sqrt{L_k/2C_{\text{oss}}}$.

The mode ends when the drain–source voltage of $Q_1$ becomes zero. In order to realize ZVS of the switch $Q_1$, the energy stored in the leakage inductor at this mode should be greater than the energy stored in the parasitic capacitor of the switch $Q_1$. Therefore, the condition for $Q_1$ to achieve ZVS is as follows:

$$L_{lk} \geq \frac{C_{\text{oss}} V_{ds.Q1}^2(t_6)}{i_{Lk}^2(t_6)}. \tag{9}$$

*Mode 8 ($t_7$ – $t_8$):* When the parasitic capacitor of the switch $Q_1$ is fully discharged, this mode starts. At the same time, the body diode of the switch $Q_1$ conducts. To realize ZVS for $Q_1$, the gate signal $V_{g1}$ should be applied during this interval.

*Mode 9 ($t_8$ – $t_9$):* At $t = t_8$, the switch $Q_1$ is turned ON with ZVS. The magnetizing and leakage current start to increase linearly. The current of diode $D_1$ starts to decrease. This interval lasts until the current $i_{Ns}$ decreases to zero and changes its direction at $t_9$. Afterwards, the operation modes repeat again.

## III. Steady-State Analysis and Design of the Proposed Converter

### A. Voltage Gain of the Converter

In order to simplify the steady-state analysis, only modes 1, 4, 5, and 6 are considered and other modes during the deadtime are ignored. The non-ideal factors that affect the voltage gain mainly includes the leakage inductor of the coupled inductor, the parasitic resistor of the coupled inductor, the ON-state resistor of a switch, and the equivalent series resistor of a capacitor. In order to simplify the calculation, only the leakage inductor of the transformer is considered here, and the theoretical voltage gain is obtained as follows.

When the switch $Q_1$ is turned ON, the input voltage source $V_g$ charge the magnetizing inductor $L_m$ and leakage inductor $L_{lk}$. Meanwhile, the input voltage source, $C_2$, $C_3$, and the secondary winding are in series to charge the output capacitor $C_{02}$. Based on the Kirchhoff's voltage law, the equations can be written as follows:

$$V_g - V_{Lm} - V_{lk} = 0 \tag{10}$$

$$V_{C3} + V_{Ns} + V_g + V_{C2} = V_{C02} \tag{11}$$

$$V_{Ns} = n_s V_{Lm} \tag{12}$$

$$V_{Nt} = n_t V_{Lm} \tag{13}$$

$$\frac{V_{Lm}}{k} = \frac{V_{lk}}{1-k} \tag{14}$$

where $k$ is the coupling coefficient of a coupled inductor, which is equal to $L_m/(L_m + L_{lk})$. The ratio of a coupled inductor is $1 : n_s : n_t$. The directions of the voltage are shown in Fig. 2.

When the switch $Q_1$ is turned OFF and the switch $Q_2$ is turned ON. The switched capacitor $C_2$ and $C_3$ are charged in parallel. Based on the Kirchhoff's voltage law, the equations can be obtained as follows:

$$V_{C2} + V_{lk} + V_{Lm} = 0 \tag{15}$$

$$V_g - V_{Lm} - V_{lk} - V_{Ns} - V_{C3} = 0 \tag{16}$$

$$V_{Nt} + V_{Co1} = 0. \tag{17}$$

By applying the volt-second balance principle on $N_p$, $N_t$, and $N_s$, we obtain

$$\int_0^{DT} V_{Lm} dt + \int_{DT}^{T} V_{Lm} dt = 0 \tag{18}$$

$$\int_0^{DT} V_{Nt} dt + \int_{DT}^{T} V_{Nt} dt = 0 \tag{19}$$

$$\int_0^{DT} V_{Ns} dt + \int_{DT}^{T} V_{Ns} dt = 0. \tag{20}$$

Based on (10), (14), (15), and (18), (21) can be obtained as

$$V_{C2} = \frac{D}{1-D} V_g. \tag{21}$$

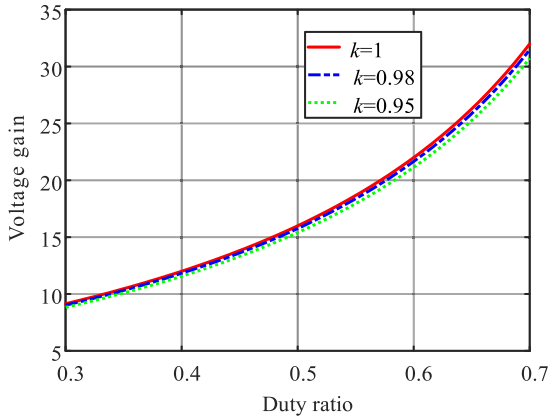


Fig. 5. Relationship between voltage gain, duty ratio, and coupling coefficient.

Based on (10), (14), (16), and (18), the voltage of the switched capacitor $C_3$ can be expressed as

$$V_{C3} = V_g + \frac{Dk(1/k + n_s)}{1-D} V_g. \tag{22}$$

Combining (13), (14), (17), and (19), the following equation can be calculated as:

$$V_{C01} = \frac{kDn_t}{1-D} V_g. \tag{23}$$

Combining (20)–(22), and (24) can be obtained as

$$V_{C02} = V_{C2} + V_g + V_{C3} = \frac{kn_s + 2}{1-D} V_g. \tag{24}$$

According to the aforementioned assumption, the output capacitor $C_{01}$ and $C_{02}$ are large enough; hence, their voltage is constant during one switching period. Thus, the output voltage is finally derived as follows:

$$V_{\text{out}} = V_{C01} + V_{C02} = \frac{kDn_t + kn_s + 2}{1-D} V_g. \tag{25}$$

The voltage gain is

$$M = \frac{V_{\text{out}}}{V_g} = \frac{kDn_t + kn_s + 2}{1-D}. \tag{26}$$

Fig. 5 shows the effect of the coupling coefficient of the coupled inductor on the voltage gain, where the turn ratio is set as 1:2:8. Obviously, the coupling coefficient of the coupled inductor has almost no effect on the voltage gain. In other words, the leakage inductor of the coupled inductor has almost no effect on the voltage gain. Thus, the voltage gain can be approximately calculated as

$$M = \frac{Dn_t + n_s + 2}{1-D}. \tag{27}$$

Fig. 6 shows the voltage gain versus duty ratio of the proposed converter and the converters in [20]–[24] under $k = 1$ and $n = 2$. As three winding of a coupled inductor is utilized, the proposed converter is able to get higher voltage gain than other converters in [20]–[24], in the case of using the same device and duty ratio. The proposed converter can achieve the same voltage gain by

TABLE I
COMPARISONS OF THE PROPOSED CONVERTER WITH [20]–[24]

| Topology | Proposed converter | Reference [20] | Reference [21] | Reference [22] | Reference [23] | Reference [24] |
|---|---|---|---|---|---|---|
| Voltage gain $M$ | $\frac{Dn_t+n_s+2}{1-D}$ | $\frac{(2-D)(1+n)}{1-D}$ | $\frac{2(1+nD)}{1-D}$ | $\frac{1+n+nD}{1-D}$ | $\frac{n(2-D)}{1-2D}$ | $\frac{2+nD}{1-D}$ |
| Switches count | 2 | 2 | 2 | 1 | 1 | 2 |
| Diodes count | 3 | 3 | 4 | 4 | 6 | 8 |
| Capacitor count | 4 | 4 | 2 | 4 | 7 | 5 |
| Inductor count | 1 | 1 | 1 | 1 | 2 | 2 |
| Voltage stress of switch | $\frac{V_g}{1-D}$ | $\frac{V_{in}}{1-D}$ | $\frac{(1+nD)V_{in}}{1-D}$ | $\frac{V_{in}}{1-2D}$ | $\frac{V_{in}}{1-2D}$ | $\frac{V_{in}}{1-D}$ |
| Voltage stress of output capacitors | Lower | Higher | Lower | Higher | Higher | Higher |
| Voltage stress of output diodes | $\frac{Dn_t}{1-D}V_g$ | $\frac{1+n}{1-D}V_{in}$ | $\frac{1+nD}{1-D}V_{in}$ | $\frac{n}{1-D}V_{in}$ | $\frac{(2n-2-nD)V_g}{1-2D}$ | $\frac{2+n(1+D)}{1-D}V_{in}$ |
| Soft switching | ZVS | Hard switching | Hard switching | Hard switching | Hard switching | ZCS |
| Efficiency | $\eta$ =96% $P_{out}$=100W | $\eta$ =93.5% $P_{out}$=160W | $\eta$ =91.1% $P_{out}$=250W | $\eta$ =95.03% $P_{out}$=200W | $\eta$ =90.5% $P_{out}$=250W | $\eta$ =94.55% $P_{out}$=400W |

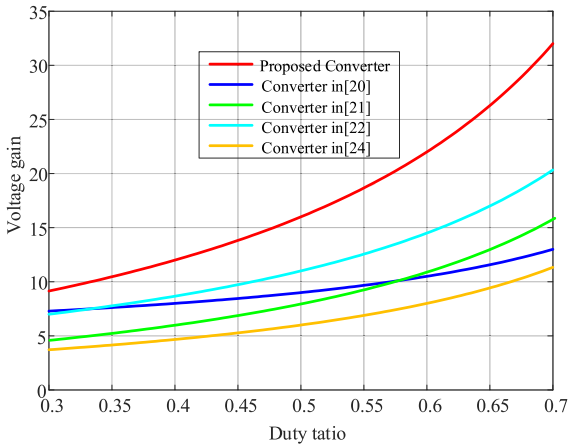


Fig. 6. Voltage gain versus duty ratio of the proposed converter, the converter in [20], the converter in [21], and the converter in [22].

using less turns ratio, which is beneficial to the reduction of the converter volume.

The other characteristics comparisons are shown in Table I. It can be clearly seen that the components' devices number of the proposed converter is almost the same as the converters in [20]–[22], and is less than the converter in [23] and [24]. The converter proposed in [20] and [24] has the same voltage stress of the switches as the proposed converter, but the voltage stress of the output diodes is higher than the proposed converter in this article. Both of voltage stress of switches and diodes in [21]–[23] is higher than the proposed converter. More importantly, soft switching cannot be achieved for switches in [20]–[23], which leads to a large switching loss. The efficiency of the converter in [20]–[23], can be severely affected by hard switching. Although the converter in [24] can realize ZCS, but the number of diodes is large, which leads to much diodes conduction loss. In addition, its two inductors occupy a large volume. In short, the proposed converter can achieve higher voltage gain and higher efficiency with the same or fewer devices.

### B. Voltage and Current Stresses

Ideally, referring to Fig. 4(a), the voltage stresses of $Q_2$, $V_{D1}$, and $V_{D3}$ are

$$V_{Q2} = V_g + V_{C2} = \frac{1}{1-D}V_g \tag{28}$$

$$V_{D1} = V_{\text{out}} - V_{C2} - V_{C3} - (n_s+1)V_g = \frac{Dn_t}{1-D}V_g \tag{29}$$

$$V_{D3} = V_{C02} - V_{C2} - V_g = \frac{n_s+1}{1-D}V_g. \tag{30}$$

Ideally, referring to Fig. 4(d) with the similar method, the voltage stresses of $Q_1$ and $V_{D2}$ are

$$V_{Q1} = V_g + V_{C2} = \frac{1}{1-D}V_g \tag{31}$$

$$V_{D2} = V_{C02} - V_{C2} - V_g = \frac{n_s+1}{1-D}V_g. \tag{32}$$

In addition, voltage stress on the switches $C_2$ and $C_3$ are given by

$$V_{C2} = \frac{D}{1-D}V_g \tag{33}$$

$$V_{C3} = \frac{(1+Dn_s)}{1-D}V_g. \tag{34}$$

By applying the amp-second balance principle of the output capacitors $C_{01}$, $C_{02}$, and switched capacitors $C_2$, $C_3$, it is clear that the average value of the current through the diodes $D_1$, $D_2$, and $D_3$ is equal to the output current. Therefore, the peak currents of diodes $D_1$, $D_2$, $D_3$ are given by

$$I_{D1(\text{peak})} = I_{D3(\text{peak})} = \frac{2V_{\text{out}}}{(1-D)R} \tag{35}$$

$$I_{D2(\text{peak})} = \frac{2V_{\text{out}}}{DR}. \tag{36}$$

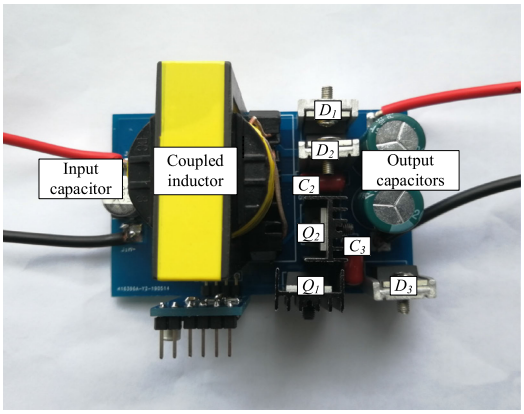


Fig. 7. Prototype photograph of the proposed converter (77 mm × 50 mm × 48 mm).

TABLE II
SELECTED PARAMETERS AND SPECIFICATIONS OF THE CONVERTER

| Component | Specifications |
|---|---|
| MOSFETs | IPP111N15 N3G |
| $D_1$, $D_2$, $D_3$ | IDH03SG60C |
| Drive chip | 2ED020I12-FI |
| Switching Frequency | 100kHz |
| Turn ratio | 1:2:8 |
| Magnetizing Inductor | 120uH(core：ETD39) |
| $C_2$ | 1.68uF |
| $C_3$ | 0.62uF |
| $C_{01}$, $C_{02}$ | 100uF |

The current stress of switches can be expressed as

$$I_{Q1(\text{peak})} = \frac{V_{\text{out}}(kDn_t + kn_s + 2)}{(1-D)R} + \frac{V_{\text{out}}(1-D)D}{2(kDn_t + kn_s + 2)(L_m + L_k)f_s} \quad (37)$$

$$I_{Q2(\text{peak})} = \frac{V_{\text{out}}(1-D)\sqrt{(L_m + L_k)/C_2}}{kDn_t + kn_s + 2}. \quad (38)$$

## IV. EXPERIMENTAL RESULTS

In order to verify the feasibility of the proposed converter, a 100-W experimental prototype is implemented in the laboratory, as is shown in Fig. 7. The electrical specifications are as follows: $V_g = 25 - 45$ V, $V_{\text{out}} = 380$ V, $f_s = 100$ kHz, and $P_{\text{out}} = 100$ W. Based on the relationship between the output and the input voltage, the ratio of the coupled inductor is designed to be 1:2:8. Table II shows the parameters and specifications based on the mathematical calculation. The TMS320F28027 is chosen as the controller and the drive chip is 2ED020I12-FI.

### A. Design of a Coupled Inductor and a Capacitor

*1) Coupled Inductor Design:* The coupled inductor is designed based on a current ripple, which is typically designed to limit the maximum current ripple to 20% of the maximum average inductor current. When the output power $P_{\text{out}} = 100$ W and the input voltage $V_g = 25$ V, the average inductor current is the largest. Therefore, the largest average inductor current $I_{L\_\max}$ equals to 4 A and the ripple current is $\Delta i_L = 0.8$ A.

The expression of the current ripple can be calculated as

$$\Delta i_L = \frac{V_g DT}{L_m} = \frac{D(1-D)TV_{\text{out}}}{L_m(2 + n_s + Dn_t)}. \quad (39)$$

Thus, the value of the magnetizing inductance can be calculated as follows:

$$L_m = \frac{D(1-D)TV_{\text{out}}}{\Delta i_L(2 + n_s + Dn_t)}. \quad (40)$$

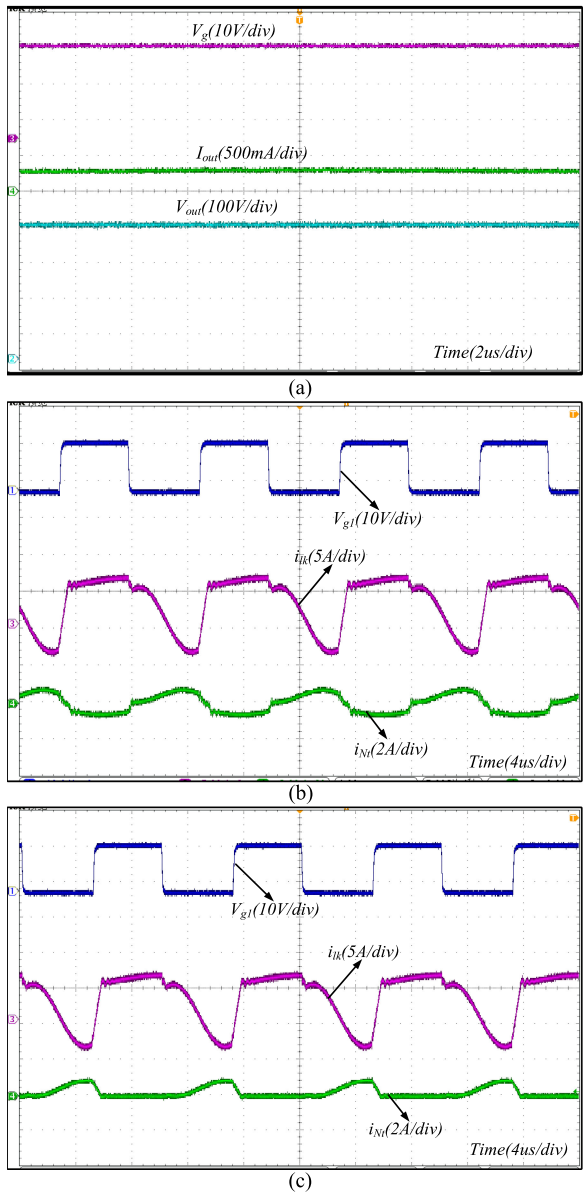


Fig. 8. Measured waveforms of output, input voltage and main current of the converter. (a) Input voltage, output voltage, and current. (b) Gate signal of $Q_1$, the current of the leakage inductor, and the second winding. (c) Gate signal of $Q_1$, the current of the leakage inductor, and the third winding.

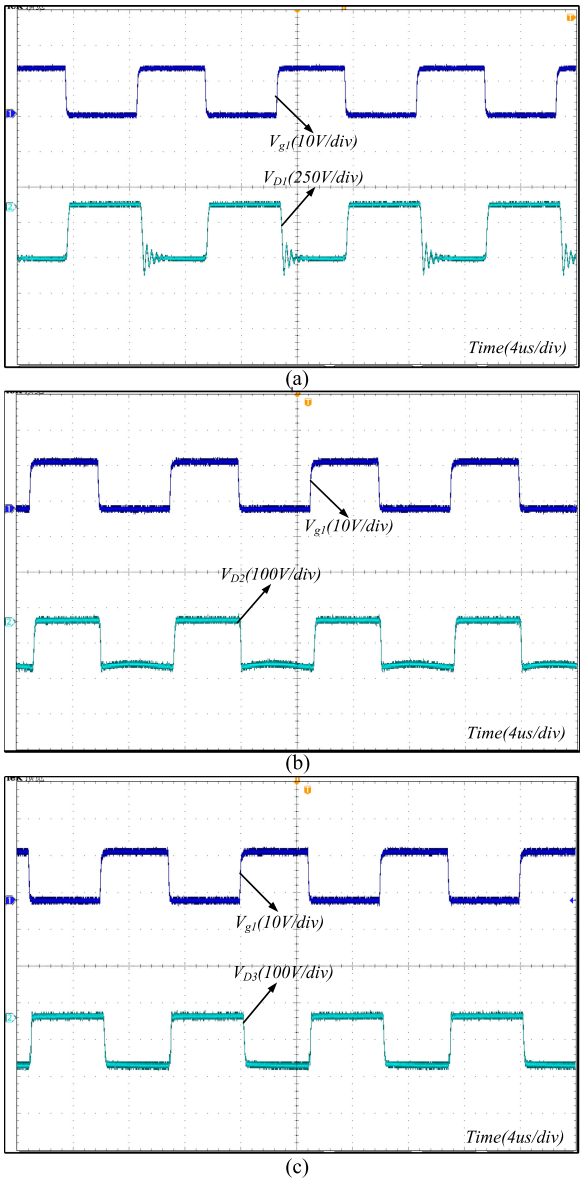


Fig. 9. Measured voltage waveforms of diodes $D_1$, $D_2$, and $D_3$. (a) Voltage of the diode $D_1$. (b) Voltage of the diode $D_2$. (c) Voltage of the diode $D_3$.

*2) Switched Capacitor Design:* The selection of the switched capacitor is based on two factors: 1) a voltage ripple of the switched capacitor, and 2) an output power lever. By utilizing a charge-second balance, the switched capacitor can be calculated by

$$C_2 \geq \frac{I_{\text{out}} DT}{\Delta C_2} \tag{41}$$

$$C_3 \geq \frac{I_{\text{out}} DT}{\Delta C_3}. \tag{42}$$

A maximum voltage ripple of the switched capacitor is taken as 1% of the switched capacitor voltage. Therefore, the switched capacitor $C_2$ and $C_3$ are selected as 1.68 and 0.62 uF, respectively, where $\Delta C_2$ and $\Delta C_3$ are the voltage ripple of the switched capacitor $C_2$ and $C_3$, respectively.

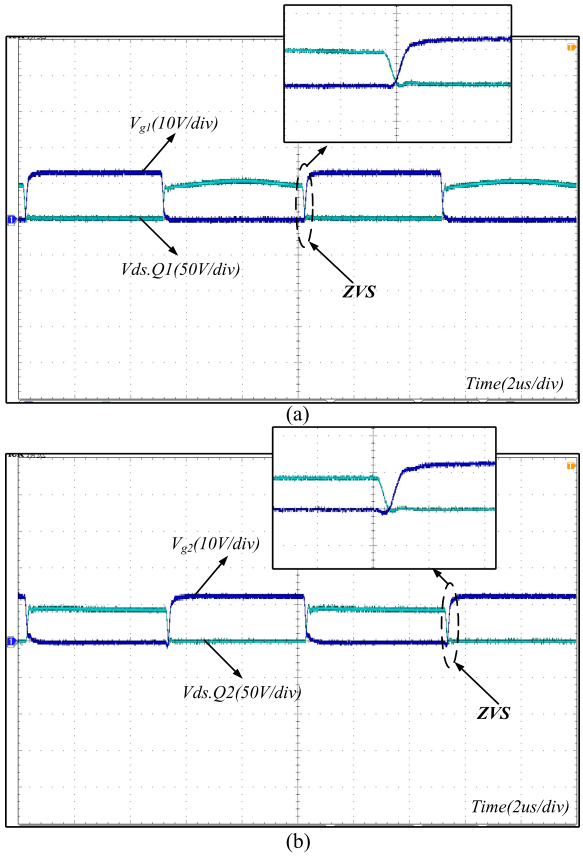


Fig. 10. Measured waveforms of the switch $Q_1$ and $Q_2$. (a) Gate signal and the drain–source voltage of $Q_1$. (b) Gate signal and drain–source voltage of $Q_2$.

## B. Experiment Results

The experimental results are shown in Figs. 8–10 for full-load $P_{\text{out}} = 100$ W and input voltage $V_g = 25$ V. As shown in Fig. 8(a), the output voltage and current are about 380 V and 0.263 A, respectively, so the output power is about 100 W. The current through the leakage inductor and the secondary winding are shown in Fig. 8(b), along with the gate signal of MOSFET $Q_1$. The third winding current is given in Fig. 8(c). It can be seen from the above experimental results that the experimental results are consistent with the previous steady-state analysis.

From Fig. 9(a)–(c), the voltage of the diodes $D_1$, $D_2$, and $D_3$ are presented. It can be seen that the voltage stress of $D_2$ and $D_3$ are both less than 150 V, which is fully in line with the theoretical analysis. In addition, both of diodes $D_2$ and $D_3$ are able to turn OFF naturally, which means that they do not suffer from voltage spikes during turn-OFF transition. Voltage stress on the diode $D_1$ is shown in Fig. 9(a). The leakage inductor of the third winding causes a resonance with the parasitic capacitor of $D_1$ for a small duration. This leads to a voltage spike on the diode $D_1$. However, overall voltage stress on $D_1$ is below the output voltage.

In Fig. 10, the gate signal and drain–source voltage of $Q_1$ and $Q_2$ are presented, respectively. To show that the converter can achieve ZVS, the zoomed waveform is also given in the corresponding figures. Fig. 11 shows the drain–source current of $Q_1$ and $Q_2$. The drain–source current of the switch is in the negative

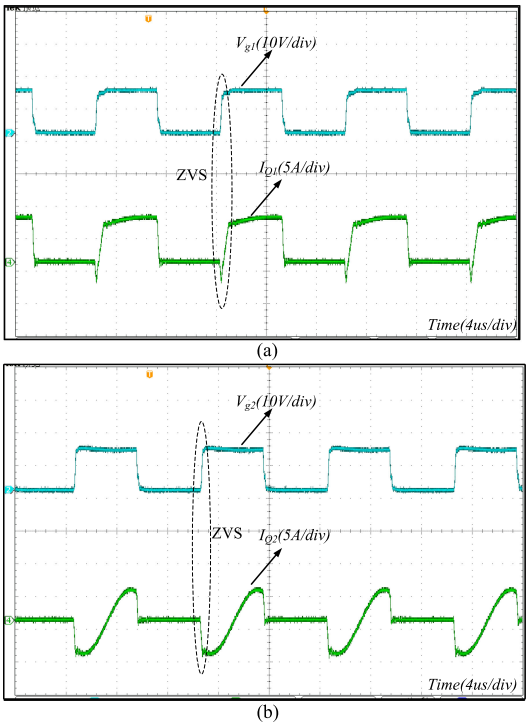


Fig. 11. Measured waveforms of the switch $Q_1$ and $Q_2$. (a) Gate signal and the drain–source current of $Q_1$. (b) Gate signal and drain–source current of $Q_2$.

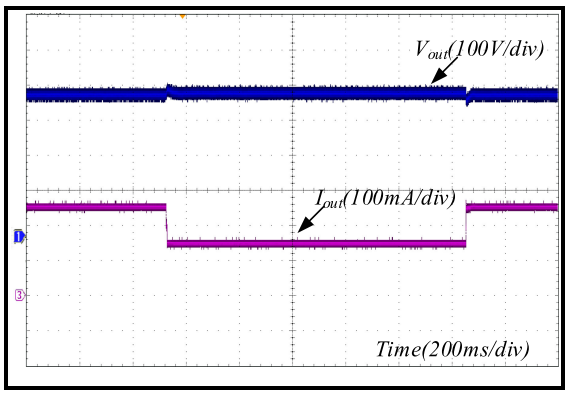


Fig. 12. Load transient experiment waveforms.

direction before it turned ON, the body diode of the switch is conducted, and the drain–source voltage is clamped to zero. From those experimental results, it is clear that both the switches $Q_1$ and $Q_2$ are able to achieve ZVS, which can effectively improve efficiency and reduce electromagnetic interference (EMI). In addition, the voltage of the switches $Q_1$ and $Q_2$ are both less than 60 V. Thus, the low-voltage rated switch with low on-state resistance and low cost can be chosen to achieve high efficiency for the proposed converter. Meanwhile, the voltage spike of $Q_1$ caused by the resonance between the leakage inductor of the coupled inductor and the parasitic capacitor can be absorbed by the switched capacitor $C_2$.

Fig. 12 shows the output voltage dynamic response when the load changes by duty cycle adjustment. Now the transfer

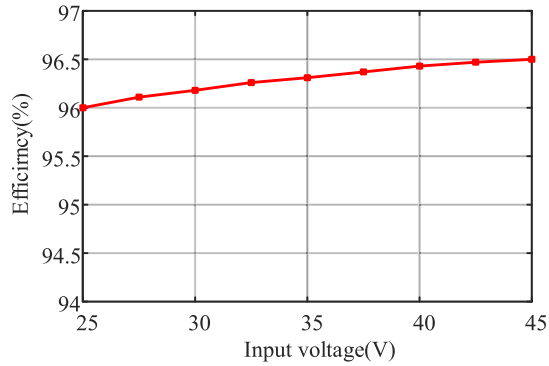


Fig. 13. Efficiency of the proposed converter under different input voltages.

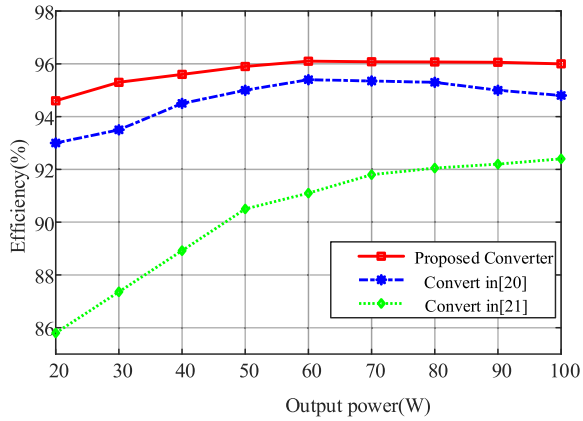


Fig. 14. Efficiency comparison under different output power.

function is established based on the generalized state space averaging method. However, the dynamic response characteristics are expected to be further improved. Other modeling and proper compensation methods are under studying.

Fig. 13 shows the experimental efficiency curve of the converter under different input voltages. As the input voltage increases, the input current decreases, and the loss of coupled inductors, semiconductor devices also decrease. Thus, the system efficiency is improved with the increment of the input voltage.

The efficiency comparison between the proposed converter [20] and [21], is shown in Fig. 14. The peak efficiency of the proposed converter is 96.21%, which is much higher than 95.3% in [20] and 92.4% in [21]. It is clear that the efficiency of the proposed converter is higher in all load range from 20 to 100 W. The experimental results show the high efficiency characteristics of the proposed converter.

The converter power loss can be mainly divided into switch loss, inductor loss, and diode loss. The switch loss mainly consists of a conduction loss and a switching loss.

The conduction loss of the switch can be obtained by [25]

$$P_{\text{cond}} = I_s^2 R_{DSon} \tag{43}$$

where $R_{DSon}$ is the ON-state resistance of the switch. The value in the experimental prototype is10.8 m$\Omega$. $I_s$ is the current rms value flowing through switch.

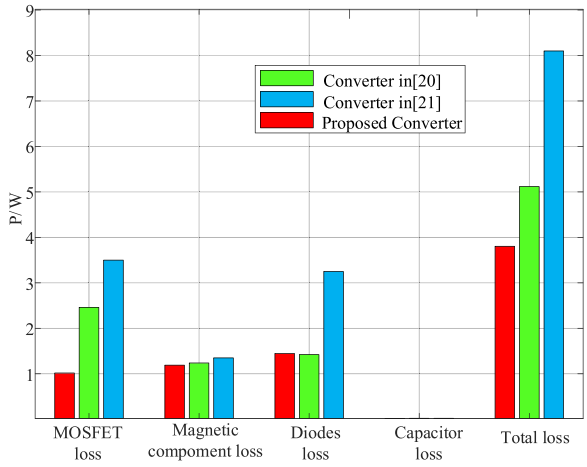


Fig. 15. Loss comparison between the proposed converter with the References [20] and [21].

The switching loss can be calculated by the formula in [26]

$$P_{\rm on}+P_{\rm off}=\frac{V_{\rm ds}I_{\rm on}t_{\rm on}}{6T}+\frac{V_{\rm ds}I_{\rm off}t_{\rm off}}{6T} \tag{44}$$

where $t_{\rm on}$ and $t_{\rm off}$ represent the time of the turn-ON and turn-OFF transitions, respectively, i.e, 16 and 25 ns, respectively. $V_{\rm ds}$, $I_{\rm on}$, and $I_{\rm off}$ represent the voltage across the switch, the value of turn-ON current and the value of turn-OFF current, respectively.

The loss in the diode is given by [27]

$$P_{\rm diode}=U_{D0}I_D \tag{45}$$

where $U_{D0}$ and $I_D$ is the forward conduction voltage of diode and the current flowing through the diode, respectively.

The loss of the coupled inductor includes a core loss and a copper loss. The core loss can be calculated as follows [28]:

$$P_{\rm core}=K_{Fe}\left(\frac{V_{\rm ave}}{8f_sN_LA_e}\right)^{\beta}A_el_m \tag{46}$$

where $K_{Fe}$ and $\beta$ are constant values related to loss. $N_L$, $V_{\rm ave}$, $A_e$, and $l_m$ represent the number of turns in inductor winding, the average voltage across the winding in the positive half cycle, the effective core-sectional area, and the magnetic path length of the core, respectively.

The copper loss can be calculated by the following equation:

$$P_{\rm copper}=I_{\rm rms}^2R_{\rm eff} \tag{47}$$

where $R_{\rm eff}$ is the equivalent value of copper resistance, and $I_{\rm rms}$ is the current flowing through the winding.

The power loss of the capacitor can be expressed as

$$P_c=I_c^2R_{\rm ESR} \tag{48}$$

where $R_{\rm ESR}$ is the equivalent series resistor of the capacitor, and $I_c$ is the rms capacitor current.

Fig. 15 shows the loss of the proposed converter and the references [20] and [21] according to (39)–(43), which work under the same output power. As can be seen from the figure, the proposed converter core loss is very close to the references [20] and [21]. The diodes loss in [21] is higher than the proposed converter due to the large average current. The main different loss is from the switches. Although the proposed converter has the same number of switches with references [20] and [21], the loss of the switches is small due to the ZVS. So, the proposed system has the lowest loss.

## V. Conclusion

This article proposes a novel high step-up, high efficiency soft-switching dc–dc converter based on the coupled inductor and switched capacitor. The proposed converter adopts capacitors charged in parallel and discharged in series with a coupled inductor to achieve a high step-up voltage gain. By utilizing the energy stored in the leakage of the coupled inductor, both of the switches can realize the ZVS. Thus, the efficiency is improved. In addition, the voltage stress of the semiconductor device is very low. This helps to select the low-voltage rated MOSFETs with low ON-state resistance, leading to a smaller conduction loss and cost. The input current of the proposed converter is continuous, which is very important for PV applications. Finally, a 100-W experimental prototype of the proposed converter is implemented in the laboratory. The highest efficiency is 96.21%. The experimental results verify that the proposed converter can get a high voltage gain without a large duty cycle and with reduced voltage stress on the MOSFETs.

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