Model-Based Design and Optimization of Hybrid DC-Link Capacitor Banks

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***Abstract*—For the applications where a single capacitor is incapable to meet the needs, multiple capacitors are connected in series or in parallel as a bank to fulfill the capacitance and voltage rating requirements. Even though some commercial products have already existed in the market, most of the designs use the same capacitors or combine different types of capacitors by experience, so that the volume, cost, reliability, and power loss are not optimized. To the best knowledge, no quantitative design considering all these design aspects is available for capacitor banks. This article proposes a model-based optimal design method for hybrid capacitor banks consisting of both electrolytic capacitors and film capacitors. Performance factors, such as impedance characteristics, lifetime, power loss, cost, and volume, are modeled and considered in the optimization process. The selection of the capacitance ratio between the two types of capacitors and the number of capacitors connected in parallel are analyzed based on specific design constraints. A case study of the dc-link capacitor bank design for a 5.5-kW inverter is presented to demonstrate the modeling and optimal design process.**

***Index Terms*—Capacitor banks, electrolytic capacitor (E-cap), film capacitor (Film-cap), reliability.**

I. Introduction

CAPACITOR is a basic electronic component to store electrical charges and release it as it is required by the applications [1]– [3]. They are widely used in energy conversion systems to perform a variety of functions, such as to filter the harmonics, buffer the instantaneous power, and support energy for the transient process [4]– [7]. In most applications, a number of capacitors are packaged as a bank to cope with one or more functions [8]. For example, in adjustable speed drives with dc-link voltage over 500 V, electrolytic capacitors (E-caps) are connected in series and then in parallel to withstand the voltage and filter harmonics [9], [10]; in the case study shown in [11], the wind turbine converter has more than four metallized polypropylene film capacitors (Film-caps) connected in parallel for large capacitance to filter the high-frequency harmonics and support energy during the low voltage ride through period; in the case study shown in [12] and [13], E-caps are connected in parallel for large capacitance to decouple the low-frequency instantaneous power and minimize the voltage ripple for maximum power point tracking in photovoltaic (PV) system.

A capacitor bank can be configured with either a single type of capacitor or more types. Compared to a single type of capacitor, the proper combination of different types of capacitors, such as E-caps and Film-caps [14], or E-caps and ceramic capacitors [15], [16], can leverage their respective impedance characteristics. Nevertheless, existing design is commonly experience based, there are still the following main challenges.

1) There is lack of discussion on how the capacitance ratio between two types of capacitors is determined. The quantitative modeling, design, and criteria to obtain the hybrid capacitance ratio between different types of capacitors are missed.
2) For a given required minimum capacitance, there is a limited discussion on how to physically configure the capacitor bank with a number of capacitors connected in series and/or in parallel [17], [18], which affects the impedance characteristics, power loss, and physical performance as well.
3) Besides the minimum required capacitance, ripple current, and voltage ratings, other important factors, such as volume, reliability, and cost, are usually not analyzed for a tradeoff design. To the best knowledge, no quantitative design for capacitor banks is available to consider the multiple constraints.

This article proposes a quantitative multiobjective design method for hybrid capacitor banks. First, in order to acquire the electrical stress of individual capacitor, the detailed electrical model of capacitors considering the parasitic parameters [e.g., equivalent series resistance (ESR) and equivalent series inductance (ESL)] are provided based on the physical properties of capacitor. The physical performance of capacitors in terms of volume, cost, and lifetime is also modeled, which maps the design to the performance space. Then, a multiobjective design

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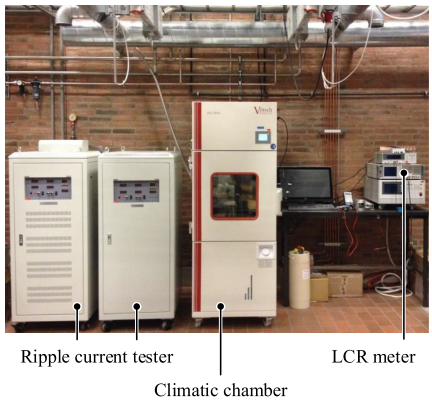

Fig. 1. Testing setup for capacitor characterization in Aalborg University [20].

procedure with the hybrid capacitance ratio feedback and the numbers of individual type of capacitor feedback is proposed. All the possible solutions that can achieve the specified design constraints or the knee points of Pareto optimal solutions can be obtained [19].

The structure of this article is shown as follows. Section II discusses the detailed models of the capacitors based on the physical properties. Section III proposes the multiobjective design method with the detailed introduction step by step. Section IV discusses experimental verification in terms of the accuracy of the capacitor models, impact of these design variables, and the multiobjective design for a 5.5-kW dc-link application. Finally, Section V concludes this article.

II. Modeling of Capacitors Based on the Physical Properties

This section discusses the detailed models of capacitors from the four aspects: electrical, thermal, reliability, and physical characteristics. As this design focuses on the high power level, two kinds of capacitors are incorporated, which are E-caps and Film-caps. The high-voltage multilayer ceramic capacitors (MLCCs) can also be a choice to implement the hybrid capacitor bank. If the database of the MLCCs are available, the proposed model-based design can also be applied. The analytical equations derived are generic ones for 450-V applications and the presented numerical results in the figures are based on the data from different manufactures or tested in the laboratory, as shown in Fig. 1 [20]. If a specified case and product is provided, a more accurate model can be built to achieve better accuracy.

A. Electrical Model

At a given frequency, the current sharing ratio among capacitors in a bank depends on the impedance of individual capacitor [21]–[23]. The equivalent circuit model of capacitors and an example of impedance curve are shown in Figs. 2 and 3, respectively. C, R_s, and L_s are the capacitance, ESR, and ESL of capacitor, respectively. At low-frequency range, the impedance is mainly determined by its capacitor value C. At the resonant-frequency points, the negative impedance of capacitance and the positive impedance of the ESL is equal while the impedance is equal to the ESR. Above the resonant

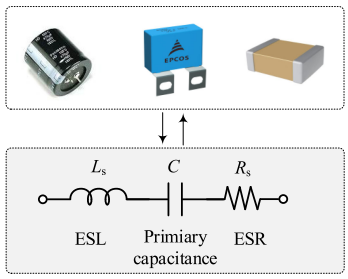

Fig. 2. Equivalent circuit model of capacitors considering parasitic parameters.

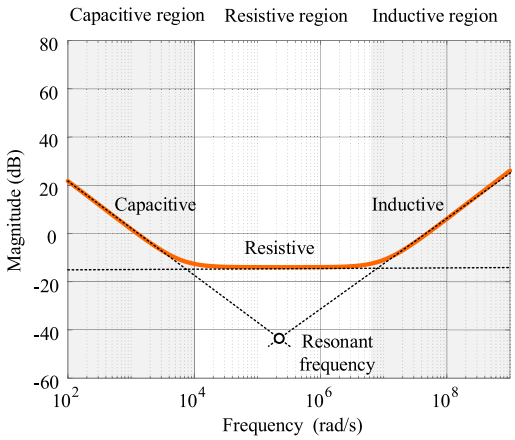

Fig. 3. Impedance characteristics of a capacitor.

frequency, the capacitor becomes inductive. The inductive reactance L_s takes over as it grows much larger than the capacitive reactance and ESR. From aforementioned discussion, it can be seen that for specified frequency, the capacitor represents different impedance that should be modeled for types of capacitors.

1) Capacitance: Capacitors contain at least two electrical conductors often in the form of metallic plates or surfaces separated by a dielectric medium. The capacitance of such a parallel plate structure is proportional to the area [24]. It is frequency (Hz) and temperature dependent. E-caps represent the capacitance reduction in the high-frequency regions (e.g., $>$10 kHz), because the tunnel-shaped pit structure of anode foil is unsuitable for the response to high-frequency switching [25]. The fitting curve of the frequency-dependent capacitance is shown in Fig. 4. Therefore, in high-frequency applications, E-cap bank may need to have a rated capacitance a few times than the required one due to its capacitance drop compared to that at 100/120 Hz. Accordingly, its power density is deteriorated compared to low-frequency applications. Compared with that of E-caps, the capacitance of Film-caps is much more stable with frequency (1% capacitance variation within 1 MHz). Therefore, only the capacitance reduction with frequency for E-caps is presented [26].

2) ESR: ESR represents the power loss of a capacitor, which includes the resistance of the dielectric material, the resistance of the terminal leads, the resistance of the connections to the dielectric, and the capacitor plate resistance. An example of ESR distribution in the physical structure of a capacitor is shown in Fig. 5. As ESR is frequency and temperature dependent, it is

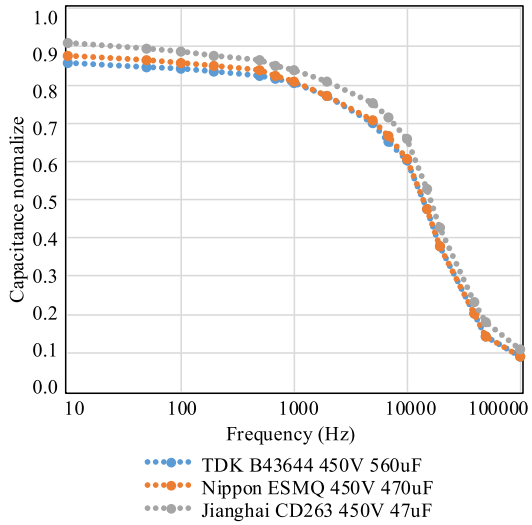

Fig. 4. Relationship between the normalized capacitance and frequency of E-caps (Data source: NCC ESMQ series, Jianghai CD263 series, and TDK B43644 series in Digikey).

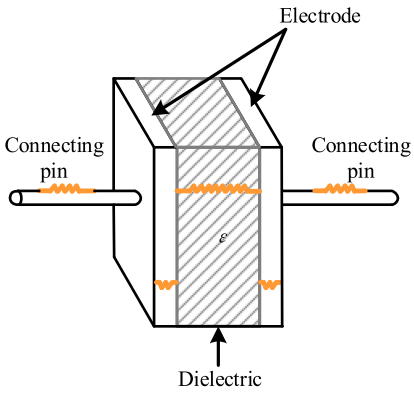

Fig. 5. ESR distribution of a capacitor.

modeled as

$$\mathrm{ESR}(C, f_i, T_h) = \mathrm{ESR}_{\mathrm{rated}}(C) \times \alpha_{\mathrm{ESR}}(f_i, T_h). \quad (1)$$

$\mathrm{ESR}_{\mathrm{rated}}(C)$ is the ESR at specified frequency (e.g., 100/120 Hz for E-caps and 10 kHz for Film-caps from the datasheet [16]), which is a function of capacitance. Higher permittivity of the dielectric material result in larger capacitance, as well as smaller resistance. Dissipation factor $\tan\delta$, which is a material-based coefficient, is defined as the ratio of the $\mathrm{ESR}_{\mathrm{rated}}$ and capacitive reactance as shown in the following [27]:

$$\tan\delta = \omega \cdot C \cdot \mathrm{ESR}_{\mathrm{rated}}. \quad (2)$$

It can be seen that, for the same capacitor package technology, there is reciprocal relationship between capacitance and $\mathrm{ESR}_{\mathrm{rated}}$, which can be written as

$$\mathrm{ESR}_{\mathrm{rated}} = k_{1,\mathrm{ESR}} C^{-1} + k_{2,\mathrm{ESR}} \quad (3)$$

where $k_{1,\mathrm{ESR}}$ and $k_{2,\mathrm{ESR}}$ are the coefficients to describe the dielectric resistance related to $\tan\delta$ and the packaging resistance, respectively, which can be obtained from curve fitting shown in Figs. 6 and 7.

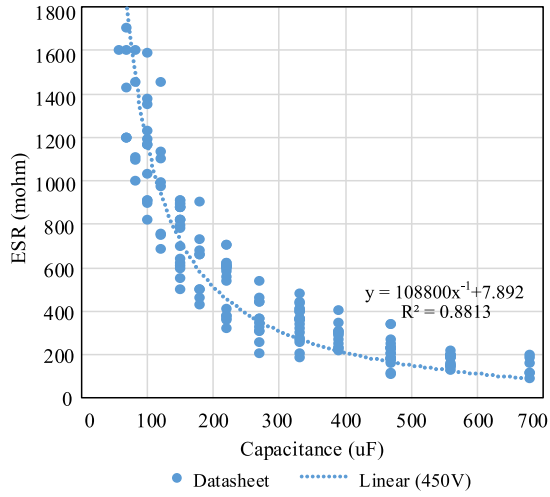

Fig. 6. Relationship between ESR at 100 Hz and capacitance of E-caps (data source: CDE 380LQ, 380LX series, Vishay 159 series, KEMET ALC series, and TDK B43642, B43545, B43508 series in Digikey).

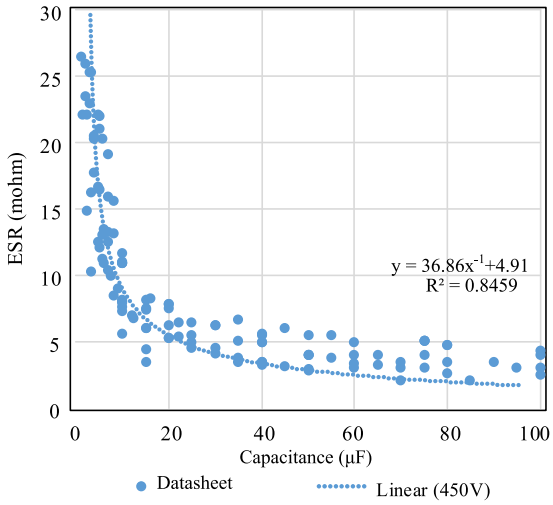

Fig. 7. Relationship between ESR at 10 kHz and capacitance of Film-caps (data source: TDK B32674, B32676, B32774, B32778 series, KEMET C4AT, C4AE series, Vishay Mkp1848 series, and WIMA DCP4I series in Digikey).

As ESR is temperature and frequency dependent, the ESR ratio $\alpha_{\mathrm{ESR}}(f_i, T_h)$ regarding to the specified frequency and temperature is introduced in (1). ESR decreases with the higher temperature, as it is usually dominated by the variation in dielectric viscosity. Moreover, ESR decreases monotonically with higher frequency until the onset of skin effect of the metallic components at 10 kHz or greater. By measuring the ESR at range of frequency and temperature, $\alpha_{\mathrm{ESR}}(f_i, T_h)$ for E-caps and Film-caps can be obtained, which are shown in Figs. 8 and 9, respectively. The ESR variation of Film-caps with temperature range from 0° to 100° is lower than 2%. Therefore, the effect of temperature on the ESR of Film-caps is negligible [28].

3) ESL: ESL of capacitor is introduced by winding layers and connected power terminals. Typical values for E-caps range from 20 to 40 nH for snap-in types and 30 to 50 nH for screw-terminal types [29]. The value for Film-caps with snap-in type

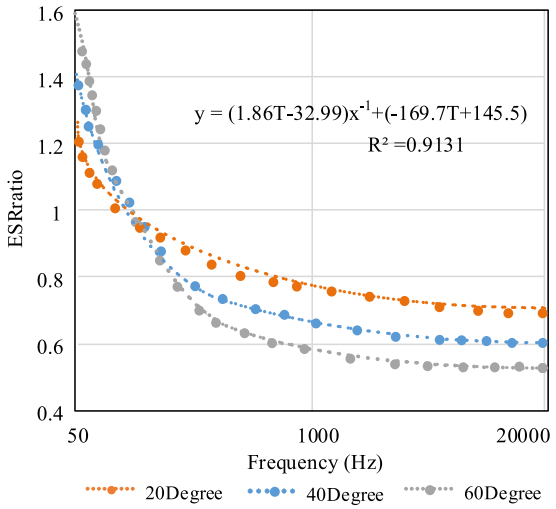

Fig. 8. Relationship among ESR ratio, frequency, and temperature of E-caps (data source: TDK B43630 series in Digikey).

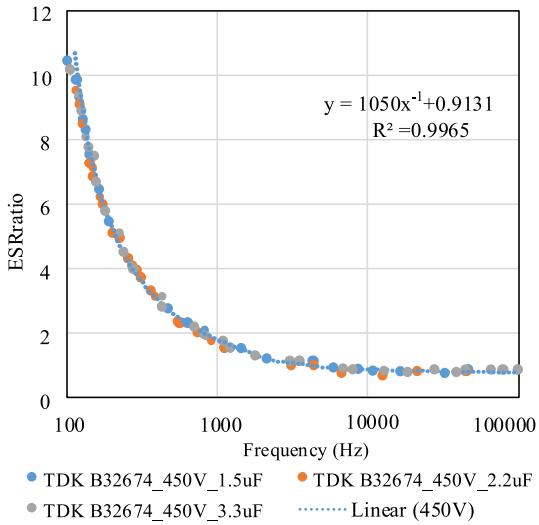

Fig. 9. Relationship between ESR ratio and frequency of Film-caps (data source: TDK B32674 series in Digikey).

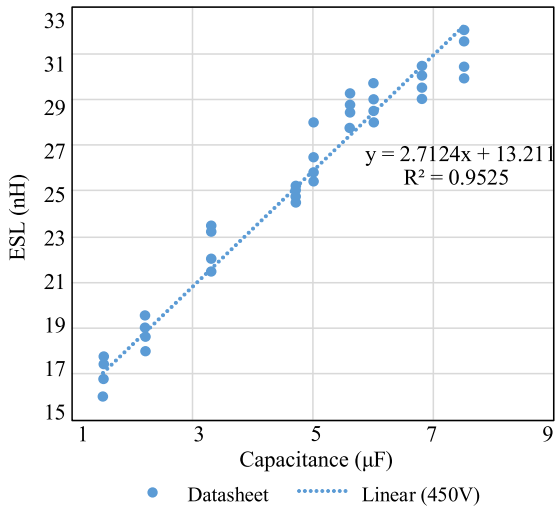

Fig. 10. Relationship between ESL and capacitance of Film-caps (data source: KEMET C4AE series and TDK B32674, B32774 series in Digikey).

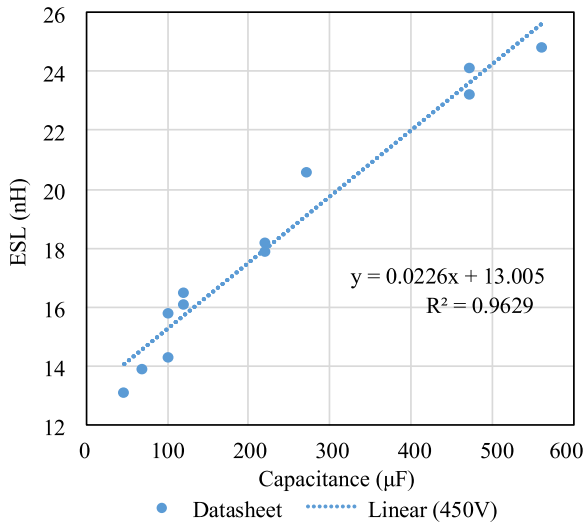

Fig. 11. Relationship between ESL and capacitance of E-caps (data source: TDK B43630, B43644 series from laboratory testing).

range from 5 to 30 nH [30]. It increases with the terminal spacing, terminal-tab loop area, and winding itself as well as capacitance. Therefore, the mathematical model for ESL can be described as a linear function with the capacitance

$$\mathrm{ESL} = k_{1,\mathrm{ESL}} C + k_{2,\mathrm{ESL}} \tag{4}$$

where $k_{1,\mathrm{ESL}}$ and $k_{2,\mathrm{ESL}}$ are the coefficients to describe the winding inductance related to capacitance and the terminal inductance of the capacitor, which can be obtained from the curve fitting, as shown in Figs. 10 and 11.

B. Thermal Model

Thermal stress is one of the critical stressors of capacitors, resulting in the reduction of capacitance and the increase of ESR due to wear out [31] [1]. The current ripple and ambient temperature are the contributors to the internal thermal stress of capacitor. Both factors lead to an increase of ESR over the operating life, so as to increase of power loss as well as higher operating temperature inside of capacitor. The hot spot temperature of capacitor is given as

$$T_h = T_a + R_{\mathrm{ha}} \times P_{\mathrm{loss}} \tag{5}$$

where T_h is the hot spot temperature, T_a is the ambient temperature, and R_{ha} is the equivalent thermal resistance from the hot spot to ambient. Power loss is estimated from ESR and ripple current flowing through the capacitor, which can be expressed as

$$P_{\mathrm{loss}} = \sum_{i}^{m} [\mathrm{ESR}(C, f_i, T_h) \times I_{\mathrm{rms}}^2(f_i)] \tag{6}$$

where $I_{\mathrm{rms}}(f_i)$ is the root-mean-square (rms) capacitor current at specified frequency f_i. m represents the mth harmonic current.

Thermal resistance of the capacitor ignores the heat dissipated from the pins and print circuit board (PCB), therefore, it only considers the heat convection and radiation from the capacitor surface. The physical mechanism of convection heat transfer is related to heat conduction through a thin boundary layer of fluid adjacent to the heated body surface. Newton's law of cooling gives a simple expression for the overall process of convection heat transfer

$$q = h_{\text{conv}} A (T_c - T_a) \tag{7}$$

where q is the heat transfer rate by convection, h_{conv} is the convection heat transfer coefficient of the material, A is the surface of heated body, T_c is the temperature of surface, and T_a is the ambient temperature. The physical mechanism of radiation heat transfer is different from the mechanism of conduction and convection heat transfer, where it is electromagnetic radiation, and heat can be transferred even through a vacuum area. The heat transfer by radiation is described by the Stefan–Boltzmann law of thermal radiation [32]

$$q = \varepsilon \sigma A T^4 \tag{8}$$

where q is the heat transfer rate by radiation, ε is the emissivity of the radiating surface, σ is the Stefan–Boltzmann constant $5.67e^{-8}$, T is the absolute temperature, and A is the radiating area. From aforementioned discussion, it can be obtained that the thermal resistance from hot spot to ambient is an inverse proportional function of surface area of the capacitor. Therefore, the mathematical model of the thermal resistance of capacitor can be given as

$$R_{\text{th}} = k_{1,\text{R}_{\text{th}}} A^{-1} + k_{2,\text{R}_{\text{th}}} \tag{9}$$

where $k_{1,\text{R}_{\text{th}}}$ and $k_{2,\text{R}_{\text{th}}}$ are the coefficients of thermal resistance model. A is the surface area of capacitor. As A is proportional to the parallel plate area of the capacitor as well as capacitance; therefore, A is linear with the capacitance for the same voltage series, which is described as

$$A = k_{1,\text{A}} C + k_{2,\text{A}}. \tag{10}$$

$k_{1,\text{A}}$ and $k_{2,\text{A}}$ are the coefficients of surface area model. All the coefficients can be extracted from the curve fitting shown in Figs. 12 and 13.

C. Lifetime Model

According to Wang and Blaabjerg [1], the lifetime model for capacitors is given as

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-n} \times \exp\left[\left(\frac{E_a}{K_{\text{B}}}\right)\left(\frac{1}{T} - \frac{1}{T_0}\right)\right] \tag{11}$$

where L and L_0 are the lifetime under the using condition and the testing condition, respectively. V and V_0 are the voltage at the using condition and the testing condition, respectively. T and T_0 are the temperature in kelvin at the using condition and the testing condition, respectively. E_a is the activation energy, K_{B} is Boltzmann's constant 8.62×10^{-5} eV/K, and n is the voltage stress exponent. Therefore, the values of E_a and n are the key parameters to be determined in the aforementioned

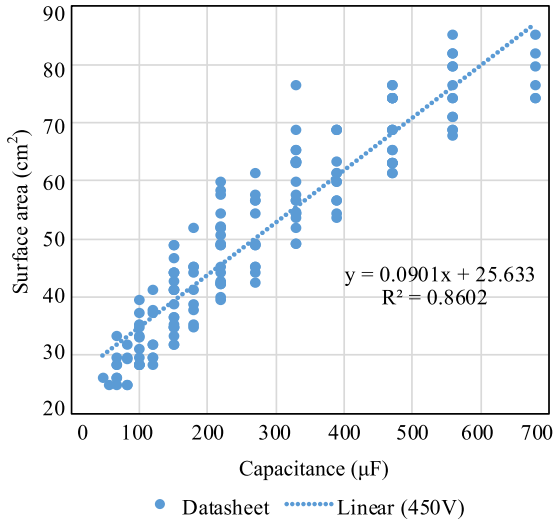

Fig. 12. Relationship between capacitance and surface area of E-caps (data source: CDE 380LQ, 380LX series, Vishay 159 series, KEMET ALC series, and TDK B43642, B43545, B43508 series in Digikey).

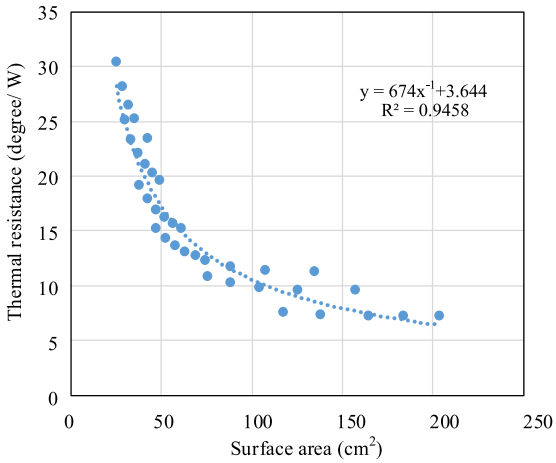

Fig. 13. Relationship between surface area and thermal resistance of E-caps (data source: CDE 380LX, SLP, SLPX series from laboratory testing).

model. For E-caps and Film-caps, a simplified model from the aforementioned equation is popularly applied as follows:

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-n} \times 2^{\frac{T_0 - T}{10}}. \tag{12}$$

The model corresponds to a specific case of first equation when $E_a = 0.94$ eV and T_0 and T are substituted by 398 K. For E-caps, the value of n typically varies from 3 to 5. For Film-caps, n is from around 7 to 9.4, which is used by leading capacitor manufacturers [1].

D. Physical Model

Volume and cost of capacitors are linear with the energy storage, which is $E_{\text{cap}} = \frac{1}{2} C V^2$ [33], where C and V are the rated capacitance and voltage, respectively. Therefore, they are linear with the capacitance for the same voltage rating series. The volume and cost models for E-caps and Film-caps are

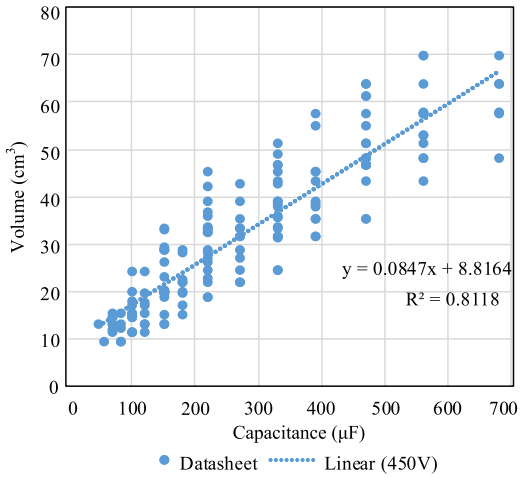

Fig. 14. Relationship between capacitance and volume of E-caps (data source: CDE 380LQ, 380LX series, Vishay 159 series, KEMET ALC series, and TDK B43642, B43545, B43508 series in Digikey).

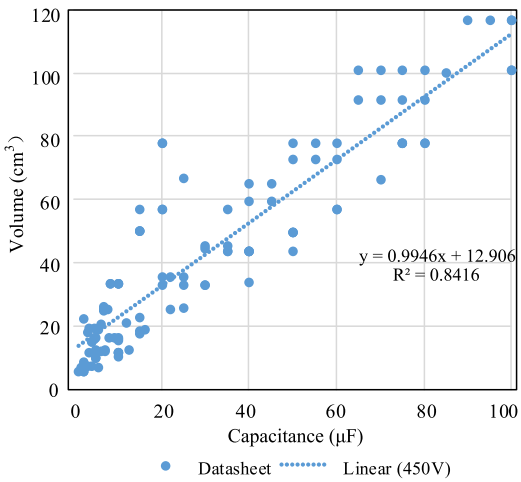

Fig. 15. Relationship between capacitance and volume of Film-caps (data source: TDK B32674, B32676, B32774, B32778 series, KEMET C4AT, C4AE series, Vishay Mkp1848 series, and WIMA DCP4I series in Digikey).

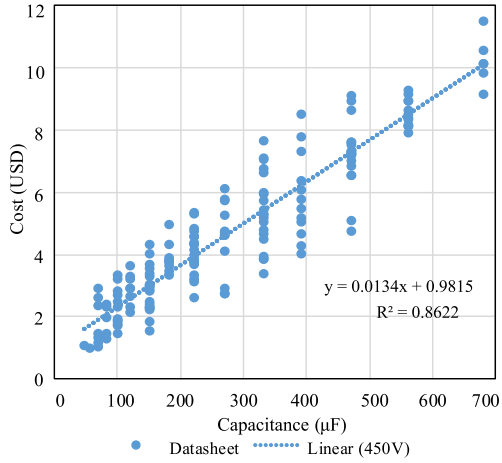

Fig. 16. Relationship between capacitance and cost of E-caps (data source: CDE 380LQ, 380LX series, Vishay 159 series, KEMET ALC series, and TDK B43642, B43545, B43508 series in Digikey).

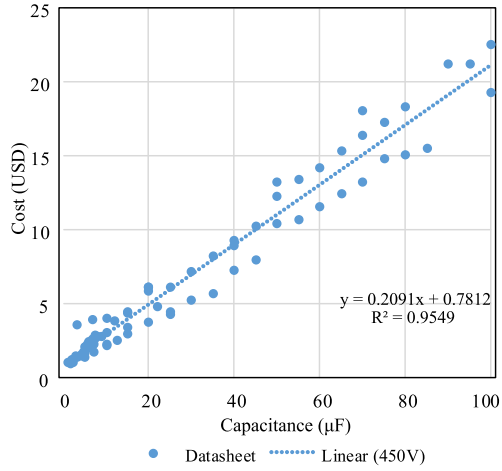

Fig. 17. Relationship between capacitance and cost of Film-caps (data source: TDK B32674, B32676, B32774, B32778 series, KEMET C4AT, C4AE series, Vishay Mkp1848 series, and WIMA DCP4I series in Digikey).

shown in Figs. 14, 15 and Figs. 16, 17, respectively, and the corresponding mathematical models are shown as

$$\text{Volume} = k_{1,\text{vol}}C + k_{2,\text{vol}} \tag{13}$$

$$\text{Cost} = k_{1,\text{cost}}C + k_{2,\text{cost}}. \tag{14}$$

$k_{1,\text{vol}}$ and $k_{1,\text{cost}}$ are the coefficients related to the capacitance on certain voltage level, and $k_{2,\text{vol}}$ and $k_{2,\text{cost}}$ are the coefficients represent the packaging volume and cost, respectively.

III. Multiobjective Design of Capacitor Bank

This section discusses the proposed multiobjective design method for capacitor bank step by step. The flowchart is shown in Fig. 18 and the detailed models of capacitors are from aforementioned section. Two design variables in terms of the hybrid capacitance ratio among types of capacitors and the numbers of capacitor connected in parallel for individual type are optimized to obtain the possible solutions to achieve the design targets.

A. System Specification

System specification indicates the terminal capability of the capacitor bank. Depending on the applications, the voltage and current stresses can be obtained from circuit analysis. For example, in a single-phase PV inverter system, when the grid-side voltage and current are unit power factor, the ac voltage $v_{\text{ac}}(t)$ and current $i_{\text{ac}}(t)$ are shown in the following equations:

$$v_{\text{ac}}(t) = V_m \sin(\omega_{\text{o}} t) \tag{15}$$

$$i_{\text{ac}}(t) = I_m \sin(\omega_{\text{o}} t) \tag{16}$$

where V_m and I_m are the amplitude of ac voltage and current, respectively, and ω_{o} is the grid frequency. In the single-phase inverter using bipolar sinusoidal pulsewidth modulation, the dc-link current can be given based on double Fourier

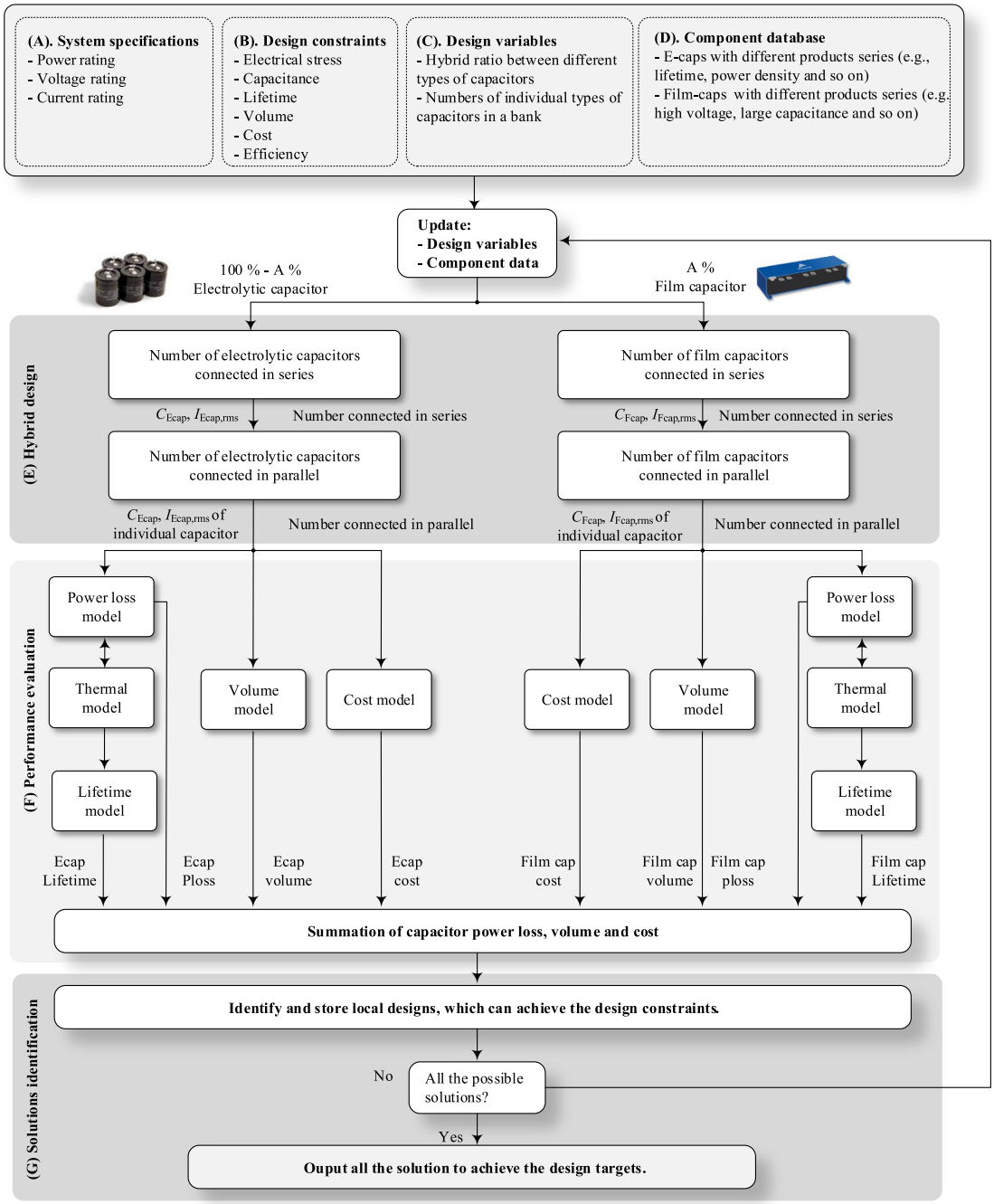

Fig. 18. Flowchart of the multiobjective design procedure for capacitor bank.

analysis [34]

$$I_{\rm dc} = \frac{I_m M}{2} + \frac{I_m M}{2}\cos(2\omega_0 t) + I_m \frac{2}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)\sin\left[(m+n)\frac{\pi}{2}\right] \times\{\cos[m\omega_c t+(n+1)\omega_o t]+\cos[m\omega_c t+(n+1)\omega_o t]\} \quad (17)$$

where $M = \frac{V_m}{V_{\rm dc}}$ is the modulation index, $J_n(x)$ donate a Bessel function of the first kind, and ω_c is the angular frequency of carrier wave. $\frac{I_m M}{2}$ is the dc current. $I_{\rm low} = \frac{I_m M}{2}\cos(2\omega_0 t)$ represents the low-frequency ripple current through the capacitor bank, and the third term $I_{\rm high} = I_m \frac{2}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{m}J_n(m\frac{\pi}{2}M)\sin[(m+n)\frac{\pi}{2}]\{\cos[m\omega_c t+(n+1)\omega_o t]+\cos[m\omega_c t+(n+1)\omega_o t]\}$ represents the high-frequency ripple current flowing through the capacitor bank. Therefore, the voltage and current stresses of dc-link capacitor bank can be obtained.

B. Design Constraints

Design constraints of the capacitor bank can be divided into three aspects: functionality, reliability, and physical performance. Functionality is the basic constraint for the system stable operation, whereas the other two aspects affect the performance space of the capacitor bank.

1) Functionality Constraints: Generally, the functionalities of the capacitor bank can be summarized to two groups: to achieve capacitance requirement (e.g., limit the voltage ripple, absorb harmonics, and buffer the pulsating power) [35] and energy storage requirement (e.g., support energy during the hold-up time and store energy to reduce overshoot voltage) [36]. For the capacitance requirement application to limit the dc-link voltage ripple $V_{\rm pp}$, the minimum capacitance used for capacitor bank can be obtained from following equation:

$$C_{\rm bank,min} = \frac{\sqrt{2} I_{\rm AB}}{\omega_h \frac{V_{\rm pp}}{2}} \tag{18}$$

where $I_{\rm AB}$ is the rms capacitor current at the specified harmonic frequency ω_h. $V_{\rm pp}$ is the maximum allowed ripple voltage.

For the energy storage application, the minimum capacitance $C_{\rm bank,min}$ required is determined by the energy requirement of system and the allowable dc-link voltage drop/rise during the time period, which is given as

$$C_{\rm bank,min} = \frac{2\int_0^{t_h} P(t)\,dt}{(V_{\rm max}^2 - V_{\rm min}^2)} \tag{19}$$

where $P(t)$ is the rated power of the system (e.g., constant power load or time-dependent load) and t_h is the operating time. $V_{\rm max}$ and $V_{\rm min}$ are the maximum and minimum allowable dc-link voltage, respectively.

2) Reliability Constraint: The reliability performance has influences on the safety, service quality, lifetime, availability, and life-cycle cost of specific applications. With the increasing penetration of renewable energy sources and adoption of more efficient variable-speed motor drives, the failure of power electronic converters in wind turbines, PV systems, and motor drives are becoming an unnegligible issue. Typical lifetime targets in these applications are listed in [37].

3) Physical Performance Constraints: Cost, volume, and efficiency are also the key performance factors of capacitor bank. These performance should be considered in the multiobjective design procedure for various applications.

C. Design Variables

Two design variables are considered in the proposed multiobjective design: hybrid capacitance ratio between different types of capacitors and the number of capacitors connected in series of in parallel. By changing these design variables, the electrothermal stress and the physical characteristics will be changed.

1) Hybrid Capacitance Ratio: Hybrid capacitance ratio is defined as the ratio between the rated capacitance of Film-caps and the total rated capacitance, which is written as

$$\alpha_{\rm capacitance} = \frac{C_{\rm Film}}{C_{\rm Film} + C_{\rm E-cap}} \times 100\% \tag{20}$$

where $C_{\rm Film}$ and $C_{\rm E-cap}$ are the capacitance of the Film-caps and E-caps at rated frequency, respectively. By changing the hybrid capacitance ratio $\alpha_{\rm capacitance}$, the sharing current at low-frequency range will change according to the capacitance ratio, whereas for the high-frequency range, it follows the impedance ratio $\alpha_{\rm impedance}$. The impedance ratio $\alpha_{\rm impedance}$ at f_n between the two types of capacitor is defined as

$$\alpha_{\rm impedance}(f_n) = \frac{Z_{\rm Film}(f_n)}{Z_{\rm Film}(f_n) + Z_{\rm E-cap}(f_n)} \times 100\% \tag{21}$$

where the impedance of capacitor is a function of capacitance, ESR, and ESL, as shown in Fig. 19 and given as follows:

$$Z_{\rm Film}(f_n) = \frac{1}{2\pi f_n C_{\rm Film}} + {\rm ESR}_{\rm Film}(C_{\rm Film}, f_n) + 2\pi f_n {\rm ESL}_{\rm Film}(C_{\rm Film}) \tag{22}$$

$$Z_{\rm E-cap}(f_n) = \frac{1}{2\pi f_n C_{\rm E-cap}} + {\rm ESR}_{\rm E-cap}(C_{\rm E-cap}, f_n) + 2\pi f_n {\rm ESL}_{\rm E-cap}(C_{\rm E-cap}). \tag{23}$$

2) Numbers Connected in Parallel: For individual type, the number of capacitors connected in parallel is the second design variable, which should be optimized. To achieve a specified capacitance, single capacitor is able to use, whereas it is also possible to use multiple small capacitors connected in parallel, so as to achieve larger capacitance, lower ESR, and lower ESL. For example, the impedance of a capacitor bank with $C_{\rm E-cap} = N_{\rm E-cap} \cdot C_{\rm E-cap,single}$ capacitors connected in parallel can be expressed as

$$Z_{\rm E-cap}(f_n) = \frac{1}{2\pi f_n N_{\rm E-cap} C_{\rm E-cap,single}} + \frac{{\rm ESR}_{\rm E-cap}(C_{\rm E-cap,single})}{N_{\rm E-cap}} + \frac{2\pi f_n {\rm ESL}_{\rm E-cap}(C_{\rm E-cap,single})}{N_{\rm E-cap}}. \tag{24}$$

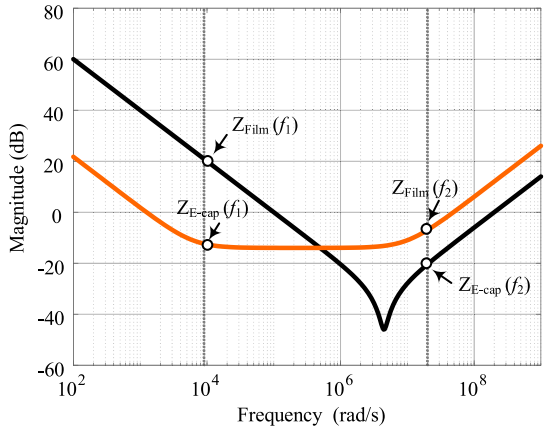

Fig. 19. Impedance examples of capacitors in hybrid capacitor bank.

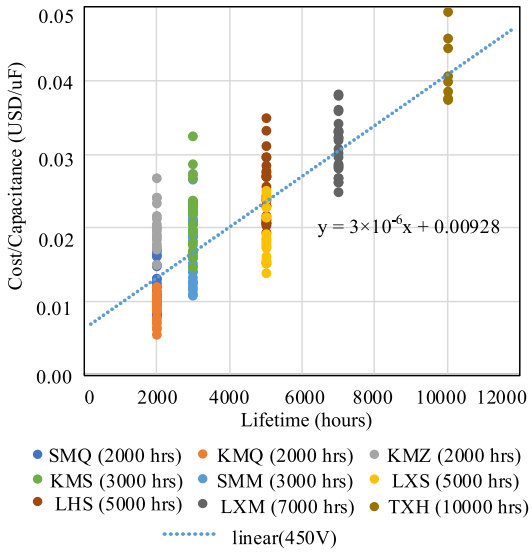

Fig. 20. Relationship between rated lifetime and cost of E-caps oriented from NCC (data source: NCC SMQ, KMQ, KMZ, KMS, SMM, LXS, LHS, LXM, and TXH series in Digikey).

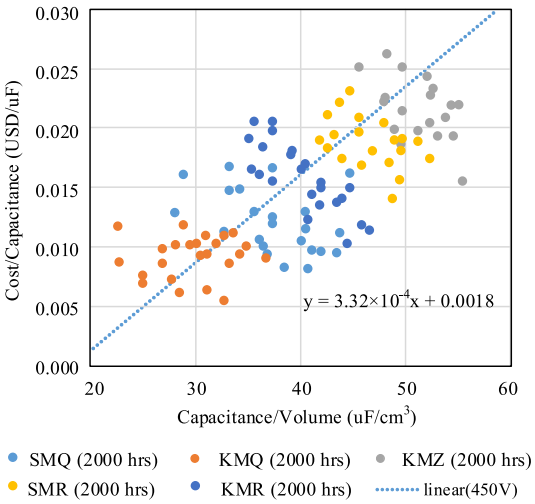

Fig. 21. Relationship between capacitance density and cost of E-caps from NCC (data source: NCC SMQ, KMQ, KMZ, SMR, and KMR series in Digikey).

It can be seen that the more capacitors connected in parallel could lead to the reduction of ESR and ESL, so as to benefit the power loss and the thermal stress of individual capacitor.

D. Component Database

The hybrid capacitor bank aims to combine different types and series of capacitors to achieve specified impedance characteristics, lifetime, and power density. Therefore, various series products with scalable current rating, rated lifetime, and size are included in the database [38]. Figs. 20 and 21 present the statistical data of different rated lifetime and size series of E-caps from Nippon Chemi-Con (NCC) [39]. Along with longer rated lifetime, the unit capacitance cost increases. For capacitors with the same rated lifetime, the higher power density indicates higher cost. The statistical data show that it is possible to achieve the design targets by fully utilization of different advanced capacitor products.

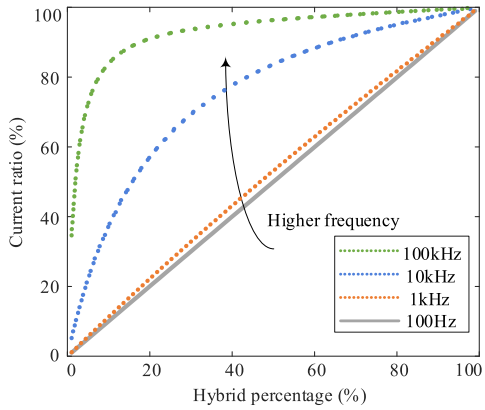

Fig. 22. Relationship between hybrid capacitance ratio and current sharing ratio of capacitor bank.

E. Hybrid Capacitor Bank Design

The hybrid design contains two main steps. First is to sweep the hybrid capacitance ratio $\alpha_{\text{capacitance}}$ to derive the capacitance of E-caps and Film-caps, respectively. It affects the impedance ratio $\alpha_{\text{impedance}}$ as well as the sharing current. The current sharing ratio between capacitors in a bank is defined as

$$\alpha_{\text{current}}(f_n) = \frac{I_{\text{Film}}(f_n)}{I_{\text{Film}}(f_n) + I_{\text{E-cap}}(f_n)} \times 100\%. \quad (25)$$

As an example, the relationship between the current sharing ratio α_{current} and the hybrid capacitance ratio $\alpha_{\text{capacitance}}$ at different frequency is shown in Fig. 22. It can be seen that in the low-frequency range ($\leq$1 kHz), due to the small impact of ESR and ESL, the current sharing ratio α_{current} is determined by the capacitance value, so as to linear with $\alpha_{\text{capacitance}}$. In the high-frequency range, ESR and ESL have great impact on the current sharing, so that the current ratio curve becomes nonlinear. For the individual type of capacitors, the numbers of capacitors connected in parallel sweep in a range, then the corresponding current stress of individual capacitor can be derived. As an example, the relationship between parallel number, impedance of E-caps, and current sharing ratio in hybrid bank is shown in Figs. 23 and 24. It can be seen that with the more capacitors connected in parallel, the impedance of E-caps decreases as well as the current ratio α_{current}.

F. Performance Evaluation

Based on the hybrid design, the specified capacitors are selected to implement the capacitor bank, which are the input of capacitor bank evaluation. At this step, the performance of capacitor bank is evaluated in terms of power loss, lifetime, volume, and cost with the help of the capacitor models from aforementioned section and component database.

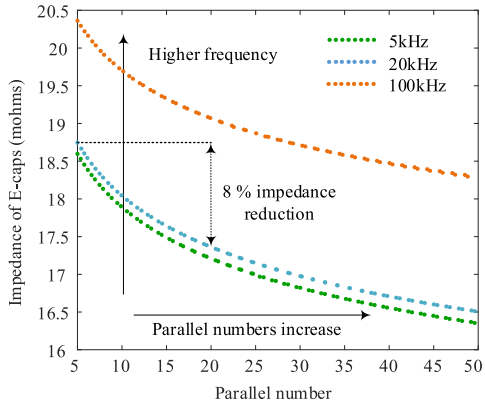

Fig. 23. Relationship between parallel number and impedance of E-caps (data source: TDK B43644 series in Digikey).

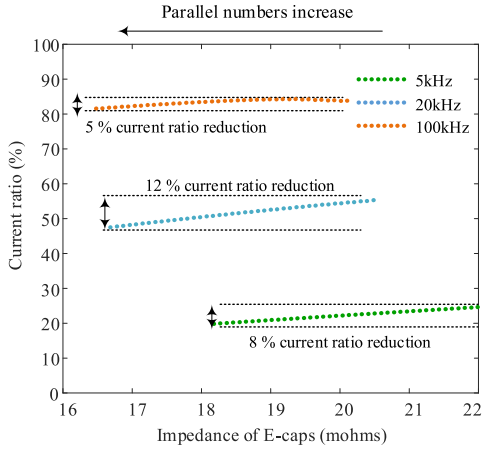

Fig. 24. Relationship between impedance of E-caps and current sharing ratio of capacitor bank.

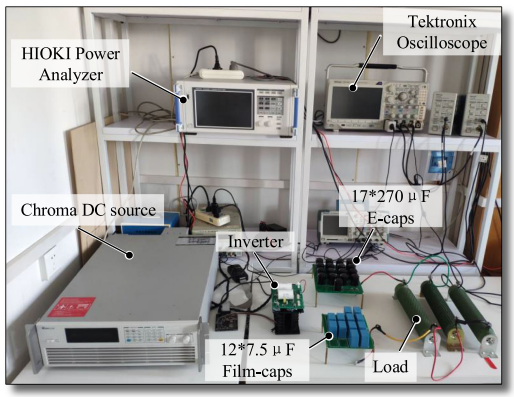

Fig. 25. Experimental setup for capacitor bank testing.

G. Solution Identification

By sweeping the hybrid capacitance ratio and the number of capacitors connected in parallel, the possible solutions with their corresponding performance space can be obtained. Then, the potential implementations, which can achieve the design targets, are selected and stored in the output space.

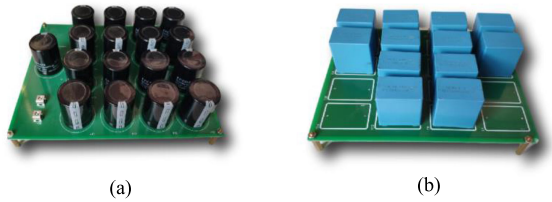

Fig. 26. Capacitor bank prototype to verify the mathematical model for current sharing. (a) E-caps bank with 17 × 270 μF. (b) Film-caps bank 12 × 7.5 μF.

TABLE I
SPECIFICATION THE CAPACITOR BANK FOR MODEL VALIDATION

Item	Value	Unit
DC voltage v_{DC}	320	V
Voltage ripple V_{pp}	6	V
Total capacitance (Minimum capacitance)	4560	μF
Low frequency f_{LF}	100	Hz
High frequency f_{HF}	20	kHz
Low frequency current I_{LF}	17.18	A
High frequency current I_{HF}	12.64	A

TABLE II
PARAMETERS OF THE E-CAPS AND FILM-CAPS USED FOR VALIDATION

Ordering code	type	C (μF)	ESR $(m\Omega)$	ESL (nH)
TDK B43630	E-cap	100-1000	-	-
TDK B43630A5277M000	E-cap	270	440	20
TDK B43630A5567M000	E-cap	560	220	20
TDK B32674	Film-cap	1.5-7.5	-	-
TDK B32674D4335K	Film-cap	3.3	10.3	22
TDK B32674D4605K	Film-cap	6.0	5.9	28
TDK B32674D4755K	Film-cap	7.5	5.0	32

IV. VALIDATION OF THE PROPOSED MULTIOBJECTIVE DESIGN FOR CAPACITOR BANK

The validation of the proposed model based multiobjective design method for capacitor bank is conducted from three aspects. The analytical model to obtain the current of individual capacitor in a bank is verified by experimental testing first. Then, the impact of hybrid capacitance ratio and numbers of capacitor connected in parallel on the current sharing, power loss distribution, lifetime, and physical performance of the capacitor bank are discussed. Finally, two case studies with multiple design constraints are presented to demonstrate the accuracy of the proposed model based multiobjective design method. The experimental testing is based on a 5.5-kW single-phase system with the specification shown in Table I. The experimental setup for capacitor bank testing is shown in Fig. 25, and the capacitor bank prototype to verify the mathematical model for current sharing is shown in Fig. 26.

A. Validation of the Capacitor Models

The current of the capacitor bank is shared among individual capacitors based on its impedance characteristics. This section verifies the impedance model of capacitors to acquire the sharing current. The current of the capacitor bank in this article case includes 12.64 A/20 kHz high-frequency harmonics and 17.18 A/100 Hz low-frequency harmonics. The parameters of the capacitors used in the experiment is shown in the Table II. The comparison of the sharing current between the testing and the

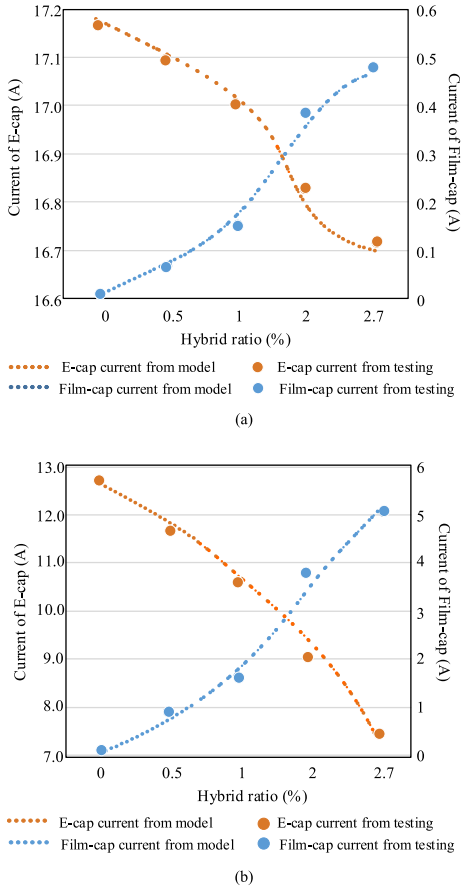

Fig. 27. Validation of capacitor models for current sharing calculation in hybrid capacitor bank. (a) Current sharing between E-caps and Film-caps at 100 Hz in procedure and experiment. (b) Current sharing between E-caps and Film-caps at 20 kHz in procedure and experiment.

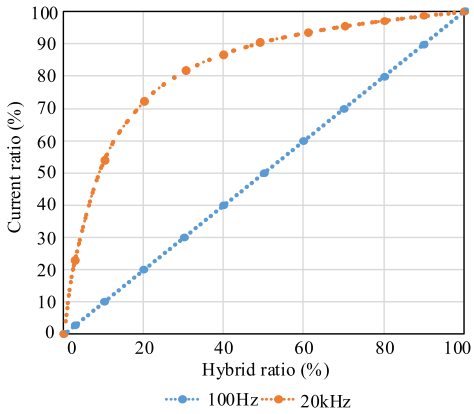

Fig. 28. Relationship between hybrid capacitance ratio and current ratio of Film-caps in 100 Hz and 20 kHz.

analytical modeling results is shown in Fig. 27. The estimation error are lower than 5%, which are in good agreement in both the low-frequency and high-frequency ranges for both the E-caps and Film-caps.

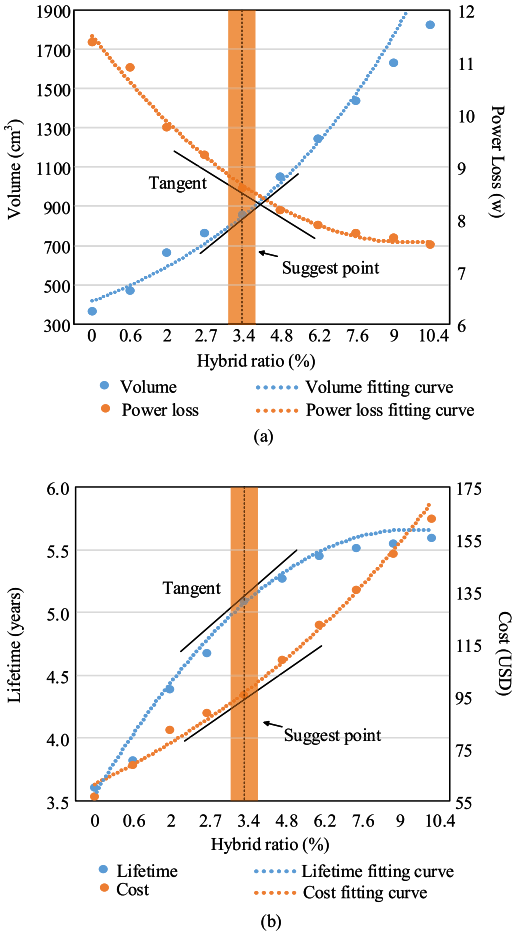

Fig. 29. Performance of capacitor bank with the same parallel number and scalable hybrid capacitance ratio. (a) Volume and power loss of capacitor bank in different hybrid ratio and same parallel number. (b) Lifetime and cost of capacitor bank in different hybrid ratio and same parallel number.

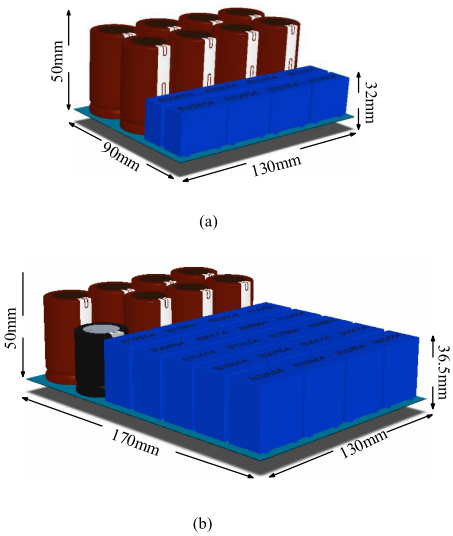

Fig. 30. Three-dimensional (3-D) prototype of capacitor bank in different hybrid capacitance ratio. (a) 8 × 560 μF E-caps and 8 × 3.3 μF Film-caps in parallel. (b) 7 × 560 μF + 1 × 470 μF E-caps and 20 × 7.5 μF Film-caps in parallel.

TABLE III
PERFORMANCE OF CAPACITOR BANK WITH DIFFERENT HYBRID CAPACITANCE RATIO AND SCALABLE NUMBERS OF CAPACITORS CONNECTED IN PARALLEL

	Hybrid ratio	C_{Film} (μF)	$C_{\mathrm{E-cap}}$ (μF)	T_h (°C)	Vol (cm^3)	P_{loss} (w)	Lifetime (years)	Cost (USD)
Case I	0.6%	8*3.3	8*560	50.2	585	10.89	3.8	65.36
Case II	3.4%	20*7.5	7*560+470	45.9	1005	8.79	5.2	92.26
Case III	3.4%	20*7.5	17*270	39.9	1560	8.21	7.5	106.44
Case IV	3.4%	20*7.5	12*390	42.6	1065	8.45	6.5	98.57

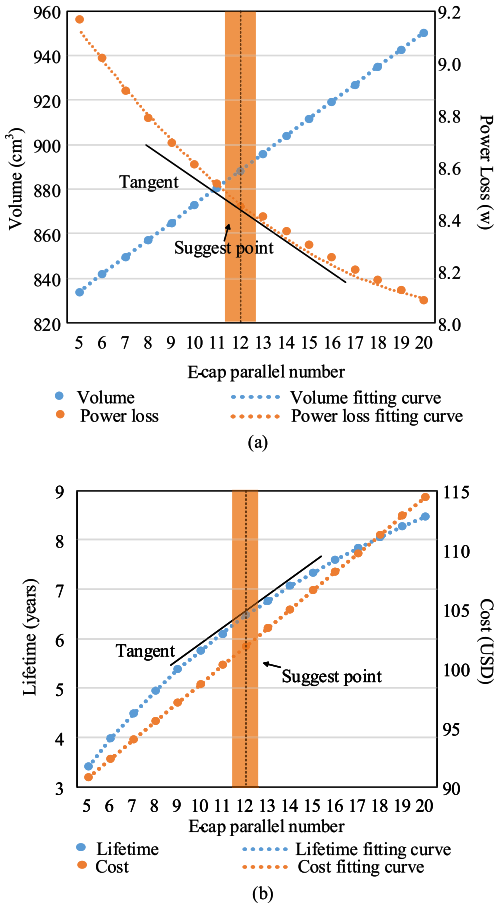

Fig. 31. Performance of capacitor bank with the same hybrid capacitance ratio and different parallel number. (a) Volume and power loss of capacitor bank in different E-cap parallel number and same hybrid ratio. (b) Lifetime and cost of capacitor bank in different E-cap parallel number and same hybrid ratio.

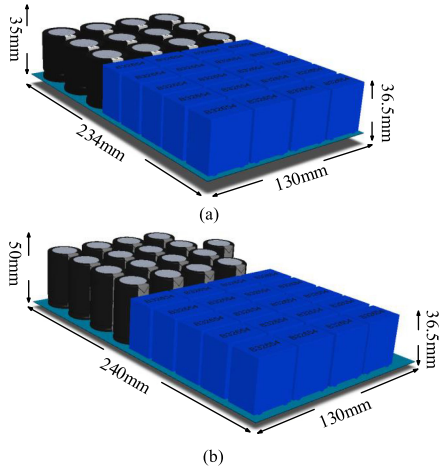

Fig. 32. 3-D prototype of capacitor bank with different parallel numbers. (a) 12 × 390 μF E-caps and 20 × 7.5 μF Film-caps in parallel. (b) 17 × 270 μF E-caps and 20 × 7.5 μF Film-caps in parallel.

B. Impact of Hybrid Capacitance Ratio

With different hybrid capacitance ratio, the current sharing ratio, power loss distribution as well as the physical performance of individual type of capacitor will be different. Fig. 28 presents the relationship between the hybrid capacitance ratio and the current sharing ratio. It can be seen that at 100 Hz, the current sharing ratio is mainly determined by the capacitance, so the curve is linear proportion to the hybrid capacitance ratio. In the high-frequency range, ESR and ESL have the great impact on the current sharing, so the curve is nonlinear with the hybrid capacitance ratio. Applying the evaluation method proposed in the article, the performance space of the capacitor bank with range of hybrid capacitance ratio can be obtained, as shown in Fig. 29. As the hybrid capacitance ratio increasing, the power loss of the capacitor bank is reduced and the lifetime is extend, but it sacrifices its volume and cost at the same time. According to the fitted curves, the tangent at the maximum slope can be obtained for individual performance factor. For this specified specification, 3.4% hybrid capacitance ratio is recommended, because the slope of the lifetime improvement is slowed down, and the volume and cost of capacitor bank are significantly increased after this point. As a case study, two capacitor banks with 0.6% and 3.4% hybrid capacitance ratio are compared in detail as examples. The physical performance can be seen from the 3-D prototype shown in Fig. 30, and the detailed performance is shown in Table III in terms of hybrid ratio between Film-caps and E-caps, capacitance for individual types, hot spot temperature T_h of E-caps, volume, power loss, lifetime, and cost. Cases I and II have the same capacitance but the different hybrid capacitance ratios. Case II is the recommended solution at the maximum slope point, which achieves 37.1% lifetime extension compared with Case I, but with 41.1% and 88.8% increase on cost and volume, respectively. The physical performance are compatible with the modeling results.

C. Impact of Numbers of Capacitors Connected in Parallel

This section studies the impact of the numbers of capacitors connected in parallel on the performance of the capacitor bank in the case of the same hybrid percentage (3.4%). The maximum single capacitance in TDK B43630 product series is 1000 μF, therefore, the minimum parallel number of E-caps is five. From the results in Fig. 31, it can be seen that as the parallel number increasing, the power loss of the capacitor bank is reduced and the lifetime is extended, but its volume and cost are increasing at the same time. According to the fitted curves, the tangent of individual curve at the maximum slope are obtained. The parallel numbers of E-caps at 12 in this design case are recommended. When more capacitors are connected in parallel, the slope of

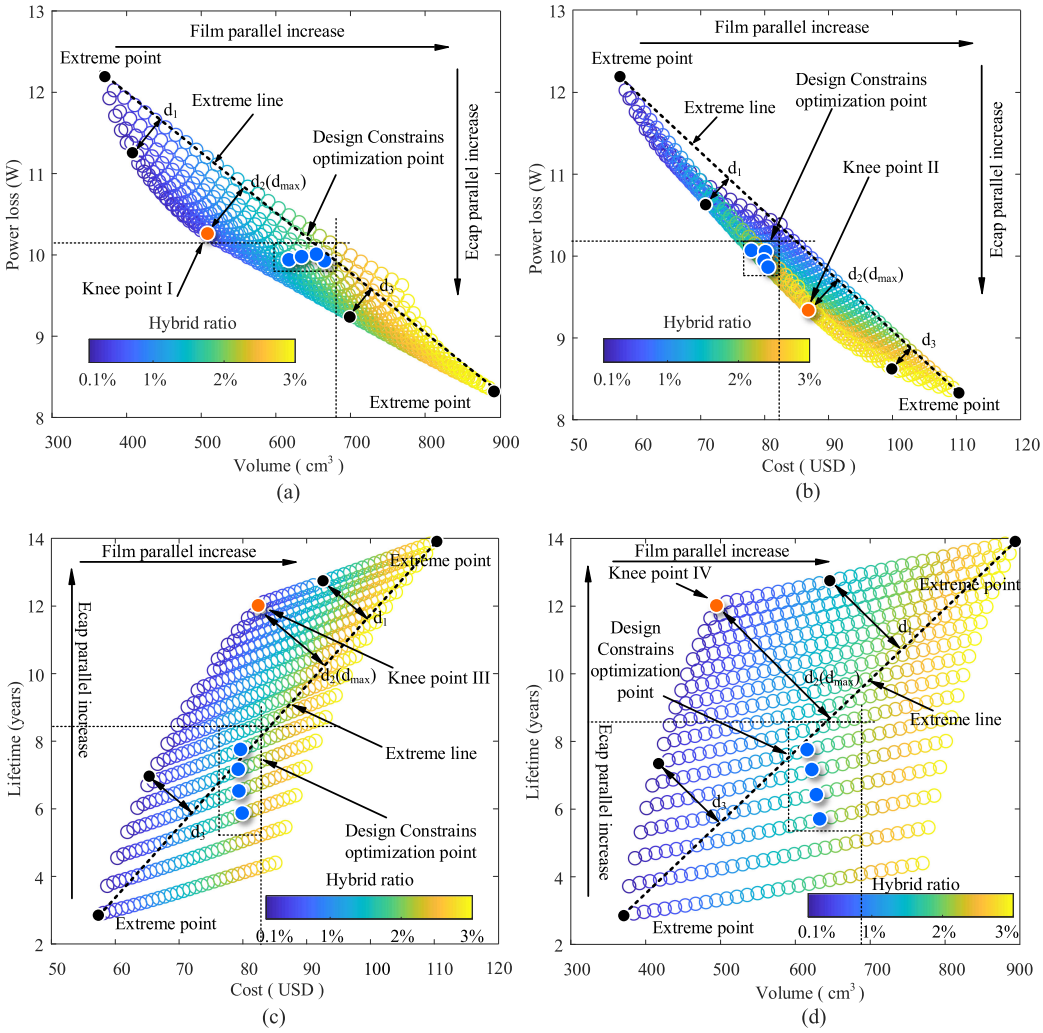

Fig. 33. Performance space of capacitor bank. (a) Performance space between power loss and volume. (b) Performance space between power loss and cost. (c) Performance space between lifetime and cost. (d) Performance space between lifetime and volume.

life improvement is slowed down, and the volume and cost of capacitor bank are significantly increased. For Film-caps parallel number, the minimum number in parallel is suggested, due to the parallel connection of the Film-caps will significant increase the cost and volume while the power loss reduction has a little effect. The physical performance can be seen from the 3-D prototype shown in Fig. 32 and the detailed performance is shown in Table III. Cases III and IV have the same capacitance and hybrid capacitance ratio, but the different parallel numbers of E-caps. Compared with Case III, Case IV at the maximum slop point is the recommended solution, which achieves 31.7% and 7.5% volume and cost reduction, whereas 11.7% lifetime reduction. The physical performance are compatible with the modeling results.

D. Optimization of Capacitor Bank

This section studies two capacitor bank design cases with multiple objectives. The first case is designed with the specified preset constraints for a 5.5-kW PV application in Table IV. All the solutions are mapped into performance space and the solutions which can achieve the design constraints are selected. The second case is designed for the same application, but does not has specified design targets. The knee points from Pareto front are found out.

TABLE IV
PRESET DESIGN CONSTRAINS OF A 5.5-KW PV APPLICATION

Design objective	Design constraints	units
Minimum lifetime	5	year
Maximum volume	0.7	L
Maximum cost	80	USD

1) Optimization With Specified Design Constraints: Applying the multiobjective design method proposed in this article, the performance space with scalable components parameters is shown in Fig. 33 and the optimization points that satisfy the given design constraints are marked. It can be seen that as the hybrid capacitance ratio of Film-caps increases from 0% to 3%, the volume and cost of the entire capacitor bank increase while the power loss reduces. Similar trend can be seen on the parallel numbers impact. Along with more capacitors connected

TABLE V
MULTIOBJECTIVE DESIGN RESULTS OF CAPACITOR BANK

	Hybrid ratio	$N_{\mathrm{E-cap}}$	N_{Film}	C_{Film} (μF)	$C_{\mathrm{E-cap}}$ (μF)	T_h (°C)	Vol (cm^3)	P_{loss} (w)	Lifetime (years)	Cost (USD)
Optimization I	1.6%	9	16	72.96	4487.04	47.4	617.22	9.96	7.7	79.79
Optimization II	1.7%	8	16	77.52	4482.48	48.6	623.25	9.99	7.1	79.18
Optimization III	1.9%	7	16	86.64	4473.36	49.9	643.04	9.95	6.5	79.53
Optimization IV	2.1%	6	16	95.76	4464.24	51.5	662.83	9.93	5.8	79.88
Knee point I	0.2%	20	6	9.12	4551.88	40.9	509.64	10.24	12.1	83.64
Knee point II	2.7%	7	16	123.12	4436.88	48.8	753.16	9.35	7.0	87.22
Knee point III and IV	0.1%	20	3	4.56	4555.44	41.1	495.88	10.37	12.0	82.67

in parallel from 5 to 20, the volume and cost of the capacitor bank increase and power loss reduces. Based on the design constraints shown in Table IV, the solutions which can fulfill the design targets can be selected, as shown in Table V.

2) Optimization With Pareto Front: Knee points are defined as a set of Pareto optimal solutions for which an improvement in one objective will result in a severe degradation in at least another one [40]. According to the distances of all solutions in the Pareto front to extreme line, the knee point will be selected. Two extreme point [i.e., in Fig. 33(a), maximum and minimum power loss point] will determine the extreme line and the mathematical form of the extreme line can be defined as follows [41]:

$$Ax + By + C = 0 \tag{26}$$

where $-\frac{A}{B}$ represent the slope of the extreme line and C is the intercept of the line. The distance to extreme line calculated by (27) to fix the point can be treated as a knee point

$$d_i = \frac{|Ax_i + By_i + C|}{\sqrt{A^2 + B^2}} \tag{27}$$

where d_i represented the distance from the ith solution in the Pareto front to the extreme line. According to the idea of the distance to the extreme line method, the maximum distances $d_{\max} = \max(d_i)$ will be selected as knee point. For example, d_1, d_2, and d_3 represent the distance of these three nondominated solutions in the Pareto front. Of all the nondominated solutions, distance d_2 is the longest so that it is the knee point. The knee point between the objective function of cost, loss, volume, and lifetime is shown in Table V. Knee points I and II indicate that after this point, increasing the parallel number and the hybrid capacitance ratio does not result in a large loss reduction, but rather a large increase in volume and cost. Knee points III and IV indicate that after this points, increasing the volume and cost of the capacitors can not lead to a significant improvement in lifetime. Compared with the other knee points, knee points III and IV that use 20 450 V/220 μF E-caps and three 450 V/1.5 μF Film-caps connected in parallel is able to achieve higher lifetime and lowest volume and cost.

V. CONCLUSION

This article proposes a model-based multiobjective design method for hybrid capacitor banks. Based on the detailed modeling of capacitors in terms of electrical, thermal, and physical characteristics, the performance space of capacitor bank can be obtained. By optimizing the hybrid capacitance ratio among types of capacitors and the numbers of capacitor connected in parallel, the possible solutions that can achieve specified design constraints and the knee points of Pareto optimal solutions can be obtained. The model based design method is helpful for automatic design in Industry 4.0. The component sizing and selection procedure is able to be described as a program and be integrated as a function of the system model for optimal design, instead of experience-based design. From the case study, the following conclusions can be drawn.

1) These electrical, thermal, and physical models of 450-V series capacitors provided in this article are general ones with acceptable error, which can be extended to other applications with the same voltage rating with minimum adaptation.
2) The selection of hybrid capacitance ratio between types of capacitors depends on the component parameters and the electrical profile, which affects the reliability and the physical performance of the capacitor bank. The hybrid capacitance ratio recommended in the case study is 3.4% at the maximum slop point, which achieves 37.1% lifetime extension and 41.1% and 88.8% cost and volume rise, respectively, compared with the capacitor bank with 100% E-caps.
3) The numbers of capacitors connected in parallel affect the impedance characteristics and physical performance space of the capacitor bank. In this case study, 12 E-caps connected in parallel at the maximum slop point are recommended, which achieve 31.7% and 7.5% volume and cost reduction while 11.7% lifetime reduction, compared with the bank with 17 E-caps connected in parallel.
4) For a 5.5-kW PV application, the design of the capacitor bank with specified constraints and the design at the knee points from the Pareto optimization are identified. It proves the feasibility and the accuracy of the proposed multiobjective design method by comparing the performance of virtual design with optimized parameters and other design parameters. The proposed design method can be applied to other applications as well.

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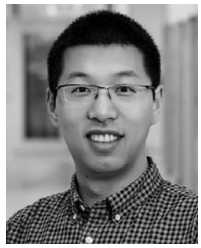

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