# High Step-Up DC–DC Converter With Zero Voltage Switching and Low Input Current Ripple

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***Abstract*—A high step-up dc–dc converter is proposed in this article. With magnetic-coupling-based voltage multiplier technique, the proposed converter achieves high voltage gain and low switch voltage stress. Also, due to a boost inductor at the input, continuous input current is obtained, which is beneficial for battery, fuel cell, and photovoltaic applications. Moreover, zero voltage switching of the MOSFETs is achieved, leading to low switching losses. Furthermore, zero dc bias of the coupled inductor is realized, resulting in small magnetic size and low core losses. The operation principles, performance analysis, and design considerations of the proposed converter are discussed. A prototype with 40-V input and 400-V output has been developed to verify the theoretical analysis.**

***Index Terms*—Continuous input current, coupled inductor, high gain, high step-up converter, zero dc bias, zero voltage switching.**

## I. Introduction

MANY applications call for high step-up dc–dc converters. For example, a high-intensity-discharge lamp ballast requires a high step-up converter to boost 12 high-intensity-discharge V battery voltage to more than 100 V [1]. In network server power supplies, the high step-up converter is needed to increase the 48 V of the dc battery plant to a 380 high-intensity-discharge V intermediate bus voltage [2]. In renewable energy systems, a front-end dc–dc converter is needed to step up the low voltage of photovoltaic modules or fuel cells to a sufficient dc-link voltage for grid connection [3]. High step-up converters may also find applications in other systems such as piezoelectric element drive and uninterruptible power supplies.

The conventional boost converter is not suitable in high step-up applications due to high voltage stress and high power losses. Various voltage-boosting techniques have been reported [4]. High step-up converters utilizing the switched capacitor (SC) technique have been proposed [5]–[9]. By adopting multiple SC cells, extended voltage gain and reduced semiconductor voltage stresses are achieved, but the component count could be large in high step-up applications. Utilizing magnetic coupling has attracted much attention in high conversion ratio applications. Magnetic coupling provides an extra degree of freedom, i.e., the voltage gain is not only adjusted by the duty cycle but also extended by the turns ratio. Thus, high voltage gain can be achieved with a relatively low number of components. However, the leakage inductance of magnetic coupling components may cause a high voltage spike across the switches. Clamp circuits can be employed to absorb the leakage energy and improve efficiency [1]. In [10]–[14], magnetic coupling integrated with the SC (or voltage multiplier) has been utilized to further extend the voltage gain and recycle the leakage energy. Three-winding coupled-inductor based converters were also proposed for high gain applications [15]. More design degrees of freedom are obtained with increased circuit complexity. The converters, using the magnetic coupling technique may suffer from pulsating input current. The input current ripple becomes even larger when the power level or turns ratio is increased. Hence, large electrolytic input capacitor is needed, which increases the cost, degrades the efficiency, and limits the lifetime of the system [16]. Utilizing the interleaving technique is an effective way for magnetically coupled converters to reduce the input current ripple [17], [18]. It is more suitable for high power applications. Some single-phase coupled-inductor converters with low input current ripples have also been reported in the literature. In [19] and [20], a combination of quadratic boost and coupled inductor techniques were proposed. In [21]–[24], Sepic-based coupled-inductor converters were introduced. In [25], a quasi-Y-source dc–dc converter was reported. These converters achieve high voltage gain due to the magnetic coupling and obtain continuous input current with the aid of a discrete inductor at the input side. Unfortunately, the switches are turned ON under hard switching, which may lead to high switching losses at high switching frequencies. Also, the coupled inductor in these converters has a large dc bias current, resulting in poor core utilization and high core losses [26].

Soft-switching methods for high step-up converters have been proposed in the literature to improve efficiency and potentially allow size reduction under high-frequency operation. The converters, proposed in [27]–[29], achieve zero-current switching in order to reduce switching loss. Unfortunately, the conduction loss is increased due to resonant operation. In [30] and [31], zero-voltage-switching (ZVS) step-up converters were proposed, but the voltage gain is still low. In [32]–[34], an active clamp

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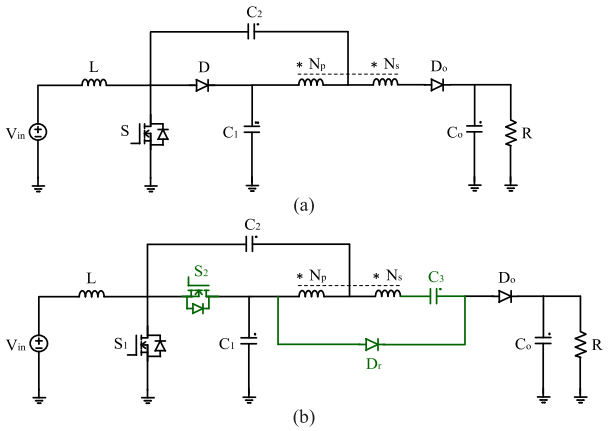



Fig. 1. (a) Converter in [42]. (b) Proposed converter.

circuit is employed in coupled-inductor converters to realize ZVS and high voltage gain. In [35] and [36], stacked ZVS coupled-inductor converters were introduced, where distributed capacitor voltage stress is obtained. In [37] and [38], high step-up converters with ZVS were proposed. The clamping switch and clamping capacitor not only help recycle the leakage energy but also boost the voltage gain. In [39], a step-up converter with minimum switch voltage stress was introduced. ZVS can be achieved by proper design of the inductance, but the voltage gain could be low for some applications. In [40] and [41], boost-derived ZVS high step-up converters were proposed. Unfortunately, the primary winding in these converters is not utilized for voltage gain extension, which may lead to large primary conduction loss.

In [42], a single-switch coupled-inductor boost converter was proposed, as shown in Fig. 1(a). It has advantages of extended voltage gain, continuous input current, alleviated diode reverse recovery and low component count. Based on this converter, a new converter is proposed by adding one capacitor and one diode, and replacing the boost diode with an active switch, as shown in Fig. 1(b). Compared to [42], the new converter not only retains continuous input current but also achieves the following improvements.

1) Higher voltage gain and lower switch and diode voltage stress are obtained due to the series connection of $C_3$ with the secondary winding.
2) Semiconductor voltage stresses are constant and independent of the operating point (i.e., duty cycle); hence the semiconductor devices can be operated safely without the danger of voltage breakdown when the input voltage varies.
3) Due to the charge balance of $C_2$ and $C_3$, the coupled inductor in the proposed converter has zero dc bias, resulting in small magnetic size and low core losses.
4) ZVS turn-ON of the switches is realized, leading to low switching losses.

The rest of this article is organized as follows. The description of the converter and the operation principles are provided in Section II. Performance analysis is presented in Section III. Design considerations are discussed in Section IV. Experimental results are presented in Section V. The conclusion is given in Section VI.

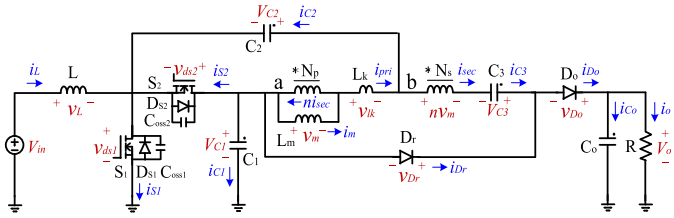



Fig. 2. Eequivalent circuit.

## II. Operation Principles

The proposed converter is composed of one input inductor, one coupled inductor, two switches, two diodes, three energy transfer capacitors, and one output capacitor. The two switches are driven complementary with dead time. Fig. 2 shows the equivalent circuit of the proposed converter. The coupled inductor is modeled as an ideal transformer with a magnetizing inductance ($L_m$) and leakage inductance ($L_k$). In order to simplify the analysis, the following assumptions are made: 1) all switches are composed of an ideal switch in parallel with its body-diode and drain-source capacitance; 2) all capacitors are large enough so that the voltages across them are constant without ripples. The key waveforms of the proposed converter are shown in Fig. 3. Eight modes are observed during one switching period. The corresponding circuits in each mode are shown in Fig. 4.

*Mode 1 [$t_0 - t_1$]:* Switch $S_1$ is ON, and switch $S_2$ is OFF. The current flow paths are shown in Fig. 4(a). The input inductor is being charged. The primary side of the coupled inductor is clamped at $V_{C1} - V_{C2}$, and the coupled inductor is magnetized. Capacitor $C_1$ is transferring a portion of its energy to $C_2$, and meanwhile, delivering the other portion of the energy from primary winding $N_p$ to secondary winding $N_s$ to charge capacitor $C_3$ through diode $D_r$. The output capacitor releases energy to the load. The following equations can be obtained in this mode. As the leakage inductance is very small compared to the magnetizing inductance, the voltage of the leakage inductance has been neglected in the equations

$$v_L = V_{\text{in}} \tag{1}$$

$$v_m = V_{C1} - V_{C2} \tag{2}$$

$$(n+1)\, v_m = V_{C3} \tag{3}$$

$$i_{\text{Dr}} = -i_{\text{sec}} = \frac{(n+1)\,(V_{C1} - V_{C2}) - V_{C3}}{n^2 L_k} t;$$

$$i_{\text{pri}} = i_m - n i_{\text{sec}}. \tag{4}$$

*Mode 2 [$t_1 - t_2$]:* At $t_1$, switch $S_1$ is turned OFF. The output capacitances ($C_{\text{oss1}}$/$C_{\text{oss2}}$) of the switches are being charged/discharged, as shown in Fig. 4(b). The voltage $v_{\text{ds1}}$ across $S_1$ is increasing and the voltage $v_{\text{ds2}}$ across $S_2$ is decreasing. This mode ends when $v_{\text{ds1}}$ rises to $V_{C1}$ and $v_{\text{ds2}}$ drops to zero.

*Mode 3 [$t_2 - t_3$]:* At $t_2$, as $v_{\text{ds2}}$ becomes zero, the body-diode of $S_2$ conducts, as shown in Fig. 4(c). A voltage of $-V_{C2}$ is applied to the primary side of the coupled inductor. Therefore, $i_{\text{lk}}$ is decreasing linearly, which makes $i_{\text{Dr}}$ decreasing linearly. The current changing rate is controlled by the leakage inductance

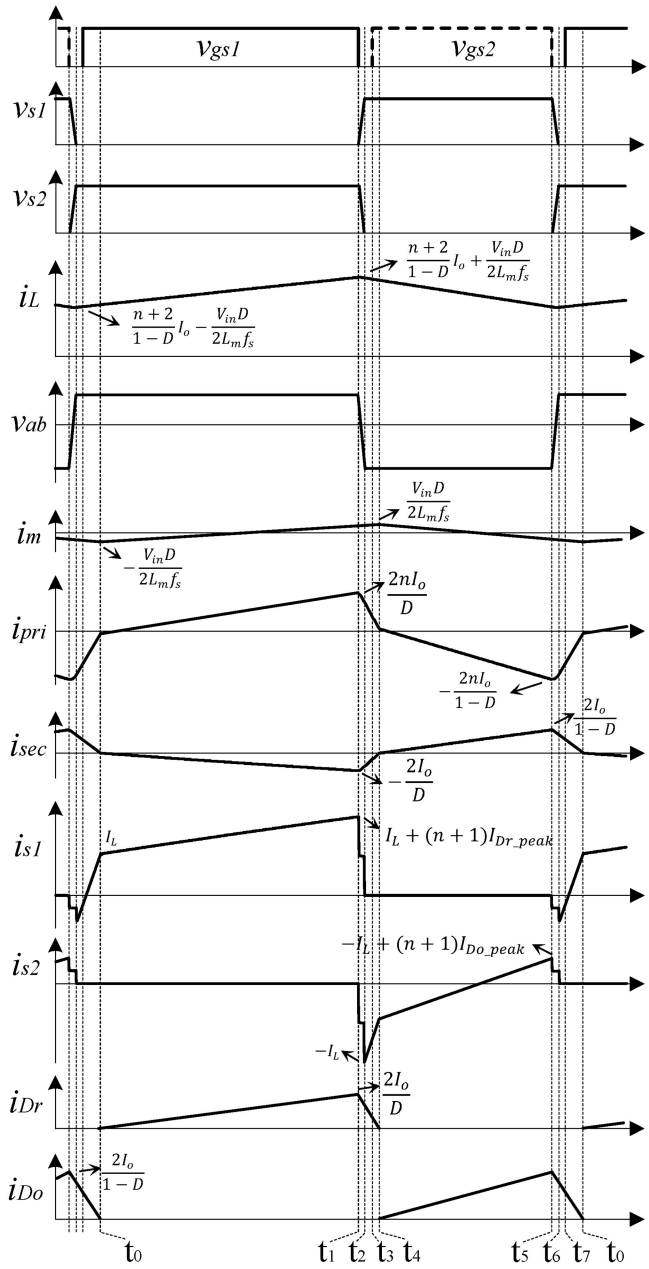



Fig. 3. Key waveforms.

of the coupled inductor. The following equation can be obtained in this mode

$$i_{\mathrm{Dr}} = -i_{\mathrm{sec}} = i_{\mathrm{Dr}}(t_2) - \frac{V_{C3} + (n+1)V_{C2}}{n^2 L_k} t. \qquad (5)$$

*Mode 4 [$t_3 - t_4$]:* At $t_3$, switch $S_2$ is turned ON under ZVS, as shown in Fig. 4(d). The other circuit conditions are the same as in the last mode. Equation (5) still holds.

*Mode 5 [$t_4 - t_5$]:* At $t_4$, $i_{\mathrm{Dr}}$ decreases to zero and then $D_r$ is naturally turned OFF, which alleviates the reverse recovery problem. The secondary current $i_{\mathrm{sec}}$ changes its direction and diode $D_o$ starts conducting. The primary side of the coupled inductor is still clamped at $-V_{C2}$, and the coupled inductor is demagnetized. The current flow paths are shown in Fig. 4(e). The

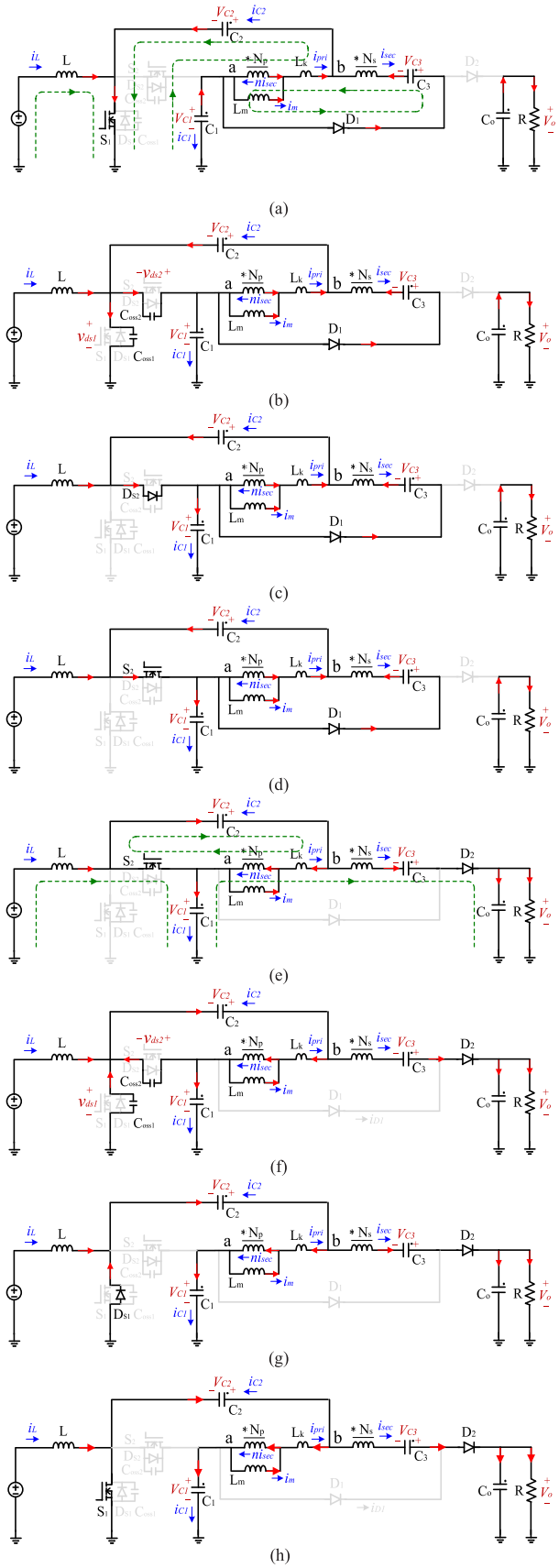



Fig. 4. Operation modes. (a) Mode 1 [$t_0 - t_1$]. (b) Mode 2 [$t_1 - t_2$]. (c) Mode 3 [$t_2 - t_3$]. (d) Mode 4 [$t_3 - t_4$]. (e) Mode 5 [$t_4 - t_5$]. (f) Mode 6 [$t_5 - t_6$]. (g) Mode 7 [$t_6 - t_7$]. (h) Mode 8 [$t_7 - t_0$].

boost inductor together with the input source is delivering energy to capacitor $C_1$. At the same time, capacitor $C_2$ is releasing energy via the coupled-inductor windings to the load. Meanwhile, the primary and secondary windings are linked in series with $C_1$ and $C_3$ to support the load. The following equations can be obtained in this mode

$$v_L = V_{\text{in}} - V_{C1} \tag{6}$$

$$v_m = -V_{C2} \tag{7}$$

$$-(n+1)\,v_m + V_{C1} + V_{C3} = V_o \tag{8}$$

$$i_{\text{Do}} = i_{\text{sec}} = \frac{V_{C1} + (n+1)\,V_{C2} + V_{C3} - V_o}{n^2 L_k} t;$$

$$i_{\text{pri}} = i_m - n i_{\text{sec}}. \tag{9}$$

*Mode 6 [$t_5 - t_6$]:* At $t_5$, switch $S_2$ is turned OFF. The output capacitances ($C_{\text{oss1}}$/$C_{\text{oss2}}$) of the switches are being discharged/charged, as shown in Fig. 4(f). $v_{\text{ds2}}$ is increasing and $v_{\text{ds1}}$ is decreasing. This mode ends when $v_{\text{ds2}}$ rises to $V_{C1}$ and $v_{\text{ds1}}$ drops to zero.

*Mode 7 [$t_6 - t_7$]:* At $t_6$, as $v_{\text{ds1}}$ becomes zero, the body-diode of $S_1$ conducts, as shown in Fig. 4(g). A voltage of $V_{C1} - V_{C2}$ is applied to the primary side of the coupled inductor. Therefore, $i_{\text{lk}}$ is decreasing linearly in the opposite direction, which makes $i_{\text{Do}}$ decreasing linearly. The current changing rate is controlled by the leakage inductance of the coupled inductor. The following equation can be obtained in this mode:

$$i_{\text{Do}} = i_{\text{sec}} = i_{\text{Do}}(t_6) - \frac{nV_{C1} + V_o - (n+1)\,V_{C2} - V_{C3}}{n^2 L_k} t. \tag{10}$$

*Mode 8 [$t_7 - t_0$]:* At $t_7$, switch $S_1$ is turned ON under ZVS, as shown in Fig. 4(h). The other circuit conditions are the same as in the last mode. Equation (5) still holds. This mode ends when $i_{\text{Do}}$ decreases to zero. At $t_0$, $D_o$ is naturally turned OFF, which alleviates the reverse recovery problem. After $t_0$, mode 1 begins.

## III. Performance Analysis

### A. Voltage Gain

In order to derive the ideal voltage gain, the effect of the leakage inductance and the transitional modes are neglected. By applying the voltage-second balance principle to $L$ and $L_m$, the following equations are obtained:

$$V_{\text{in}} D + (V_{\text{in}} - V_{C1})(1 - D) = 0 \tag{11}$$

$$(V_{C1} - V_{C2})\,D - V_{C2}(1 - D) = 0. \tag{12}$$

Solving (11) and (12), the voltages of $C_1$ and $C_2$ are obtained as

$$V_{C1} = \frac{V_{\text{in}}}{1 - D} \tag{13}$$

$$V_{C2} = D V_{C1}. \tag{14}$$

Solving (2) and (3), the voltage relationship between the capacitors is derived as

$$(n+1)(V_{C1} - V_{C2}) = V_{C3}. \tag{15}$$

Then the voltage of $C_3$ is obtained as

$$V_{C3} = (n+1)(1 - D) V_{C1}. \tag{16}$$

Solving (7) and (8), the following relationship is derived:

$$V_{C1} + (n+1) V_{C2} + V_{C3} = V_o. \tag{17}$$

Then $V_o$ is calculated as

$$V_o = (n+2) V_{C1}. \tag{18}$$

Substituting (13) into (18), the voltage gain of the proposed converter can be expressed as

$$M = \frac{V_o}{V_{\text{in}}} = \frac{n+2}{1 - D}. \tag{19}$$

In order to add the leakage inductance effect into the voltage gain, the diode current waveforms should be evaluated as the leakage inductance determines the slopes of the diode currents. Due to the charge balance of the output capacitor $C_o$, the average current of $D_o$ equals to the output current, which is given by

$$I_{\text{Do\_avg}} = I_{\text{Co\_avg}} + I_o = I_o. \tag{20}$$

Due to the charge balance of capacitor $C_3$, the average current of $D_r$ equals to the average current of $D_o$, which is given by

$$I_{\text{Dr\_avg}} = I_{\text{Do\_avg}} - I_{C3\_\text{avg}} = I_o. \tag{21}$$

As the switching transitional intervals are very short compared to the power delivery modes, they are neglected in order to simplify the calculation. Then from the diode current waveforms, the following equations are obtained:

$$\frac{1}{2} D T_s \cdot \frac{(n+1)(V_{C1} - V_{C2}) - V_{C3}}{n^2 L_k} \cdot D T_s = I_o T_s \tag{22}$$

$$\frac{1}{2}(1 - D) T_s \cdot \frac{V_{C1} + (n+1) V_{C2} + V_{C3} - V_o}{n^2 L_k} \cdot (1 - D) T_s = I_o T_s. \tag{23}$$

In addition, according to the KVL, the following relationship is obtained:

$$-V_{\text{in}} + V_{L\_\text{avg}} - V_{C2} - V_{\text{lk\_avg}} - V_{m\_\text{avg}} + V_{C1} = 0 \tag{24}$$

where $V_{L\_\text{avg}}$, $V_{\text{lk\_avg}}$, and $V_{m\_\text{avg}}$ are the average voltages of the inductances in one switching period. According to the voltage-second balance principle, they are equal to zero. Hence, (24) can be rewritten as

$$V_{C1} - V_{C2} = V_{\text{in}}. \tag{25}$$

By applying the voltage-second balance to the boost inductor, $V_{C1}$ still holds as in (13).

Solving (13), (22), (23), and (25), the voltage gain considering the leakage inductance can be expressed by

$$M = \frac{V_o}{V_{\text{in}}} = \frac{n+2}{1 - D} \cdot \frac{1}{1 + 2n^2 Q\left(\frac{1}{D^2} + \frac{1}{(1-D)^2}\right)} \tag{26}$$

where $\text{Q} = L_k f_s / R$.

Fig. 5 shows the voltage gain with the effect of the leakage inductance. As the leakage inductance increases, the voltage gain decreases, especially at high duty cycles. If the leakage inductance is ignored, (26) will be equal to (19).

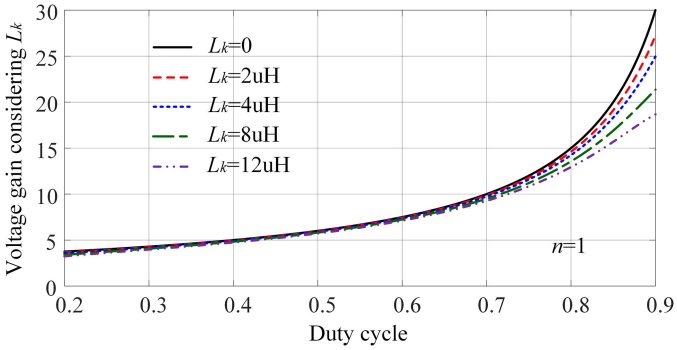



Fig. 5. Voltage gain considering the effect of leakage inductance (assuming $f_s = 100$ kHz and $R_o = 400\ \Omega$).

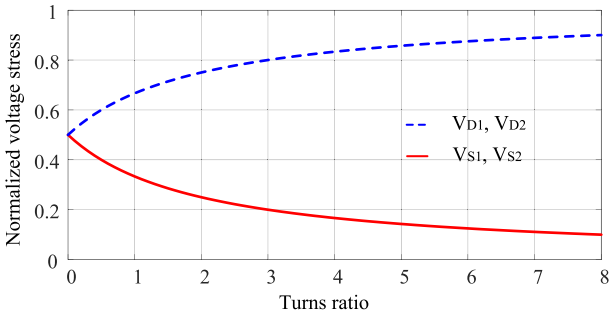



Fig. 6. Semiconductor voltage stresses normalized to output voltage.

### B. Voltage and Current Stresses

The voltages of the two switches are clamped by $V_{C1}$. Thus, the voltage stress of the switches is expressed as

$$V_{S1} = V_{S2} = \frac{1}{1-D}V_{\text{in}} = \frac{1}{n+2}V_o. \tag{27}$$

The voltage stress of the switches is only a small fraction of the output voltage. Therefore, low-voltage-rating MOSFETs with small on-resistance can be adopted to lower the conduction loss.

The voltages of the two diodes are clamped by $V_o - V_{C1}$. Thus, the voltage stresses of the diodes are given by

$$V_{\text{Dr}} = V_{\text{Do}} = \frac{n+1}{1-D}V_{\text{in}} = \frac{n+1}{n+2}V_o. \tag{28}$$

The semiconductor voltage stresses normalized to output voltage under different turns ratio are plotted in Fig. 6. The switch voltage stress becomes lower as the voltage gain is extended by increasing the turns ratio. The diode voltage stress increases with the turns ratio, but they are always lower than the output voltage.

The average currents of the diodes equal to the output current, as shown in (20) and (21). The peak currents of the diodes can be expressed by

$$I_{\text{Dr\_peak}} = \frac{2I_o}{D} \tag{29}$$

$$I_{\text{Do\_peak}} = \frac{2I_o}{1-D}. \tag{30}$$

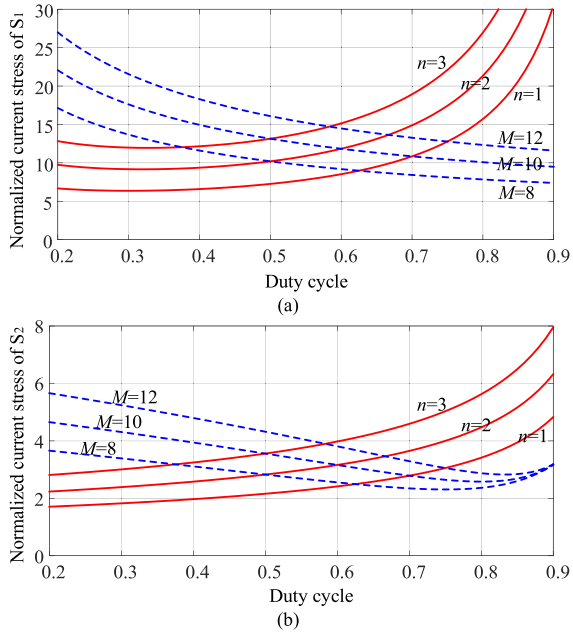



Fig. 7. Switch rms current stress normalized by output current under different turns ratio $n$ and voltage gain $M$. (a) $S_1$. (b) $S_2$.

From the steady-state analysis, the average currents of the switches are calculated as

$$I_{S1\_\text{avg}} = \frac{D+n+1}{1-D}I_o \tag{31}$$

$$I_{S2\_\text{avg}} = I_o. \tag{32}$$

The rms currents of the switches can be evaluated as

$$I_{S1\_\text{rms}} = I_o\sqrt{\frac{4(n+1)^2}{3D} + \frac{2(n+1)(n+2)}{1-D} + \frac{D(n+2)^2}{(1-D)^2}} \tag{33}$$

$$I_{S2\_\text{rms}} = I_o\sqrt{\frac{4(n+1)^2 - 3n(n+2)}{3(1-D)}}. \tag{34}$$

The switch rms currents normalized by the output current are plotted Fig. 7. It can be seen that the switch current stresses increase with the turns ratio under given voltage gain.

The rms currents through the windings of the coupled inductor can be evaluated as

$$I_{\text{pri\_rms}} = \frac{2nI_o}{\sqrt{3D(1-D)}} \tag{35}$$

$$I_{\text{sec\_rms}} = \frac{2I_o}{\sqrt{3D(1-D)}}. \tag{36}$$

### C. DC Offset of the Magnetizing Current

In the proposed converter, zero magnetizing current can be achieved due to the charge balance of capacitor $C_2$ and $C_3$. As the secondary winding of the coupled inductor is connected in series with capacitor $C_3$, the average secondary current is given by

$$I_{\text{sec\_avg}} = I_{C3\_\text{avg}} = 0. \tag{37}$$

The primary current is the sum of the current of capacitor $C_2$ and the secondary current. Hence, the average primary current is

$$I_{\text{pri\_avg}} = I_{\text{sec\_avg}} + I_{C2\_\text{avg}} = 0. \tag{38}$$

Then the dc magnetizing current is derived by

$$I_{m\_\text{dc}} = I_{\text{pri\_avg}} + nI_{\text{sec\_avg}} = 0. \tag{39}$$

It can be seen that the coupled inductor in the proposed converter has zero dc bias due to the charge balance of the capacitors.

According to the magnetic theory, core area $A_c$ is expressed by

$$A_c = \frac{L_m\left(I_m + \Delta i_m/2\right)}{NB_{\max}} \tag{40}$$

where $\Delta i_m$ is the magnetizing current ripple, *N* is the primary number of turns, and $B_{\text{mas}}$ is the maximum flux density of the core. As can be seen, zero dc bias ($I_m = 0$) helps reduce the magnetic size.

In addition, as studied in [43]–[45], the loss of the core under dc bias condition could be much larger than that with no bias. Therefore, zero dc bias would also help reduce core losses.

### *D. Impact of Inductor Resistance on the Voltage Gain*

If inductor resistance $r_L$is considered, the voltage-second balance of the inductor is rewritten as

$$\left(V_{\text{in}} - I_L r_L\right) D + \left(V_{\text{in}} - V_{C1} - I_L r_L\right)(1 - D) = 0. \tag{41}$$

Then $V_{C1}$ is calculated as

$$V_{C1} = \frac{V_{\text{in}} - I_L r_L}{1 - D}. \tag{42}$$

The relationship of the capacitor voltages and output voltage shown in (14), (16), and (18) still hold when inductor resistance is considered.

The inductor current $I_L$ can be solved by the charge balance of the capacitors, which are expressed as

$$\int_{DT}^{T} i_{C3}dt - \int_{DT}^{T} I_o dt = \int_{0}^{DT} I_o dt \tag{43}$$

$$\int_{DT}^{T} i_{C3}dt = \int_{0}^{DT} i_{C3}dt \tag{44}$$

$$\int_{DT}^{T} i_{C2}dt = \int_{0}^{DT} i_{C2}dt \tag{45}$$

$$\int_{DT}^{T} i_{C1}dt = \int_{0}^{DT} i_{C1}dt. \tag{46}$$

According to KCL, the following relationships can be obtained:

$$\int_{DT}^{T} i_L dt = \int_{DT}^{T} i_{C1}dt + \int_{0}^{DT} i_{C3}dt \tag{47}$$

$$\int_{DT}^{T} i_{C2}dt = \int_{DT}^{T} \left(i_{\text{pri}} - i_{\text{sec}}\right)dt = -(n+1)\int_{0}^{DT} i_{C3}dt \tag{48}$$

$$\int_{0}^{DT} i_{C1}dt = -\int_{0}^{DT} i_{C2}dt. \tag{49}$$

By solving (42)–(48), the inductor current is calculated as

$$I_L = \frac{n+2}{1-D} I_o \tag{50}$$

where $I_o = V_o/R$.

By combining (18), (42), and (50), the voltage gain considering the inductor resistance is expressed by

$$\frac{V_o}{V_{\text{in}}} = \frac{n+2}{1-D} \cdot \frac{1}{1 + \frac{(n+2)^2}{(1-D)^2} \cdot \frac{r_L}{R}}. \tag{51}$$

### *E. ZVS Condition*

The switches in the proposed converter are turned ON under ZVS, leading to low switching loss. ZVS turn-ON can be achieved by gating on the switch while the body-diode is conducting.

According to mode 2, ZVS of switch $S_2$ is always achieved because the input inductor current helps charge/discharge the output capacitances.

According to mode 6, in order to achieve ZVS of switch $S_1$, the following two conditions must be satisfied.

1) $i_L(t_5) + i_{C2}(t_5)$ must be smaller than zero in order to discharge $C_{\text{oss1}}$ and charge $C_{\text{oss2}}$.
2) The inductive energy available must be sufficient so that $i_L + i_{C2}$ will still remain negative after $C_{\text{oss1}}$/$C_{\text{oss2}}$ are completely discharged/charged. Then the current could flow through the body-diode of $S_1$ and thus ZVS can be achieved.

$i_L + i_{C2}$ at the switching point can be written as

$$\begin{aligned} i_L\left(t_5\right) + i_{C2}\left(t_5\right) &= i_L\left(t_5\right) + i_m\left(t_5\right) - (n+1)\, i_{\text{sec}}\left(t_5\right) \\ &= I_L - \frac{\Delta i_L}{2} - \frac{\Delta i_m}{2} - (n+1)\, I_{\text{Do\_peak}} \end{aligned} \tag{52}$$

where $\Delta i_L$ and $\Delta i_m$ are the peak-to-peak current ripples of the boost inductor and magnetizing inductance, respectively, They are given by

$$\Delta i_L = \frac{V_{\text{in}} D}{L f_s};\ \Delta i_m = \frac{V_{\text{in}} D}{L_m f_s}. \tag{53}$$

Substituting (30), (50), and (53) into (52), (52) is rewritten as

$$i_L\left(t_5\right) + i_{C2}\left(t_5\right) = -\frac{nI_o}{1-D} - \frac{V_{\text{in}} D}{2f_s}\left(\frac{1}{L} + \frac{1}{L_m}\right) < 0. \tag{54}$$

Therefore, the first condition for ZVS of $S_1$ is always achieved. To satisfy the second condition, the following must be satisfied:

$$\begin{aligned} &\frac{1}{2} L_k (nI_{\text{Do\_peak}})^2 - \frac{1}{2} L_k \left(\frac{n}{n+1} I_L\right)^2 \\ &\quad > \frac{1}{2}\left(C_{\text{oss1}} + C_{\text{oss2}}\right)\ {V_{C1}}^2. \end{aligned} \tag{55}$$

TABLE I
COMPARISON OF THE PROPOSED CONVERTER TO OTHER ZVS CONVERTERS

| Topologies | [30] | [31] | [32] | [33] | [39] | [40], [41] | PROPOSED |
|---|---|---|---|---|---|---|---|
| Switches | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Diodes | 2 | 5 | 2 | 3 | 3 | 2 | 2 |
| Capacitors | 3 | 3 | 3 | 4 | 4 | 4 | 4 |
| Voltage gain | $\frac{2}{1-D}$ | $\frac{3-D}{1-D}$ | $\frac{n+1}{1-D}$ | $\frac{n+1}{1-D}$ | $2+n(1+D)$ | $\frac{n+1}{1-D}$ | $\frac{n+2}{1-D}$ |
| Switch voltage stress | $\frac{V_o}{2}$ | $\frac{2V_o}{3-D}$ | $\frac{V_o}{n+1}$ | $\frac{V_o}{n+1}$ | $\frac{V_o}{2+n(1+D)}$ | $\frac{V_o}{n+1}$ | $\frac{V_o}{n+2}$ |
| Max. diode voltage stress | $\frac{V_o}{2}$ | $\frac{2V_o}{3-D}$ | $V_o$ | $\frac{nV_o}{n+1}$ | $\frac{(n+1)V_o}{2+n(1+D)}+\frac{I_oT_s}{2C}$ | $\frac{nV_o}{n+1}$ | $\frac{(n+1)V_o}{n+2}$ |
| Input current | Continuous | Pulsating | Pulsating | Pulsating | Pulsating | Continuous | Continuous |

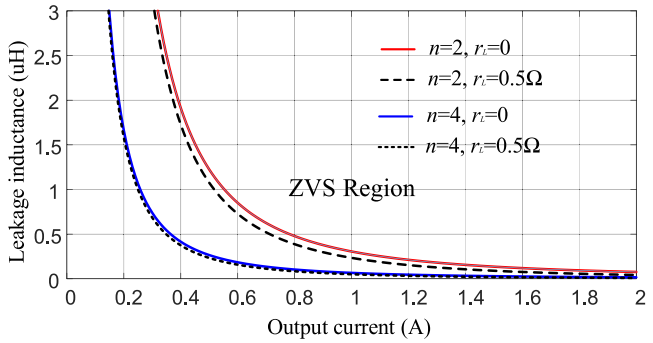



Fig. 8. ZVS condition (assuming $V_{\text{in}} = 40$ V, $V_o = 400$ V, and $C_{\text{oss1}} = C_{\text{oss2}} = 0.85$ nF).

Substituting (13), (41), and (50) into (55), the ZVS condition can be rewritten as

$$\left(4-\frac{(n+2)^2}{(n+1)^2}\right)n^2L_k{i_o}^2 > (C_{\text{oss1}}+C_{\text{oss2}})\,{V_{\text{in}}}^2. \quad (56)$$

The inductor resistance $r_L$ has a slight impact on the ZVS condition. As mentioned above, if inductor resistance is considered, $V_{C1}$ is expressed by (42). Substituting (42) into (55), the ZVS condition is manipulated as

$$\left(4-\frac{(n+2)^2}{(n+1)^2}\right)n^2L_k{i_o}^2 > (C_{\text{oss1}}+C_{\text{oss2}}) \times\left(V_{\text{in}}-\frac{n+2}{1-D}I_or_L\right)^2. \quad (57)$$

The leakage inductance versus output current is plotted in Fig. 8. As can be seen, the larger turns ratio or larger leakage inductance lead to a wider ZVS range. Also, it is easier to achieve ZVS when the output current increases. Inductor resistance has little impact on the ZVS region especially when $r_L$ is small.

In addition, it is seen from (56) that higher input voltage makes it harder to achieve ZVS due to larger capacitive energy. Therefore, the maximum input voltage is the worst case for design in order to satisfy the ZVS requirement.

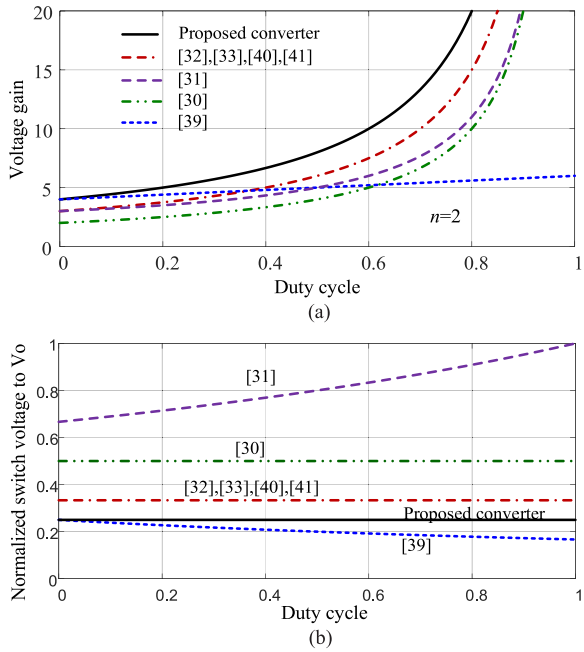



Fig. 9. Comparison. (a) Voltage gain. (b) Normalized switch voltage stress.

## F. Comparison

Table I provides a comparison of the proposed converter to other ZVS high step-up converters. The number of components, voltage gain, switch voltage stress, maximum diode voltage stress, and the feature of the input current are listed in Table I.

Compared to the other converters, the proposed converter achieves higher voltage gain, as illustrated in Fig. 9(a). Compared to [30]–[33] and [40], [41], the proposed converter achieves lower switch voltage stress, as shown in Fig. 9(b), thus low-voltage-rating MOSFET with small on-resistance can be used to lower conduction loss. The proposed converter has higher switch voltage stress compared to [39], however, it can achieve much higher voltage gain with a lower component count. Furthermore, the proposed converter features continuous input current, which is advantageous in the battery, fuel cell, and photovoltaic applications.

TABLE II
COMPARISON OF THE PROPOSED CONVERTER WITH [42]

| Topologies | PROPOSED | [42] |
|---|---|---|
| Voltage gain | $\frac{n+2}{1-D}$ | $\frac{1+(n+1)D}{1-D}$ |
| Switch voltage stress | $\frac{1}{n+2}V_o$ (Independent of operating point) | $\frac{1}{1+(n+1)D}V_o$ (dependent on operating point) |
| Diode voltage stress | $\frac{n+1}{n+2}V_o$ (Independent of operating point) | $\frac{n+1}{1+(n+1)D}V_o$ (dependent on operating point) |
| Average magnetizing current | Zero | $(n+1)I_o$ |
| ZVS of the switches? | Yes | No |
| Continuous input current? | Continuous | Continuous |

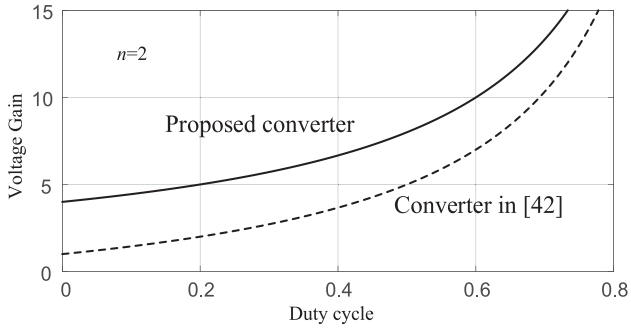



Fig. 10. Voltage gain of the proposed converter compared to [42].

The proposed converter is also compared with the converter in [42], as shown in Table II. The proposed converter achieves higher voltage gain and lower switch and diode voltage stresses, as illustrated in Figs. 10 and 11. Also, the switch and diode voltage stresses are constant and independent of the operating point (i.e., duty cycle). Hence the semiconductor devices can be operated safely without the danger of voltage breakdown when the input voltage varies. Furthermore, the coupled inductor in the proposed converter has zero dc bias, resulting in small magnetic size and low core losses. In addition, ZVS turn-ON of the switches is achieved in the proposed converter, leading to low switching losses.

## IV. DESIGN CONSIDERATIONS

In this section, a 40–400-V 400-W converter is considered as a design example. The switching frequency $f_s$ is chosen as 100 kHz.

### A. Coupled-Inductor Design

The turns ratio of the coupled inductors is determined by the required voltage gain and the duty cycle. A large duty

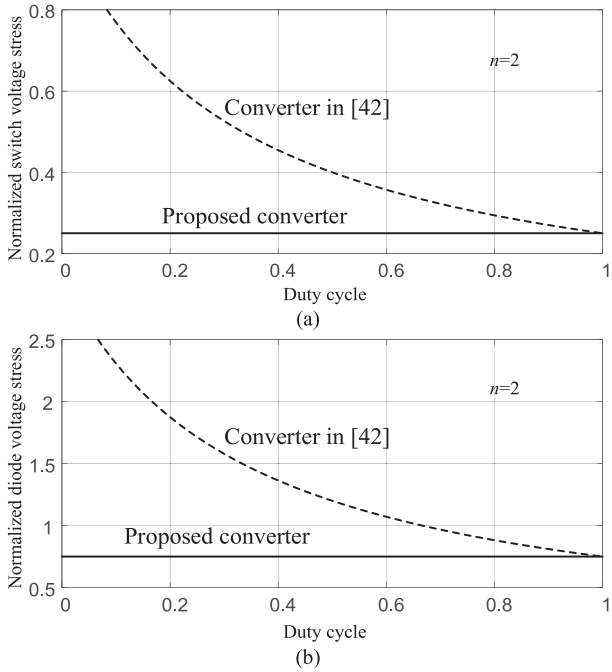



Fig. 11. Normalized semiconductor voltage stresses of the proposed converter compared to [42]. (a) Switch stress. (b) Diode stress.

cycle results in a low turns ratio, which would increase the switch voltage stress, leading to a use of higher voltage rating MOSFETs with larger on-resistance. On the other hand, if the duty cycle is too small, a high turns ratio is needed, which causes high conduction loss and large leakage inductance. Therefore, a compromise should be considered. In this design example, the duty cycle is selected as 0.6. Then the turns ratio is calculated as 2 according to (19).

The leakage inductance of the coupled inductor determines the boundary of the ZVS region. In this design example, the leakage inductance is designed to guarantee ZVS operation from 40%-load to 100%-load. According to (56), the minimum leakage inductance is calculated as 1.91 $\mu$H.

As zero dc bias is achieved, the design of the coupled inductor follows the transformer design method [46]. In practice, it may be difficult to accurately control the leakage inductance. The external inductor may be needed in order to satisfy the ZVS requirement [47].

### B. Input Inductor Design

The input inductor is designed based on the input current ripple requirement. Considering a peak-to-peak current ripple ($r_L\%$) of 25%, the boost inductor can be calculated by

$$L > \frac{V_{\text{in}}D}{r_L\% \cdot I_L f_s} = \frac{V_{\text{in}}\left(V_o - (n+2)\,V_{\text{in}}\right)}{r_L\% \cdot I_L f_s V_o} = 96\,\mu\text{H}. \quad (58)$$

### C. Semiconductor Selection

According to (27) and (28), the switch voltage stress is calculated as 100 V and the diode voltage stress is calculated as 300 V. Considering the voltage overshoot and ringing in practice,

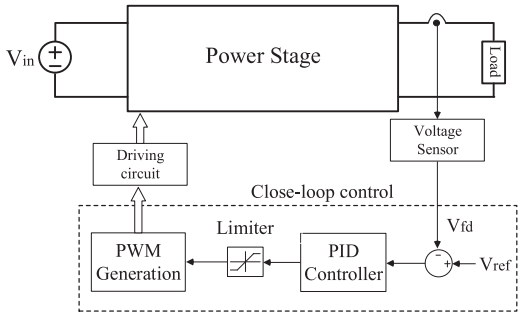



Fig. 12. Control scheme of the proposed converter.

150-V voltage-rating MOSFETs and 400-V voltage-rating diodes are selected in order to achieve reliable operation.

### D. Capacitor Design

The capacitors can be designed based on the voltage ripple and the output power. Assuming minimum voltage ripple ($r_c\%$) to be 2%, the calculations of the capacitors are given by

$$C_1 = \frac{(n+1)\,I_o}{r_c\% \cdot V_{c1} f_s} > 15\,\mu\text{F} \tag{59}$$

$$C_2 = \frac{(n+1)\,I_o}{r_c\% \cdot V_{c2} f_s} > 25\,\mu F \tag{60}$$

$$C_3 = \frac{I_o}{r_c\% \cdot V_{c3} f_s} > 4.2\,\mu\text{F} \tag{61}$$

where $V_{C1} = \frac{V_o}{n+2}$; $V_{C2} = \frac{V_o}{n+2} - V_{\text{in}}$ and $V_{C3} = (n+1)V_{\text{in}}$.

The rms current stress of the capacitors is calculated by

$$I_{C1\_\text{rms}} = I_o \sqrt{\frac{(n+1)^2 (4-D) + D}{3D\,(1-D)}} \tag{62}$$

$$I_{C2\_\text{rms}} = \frac{2\,(n+1)\,I_o}{\sqrt{3D\,(1-D)}} \tag{63}$$

$$I_{C3\_\text{rms}} = \frac{2I_o}{\sqrt{3D\,(1-D)}} \tag{64}$$

$$I_{\text{Corms}} = \frac{(1+D)\,I_o}{\sqrt{3D\,(1-D)}}. \tag{65}$$

Capacitors with low ESR are preferred in order to reduce power losses. It is a favorable solution that film capacitors or multilayer chip-type ceramic capacitors are adopted. In this design example, 30-$\mu$F film capacitors are selected.

### E. Control Scheme

The control scheme of the proposed converter is shown in Fig. 12. A PID controller is used to regulate the output voltage. In this design example, digital signal processor TMS320F28335 is adopted to implement the control.

By using the small-signal averaged modeling method and assuming that the capacitor charge balance is achieved, the control-to-output transfer function of the proposed converter is derived as

$$\frac{\hat{v}_o}{\hat{d}} = \frac{\frac{V_o}{1-D}\left(1 - \frac{(n+2)^2 L}{R(1-D)^2}\text{S}\right)}{1 + \frac{(n+2)^2 L}{R(1-D)^2}\text{S} + \frac{(n+2)^2 L C_o}{(1-D)^2}\text{S}^2}. \tag{66}$$

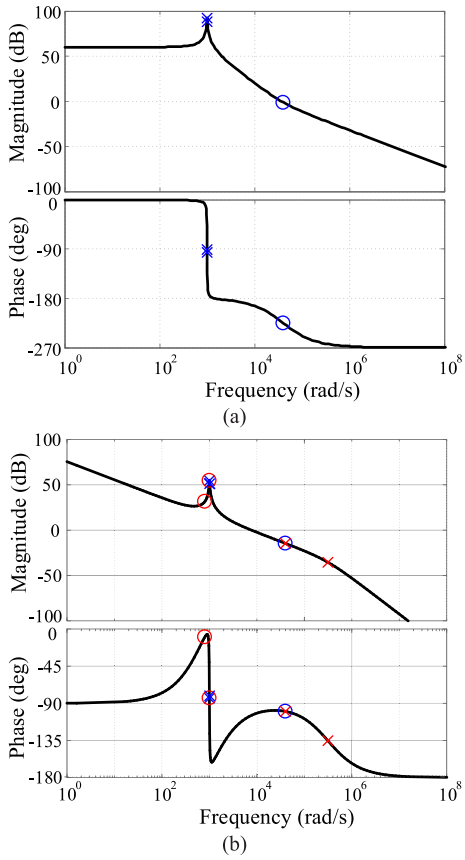



Fig. 13. Bode plot. (a) Before compensation. (b) After compensation. (Assuming $V_{\text{in}} = 40$ V, $V_o = 400$ V, $P_o = 400$W, $n = 2$, L $= 100\,\mu$H, and $C_o = 100\ \mu$F).

The bode plot of the converter is given in Fig. 13(a). Similar to the conventional boost converter, the proposed converter is a second-order system with a double pole and right-half-plane (RHP) zero.

The pulsewidth modulator and feedback sensor have constant gain. A practical PID controller can be expressed by

$$G_c(s) = G_{cm} \frac{\left(1 + \frac{\omega_L}{s}\right)\left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)\left(1 + \frac{s}{\omega_{P2}}\right)}. \tag{67}$$

The practical PID controller has two zeros, one origin pole and two nonzero poles, which have the capability to obtain zero steady-state error, good phase margin, and wide bandwidth. The discussion of controller parameters is given below.

1) The pole at origin increases the low-frequency loop gain, such that the steady-state error to a step reference is zero.
2) The two zeros are placed around the double pole of the converter. This will counteract the effect of the double

TABLE III
KEY PARAMETERS OF THE PROTOTYPE

| Components | Parameters |
|---|---|
| Switches | IPA075N15N3 ($r_{on} = 7.5\ m\Omega$) |
| Diodes | MUR1640CT ($V_F = 1.3\ V$) |
| Coupled inductor | Turns ratio = 2<br>Magnetizing inductance = 208 uH<br>Leakage inductance = 2.6 uH<br>($r_{pri} = 50\ m\Omega, r_{sec} = 100\ m\Omega$) |
| Input inductor | 100 uH ($r_L = 30\ m\Omega$) |
| Capacitor $C_1$-$C_3$ | 30 uF film capacitor ($r_C = 12\ m\Omega$) |
| Capacitor $C_o$ | 2×56 uF electrolytic capacitor<br>($r_{Co} = 100\ m\Omega$) |

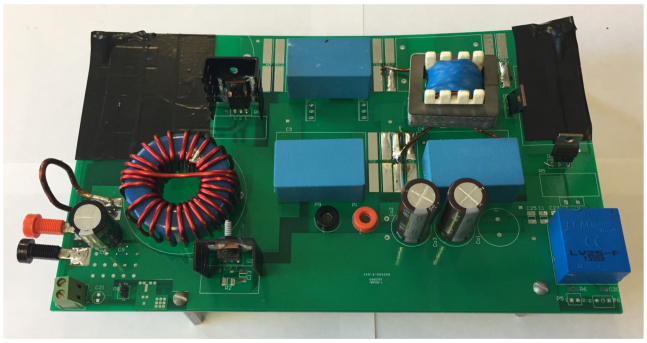


Fig. 14. Picture of the prototype.

pole so that the slope of the bode plot at crossover is about $-20$ dB/dec.

3) One of the nonzero poles is placed at the RHP zero of the converter to nullify the effect of RHP zero.
4) The other nonzero pole is placed at one half switching frequency to provide more attenuation at high frequencies.
5) The gain of the controller $G_{cm}$ shifts the magnitude plot up or down. $G_{cm}$ is selected to meet the required phase margin, which is typically greater than 50°.

In this design, compensation is performed with the aid of Matlab sisotool. The bode plot after compensation is given in Fig. 13(b).

## V. EXPERIMENTAL RESULTS

In order to verify the performance of the proposed converter, a 400-W 40-V input 400-V output prototype was built and tested. The switching frequency is 100 kHz. The duty cycle is around 0.6. The key parameters of the prototype are listed in Table III. A picture of the prototype is shown in Fig. 14.

Fig. 15 shows the gate signals and drain-to-source voltages of the switches. The blocking voltage of the switches is around 100 V, which is consistent with the calculation from (27). The horizontally enlarged waveforms at the switching transitions are provided in Fig. 16. It can be seen that ZVS turn-ON of the switches is achieved.

Fig. 17 shows the voltages of the diodes. The blocking voltage of the diodes is around 300 V, which is consistent with the calculation from (28). Fig. 18 shows the current waveforms of the diodes. The reverse recovery problem of the diodes is alleviated.

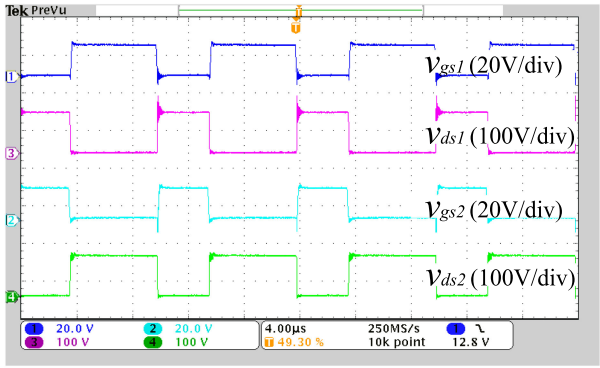
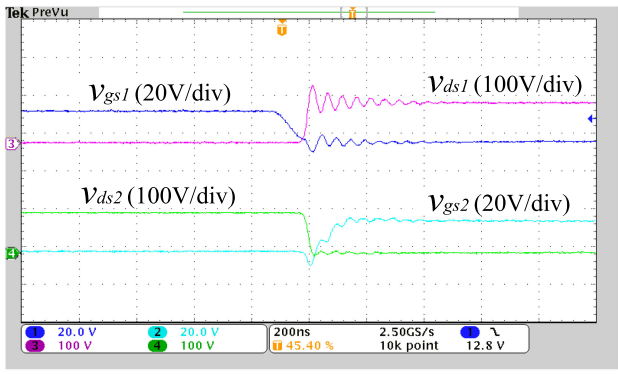
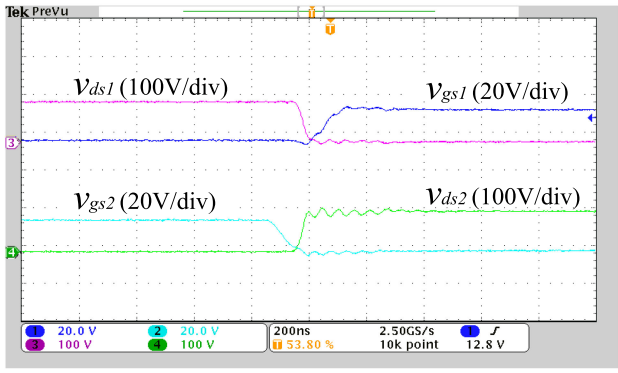



Fig. 15. Gate signals and drain-to-source voltages of the switches.




(a)




(b)

Fig. 16. ZVS operation. (a) ZVS ON of $S_2$. (b) ZVS ON of $S_1$.

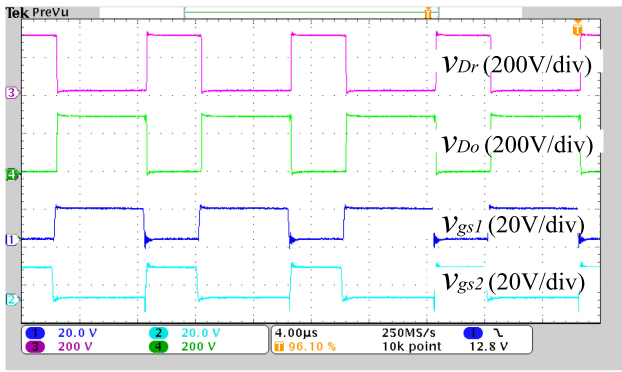



Fig. 17. Diode voltages.

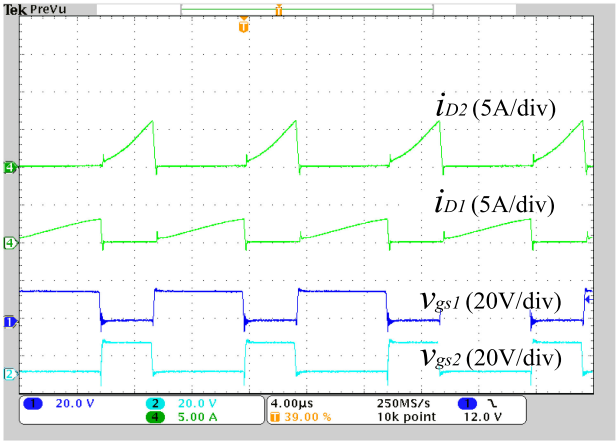



Fig. 18. Diode currents.

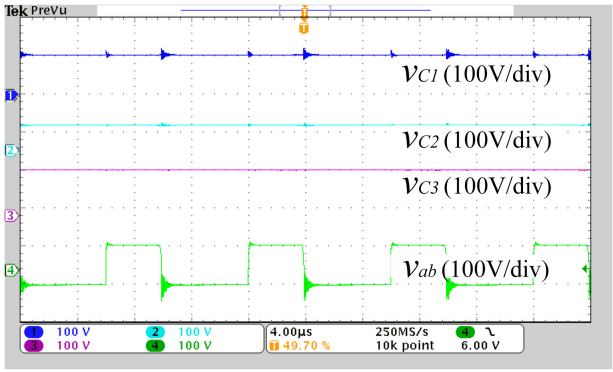



Fig. 19. Capacitor voltages and the primary voltage of the coupled inductor.

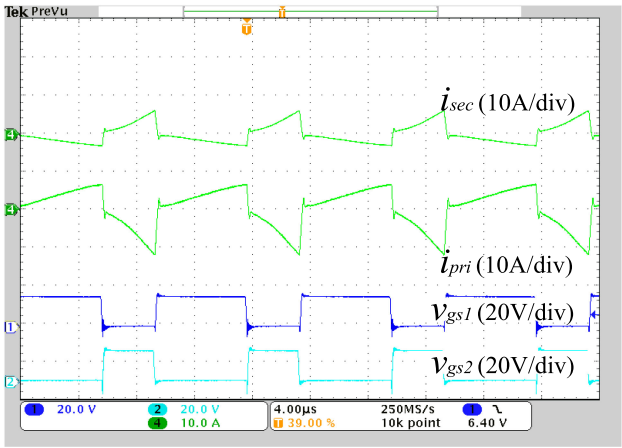



Fig. 20. Primary and secondary current of the coupled inductor.

Fig. 19 shows the voltages across the capacitors $C_1$–$C_3$. It can be seen that $V_{C1}$, $V_{C2}$, and $V_{C3}$ are around 100, 63 and 120 V, respectively, which agree with the calculations. Fig. 19 also shows the primary voltage of coupled inductor, and Fig. 20 shows the primary current and the secondary current, which are consistent with the theoretical analysis.

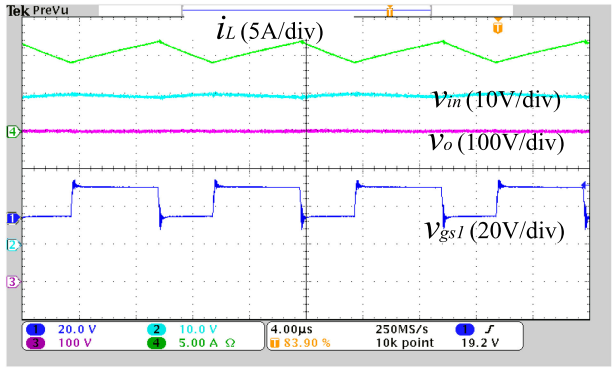



Fig. 21. Input current, input voltage, and output voltage.

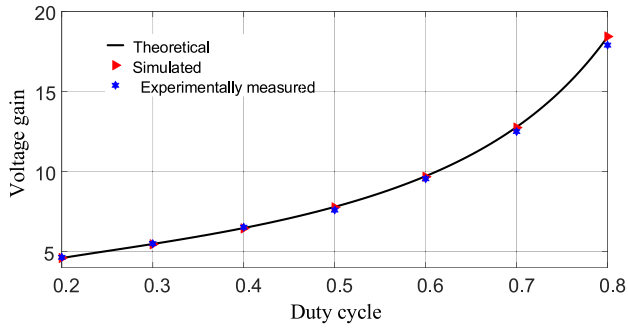



Fig. 22. Voltage gain considering leakage inductance at $R = 640\,\Omega$.

Fig. 21 shows the input current of the proposed converter. Continuous input current is achieved, which is beneficial to the battery and fuel cell and photovoltaic systems. Also, it is seen that 40-V input and 400-V output are obtained.

Fig. 22 shows the theoretical, simulated, and experimental measured voltage gain curves considering leakage inductance. It can be seen that the simulated voltage gain agrees well with the theory. The experimental measured voltage gain slightly deviates from the theoretical one due to the power losses.

Fig. 23(a) shows load transient response due to step load increase from 30% load to 100% load, and Fig. 23(b) shows load transient response due to step load decrease from 100% load to 30% load.

The measured efficiency versus output power is shown in Fig. 24. The peak efficiency is 95.2%, which is achieved at 250 W. The efficiency at the full load is measured as 94.8%. Also, the proposed converter achieves higher efficiency compared to [42] because of lower coupled inductor losses and lower switching losses.

Loss analysis is performed based on the selected components of the hardware prototype. Power losses of the proposed converter include losses of the input inductor, coupled inductor, switch, diodes, and capacitors. In order to simplify analysis, the effects of dead time and leakage inductance are ignored.

The copper loss of the input inductor is calculated by

$$P_{L\_} = {I_L}^2 r_L. \tag{68}$$

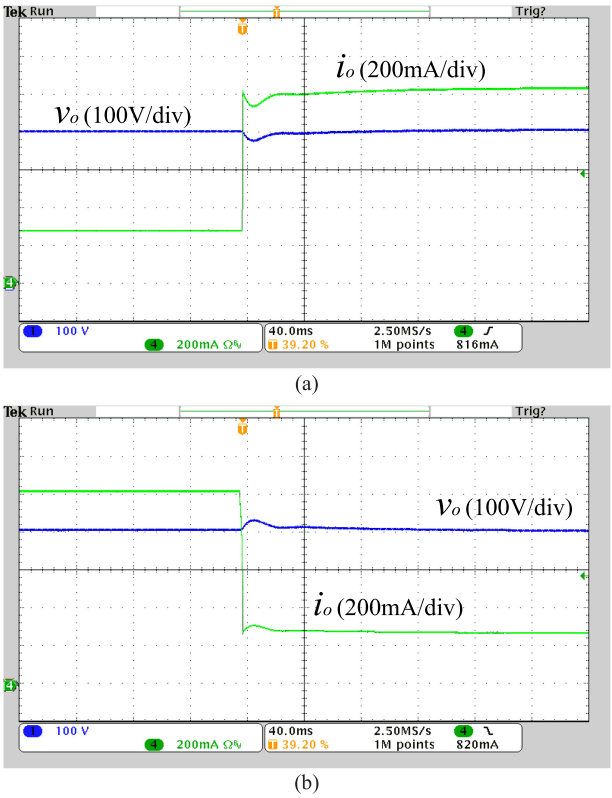



Fig. 23. Load transients. (a) Load increase. (b) Load decrease.

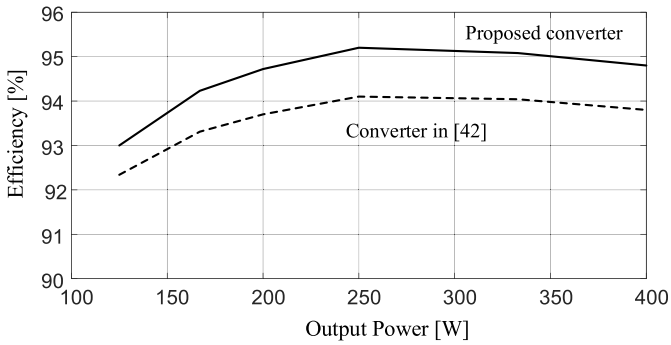



Fig. 24. Measured efficiency versus output power.

The copper loss of the coupled inductor is calculated by

$$P_{CI\_\text{copper}} = {I_{\text{pri\_rms}}}^2 r_{\text{pri}} + {I_{\text{sec\_rms}}}^2 r_{\text{sec}} \tag{69}$$

where $I_{\text{pri}_{\text{rms}}}$ and $I_{\text{sec\_rms}}$ are given by (35) and (36).

As ZVS turn-ON of the switches are achieved, switching loss is neglected and only switch conduction loss is considered. The conduction loss of the switches is calculated by

$$P_S = {I_{S1\_\text{rms}}}^2 r_{\text{on}} + {I_{S2\_\text{rms}}}^2 r_{\text{on}} \tag{70}$$

where $I_{S1\_\text{rms}}$ and $I_{S2\_\text{rms}}$ are given by (33) and (34).

The conduction loss of the diodes is calculated as

$$P_D = 2I_o V_F + \left({I_{D1\_\text{rms}}}^2 + {I_{D2\_\text{rms}}}^2\right) r_D \tag{71}$$

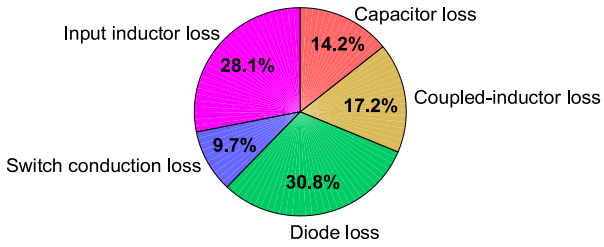



Fig. 25. Loss distribution.

where $I_{D1\_\text{rms}}$ and $I_{D2\_\text{rms}}$ are given by

$$I_{D1\_\text{rms}} = \frac{2I_o}{\sqrt{3D}} \tag{72}$$

$$I_{D2\_\text{rms}} = \frac{2I_o}{\sqrt{3\left(1-D\right)}}. \tag{73}$$

The conduction loss of the capacitors is calculated as

$$P_C = {I_{C1\_\text{rms}}}^2 r_C + {I_{C2\_\text{rms}}}^2 r_C + {I_{C3\_\text{rms}}}^2 r_C + {I_{Co\_\text{rms}}}^2 r_{Co} \tag{74}$$

where the capacitor currents are given by (62)–(65).

The loss breakdown of the prototype at full load is shown in Fig. 25. It is observed that major percent of the losses occurs in the input inductor and diodes.

If ZVS was not achieved, the switching loss of the main switch should be given by

$$P_{\text{Sw}} = \frac{1}{2} V_S I_S\left(t_7\right) t_{\text{on}} f_s + \frac{1}{2} V_S I_S\left(t_1\right) t_{\text{off}} f_s + \frac{1}{2} {V_S}^2 C_{\text{oss}} f_s. \tag{75}$$

$P_{\text{Sw}}$ is calculated as 3.17 W, which means 0.8% of efficiency improvement is obtained as a result of ZVS. The saving of switching loss would be more significant if switching frequency of the converter is selected higher.

## VI. Conclusion

A new high step-up dc–dc converter has been proposed in this article. It features high voltage gain, low switch voltage stress, low input current ripple, ZVS turn-ON of the switches, and alleviated diode reverse recovery. Characteristics of the converter have been analyzed and design considerations have been provided. A 400-W 40-V input 400-V output prototype has been built and experimental results have been provided to validate the analysis. The proposed converter is a suitable candidate for power conversion in battery, fuel cell, and PV applications.

## Appendix

The comparison of the total device rating (TDR) of the proposed converter with other similar converters is listed in Table IV. These converters have similar nonresonant operations, and the TDR is only determined by output power, voltage gain *M*, and turns ratio *n*. The curves of normalized TDR to the output power are provided in Fig. 26. As can be seen, the proposed converter achieves lower TDR.

TABLE IV
COMPARISON OF TOTAL DEVICE RATING

| Topology | TOTAL DEVICE RATING |
|---|---|
| [32] | $TDR = \frac{2V_oI_o}{n+1}(M + \frac{2nM}{M-n-1})$ |
| [40],[41] | $TDR = \frac{2V_oI_o}{n+1}(M + \frac{2nM}{M-n-1})$ |
| Proposed | $TDR = \frac{2V_oI_o}{n+2}(M + \frac{2(n+1)M}{M-n-2})$ |

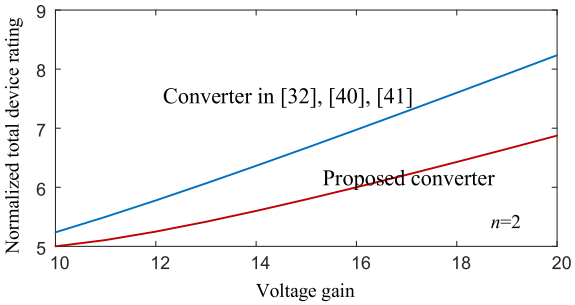



Fig. 26. Comparison of the normalized total device rating to output power.

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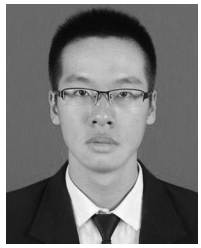

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