Full-Bridge Current-Fed PV Microinverter With DLFCR Reduction Ability

Dongchun Wu, Yunya Wu, Jiarong Kan, *Member, IEEE*, Yu Tang, *Senior Member, IEEE*, Jian Chen, and Lin Jiang, *Member, IEEE*

***Abstract*—A simple current-fed full-bridge converter (CF-FBC) is proposed as a prestage for photovoltaic (PV) microinverter after comparing it with the existing topologies. A modulation strategy based on the CF-FBC with two control freedoms is presented in this article. One freedom is the boost duty cycle, which controls the voltage of the PV panel. The power duty cycle is other freedom, which controls the voltage in the low-voltage side. The operational principle of the proposed CF-FBC is analyzed. A control strategy composing three closed loops is proposed. The regulator parameters are designed based on the small signals model of the converter. The experimental results verify the effectiveness of the proposed converter and its corresponding modulation and control strategy.**

***Index Terms*—Current-fed full-bridge converter (CF-FBC), double-line-frequency current ripple (DLFCR) reduction, photovoltaic (PV) microinverter, resonant regulator, two control freedoms.**

I. Introduction

In RECENT years, various types of inverters used in photovoltaic (PV) generation systems are extensively researched [1]–[4]. PV microinverter, whose typical power is 100–300 W, has been paid more and more attention due to the following advantages: maximum of energy harvest, low cost of mass production, plug and play operation, easier installation, and expansion [5]–[7].

The most commonly used topologies for PV microinverters are based on flyback converter [8] and forward converter [9]. The interleaved flyback [10] and forward [11] converters are adopted for high rated power. With the increment of photoelectric transformation efficiency, the rated power of the PV microinverter becomes larger and larger whose maximum value is upto 500 W [12]. More interleaved units make the PV microinverter more complicated and more expensive, which reduces the competitiveness of the PV microinverter. Therefore, the PV microinverters based on the half-bridge [13], current fed, and voltage-fed push–pull [14], [15], current-fed isolated dual-boost [16], various kinds of resonant full-bridge [17], [18] have been proposed to achieve higher efficiency and relatively lower cost compared with the interleaved topology.

The requirement of another important performance for PV microinverter is that its lifespan must match the lifespan of PV panel whose lifespan is normally about 25 years [19]. However, there is a power difference between the input side and the grid side of the PV microinverter. The input-side power generating from the PV panel is constant in steady state. The grid-side power is determined by the grid voltage and grid current and its instantaneous fluctuation range is very large. Therefore, an element for balancing energy difference between the grid side and the PV side must be equipped in the PV microinverter [20], [21]. An electrolytic capacitor with large capacitance is usually employed to realize this function. It is the most economical method and easy to decouple the power difference. However, the PV microinverter usually operates in a harsh environment, such as on the top of the building or in the barren desert. The utilization of the electrolytic capacitor decreases the lifespan of the PV microinverter [22]. Compared with the same volume of the electrolytic capacitor, the film capacitor has much smaller capacitance while with longer lifespan. Larger double-line-frequency current ripple (DLFCR) component will be included in the output current of the PV panel if the electrolytic capacitor is substituted by the film capacitor with smaller capacitance [23]. The DLFCR leads to the decrement of the energy harvest for the PV panel [24]. Hence, the DLFCR must be removed by proper control strategy [25] or an additional active power decoupling circuit (APDC) [26] used to store the energy difference between the PV panel and the grid. Although the method of APDC can effectively reduce DLFCR, it also brings the cost and the efficiency to an unacceptable level. Therefore, the method of swing dc bus voltage is a more feasible solution after adopting the film capacitor with smaller capacitance, which requires high-performance regulator to reduce DLFCR in the output current of the PV panel.

According to the description mentioned above, the purpose of this article is to find a simple topology with a proper control strategy for low cost, high efficiency, and an acceptable current ripple level. The existing methods are with some shortcomings

Manuscript received June 24, 2019; revised October 3, 2019 and January 5, 2020; accepted February 13, 2020. Date of publication February 17, 2020; date of current version May 1, 2020. This work was supported in part by the National Natural Science Foundation of China under Grants 51577164 and 51677084, in part by Jiangsu Province Qinglan Project, in part by Jiangsu Province Fifth 333 Research Project, and in part by Six Talent Peaks Project in Jiangsu Province under Grant XNY-045. Recommended for publication by Associate Editor M. A. E. Andersen. *(Corresponding author: Yu Tang.)*

Dongchun Wu, Yunya Wu, Jiarong Kan, and Jian Chen are with the College of Electrical Engineering, Yancheng Institute of Technology, Yancheng 224053, China (e-mail: wudc1975@163.com; wuyunyayi@126.com; kanjr@163.com; cjycit@163.com).

Yu Tang is with the State Key Laboratory of Reliability and Intelligence of Electrical Equipment, Hebei University of Technology, Tianjin 300130, China, and also with the Hebei Key Laboratory of Electromagnetic Field and Electrical Apparatus Reliability, Hebei University of Technology, Tianjin 300401, China (e-mail: ty8025@hotmail.com).

Lin Jiang is with the Department of Electrical Engineering and Electronics, The University of Liverpool, Liverpool L69 3GJ, U.K. (e-mail: ljiang@liv.ac.uk).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2020.2974516

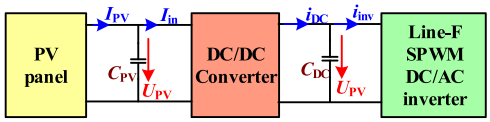


Fig. 1. Commonly used structure for the PV microinverter.

for achieving this purpose. In [27], the employed converter is the conventional full-bridge converter. The controlled current is the inductor current in the output side and the current in the input side is not directly controlled. The satisfactory effect of DLFCR reduction can be obtained only if the electrolytic filter capacitor with large capacitance is in the output side. In [28], a current-fed dual-half-bridge converter is used as the prestage of a two stages inverter, where the input-side current is directly controlled. However, the control strategy is designed for the fuel cell system. Meanwhile, the control strategy is coupling because the output voltage and the input current are also regulated by the phase-shift angle. In [13], the simplest topology is employed in all existing methods. Its voltages in the low-voltage side (LVS) and the high-voltage side (HVS) does not match well, which results in high current stress. In [29], all control objectives have been achieved, but the topology is too complicated for the PV microinverter.

In this article, a simple topology based on the current-fed full-bridge converter as the prestage of the PV microinverter has been proposed. There are two control freedoms [30]. One freedom is used to control the voltage and current of the PV panel. Thus, the maximum power point tracking (MPPT) of the PV and DLFCR reduction can be achieved. The other freedom is used to control the voltage in LVS, which can match the voltage between LVS and HVS. Thus, the current stress can be effectively reduced. The experimental results verify the correctness of the theoretical analysis.

II. Motive of the Proposed PV Microinverter

A. Performance Requirement of the PV Microinverter

The two-stage topology for a grid-connected inverter is very prevalent among industrial applications. The output filter capacitor of the prestage dc/dc converter is selected to buffer the power difference between the dc input side and the ac grid side by swinging its voltage. The commonly used structure for the PV microinverter is shown in Fig. 1.

In order to achieve high performance and requirements of different commissions, PV microinverter should satisfy the following index:

1) MPPT should be realized and it is usually achieved by controlling the output voltage ($U_{\rm PV}$) of the PV panel;
2) it is preferred to use the film capacitor with smaller capacitance instead of electrolytic capacitor in the microinverter due to the short life of the electrolytic capacitor and bad working environment;
3) smaller capacitance results in large ripples in the HVS of the dc/dc converter ($U_{\rm dc}$) due to the instantaneous power difference between the PV side and grid side. A proper control strategy should guarantee that there is no DLFCR in the output current of the PV panel ($I_{\rm PV}$);
4) a proper control strategy should be adopted to guarantee low current stress of elements and high efficiency;
5) it is necessary to adopt a structure with relatively simple topology and low cost.

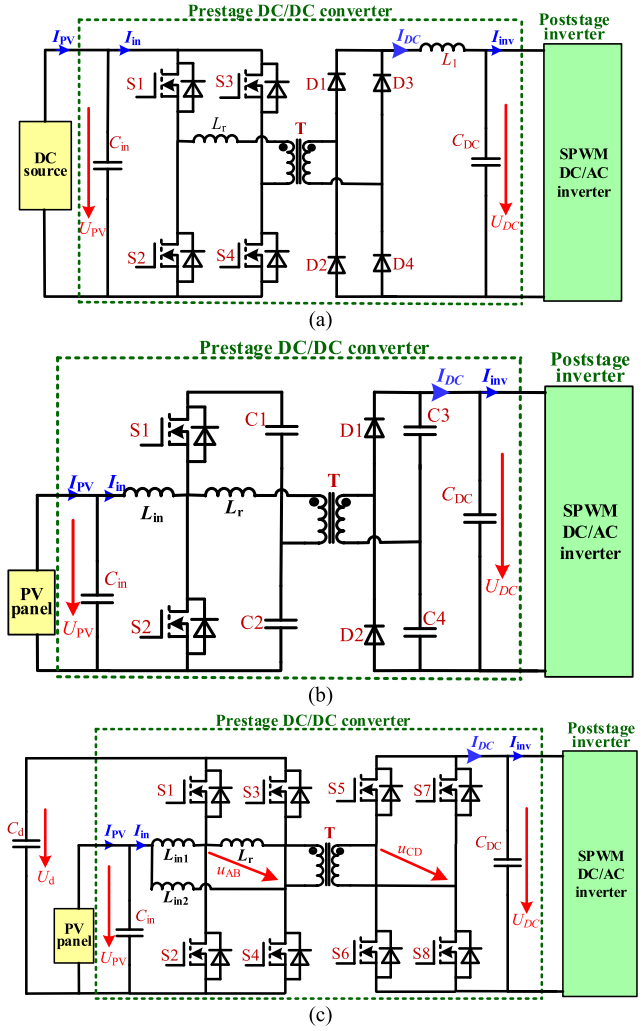


Fig. 2. Three types of prestage converter for PV microinverter. (a) Conventional voltage-fed full-bridge in [26] and [27]. (b) Current-fed boost-half-bridge in [13]. (c) Current-fed full-bridge in [29].

B. Conventional Voltage-Fed Full-Bridge Converter

In [26] and [27], the used prestage dc/dc converter is based on the conventional voltage-fed phase-shift full-bridge, as shown in Fig. 2(a). The output current $I_{\rm DC}$ is selected as the feedback variable. Meanwhile, there is almost no DLFCR component in $I_{\rm DC}$ through proper control strategy. Hence, there is no DLFCR in $I_{\rm DC}$, and it can be expressed as follows if high-frequency components over switching frequency are neglected:

$$i_{\rm DC}(\omega t) = I_{\rm DC}. \tag{1}$$

The input current $I_{\rm inv}$ of the poststage inverter can be expressed as follows if the unity power factor is obtained in the grid side:

$$i_{\rm inv}(\omega t) = \sqrt{2}\frac{P}{U_G}\,|\sin\omega t| \tag{2}$$

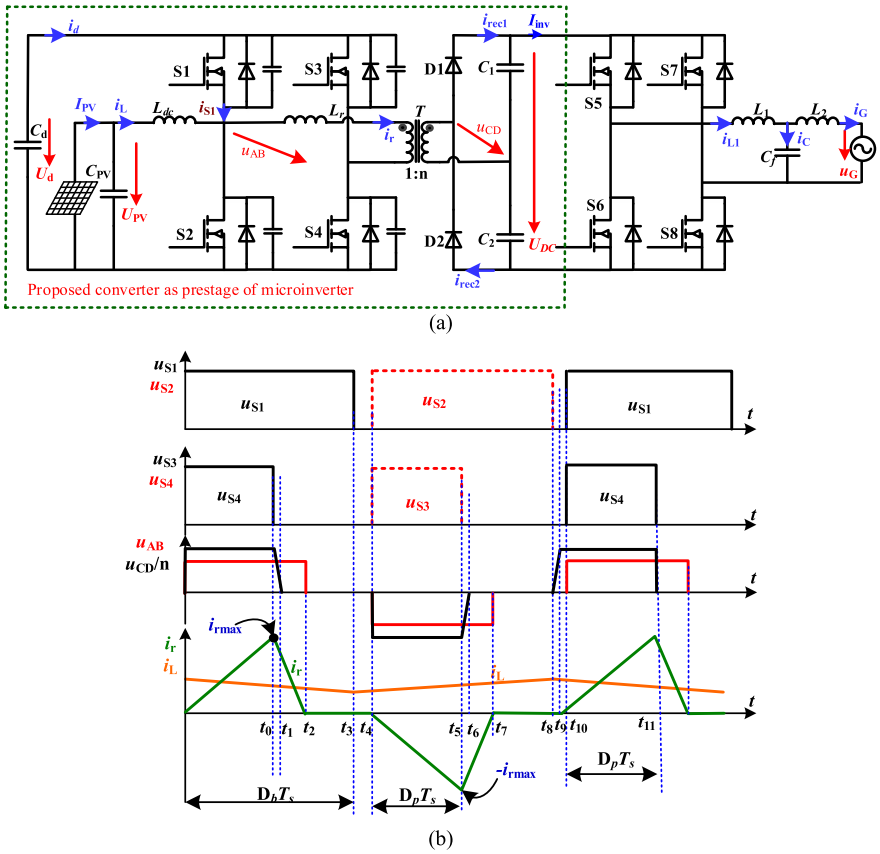


Fig. 3. Proposed current-fed converter as the prestage of the PV microinverter and its corresponding modulation method. (a) Proposed full-bridge converter. (b) Modulation method for the proposed converter.

where P is the output power of the microinverter, U_G and ω are the voltage rms value and the angular frequency of the grid, respectively. The HVS capacitor $C_{\rm DC}$ is required to buffer the energy. The HVS voltage can be calculated as follows, as derived in [29]:

$$U_{\rm DC}(\omega t) = U_{\rm DC1} + \frac{P}{2\omega C_{\rm DC} U_{\rm DC1}} \sin 2\omega t \tag{3}$$

where $U_{\rm DC1}$ is the mean value of $U_{\rm DC}$. There is a double-line-frequency component in HVS voltage. Thus, the power from the input side is expressed as

$$P_{\rm in}(\omega t) = I_{\rm DC} U_{\rm DC}(\omega t) = I_{\rm DC} U_{\rm DC1} + \frac{I_{\rm DC} P}{2\omega C_{\rm DC} U_{\rm DC1}} \sin 2\omega t. \tag{4}$$

The fluctuation of input-side power results in the DLFCR in the input current $I_{\rm PV}$. From (3), the electrolytic capacitor must be equipped to reduce double-line-frequency component in the HVS voltage and ripple power in the input side. Therefore, it is hard to satisfy the second requirement mentioned in Section II-A.

C. Current-Fed Boost-Half-Bridge

A type of current-fed boost-half-bridge is presented in [13], as shown in Fig. 2(b). There is no DLFCR in $I_{\rm PV}$ if boost inductor current $I_{\rm in}$ is selected as a feedback variable and the resonant regulator is adopted. However, there is only one control freedom and duty cycle of switches S1 or S2 of the converter. The sum voltage across the capacitors C1 and C2 cannot be controlled, which is varying with different output powers of the PV panel. It results in the difficulty of current stress optimization. So, it is hard to satisfy the fourth requirement mentioned in Section II-A.

D. Current-Fed Full-Bridge Converter

A two control freedoms strategy is proposed in [29] and its corresponding topology is shown in Fig. 2(c). One control freedom is the duty cycle of the ac-side voltage [$u_{\rm AB}$ and $u_{\rm CD}$ in Fig. 2(c)] of the dual active bridge. The other one is phase-shift angle between $u_{\rm AB}$ and $u_{\rm CD}$. The two control freedoms make it possible to realize MPPT, no DLFCR in the current $I_{\rm PV}$, and low current stress. However, the topology is too complicated and too expensive for the PV microinverter with low power.

E. Proposed Converter and Its Modulation Strategy

In this article, a current-fed full-bridge converter, as shown in Fig. 3(a), is proposed as the prestage of the PV microinverter. A boost converter is integrated into the proposed converter, which contains a boost inductor $L_{\rm DC}$, a bridge arm composed of the switches S1 and S2, and a filter capacitor C_d in LVS. The voltage $u_{\rm AB}$ and $u_{\rm CD}$ are the ac side of full-bridge and the rectifier, respectively. The modulation method and the main waveform for the proposed converter are shown in Fig. 3(b).

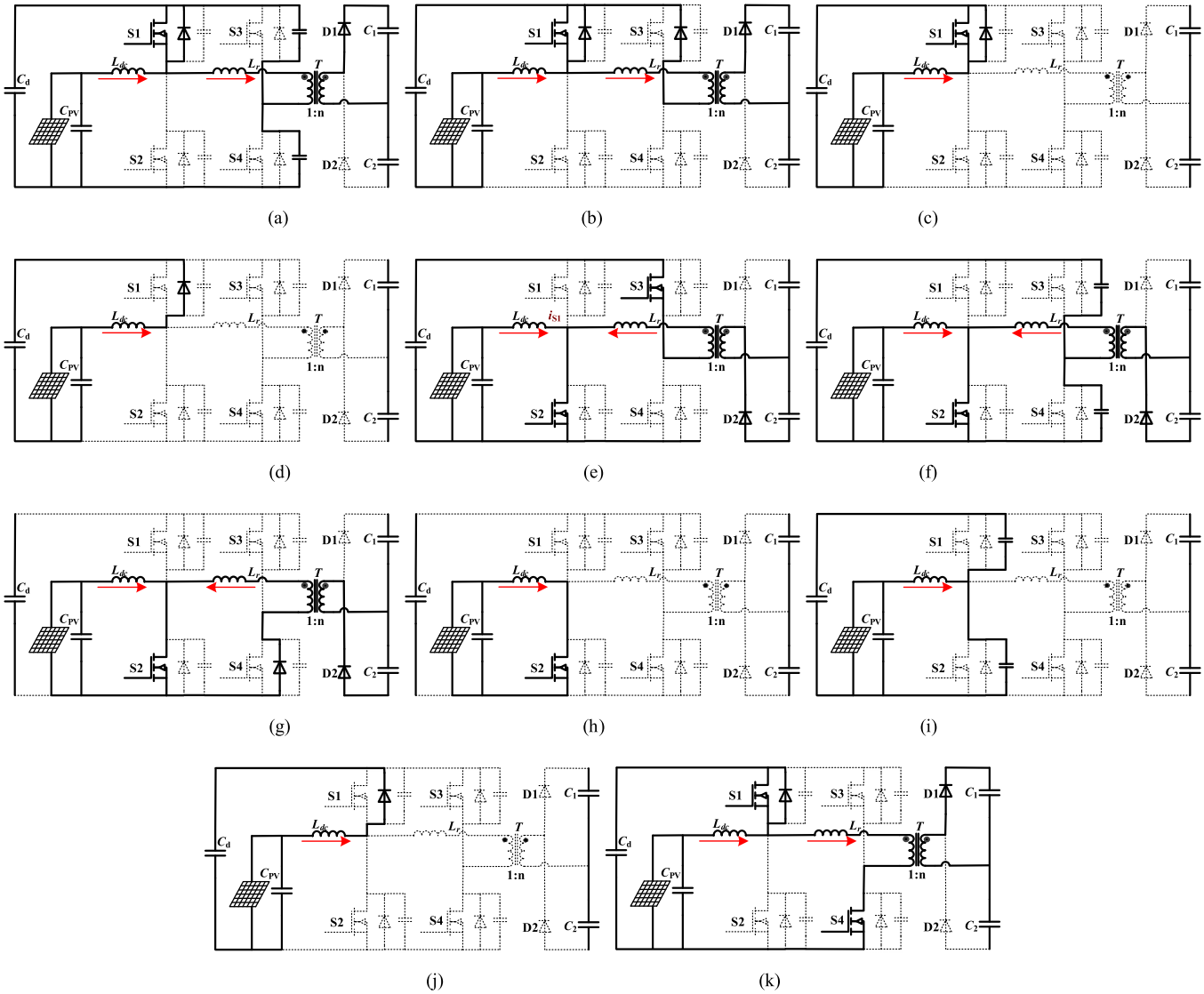


Fig. 4. Equivalent circuit of the proposed converter in different steps. (a) Step 1: t_0–t_1. (b) Step 2: t_1–t_2. (c) Step 3: t_2–t_3. (d) Step 4: t_3–t_4. (e) Step 5: t_4–t_5. (f) Step 6: t_5–t_6. (g) Step 7: t_6–t_7. (h) Step 8: t_7–t_8. (i) Step 9: t_8–t_9. (j) Step 10: t_9–t_{10}. (k) Step 11: t_{10}–t_{11}.

There are two control freedoms in the modulation strategy. One is called boost duty cycle D_b, which is defined in (5). The other control freedom is called power duty cycle D_p and it is defined in (6). In fact, D_b and D_p are also the duty cycles of S1 and S3/S4, respectively

$$D_b = 1 - \frac{t_{10} - t_3}{t_{11} - t_0} = 1 - \frac{t_{10} - t_3}{T_s} \tag{5}$$

$$D_p = \frac{t_{11} - t_{10}}{t_{11} - t_0} = \frac{t_5 - t_4}{t_{11} - t_0} = \frac{t_{11} - t_{10}}{T_s} = \frac{t_5 - t_4}{T_s} \tag{6}$$

where T_s is the switching cycle. The output voltage U_{DC} is called the voltage in HVS in the subsequent article. The inductor L_r acts as the energy buffering element between LVS and HVS.

The function of the proposed converter with the modulation strategy is equivalent to the combination of a boost converter and a full-bridge converter connected in series. The two control freedoms mentioned above make it possible to realize the same function with the converter in [29]. Most of all, the proposed converter is much simpler and cheaper than that in [29]. As a result, the proposed topology is fitted for the application of the PV microinverter.

One complete switching cycle can be divided into 11 steps. The former three steps are explained in detail as follows. The operating condition of the later three steps is symmetrical with the former three steps. Fig. 4 gives the commutation step diagrams during a switching cycle.

Step 1. *[t_0–t_1, Fig. 4(a)]:* Before t_0, S1 and S4 are ON. The current i_L is decreasing linearly and the current i_r is increasing linearly. The rectifier diode D1 is in the conduction state. The energy stored in C_d is transmitted to the secondary side of the transformer. At t_0, S4 is turned OFF. A resonance between the buffering inductor L_r and the parasitic capacitors (or external paralleled capacitors) of S3 and S4 begins from t_0.

TABLE I
SOFT/HARD SWITCHING CONDITION OF ELEMENTS

	S1	S2	S3	S4	D1	D2
ON	t_{10} ZVS	t_4 HS	t_4 ZCS	t_{10} ZCS	t_{10} ZCS	t_4 ZCS
OFF	t_4 HS	t_8 ZVS	t_5 ZVS	t_0 ZVS	t_2 ZCS	t_7 ZCS

Therefore, the terminal voltage of S4 (S3) gradually increases (decreases) from zero (U_d). At t_1, the terminal voltage of S4 (u_{S4}) is equal to U_d and the resonant process is over. Thus, the switch S4 achieves zero voltage switching (ZVS) OFF.

Step 2. *[t_1–t_2, Fig. 4(b)]:* After t_1, the body diode of S3 is ON. The voltage $u_{AB} = 0$ and $u_{CD} = 0.5U_{DC}$. The current i_r begins to decrease. At t_2, the current $i_r = 0$. So, there is almost no reverse recovery loss in the body diode of S3 and the rectifier diode D1 and we can say that the diode D1 achieves zero current switching (ZCS) OFF.

Step 3. *[t_2–t_3, Fig. 4(c)]:* After t_2, the current i_r holds zero. Only the current through switch S1 is not equal to zero. This step is over until t_3, when the switch S1 is turned OFF.

Step 4. *[t_3–t_4, Fig. 4(d)]:* At t_3, S1 is turned OFF. The body diode of S1 undertakes the current flowing through the boost inductor i_L.

Step 5. *[t_4–t_5, Fig. 4(e)]:* At t_4, switches S2 and S3 are turned ON simultaneously. The commutation happens immediately from the body diode of S1 and S2. So, hard switching is received during its ON process. Moreover, there is reverse recovery loss in the body diode of S1. We can say that S1 is turned OFF with hard switching and S2 is turned ON also with hard switching. After t_4, the current i_L begins to increase linearly and the current i_r begins to increase from zero with negative direction. Both of the switch S3 and diode D2 achieve ZCS ON.

Step 6. *[t_5–t_6, Fig. 4(f)]:* At t_5, switche S3 is turned OFF and this process is symmetrical with step 1. It is not discussed here. From the analysis result, the switch S3 achieves ZVS OFF.

Step 7. *[t_6–t_7, Fig. 4(g)]:* After t_6, the body diode of S4 is ON. This process is symmetrical with step 2 and the diode D2 achieves ZCS OFF.

Step 8. *[t_7–t_8, Fig. 4(h)]:* After t_7, the current i_r holds zero. This process is symmetrical with step 3.

Step 9. *[t_8–t_9, Fig. 4(i)]:* At t_8, S2 is turned OFF. A resonance between boost inductor L_{DC} and parasitic capacitors (or external paralleled capacitors) of S1 and S2 begin from t_8. At t_9, the voltage $u_{AB} = U_d$ and the resonance is over. In this resonant process, the terminal voltage of S2 is increasing linearly. At the same time, the terminal voltage of S1 is decreasing linearly. So, S2 achieves ZVS OFF.

Step 10 & Step 11. *[t_9–t_{10}, Fig. 4(j)] & [t_{10}–t_{11}, Fig. 4(k)]:* At t_9, the body diode of S1 is ON. The switches S1 and S4 are turned ON at t_{10} simultaneously. The current i_r begins to increase linearly from zero. Thus, S1 achieves ZVS ON. In the secondary side of the transformer, the rectifier D1 starts to conduct. Therefore, both of the switch S4 and rectifier diode D1 achieve ZCS ON. This process lasts until switch S4 is turned OFF at t_{11}. The next switching cycle starts after t_{11}.

From the analysis above, the soft/hard switching condition can be concluded in Table I.

It should be noted that the boost duty cycle D_b fluctuates within a small range around 0.5 due to the fluctuation of the PV panel voltage with the weather condition. The fluctuation of the LVS voltage U_d in every line cycle will be discussed in Section III. Therefore, the waveform of the current i_r is not strictly symmetric within a half switching period. However, as long as the ON-time of S3 and S4 is equal, the core of the transformer can operate normally without saturation.

III. LOW CURRENT STRESS AND LOW-FREQUENCY RIPPLE REDUCTION STRATEGY

As mentioned in Section II, a boost converter is integrated into the proposed converter. The input voltage of the boost converter is the voltage of the PV panel U_{PV}. The output voltage of the boost converter is U_d in LVS. The current i_L is designed to operate in continuous conduction mode. So

$$U_d = \frac{1}{D_b} U_{PV}. \tag{7}$$

The filter capacitor C_d in LVS also acts the role of energy buffering. Its absorbed energy is equal to its released energy in every half line cycle. In every switching cycle, there are two components in the current i_d in LVS. One part results from the current i_L between t_0 and t_3, and it is defined i_{Ld}. The other part results from the current i_r between t_0–t_1 and t_3–t_4 and it is defined i_{rd}. So

$$i_d = i_{rd} - i_{Ld}. \tag{8}$$

Therefore, the input power and the output power in LVS can be obtained according to the product of the i_d and U_d

$$P_{Ld} = D_b I_L U_d \tag{9}$$

$$P_{rd} = \frac{U_d}{T_s}\left[\int_{t0}^{t1} i_r dt + \int_{t3}^{t4} |i_r|\, dt\right] = \frac{U_d(2nU_d - U_{DC})D_p^2 T_S}{2nL_r}. \tag{10}$$

According to the expression of the power flowing, every control freedom is only related to the corresponding power. It indicates that there is no control decoupling between D_b and D_p. The equivalent circuit of the proposed converter is shown in Fig. 5, where the PV panel is viewed as a current source paralleled with a resistance. C_{12} is the equivalent capacitance of the series of C_1 and C_2. The proposed converter can be controlled as the conventional structure, where an isolated full-bridge converter follows a boost converter. So, the control strategy for the proposed converter is given in Fig. 6.

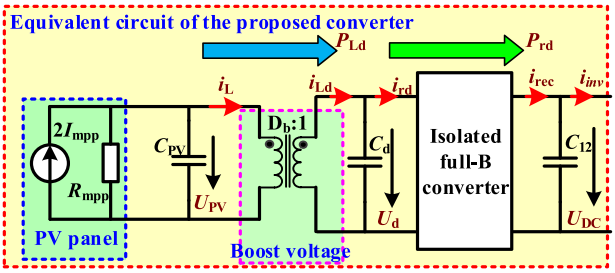


Fig. 5. Equivalent sketch circuit of the proposed full-bridge converter.

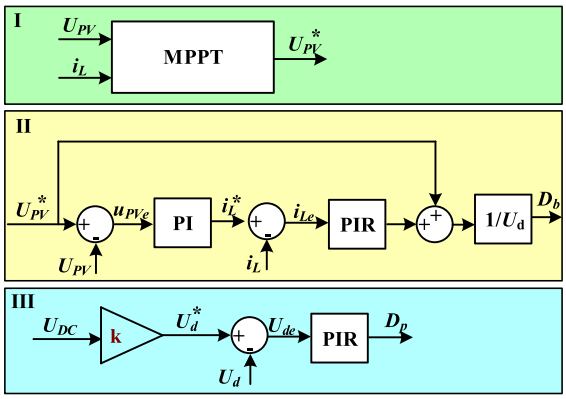


Fig. 6. Control strategy for the proposed full-bridge converter.

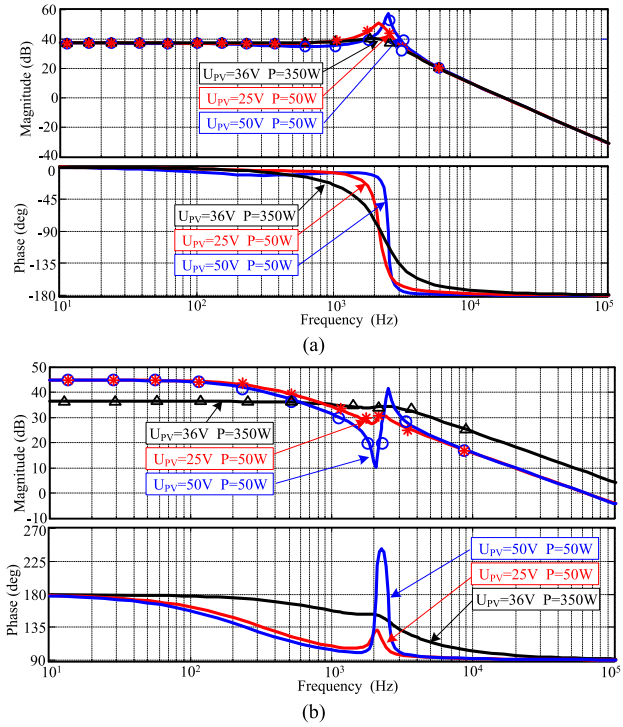


Fig. 7. Bode plot of G_{UPV_Db} and $G_{\mathrm{Ud\_Dp}}$ in different operational conditions. (a) Bode plot of G_{UPV_Db}. (b) Bode plot of $G_{\mathrm{Ud\_Dp}}$.

There are three parts to the control strategy. The first part is to fulfill the function of MPPT. The reference voltage for the PV panel (U_{PV}^*) is achieved by the MPPT controller. The second part is to stabilize the PV voltage and reduce DLFCR by boost duty cycle D_b, where a resonant regulator is adopted. There is a voltage feedforward link in the voltage control of the PV panel. Its purpose is to shorten the starting time of the converter. The voltage control cannot affect the stability of the converter. The third part is to control the voltage in LVS to match the voltage in HVS by power duty cycle D_p, which can effectively reduce the current stress of elements in the converter.

IV. Parameter Design of Regulators

According to the equivalent schematic diagram of the converter, as shown in Fig. 5, the corresponding voltage–current relationships for the PV cell side filter capacitor C_{PV}, the boost inductor L_{dc}, and the capacitor C_d in LVS are established, respectively

$$C_{\mathrm{PV}}\frac{dU_{\mathrm{PV}}}{dt} = 2I_{\mathrm{mpp}} - \frac{U_{\mathrm{PV}}}{R_{\mathrm{mpp}}} - i_L \tag{11}$$

$$L_{\mathrm{dc}}\frac{di_L}{dt} = U_{\mathrm{PV}} - D_b U_d \tag{12}$$

$$C_d\frac{dU_d}{dt} = i_{Ld} - i_{\mathrm{rd}}. \tag{13}$$

The small-signal state-space equations of the proposed converter can be obtained if the disturbances are introduced into the expression in (11)–(13) (shown in the Appendix). Accordingly, the control-to-output transfer functions $G_{UPV\_Db}(s)$ and $G_{\mathrm{Ud\_Dp}}(s)$ are summarized as follows:

$$G_{UPV\_Db}(s) = \frac{\frac{U_d}{L_{\mathrm{DC}}C_{\mathrm{PV}}}s + \frac{U_d D_p^2 T_S + L_r D_b i_L}{L_{\mathrm{DC}}L_r C_{\mathrm{PV}}C_d}}{A(s)} \tag{14}$$

$$G_{\mathrm{Ud\_Dp}}(s) = \frac{-\frac{(2nU_d - U_{\mathrm{DC}})D_p T_S}{nL_r C_d}\left(s^2 + \frac{1}{C_{\mathrm{PV}}R_{\mathrm{mpp}}}s + \frac{1}{L_{\mathrm{DC}}C_{\mathrm{PV}}}\right)}{A(s)} \tag{15}$$

where

$$A(s) = s^3 + \frac{L_r C_d + C_{\mathrm{PV}}R_{\mathrm{mpp}}D_p^2 T_S}{L_r C_{\mathrm{PV}}C_d R_{\mathrm{mpp}}}s^2 + \frac{L_{\mathrm{DC}}D_p^2 T_S + L_r C_{\mathrm{PV}}R_{\mathrm{mpp}}D_b^2 + L_r C_d R_{\mathrm{mpp}}}{L_{\mathrm{DC}}L_r C_{\mathrm{PV}}C_d R_{\mathrm{mpp}}}s + \frac{L_r D_b^2 + R_{\mathrm{mpp}}D_p^2 T_S}{L_{\mathrm{DC}}L_r C_{\mathrm{PV}}C_d R_{\mathrm{mpp}}}.$$

Fig. 7 shows the bode plots of $G_{UPV\_Db}(s)$ and $G_{\mathrm{Ud\_Dp}}(s)$ with different operational parameters, which are given in Table I. In Fig. 7, the curves with the symbols "△, ○, and ∗" represent the bode plots achieved by scanning ac signal with PSIM software. We can see that the bode plots achieved by different methods basically coincide with each other, which verifies the correctness of the small-signal state-space equations.

A. Parameter Design of Voltage and Current Regulator for the PV Panel

The second part of the proposed control strategy in Fig. 6 is composed of two closed loops. The feedback variable of

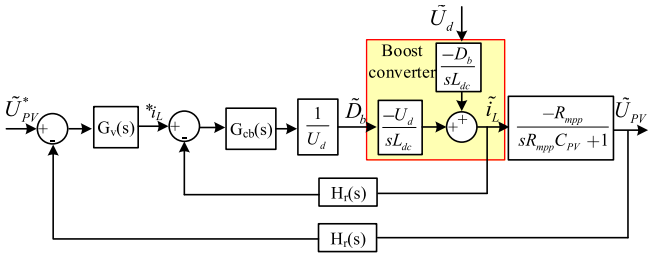


Fig. 8. Control block diagram for the PV output voltage.

the inner loop is the boost inductor current i_L. The DLFCR is reduced by employing a proportional–integral–resonant (PIR) regulator. The feedback variable of the outer loop is the PV panel voltage $U_{\rm PV}$ and only a proportional–integral (PI) regulator is used to stabilize the PV panel voltage. The bandwidth of the voltage loop can be low to ensure the robustness of the converter because the variation of operation voltage for the PV panel is slow when the weather changes.

The control diagram of the dual loop is shown in Fig. 8, where the voltage feedforward link is not shown. It is because the voltage feedforward link is not included in the feedback loop path. In Fig. 8, $G_v(s)$ and $G_{\rm cb}(s)$ are the transfer function of voltage outer loop regulator and the current inner loop regulator, respectively. $H_r(s)$ is the equivalent delay link of the sample time and feedback filter, which is a first-order low-pass filter with a corner frequency of one-fourth switching frequency in the experiment. So

$$H_r(s) = \frac{1}{1.6 \times 10^{-5} s + 1}. \tag{16}$$

According to the characteristic of the open-loop transfer function, the inner current regulator can be determined as

$$G_{\rm cb}(s) = -1.5 - \frac{250}{s} - \frac{200\pi s}{s^2 + 4\pi s + 4\omega^2}. \tag{17}$$

The total open-loop gain of the current loop is shown as follows:

$$T_{\rm cb}(s) = -\frac{1}{sL_{\rm DC}} H_r(s) G_{\rm cb}(s). \tag{18}$$

Fig. 9(a) and (b) shows the uncompensated and compensated bode plots of the inner boost inductor current loop and outer voltage loop, respectively, when $U_{\rm PV} = 36$ V and $P = 350$ W.

From Fig. 9(a), the phase margin of the current loop is 66° after adopting the current regulator in (24). The bandwidth, one-decade frequency away at dual line frequency (100 Hz), is 1020 Hz, which guarantees good dynamic performance of current tracking. The gain is high (50.8 dB) at dual line frequency (100 Hz) because of the introduction of a resonant regulator, which makes it possible to reduce the DLFCR to a proper level in the PV current.

The closed-loop transfer function of the inner current loop is

$$G_{i\_\rm loop}(s) = \frac{i_L(s)}{i_L^*(s)} = \frac{G_{\rm cb}(s)}{H_r(s) G_{\rm cb}(s) - sL_{\rm DC}}. \tag{19}$$

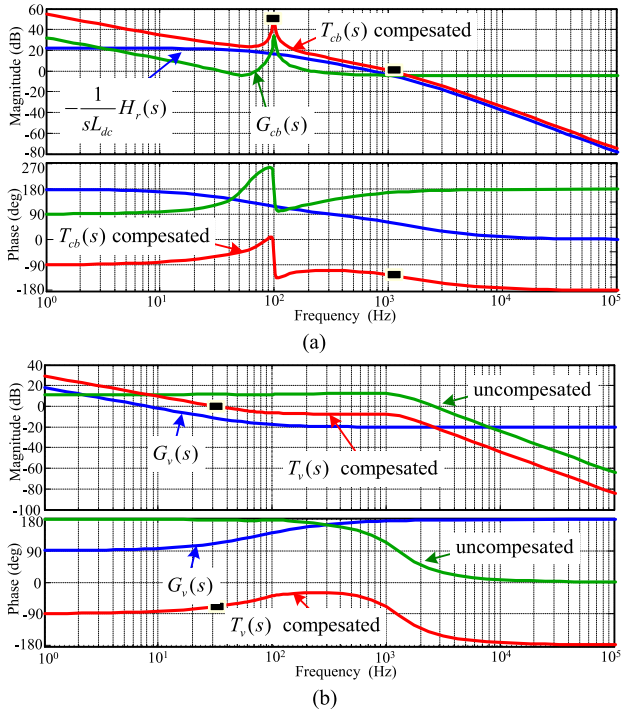


Fig. 9. Bode plot of the inner current loop and the outer voltage loop. (a) Bode plot of the inner current loop. (b) Bode plot of the outer voltage loop.

So, the total open-loop gain of the outer voltage loop with the voltage regulator is

$$T_v(s) = -\frac{R_{\rm mpp} G_{i\_\rm loop}(s) G_v(s)}{sR_{\rm mpp} C_{\rm PV} + 1}. \tag{20}$$

The voltage regulator is designed as

$$G_v(s) = -0.1 - \frac{50}{s}. \tag{21}$$

From Fig. 9(b), the phase margin of the voltage loop is 100° and the bandwidth is 30 Hz. Although the bandwidth is low, it is fast enough to control the PV voltage compared with the slow-changing weather and disturbance time intervals of MPPT.

Fig. 9 only shows the bode plots when $U_{\rm PV} = 36$ V and $P = 350$ W. It is necessary to verify the stability under different operating conditions of the PV panel. In Fig. 8, setting

$$H_1(s) = \frac{-1}{sL_{\rm DC}} \tag{22}$$

$$H_2(s) = \frac{-R_{\rm mpp}}{sR_{\rm mpp} C_{\rm PV} + 1}. \tag{23}$$

Thus, the closed-loop transfer function of the current loop and the voltage loop can be achieved respectively as

$$G_{i\_\rm loop}(s) = \frac{H_1(s) G_{\rm cb}(s)}{1 + H_1(s) H_r(s) G_{\rm cb}(s)} \tag{24}$$

$$G_{v\_\rm loop}(s) = \frac{H_2(s) G_v(s) G_{i\_\rm loop}(s)}{1 + H_r(s) H_2(s) G_v(s) G_{i\_\rm loop}(s)}. \tag{25}$$

The pole-zero locus of the closed PV voltage loop in Fig. 10 evaluates the control system stability and performance of the

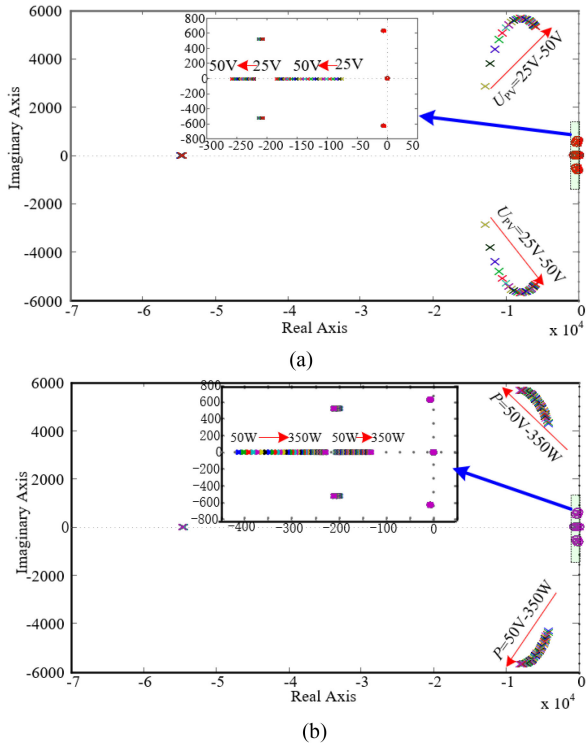


Fig. 10. Pole-zero locus of the closed transfer function of the PV voltage loop. (a) $P = 350$ W, $U_{\rm PV}$ varies from 25 to 50 V. (b) $U_{\rm PV} = 36$ V, P varies from 50 to 350 W.

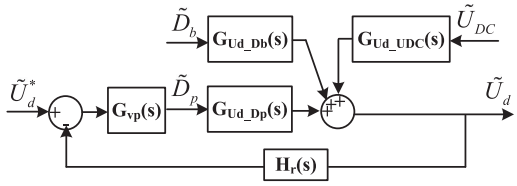


Fig. 11. Control block diagram for the voltage U_d.

proposed converter. The system is always stable in the whole operating range since all the poles of the closed-loop system are in the left half of s plane. The pole-zero locus shows that the stability is stronger in time of higher PV voltage and lower power.

B. Parameter Design of Voltage Regulator in LVS

The voltage in LVS (U_d) can be regulated by the power duty cycle D_p, which can control the power flow from LVS to dc bus. The converter can also be normally operated even if the voltage in LVS (U_d) cannot be controlled. However, the voltage in LVS (U_d) fluctuates with the variation of power. There is a large voltage variation of the dc bus $(U_{\rm DC})$ due to the power difference between the PV panel and the grid. The unmatched voltage between U_d and $U_{\rm DC}$ leads to the large current stress of the elements and the low efficiency of the microinverter. Thus, it is necessary to force the voltage U_d to follow the varying voltage $U_{\rm DC}$. This function can be fulfilled if the reference voltage U_d is set to be k times of the voltage $U_{\rm DC}$.

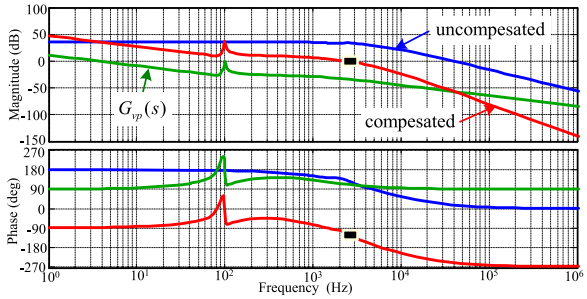


Fig. 12. Bode plot for deigning voltage loop in LVS.

The diagram for controlling the voltage in LVS is shown in Fig. 11. In the control diagram, it contains the transfer function of voltage loop regulator $G_{vp}(s)$, transfer function $G_{\rm Ud\_Dp}(s)$ derived in (21), and transfer functions $G_{\rm Ud\_Db}(s)$ and $G_{{\rm Ud}\_U{\rm DC}}(s)$ from disturbance sources to the voltage U_d.

The impact of transfer functions $G_{\rm Ud\_Db}(s)$ and $G_{{\rm Ud}\_U{\rm DC}}(s)$ cannot affect the stability of the closed loop of voltage in LVS. Thus, only the effect of the disturbance D_p in the forward channel is considered. A modified PI with plugged resonant regulator in (26) is given to control the voltage in LVS

$$G_{vp}(s) = -\frac{350(s+160\pi)}{s(s+2400\pi)} - \frac{4\pi s}{s^2+4\pi s+4\omega^2}. \tag{26}$$

A zero at 80 Hz is designed to ensure that the gain at dual line frequency is not too small. A pole at 1200 Hz, about half of the frequency with a natural resonant peak, as shown in Fig. 7, is placed to attenuate this peak at low-power condition. Moreover, the purpose of the resonant regulator is to realize high gain at 2ω frequency so that the LVS voltage is well synchronized with the HVS voltage. Fig. 12 shows the uncompensated and compensated bode plots of the voltage loop in LVS, when $U_{\rm PV} = 36$ V and $P = 350$ W. The gain at 2ω frequency is 36.7 dB and the bandwidth of the loop is 1.25 kHz, which can effectively guarantee that the voltage at LVS can quickly track the fluctuation of the dc bus voltage. Therefore, the current stress can be reduced effectively.

The pole-zero locus of the closed LVS voltage loop is shown in Fig. 13 to evaluate the control system stability and the performance of the proposed converter with the changes g of the PV voltage and the power. We can see that the position of the main characteristic roots is almost unchanged. Thus, the stability of the system cannot be affected by the variations of external parameters.

V. Experimental and Simulation Verification

In order to verify the feasibility of the proposed converter for the PV microinverter, a 350-W PV microinverter prototype is built. The parameters and elements model are presented in Table II and the PV microinverter prototype is shown in Fig. 14.

Fig. 15 shows the operational waveforms of the proposed converter in steady state when the output power is 350 W. The drive signals of switches S1–S4 $(u_{\rm GS1}$–$u_{\rm GS4})$ are shown in Fig. 15(a). The realtionships of the phases are same with

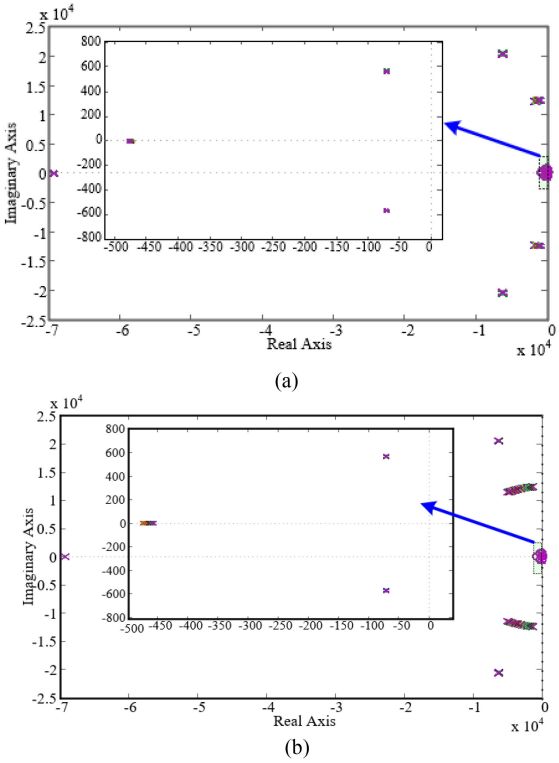


Fig. 13. Pole-zero locus of the closed-loop transfer function of LVS voltage loop. (a) $P = 350$ W, $U_{\rm PV}$ varies from 25 to 50 V. (b) $U_{\rm PV} = 36$ V, P varies from 50 to 350 W.

TABLE II
PARAMETERS FOR MICROINVERTER PROTOTYPE

Switching frequency	Proposed DC/DC:40kHz SPWM DC/AC: 10kHz
Grid voltage	$110\sqrt{2}\sin(100\pi t)$
PV panel	Maximum power：350W Voltage in MPP：36V
switches	S1-S4: IRFB4110 D1-D2:C3D05060A S5-S8: IXFX 55N50
Filter capacitors	$C_{\rm PV}$:10μF/50V C_d:22μF/100V C_1, C_2:150μF/100V $C_{\rm f}$: 5μF/250V
inductors	$L_{\rm dc}$:200μH $L_{\rm r}$:13μH L_1:1mH L_2:0.5mH
transformer	n=1.7

the theoretical waveforms in Fig. 3(a). The waveforms of drive signal and terminal voltage of switch S2 ($u_{\rm GS2}$, u_{DS2}), and the currents i_r and i_L are shown in Fig. 15(b). The rising process of i_L corresponds to the time during which the switch S2 is turned ON. The current i_r always returns to zero at every half switching cycle. The waveforms of drive signal and terminal voltage of switch S4 ($u_{\rm GS4}$, u_{DS4}), voltage $u_{\rm AB}$, and current i_r are shown in Fig. 15(c). The positive and the negative parts of the voltage $u_{\rm AB}$ synchronize with the positive direction increase and the negative direction increase of i_r, respectively. It is noted that there is a resonant process between the buffering inductor and parasitic capacitors of the switches S1–S4 after the current i_r

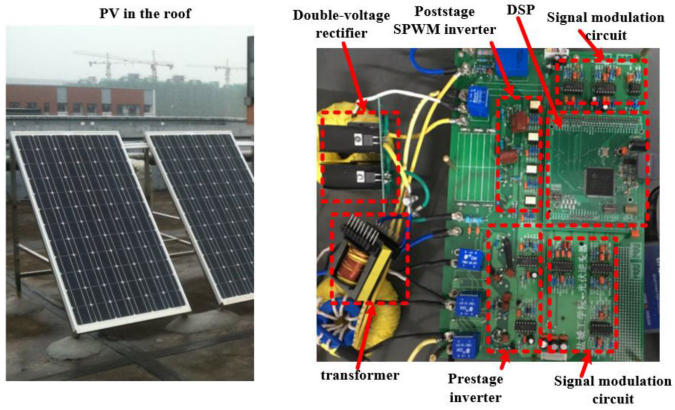


Fig. 14. Photo of PV microinverter prototype.

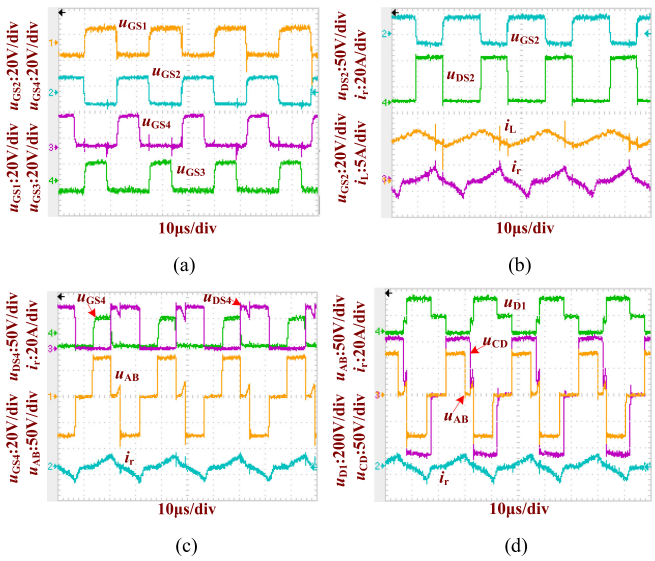


Fig. 15. Waveforms of the proposed converter within switching cycle when power is 350 W. (a) Drive signals for S1–S4. (b) Waveforms of $u_{\rm GS2}$, u_{DS2}, i_r, and i_L. (c) Waveforms of $u_{\rm GS4}$, u_{DS4}, $u_{\rm AB}$, and i_r. (d) Waveforms of u_{D1}, $u_{\rm AB}$, $u_{\rm CD}$, and i_r.

falls to zero, which results in a gap in the terminal voltage of S4 (u_{DS4}). There is almost no power loss during this resonant process due to the small resonant current. Fig. 15(d) shows the waveforms of the reverse voltage of diode D1 (u_{D1}), the voltage $u_{\rm AB}$, $u_{\rm CD}$, and the current i_r. We can see that the positive and negative parts of the voltage $u_{\rm CD}$ synchronize with the positive part and negative part of i_r. The voltage amplitude of u_{D1} is equal to half of the voltage $U_{\rm DC}$ in HVS.

The waveforms, as shown in Fig. 16(a)–(d), are obtained when the output power is 100 W with the proposed control strategy. Fig. 16(a) shows the waveforms of the voltage in LVS (U_d), dc bus voltage ($U_{\rm DC}$), grid voltage (u_G), and current i_r. There is 2ω frequency voltage ripple component both in $U_{\rm DC}$ and U_d in which they are synchronous with each other. It is because that the reference value of U_d is k times of $U_{\rm DC}$, as shown in Fig. 6. Although there is a 2ω voltage ripple with 20-V amplitude in $U_{\rm DC}$, the DLFCR is well reduced in Fig. 16(b), where I_L represents the mean value of the current i_L. It should

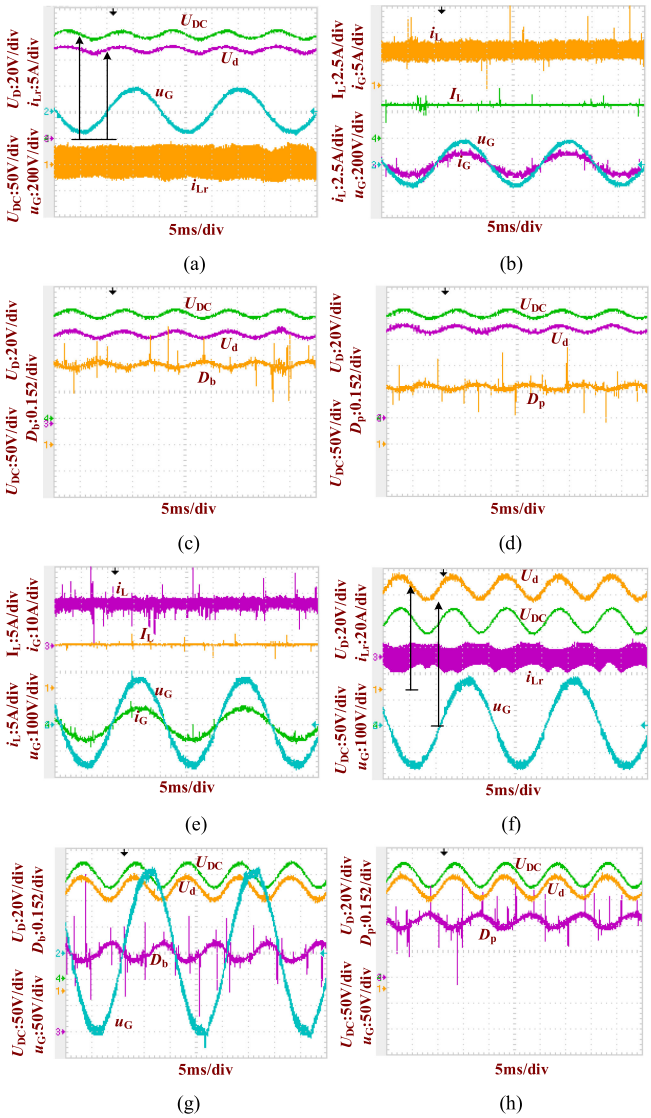


Fig. 16. Waveforms of the proposed converter within the line cycle with different powers. (a) Operational waveforms 1 with 100 W power. (b) Operational waveforms 2 with 100 W power. (c) Operational waveforms 3 with 100 W power. (d) Operational waveforms 4 with 100 W power. (e) Operational waveforms 1 with 300 W power. (f) Operational waveforms 2 with 300 W power. (g) Operational waveforms 3 with 300 W power. (h) Operational waveforms 4 with 300 W power.

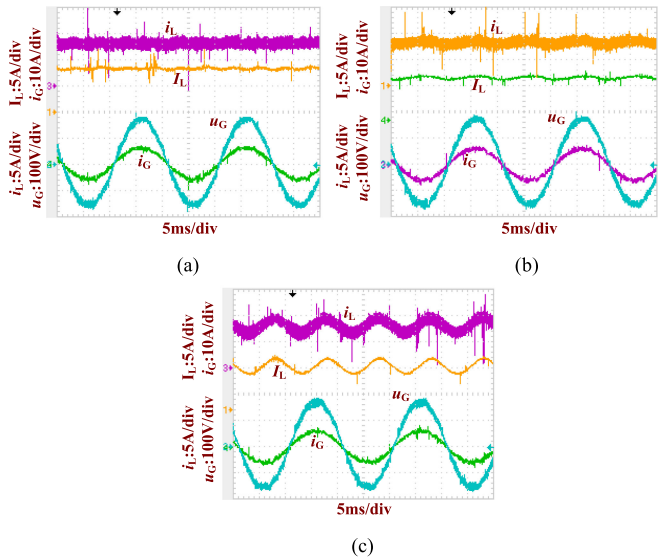


Fig. 17. Performance comparison among different inner-loop strategies. (a) Only PIR regulator. (b) PI regulator with LVS voltage link $(1/U_D)$. (c) Only PI regulator.

be mentioned that the waveform of I_L is achieved by using a second-order low-pass filter with a 10 kHz cutoff frequency. The signal with frequency lower than 1 kHz can pass through this second-order low-pass filter without attenuation. Fig. 16(c) and (d) shows the relationship among boost duty cycle D_b, power duty cycle D_p, and the voltages $U_{\rm DC}$ and U_d. The boost duty cycle D_b reduces with the increment of the voltage U_d, which is conformed to the relation in (13).

The waveforms, as shown in Fig. 16(e) and (f), are obtained when the output power is 300 W with the proposed control strategy, in this article. The amplitude of ripple voltage with 2ω frequency, about 50 V, is larger than that of the microinverter with 100 W power in Fig. 16(a)–(d). The control strategy regulates two control freedoms (D_b and D_p) with larger ripple for obtaining no DLFCR in the current $i_{\rm PV}$. From the waveforms, as shown in Fig. 16(a)–(f), with different output powers, it is verified that the proposed control strategy can reduce DLFCR effectively.

The component of DLFCR in I_L is less than 4% of the mean value of I_L from Fig. 16(b) and (e), which can guarantee that the output power can exceed 99% of the maximum power of the PV panel [4] and strategy in this article is effective in reducing DLFCR.

In Fig. 8, there are two control links in the inner current loop. One is PIR regulator and the other is LVS voltage link ($1/U_D$ in Fig. 8). In order to verify the function of each control link, the following three controllers are adopted, respectively: 1) only PIR regulator; 2) PI regulator with LVS voltage link $(1/U_D)$; and 3) only PI regulator. The waveforms in three conditions are shown in Fig. 17(a)–(c), respectively. We can see that the all waveforms of I_L in three conditions have the DLFCR component. Both of the resonant regulator and LVS voltage link play an important role in DLFCR reduction. Compared with the waveforms of I_L in Fig. 16(b) and (e) controlled by the proposed strategy, the proposed converter and strategy in this paper is effective to reduce DLFCR.

The output power of the PV panel is determined by the solar irradiance, temperature, etc. So, it is random and difficult to achieve an obvious power change in a short time. In order to observe the MPPT process obviously, a simulation model of the proposed PV microinverter has been established by MATLAB/Simulink. Fig. 18(a) shows the simulation results of the MPPT process when the solar irradiance changes from 1000 to 500 W/m^2 at 0.2 s. The algorithm for MPPT is the perturbation and observation method, which is a simple and effective method. The perturbation step is 0.5 V for the reference of the PV voltage and the perturbation interval is 0.01 s. The transient time is approximately 0.1 s after the sudden change of the solar irradiance. Fig. 18(b) shows the waveforms of the dc bus voltage, grid voltage, and grid current. Although there is a large dual-line-frequency component in HVS voltage, there is almost

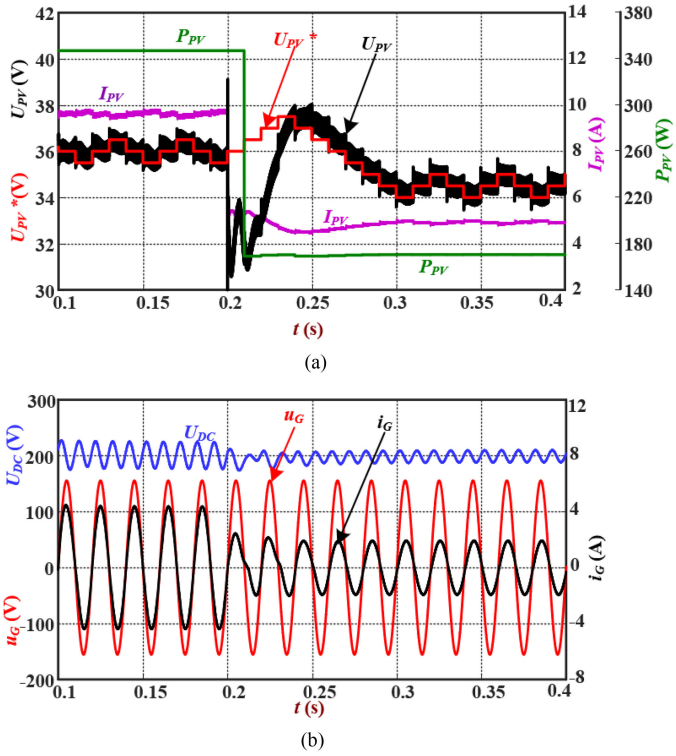


Fig. 18. Simulation results when there is a sudden change in solar irradiance. (a) MPPT process. (b) waveforms of dc bus voltage, grid voltage, and grid current.

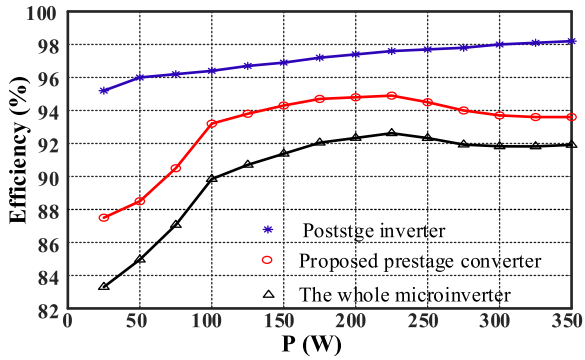


Fig. 19. Efficiency curves of the proposed microinverter.

no DLFCR in the PV output current and with a satisfactory quality of the grid current.

The efficiency curve is difficult to record accurately because the output power of the PV panel is affected by different factors, such as light irradiance and temperature. Thus, the constant voltage source is adopted as a power supply. The curve of input voltage versus power simulates the output characteristic of the PV panel. The achieved efficiency curve is shown in Fig. 19. The maximum efficiency is 92.6%.

VI. Conclusion

This article proposed a current-fed full-bridge converter as the prestage of the PV microinverter. A boost converter is integrated into the proposed converter without additional switches. A two control freedoms modulation method is presented based on the proposed converter. One freedom is used to control the PV voltage and current, where the resonant regulator is employed to reduce DLFCR due to high gain at 2ω frequency. The other freedom is employed to control the LVS voltage that varies with the dc bus voltage, which can be realized by a resonant regulator. The current stress of elements can be effectively reduced. The parameters of the regulators in the proposed strategy are designed according to the small-signal model of the proposed converter. The experimental results verify the effectiveness of the proposed converter and corresponding control strategy.

Appendix

State-space equations for the small-signal model of the proposed current-fed full-bridge converter (CF-FBH) converter

$$\dot{\tilde{x}} = A\tilde{x} + B\tilde{u} \tag{A-1}$$

where

$$\tilde{x} = \begin{bmatrix} \tilde{i}_L & \tilde{U}_{\rm PV} & \tilde{U}_d \end{bmatrix}^T \tag{A-2}$$

$$\tilde{u} = \begin{bmatrix} \tilde{D}_b & \tilde{D}_p & \tilde{U}_{\rm DC} \end{bmatrix}^T \tag{A-3}$$

$$A = \begin{bmatrix} 0 & \frac{1}{L_{\rm DC}} & -\frac{D_b}{L_{\rm DC}} \\ -\frac{1}{C_{\rm PV}} & -\frac{1}{C_{\rm PV}R_{\rm mpp}} & 0 \\ \frac{D_b}{C_d} & 0 & -\frac{T_S D_p^2}{L_r C_d} \end{bmatrix} \tag{A-4}$$

$$B = \begin{bmatrix} -\frac{U_d}{L_{\rm DC}} & 0 & 0 \\ 0 & 0 & 0 \\ \frac{i_L}{C_d} & -\frac{(2nU_d - U_{\rm DC})D_p T_S}{nL_r C_d} & \frac{D_p^2 T_S}{2nL_r C_d} \end{bmatrix}. \tag{A-5}$$

References

[1] Q. Huang, A. Q. Huang, R. Yu, P. Liu, and W. Yu, "High-efficiency and high-density single-phase dual-mode cascaded buck–boost multilevel transformerless PV inverter with GaN AC switches," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7474–7488, Aug. 2019.

[2] H. Jafarian, N. Kim, and B. Parkhideh, "Decentralized control strategy for AC-stacked PV inverter architecture under grid background harmonics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 84–93, Mar. 2018.

[3] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.

[4] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[5] F. C. Melo, L. S. Garcia, L. C. de Freitas, E. A. A. Coelho, V. J. Farias, and L. C. G. de Freitas, "Proposal of a photovoltaic AC-module with a single-stage transformerless grid-connected boost microinverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2289–2301, Mar. 2018.

[6] F. Evran, "Plug-in repetitive control of single-phase grid-connected inverter for AC module applications," *IET Power Electron.*, vol. 10, no. 1, pp. 47–58, Jan. 2017.

[7] S. A. Arshadi, B. Poorali, E. Adib, and H. Farzanehfard, "High step-up DC–AC inverter suitable for AC module applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 832–839, Feb. 2016.

[8] S. Zengin, F. Deveci, and M. Boztepe, "Volt-second-based control method for discontinuous conduction mode flyback micro-inverters to improve total harmonic distortion," *IET Power Electron.*, vol. 6, no. 8, pp. 1600–1607, Sep. 2013.

[9] D. Meneses, O. García, P. Alou, J. A. Oliver, R. Prieto, and J. A. Cobos, "Single-stage grid-connected forward microinverter with boundary mode control," in *Proc. IEEE Energy Convers. Congr. Expo.*, Phoenix, AZ, USA, Sep. 2011, pp. 2475–2480.

[10] F. F. Edwin, W. Xiao, and V. Khadkikar, "Dynamic modeling and control of interleaved flyback module-integrated converter for PV power applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1377–1388, Mar. 2014.

[11] D. Meneses, O. Garcia, P. Alou, J. A. Oliver, and J. A. Cobos, "Grid-connected forward microinverter with primary-parallel secondary-series transformer," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4819–4830, Sep. 2015.

[12] C. Felgemacher *et al.*, "Design of photovoltaic microinverter for off-grid and grid-parallel applications," in *Proc. 8th Int. IEEE. Conf. Integr. Power Electron. Syst.*, Feb. 2014, pp. 1–6.

[13] S. Jiang, D. Cao, Y. Li, and F. Z. Peng, "Grid-connected boost-half-bridge photovoltaic microinverter system using repetitive current control and maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4711–4722, Nov. 2012.

[14] C. T. Rodríguez, D. V. de la Fuente, G. Garcera, E. Figueres, and J. A. G. Moreno, "Reconfigurable control scheme for a PV microinverter working in both grid-connected and island modes," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1582–1595, Apr. 2013.

[15] Y.-H. Kim, S.-C. Shin, J.-H. Lee, Y.-C. Jung, and C.-Y. Won, "Soft-switching current-fed push–pull converter for 250-W AC module applications," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 863–872, Feb. 2014.

[16] H.-J. Chiu *et al.*, "A module-integrated isolated solar microinverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 781–788, Feb. 2013.

[17] S. M. Tayebi and I. Batarseh, "Mitigation of current distortion in a three-phase microinverter with phase skipping using a synchronous sampling DC-link voltage control," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 3910–3920, May 2018.

[18] A. Trubitsyn, B. J. Pierquet, A. K. Hayman, G. E. Gamache, C. R. Sullivan, and D. J. Perreault, "High-efficiency inverter for photovoltaic applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2010, pp. 2803–2810.

[19] K. A. Kim, P. S. Shenoy, and P. T. Krein, "Converter rating analysis for photovoltaic differential power processing systems," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1987–1997, Apr. 2015.

[20] S. Harb, M. Mirjafari, and R. S. Balog, "Ripple-port module-integrated inverter for grid-connected PV applications," *IEEE Trans. Ind. Appl.*, vol. 49, no. 6, pp. 2692–2698, Nov./Dec. 2013.

[21] C.-Y. Liao, W.-S. Lin, Y.-M. Chen, and C.-Y. Chou, "A PV micro-inverter with PV current decoupling strategy," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6544–6557, Aug. 2017.

[22] P. Fang, B. Sheng, S. Webb, Y. Zhang, and Y.-F. Liu, "LED driver achieves electrolytic capacitor-less and flicker-free operation with an energy buffer unit," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6777–6793, Jul. 2019.

[23] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the DC input for an AC photovoltaic module system," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1264–1272, Sep. 2006.

[24] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.

[25] G. C. Christidis, A. C. Kyritsis, N. P. Papanikolaou, and E. C. Tatakis, "Investigation of parallel active filters' limitations for power decoupling on single-stage/single-phase microinverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1096–1106, Sep. 2016.

[26] C. Liu and J.-S. Lai, "Low frequency current ripple reduction technique with active control in a fuel cell power system with inverter load," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1429–1436, Jul. 2007.

[27] G. Zhu, X. Ruan, L. Zhang, and X. Wang, "On the reduction of second harmonic current and improvement of dynamic response for two-stage single-phase inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1028–1041, Feb. 2015.

[28] X. Liu, H. Li, and Z. Wang, "A fuel cell power conditioning system with low-frequency ripple-free input current using a control-oriented power pulsation decoupling strategy," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 159–169, Jan. 2014.

[29] Y. Shi, R. Li, Y. Xue, and H. Li, "High-frequency-link-based grid-tied PV system with small DC-link capacitor and low-frequency ripple-free maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 328–339, Jan. 2016.

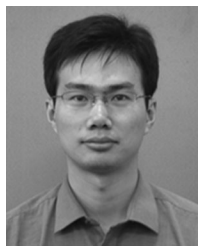
[30] W. Li, J. Xiao, Y. Zhao, and X. He, "PWM plus phase angle shift (PPAS) control scheme for combined multiport DC/DC converters," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1479–1489, Mar. 2012.

Dongchun Wu was born in Jiangsu, China, in 1975. He received the M.S. degree in material processing engineering from Hohai University, Nanjing, China, in 2007.

He joined as an Associate Professor with the College of Electrical Engineering, Yancheng Institute of Technology. He is the author or co-author of more than 20 technical papers. His current research interests include power electronics in renewable energy generation and computer control technology.

Yunya Wu was born in Jiangsu, China, in 1979. She received the M.S. degree in computer technology from the Nanjing University of Science and Technology, Nanjing, China, in 2010.

Since 2001, she has been working with the School of Electrical Engineering, Yancheng Institute of Technology, Yancheng, China, where she is currently a Senior Technician. Her current research interests include control strategy for grid-connected inverters in microgrid and islanding detection.

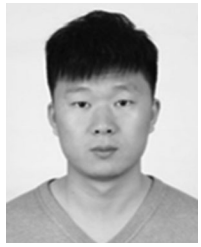


Jiarong Kan (Member, IEEE) was born in Jiangsu, China, in 1979. He received the M.S. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2007.

Since 2007, he has been working with the School of Electrical Engineering, Yancheng Institute of Technology, Yancheng, China, where he is currently an Associate Professor. He is the holder of seven patents and is the author or co-author of more than 40 technical papers. His current research interest focuses on power electronics in renewable energy generation.

Yu Tang (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2003 and 2008, respectively.

In 2008, he joined the Department of Electrical Engineering, NUAA, and the State Key Laboratory of Reliability and Intelligence of Electrical Equipment, Hebei University of Technology, in 2018. He has authored or coauthored more than 80 papers in journals and conference proceedings. His research areas include power electronics in renewable energy generation.



Jian Chen received the B.S. and Ph.D. degrees in electrical engineering from the University of Liverpool, Liverpool, U.K., in 2010 and 2015, respectively.

In 2015, he joined the Yancheng Institute of Technology, Yancheng, China, where he is currently a Lecturer with the School of Electrical Engineering. His research interests include renewable energy generation, fault ride-through, advanced control of wind energy conversion systems, permanent magnet synchronous motors, and induction motors.

Lin Jiang (Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 1992 and 1996, respectively, and the Ph.D. degree in electrical engineering from the University of Liverpool, Liverpool, U.K., in 2001.

From 2001 to 2003, he was a Postdoctoral Research Assistant with the University of Liverpool. From 2003 to 2005, he was a Postdoctoral Research Associate with the Department of Automatic Control and Systems Engineering, University of Sheffield, Sheffield, U.K. From 2005 to 2007, he was a Senior Lecturer with the University of Glamorgan, Wales, U.K. In 2007, and joined the University of Liverpool, where he is currently a Senior Lecturer with the Department of Electrical Engineering and Electronics. His current research interests include control and analysis of power systems, smart grids, and renewable energy.