Extended State Observer-Based Control of DC–DC Converters for Fuel Cell Application

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***Abstract*—Due to the nonlinear volt–ampere characteristic of fuel cell (FC) stack, a dc–dc power converter is essential to be interfaced, to regulate a stiff dc bus to properly power the load. In this article, a robust controller based on extended state observer (ESO) is proposed for a dc–dc interleaved boost converter for FC application. The proportional-integral (PI) control is also designed for comparison. By rewriting the PI control law as the unified form of disturbance observer-based control, it is revealed that the PI control in fact uses the integral action as the disturbance estimation. Then, a theoretical study is conducted to fairly evaluate and compare the performance of these two controllers. The results show that the proposed controller has superior performance to the PI controller, without the need of extra sensors. Simulation and experiment results demonstrate the effectiveness of the proposed controller.**

***Index Terms*—DC–DC power converter, extended state observer (ESO), fuel cell (FC) application, interleaved boost converter, proportional-integral (PI) control.**

I. Introduction

FUEL CELL (FC) is a device that converts the chemical energy into electricity, with the only byproducts of heat and water. Considered as a clean energy source, FC has been increasingly used in portable, stationary, and transportation applications. However, due to the nonlinear volt–ampere characteristic, the FC stack voltage varies inversely with the FC current [1]. Thus, to fulfill the load requirement, it is essential to interface with a dc–dc power converter to regulate a constant and stiff dc bus [2], [3]. The interleaved boost converter is an attractive choice. It allows a low input current ripple by making use of the phase interleaving technique [4], which is beneficial for FC stack long-time operation.

The dc–dc power converter for FC application inevitably suffers from the operation point (load resistance and source voltage) uncertainty and the disturbance caused by dynamic load demand and inconstant source voltage. Thus, a closed-loop control with feedback is requisite. The proportional control can accelerate the system response speed and improve the steady accuracy. Nevertheless, the steady-state error cannot be eliminated totally. To achieve precise regulation, the integral control is generally integrated to form a proportional-integral (PI) control. In [4], a dual-loop PI control designed based on small-signal modeling at nominal operation point is developed for a dc–dc interleaved converter. The dual-loop controller consists of an inductor current inner-loop and an output voltage outer-loop. Due to the double-loop control, accurate voltage regulation can be obtained. However, the converter dynamic performance varies with the converter operation point. The converter performance would deteriorate significantly if the operation point is far away from the nominal value. In order to achieve smaller steady-state error, faster dynamical response, and lower overshoot in presence of operation point uncertainty and disturbance, various linear or nonlinear controllers, such as sliding mode control and disturbance rejection control, are designed for dc–dc converters in the literature. In [5], a hysteresis-based sliding mode control is used as the inner-loop control for the quadratic boost converter. In [6], a sliding mode voltage control is implemented into the classic dc–dc power converters, such as buck and boost converter. Good dynamic performance can be achieved. The main limitations are the chattering phenomenon and the inconstant switching frequency. For the interleaved boost converters, in [7], a finite control set model predictive control is designed to improve the dynamic performance. The optimization of the objective function within a switching period may result in a heavy computational burden. Moreover, due to the direct manipulation of the converter switches, it suffers also the variable switching frequency. The precondition of phase interleaving to reduce the input current ripple is constant switching frequency. Thus, the controllers with variable switching frequency are not appropriate for the interleaved boost converter for FCs. In [8], a reaching law-based sliding mode inner-loop control is proposed. The constant switching frequency is guaranteed. However, the control law requires the input voltage, thus an extra sensor is mandatory.

Disturbance rejection control has been obtaining more and more research attention recently [9]–[12]. The core idea is to compensate directly and effectively the disturbance in the control law. It is well known that the system uncertainties and disturbances are generally unmeasurable, thus the disturbance

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estimation technique based on observer is indeed crucial. The related methods include unknown input observer, disturbance observer, perturbation observer, equivalent input disturbance-based estimation, and extended state observer (ESO) [13]. The disturbance observer is normally designed based on the plant model. Therefore, the dependence severity of the observer on the plant model information is a critical index in selecting the proper observer type. Among the aforementioned observers, the ESO needs the least information about the plant, only the system order is necessary [14], [15]. The original ESO is of nonlinear form. The parameterized linear ESO by replacing the nonlinear gains with linear ones has attracted much attention, as it is easier to design and simple to implement [16], [17]. It should be pointed out that the disturbance in the ESO in fact represents the so-called total disturbance, including the plant uncertainties and external disturbances. Due to the salient feature of ESO, the ESO-based control, also known as active disturbance rejection control (ADRC), has become more and more popular. It has been applied to power converters, ac motor drives, FC air supply system, and other industry applications [18]–[22]. Simulation or experiment results show satisfactory performance.

In this article, a robust controller based on ESO is proposed for a dc–dc interleaved boost converter for FC application. The converter uncertainties and external disturbances are treated as the total disturbance, which is estimated by ESO and then eliminated in the control law. Moreover, it is presented later that the PI control can be regarded as a kind of disturbance observer-based control, it in fact uses the integral action as the disturbance estimation. Based on this point, a theoretical study is conducted to fairly evaluate and compare these two controllers. It is shown that the proposed controller has stronger robustness. Moreover, due to the relatively decoupled performance between disturbance rejection and step response, the parameter tuning of the proposed controller is much simpler. Finally, an FC stack is interfaced with the converter to corroborate the proposed method.

This article is organized as follows. In Section II, the topology and modeling of dc–dc interleaved converter is presented. In Section III, the proposed controller is devised elaborately, and the PI control is also designed for comparison. Then, in Section IV, a theoretical analysis is carried out to fairly evaluate and compare these two controllers. The simulation results in Section V and experiment result in Section VI validate the effectiveness and superiority of the proposed method. In Section VII, the comparison of the proposed controller with a controller based on disturbance observer (DO) is made. Finally, Section VIII concludes this article.

II. DC–DC Converter Modeling

The dc–dc two-phase interleaved boost converter with the control scheme is shown in Fig. 1. The topology of the converter consists of two inductors L_1 and L_2, two switches S_1 and S_2, two diodes D_1 and D_2, and a capacitor C. $v_{\rm in}$ is the input voltage, v_o is the output voltage. $r_k(k=1,2)$ is the circuit lumped parasitic resistance, and R is the load resistance. $i_{\rm in}$ is the input current, i_o is the load current, $i_{L_k}(k=1,2)$ is the current

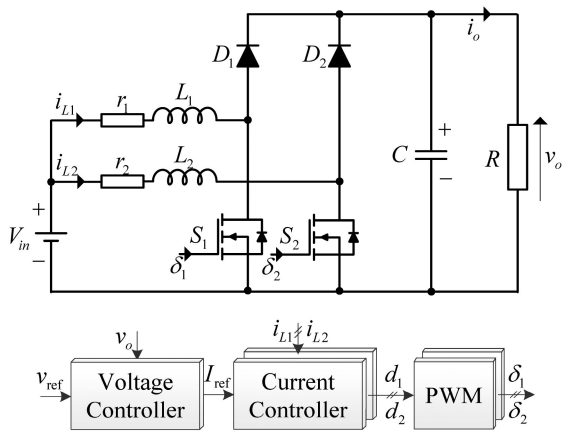

Fig. 1. Converter topology and the control scheme.

through the inductor L_k. $\delta_k(k=1,2\,)$ is the switch ON–OFF gate signal. When the switch is ON $(\delta_k=1)$, the input source charges the inductor, and the capacitor discharges to supply the load. When switch is OFF $(\delta_k=0)$, the input source together with the inductor charge the capacitor and power the load. Therefore, the converter can be modeled as:

$$\begin{cases} L_k \frac{di_{L_k}}{dt} = v_{\rm in} - r_k i_{L_k} - (1-\delta_k)\, v_o \\ C \frac{dv_o}{dt} = \sum (1-\delta_k)\, i_{L_k} - i_o \end{cases} \tag{1}$$

where $k=1,2$. The symmetric circuit parameters are generally considered for modularity design, there are $L_k = L, r_k = r$. The ideal static voltage gain of the converter operating in continuous conduction mode is

$$M\,(d) = \frac{V_o}{V_{in}} = \frac{1}{1-d} \tag{2}$$

where d is the duty cycle, V_o and $V_{\rm in}$ are the dc values of the variable v_o and $v_{\rm in}$, respectively.

The converter powered by FC suffers from input voltage variation and load current change. Therefore, to regulate a constant output voltage to better power the load, a dual-loop controller shown in Fig. 1 is requisite. The outer-loop voltage controller generates the reference current $I_{L\rm ref}$ for the inner loops, by dealing with the reference voltage and measured voltage. Then the inner loops output the duty cycles $d_i(i=1,2)$ accordingly. The duty cycle signal is sent to the pulsewidth modulation (PWM) block to produce the ON–OFF signals $\delta_i(i=1,2)$. It should be pointed out that generally the carriers in two PWM blocks are phase shifted evenly by π, in order to reduce the input current ripple based on interleaving technology.

For the inner-loop current controller, the PI algorithm based on average current control is retained. This article focuses mainly on the crucial voltage controller, and the equivalent control plant is [4]

$$G_{ie} = \frac{v_o(s)}{I_{L\rm ref}(s)} = \frac{b-cs}{s+a} \tag{3}$$

where

$$a = \frac{2}{RC}, b = 2\frac{V_{\rm in} - 2rI_L}{CV_o}, c = \frac{2LI_L}{CV_o}.$$

In the following two sections, the voltage controllers based on ESO method and PI algorithm are designed, evaluated, and compared.

III. Controller Design

A. ESO-Based Control Design

Rewrite (3) as follows by defining the control action $u = I_{Lref}$ and output variable $y = v_o$

$$\dot{y} = bu - ay - c\dot{u} = b_0 u + f \tag{4}$$

where b_0 is the value of system control gain b, $f = (b - b_0)u - ay - c\dot{u}$ is the total disturbance, which contains internal unmodeled dynamics and external unknown disturbances. Define the states as $\boldsymbol{x} = [x_1, x_2]^T = [y, f]^T$, thus (4) can be rewritten as

$$\begin{cases} \dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}u + \boldsymbol{E}\dot{f} \\ y = \boldsymbol{C}\boldsymbol{x} \end{cases} \tag{5}$$

where

$$\boldsymbol{A} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}, \boldsymbol{B} = \begin{bmatrix} b_0 \\ 0 \end{bmatrix}, \boldsymbol{E} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \boldsymbol{C} = \begin{bmatrix} 1 & 0 \end{bmatrix}.$$

In order to estimate the total disturbance, an observer named ESO, shown as follows, is constructed

$$\dot{\hat{\boldsymbol{x}}} = \boldsymbol{A}\hat{\boldsymbol{x}} + \boldsymbol{B}u + \boldsymbol{G}e \tag{6}$$

where $\hat{\boldsymbol{x}} = [\hat{x}_1, \hat{x}_2]^T = [\hat{y}, \hat{f}]^T$ is the estimation of state variable of $\boldsymbol{x} = [x_1, x_2]^T = [y, f]^T$, $e = x_1 - \hat{x}_1$ is the observer error, $\boldsymbol{G} = [g_1, g_2]^T$ is the observer gain. According to (6), the observer transfer functions are derived

$$\begin{cases} \hat{x}_1(s) = \frac{g_2 + g_1 s}{s^2 + g_1 s + g_2} y(s) + \frac{b_0 s}{s^2 + g_1 s + g_2} u(s) \\ \hat{x}_2(s) = \frac{g_2 s}{s^2 + g_1 s + g_2} y(s) - \frac{g_2 b_0}{s^2 + g_1 s + g_2} u(s). \end{cases} \tag{7}$$

To better estimate the total disturbance, g_1 and g_2 are generally tuned using the bandwidth method [16] by setting the characteristic polynomial of the observer as

$$\begin{cases} s^2 + g_1 s + g_2 = (s + \omega_0)^2 \\ g_1 = 2\omega_o,\ g_2 = \omega_o^2 \end{cases} \tag{8}$$

where ω_o is regarded as the observer bandwidth.

After obtaining the estimated total disturbance, the final control law can be designed as

$$u = \frac{u_0 - \hat{f}}{b_0}. \tag{9}$$

Thus, the control plant (4) becomes a unit gain integrator

$$\dot{y} \approx u_0 \tag{10}$$

supposing that the total disturbance is well estimated. Therefore, one can use a simple proportional control law to regulate the output voltage

$$u_0 = k_{p1}(V_{\text{ref}} - v_0) \tag{11}$$

where k_{p1} is a positive coefficient to be tuned, and V_{ref} is the output voltage reference.

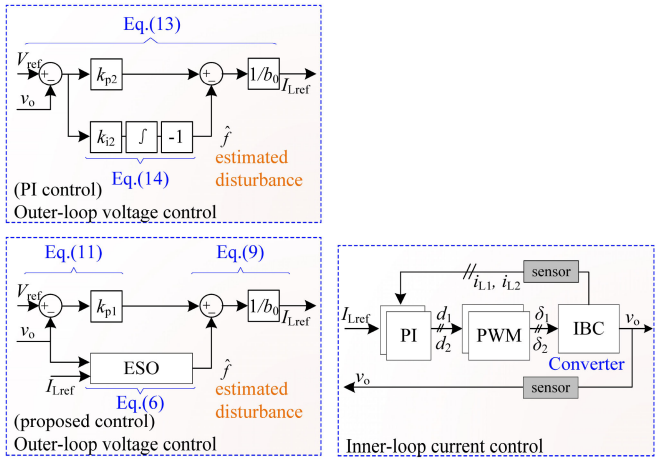

Fig. 2. Block diagram of PI controller and the proposed controller, the IBC in the figure refers to interleaved boost converter.

B. PI Control Design

The control law of PI controller is

$$u = k_p(V_{\text{ref}} - v_0) + k_i \int (V_{\text{ref}} - v_0)\, dt \tag{12}$$

where k_p and k_i are control parameters to be tuned. It is easy to rewrite (12) as follows:

$$u = \frac{k_{p2}(V_{\text{ref}} - v_0) + k_{i2} \int (V_{\text{ref}} - v_0)\, dt}{b_0} \tag{13}$$

where $k_{p2} = b_0 k_p$ and $k_{i2} = b_0 k_i$, and b_0 is a positive coefficient. By comparing (9) and (13), one can learn that the PI control in fact uses the integral action to estimate the disturbance

$$\hat{f} = -k_{i2} \int (V_{ref} - v_0)\, dt \tag{14}$$

where $\hat{f}$ is the estimated disturbance by PI controller.

Fig. 2 shows the block diagram of the PI controller and the proposed controller. According to (9), (11), and (13), both the proposed controller and PI controller have proportional control. Set $k_{p1} = k_{p2}$, then the difference between the proposed ESO-based control and the PI control is the way to estimate the total disturbance. The former controller uses the ESO, whereas the later one uses directly the integral action of voltage error. In Section IV, the performance of the two controllers in terms of antidisturbance ability, step response, and robustness are evaluated and compared.

IV. Controller Performance Evaluation and Comparison

A. Analysis of Disturbance Rejection Ability

For the proposed ESO-based controller, the transfer function from the total disturbance to the output voltage is

$$\phi_d(s) = \frac{v_o(s)}{f(s)} = \frac{s(s + g_1)}{(s + k_p)(s^2 + g_1 s + g_2)}. \tag{15}$$

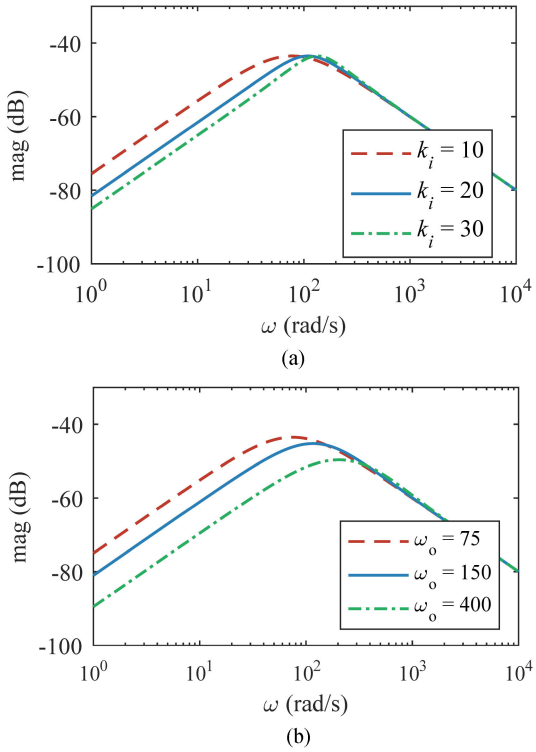

Fig. 3. Disturbance rejection performance varying with the controller parameter. (a) PI controller. (b) Proposed ESO-based controller.

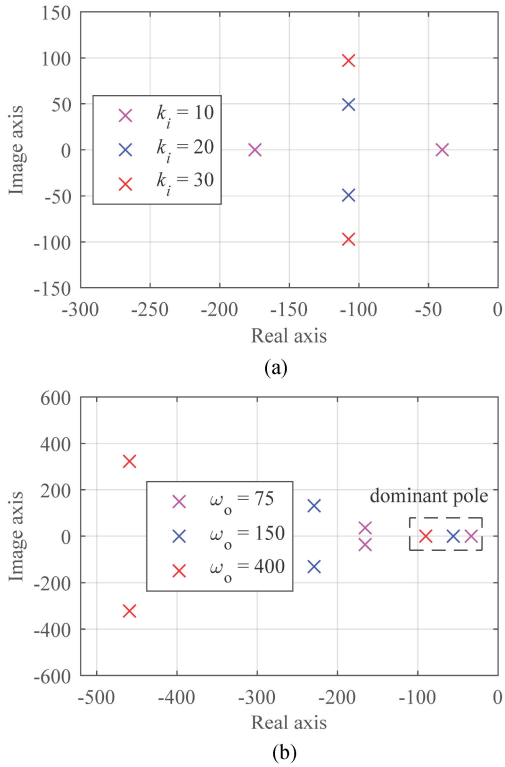

Fig. 4. Closed-loop poles location varying with the controller parameter. (a) PI controller. (b) Proposed ESO-based controller.

For the PI controller, the transfer function from the total disturbance to the output voltage is

$$\phi_d(s) = \frac{v_o(s)}{f(s)} = \frac{s}{s^2 + k_{p2}s + k_{i2}}. \tag{16}$$

The PI controller and the proposed controller have the same proportional control law, by setting $k_{p2} = 125$ ($k_p = 0.25$) and $b_0 = 500$, $k_{p1} = 125$. Fig. 3 shows the bode plot of (15) and (16). It is seen from Fig. 3(a) that the increase of k_i leads to the enhancement of the disturbance rejection ability of PI controller, as the disturbance is generally of low frequency. According to Fig. 3(b), for the proposed ESO-based controller, the increase of ω_o would strengthen the antidisturbance ability.

B. Analysis of Step Response Performance

In this section, the step response performance is evaluated by studying the closed-loop poles. For the proposed ESO-based controller, the closed-loop transfer function can be derived as

$$G_{cl}(s) = \frac{v_o(s)}{V_{ref}(s)} = \frac{H(s)C(s)G_{ie}(s)}{1 + C(s)G_{ie}(s)} \tag{17}$$

$$H(s) = k_{p1}\frac{s^2 + g_1 s + g_2}{k_{p1}\left(s^2 + g_1 s + g_2\right) + g_2 s} \tag{18}$$

$$C(s) = \frac{1}{b_0}\frac{k_{p1}\left(s^2 + g_1 s + g_2\right) + g_2 s}{s^2 + g_1 s}. \tag{19}$$

For the PI controller, the closed-loop transfer function is

$$G_{cl}(s) = \frac{v_o(s)}{V_{ref}(s)} = \frac{G_c(s)G_{ie}(s)}{1 + G_c(s)G_{ie}(s)}, G_c(s) = \frac{k_p s + k_i}{s} \tag{20}$$

$$G_{cl}(s) = \frac{-k_p c s^2 + (k_p b - k_i c)\, s + k_i b}{(1 - k_p c)\, s^2 + (a + k_p b - k_i c)\, s + k_i b}. \tag{21}$$

Based on (17) and (21), the closed-loop poles varying with the value of k_i or ω_o are plotted in Fig. 4. It can be seen from Fig. 4(a) that for the PI controller, with the increase of k_i from 10 to 20 and 30, the poles deviate the real axis, which is easy to cause overshoot during step response. Moreover, a larger k_i results in a more serious overshoot. In contrast, according to Fig. 4(b), for the proposed ESO-based controller, with the increase of ω_o from 75 to 150 and 400, the dominant pole stays in the real axis, the overshoot during step response could be avoided.

C. Robustness and Stability Analysis

To study fairly the robustness and stability performance of the proposed controller and the PI controller, both controllers are tuned based on the converter nominal operation point ($V_{\text{in}} = 18$ V, $R = 50\ \Omega$). The tuning objective is to avoid overshoot in step response and ensure the disturbance rejection ability as strong as possible.

According to the abovementioned analysis, for the PI controller, the increase of k_i leads to the enhancement of the disturbance rejection ability. However, a large value of k_i would

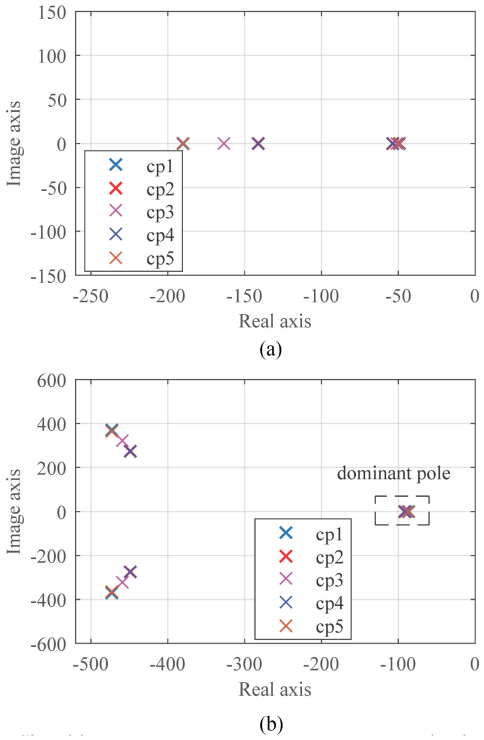

Fig. 5. Closed-loop poles location varying with the circuit parameter deviation. cp1 is $L = 440\ \mu$H, $C = 900\ \mu$F; cp2 is $L = 360\ \mu$H, $C = 1100\ \mu$F; cp3 is $L = 400\ \mu$H, $C = 1000\ \mu$F; cp4 is $L = 440\ \mu$H, $C = 1100\ \mu$F; cp5 is $L = 360\ \mu$H, $C = 900\ \mu$F. (a) PI controller. (b) Proposed ESO-based controller.

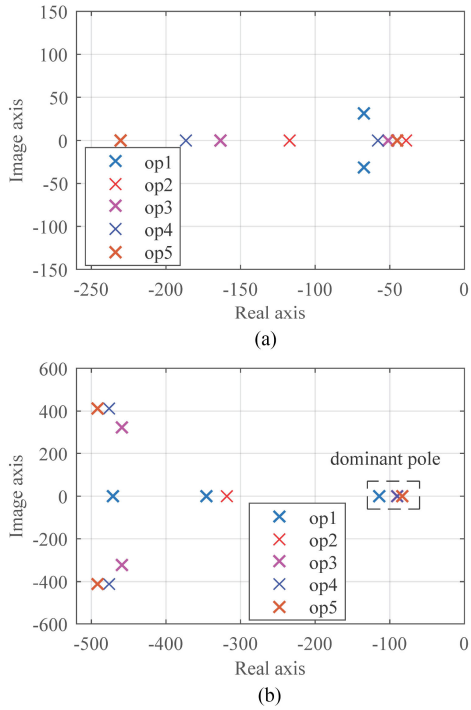

Fig. 6. Closed-loop poles location varying with the operation point. op1 is $V_{\rm in} = 12$ V, $R = 100\ \Omega$; op2 is $V_{\rm in} = 12$ V, $R = 33\ \Omega$; op3 is $V_{\rm in} = 18$ V, $R = 50\ \Omega$; op4 is $V_{\rm in} = 22$ V, $R = 100\ \Omega$; op5 is $V_{\rm in} = 22$ V, $R = 33\ \Omega$. (a) PI controller. (b) Proposed ESO-based controller.

cause overshoot during step response. Therefore, $k_i = 12$ is finally selected to avoid overshoot in step response and ensure the disturbance rejection ability as strong as possible. For the proposed ESO-based controller, the disturbance rejection ability can be strengthened by raising the value of ω_o. It is also noticed that the value of ω_o has ignored influence on step response performance, due to the existence of dominant poles. Thus, $\omega_o = 400$ can be chosen by adhering the same tuning objective with that of PI controller.

The converter for FC application inevitably suffers from circuit parameter deviation (inductance tolerance and capacitance tolerance caused by the manufacture) and operation point (source voltage and load resistance) variation. Here the robustness and stability of the two controllers are evaluated by analyzing the location of the closed-loop poles varying with the circuit parameter deviation and the converter operating point. The results are shown in Figs. 5 and 6. It is observed that the poles of both controllers are located in the left half-plane, demonstrating the good controller stability.

It can be seen from Fig. 5 that for both controllers, the deviation of the inductance and capacitance have small influence on the poles location, showing good robustness. It can be also seen from Fig. 6(a) that for the PI controller, the poles in case of $V_{\rm in} = 12$ V, $R = 100\ \Omega$ (op1 in the figure) deviates from the real axis, which would result in overshoot during step response. In contrast, as shown in Fig. 6(b), for the proposed ESO-based controller, the dominant poles keep in the real axis, good step response performance could be achieved. Therefore, the proposed controller shows stronger robustness to the operation point variation.

TABLE I
NOMINAL CIRCUIT PARAMETER OF IBC CONVERTER

Description	Variable	Value
Output voltage	$V_{\rm o}$	48 V
Input voltage	$V_{\rm in}$	12 ~ 22 V
Inductor current	$I_{\rm L}$	0 ~ 7 A
Inductor	L	400 µH
Inductor resistor	$r_{\rm L}$	0.43 Ω
Capacitor	C	1000 µF
Capacitor resistor	$r_{\rm C}$	0.04 Ω
Switching frequency	$f_{\rm s}$	25 kHz

V. SIMULATION VALIDATION

To validate the theoretical analysis and demonstrate the effectiveness of the proposed method, the interleaved boost converter and the controllers are established using the SimPowerSystem library based on MATLAB/Simulink. The converter circuit parameters are $L = 400\ \mu$H, $r_{\rm L} = 0.43\ \Omega$, $C = 1000\ \mu$F, $r_{\rm C} = 0.04\ \Omega$, as listed in Table I. The nominal input voltage is 18 V, and the nominal load resistance is 50 Ω. For the inductor current inner-loop, the parameter of PI controller is $k_p = 0.085$, $k_i = 40$. For the output voltage outer-loop, the controller parameters tuned in Section IV is adopted, that is, $k_p = 0.25$ ($k_{p2} = 125$), $k_i = 12$ for PI controller, and $b_0 = 500, k_{p1} = 125, \omega_o = 400$ for the proposed controller.

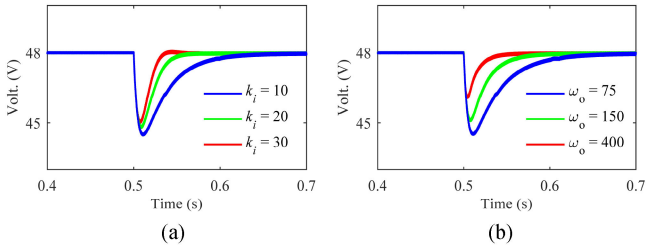

Fig. 7. Simulation results of the converter voltage response under step load disturbance from 100 to 33 Ω at $t = 0.5$ s, $v_{\text{in}} = 18$ V. (a) PI controller. (b) Proposed ESO-based controller.

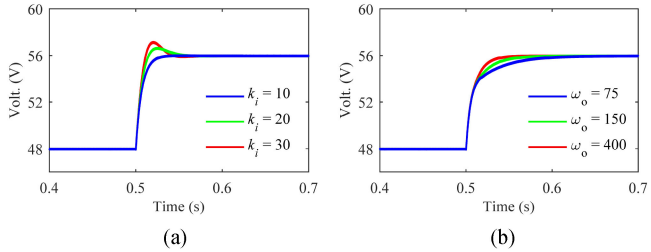

Fig. 8. Simulation results of the converter voltage response under step voltage reference from 48 to 56 V at $t = 0.5$ s, $v_{\text{in}} = 18$ V, $R = 50$ Ω. (a) PI controller. (b) Proposed ESO-based controller.

A. *Influence of Controller Parameter on Controller Performance*

The influence of the controller parameter (k_i and ω_o) on the controller performance is studied. Fig. 7 shows the simulation result of the voltage response under step load disturbance with PI controller and proposed ESO-based controller, respectively. It is observed from the figure that the increase of k_i or ω_o would accelerate the voltage recovery and reduce the voltage drop after applying the disturbance, showing better antidisturbance ability. The simulation results coincide with the theoretical analysis in Section IV-A.

Fig. 8 presents the simulation result of the voltage response under step reference with PI controller and proposed ESO-based controller, respectively. It is seen from the figure that for the PI controller, the increase of k_i could cause overshoot in step response. In contrast, it is noted that for the proposed controller, raising the value of ω_o would not introduce overshoot in step response. This is because that according to Fig. 4 of Section IV-B, for the PI controller, the increase of k_i would cause the deviation of the poles from the real axis. However, for the proposed controller, despite the increase of the value of ω_o, the introduced dominant pole by ESO stays in the real axis, resulting in zero overshoot.

B. *Robustness to Converter Circuit Parameter Deviation*

Fig. 9 shows the simulation results of the converter performance of the PI controller and the proposed controller in terms of inductance and capacitance deviation. The voltage reference steps from 48 to 56 V at $t = 0.5$ s, it is shown that the voltage responses of both controller are almost consistent. The good

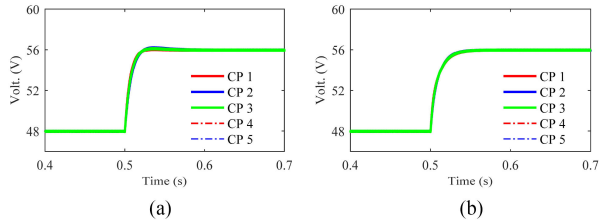

Fig. 9. Simulation results of the voltage response under step voltage reference from 48 to 56 V at $t = 0.5$ s with circuit parameter deviation. CP 1 is $L = 440$ μH, $C = 900$ μF; CP 2 is $L = 360$ μH, $C = 1100$ μF; CP 3 is $L = 400$ μH, $C = 1000$ μF; CP 4 is $L = 440$ μH, $C = 1100$ μF; CP 5 is $L = 360$ μH, $C = 900$ μF. (a) PI controller. (b) Proposed ESO-based controller.

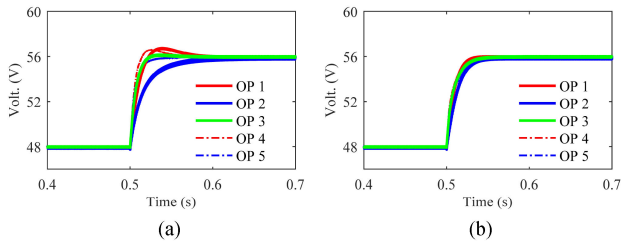

Fig. 10. Simulation results of the voltage response under step voltage reference from 48 to 56 V at $t = 0.5$ s with different operation point. OP 1 is $V_{\text{in}} = 12$ V, $R = 100$ Ω; OP 2 is $V_{\text{in}} = 12$ V, $R = 33$ Ω; OP 3 is $V_{\text{in}} = 18$ V, $R = 50$ Ω; OP 4 is $V_{\text{in}} = 22$ V, $R = 100$ Ω; OP 5 is $V_{\text{in}} = 22$ V, $R = 33$ Ω. (a) PI controller. (b) Proposed ESO-based controller.

robustness of the controllers to the inductance and capacitance tolerance are verified.

C. *Robustness to Converter Operation Point Variation*

The robustness of the controllers against the operation point change is tested by selecting five typical operation points. Fig. 10 shows the converter performance of PI controller and the proposed ESO-based controller, respectively. It is observed from Fig. 10(a) that for the PI controller, the voltage overshoot varies from 0% to 9.25%. According to Fig. 10(b), for the proposed controller, the zero voltage overshoot is maintained. It is also noted that the voltage responses of the proposed controller are almost overlapped, demonstrating stronger robustness. The simulation results are consistent with the theoretical analysis in Section IV-C.

VI. Experiment Results

To experimentally validate the proposed method, a 100-W converter prototype is built. The circuit parameter configuration is the same as that in the simulations (see Table I). The controllers model established in Section V are then implemented into the dSPACE platform. The controller parameters are the same as that in the simulations. An FPGA board is utilized for even phase shifting to optimize the input current ripple. After passing through the FPGA board, the phase of signal δ_2 is delayed by π, in comparison with that of signal δ_1. Fig. 11 shows the block diagram and picture of the experiment setup. To validate the effectiveness of the proposed method for FC application, a 20-cell 100-W FC stack modeled in [23] and [24] is used. This

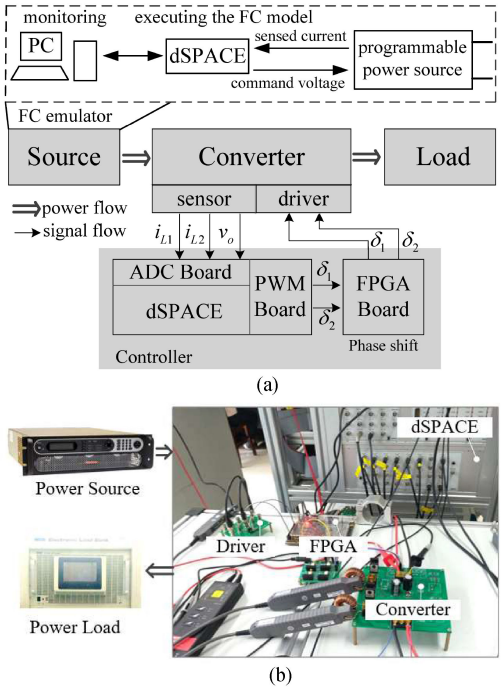

Fig. 11. Block diagram and picture of the experiment setup. (a) Block diagram of the experiment setup. (b) Picture of the experiment setup.

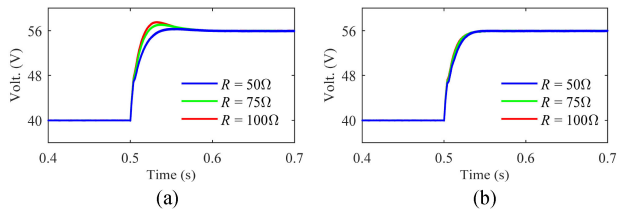

Fig. 12. Simulation results of the output voltage response of the converter interfaced with an FC stack under step voltage reference from 40 to 56 V at $t = 0.5$ s with different load resistance. (a) PI controller. (b) Proposed ESO-based controller.

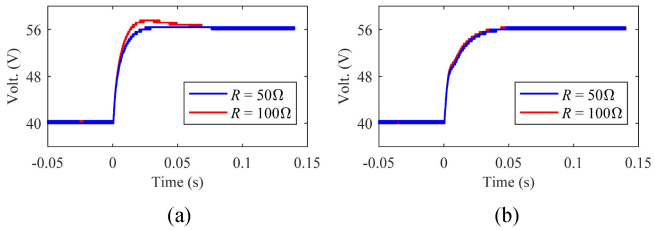

Fig. 13. Experiment results of the output voltage response of the converter interfaced with an FC stack under step voltage reference from 40 to 56 V at $t = 0$ s with different load resistance. (a) PI controller. (b) Proposed ESO-based controller.

FC stack model is executed in dSPACE in real time, then the computed FC voltage value is sent to a programmable power source to output the desired voltage to power the converter. The oscilloscope DPO2014B from Tektronix is utilized to acquire the experiment results.

Figs. 12 and 13 show, respectively, the simulation and experimental results of the voltage response of the converter interfaced

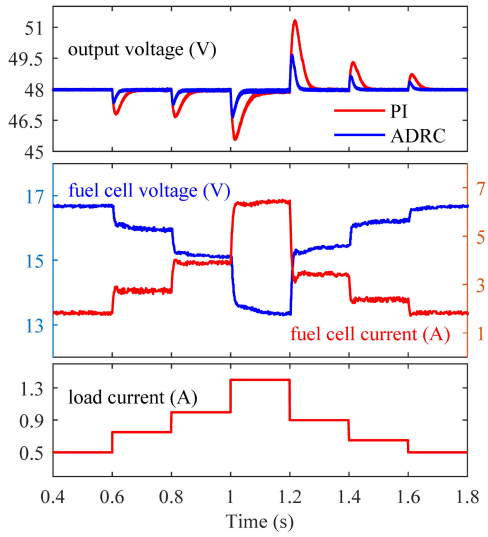

Fig. 14. Simulation results of the converter interfaced with an FC stack under load current disturbance.

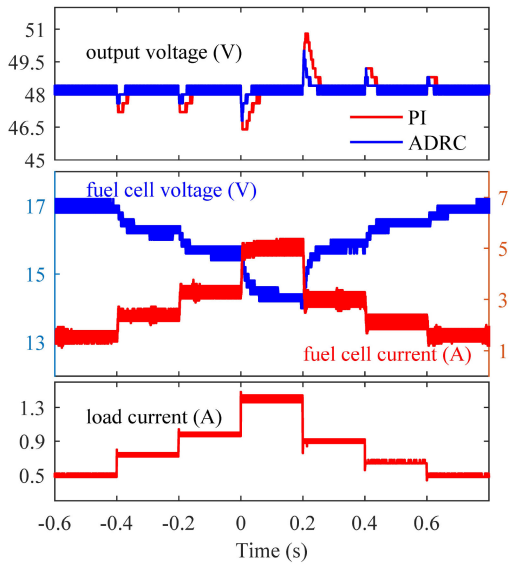

Fig. 15. Experiment results of the converter interfaced with an FC stack emulator under load current disturbance.

with the aforementioned FC stack under step voltage reference with different load resistance. The experiment results agree with the simulation results. It is calculated from the simulation results that during the transient of step reference from 40 to 56 V, for the PI controller, the voltage overshoot varies from zero (load resistance $R = 50\ \Omega$) to 9.4% (load resistance $R = 100\ \Omega$). In comparison, the voltage responses of the proposed ESO-based controller are almost overlapped, and the overshoot is zero, despite the variation of the load resistance. It is verified that the proposed controller is effective for FC application and has stronger robustness than PI controller against the converter operation point deviation.

Figs. 14 and 15 display, respectively, the simulation and experiment results of the converter interfaced with an FC stack under

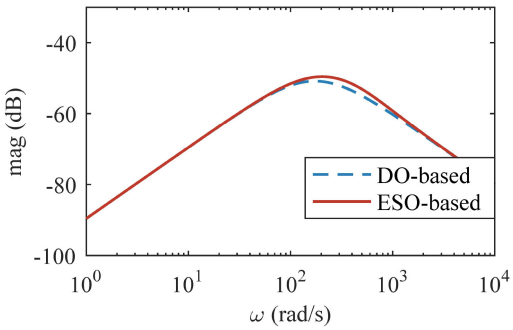

Fig. 16. Comparison of the DO-based controller and the proposed ESO-based controller in terms of disturbance rejection ability.

load current disturbance. The experiment results coincide with the simulation results. The ripple of fuel cell voltage and current in the simulation results are less than that in the experimental results, as they are sampled value. The dynamic step load current disturbance is applied to the converter, it is noted from the simulation results that the FC current varies from 1.8 to 6.4 A, and the FC voltage varies from 16.7 to 13.3 V accordingly. Both controllers can achieve accurate voltage regulation in steady state. Meanwhile, it is noted that the proposed ESO-based ADRC controller shows much better voltage response during disturbance transient than PI controller, with less voltage drop/raise and shorter recovery time. The stronger disturbance rejection ability of the proposed controller is thus demonstrated, and the feasibility of the proposed method for FC application is also verified.

VII. Comparison of the Proposed Controller With a Controller Based on Disturbance Observer

In this section, the comparison with a disturbance observer (DO) based controller, which has similar structure with the proposed method, is made. It uses the DO to estimate the total disturbance, and then cancel it in the control law. The DO is constructed as follows:

$$\dot{\hat{f}} = \omega_o \left(f - \hat{f} \right) = \omega_o \left(\dot{y} - b_0 u - \hat{f} \right) \tag{22}$$

where $\hat{f}$ is the disturbance estimation, and ω_o is the observer bandwidth. Therefore, the final control law is

$$u = \frac{u_0 - \hat{f}}{b_0}, u_0 = k_{p3} \left(V_{\text{ref}} - v_o \right) \tag{23}$$

which is the same as (9) and (11). The corresponding transfer function from the total disturbance to the output voltage can be derived as

$$\phi_d(s) = \frac{v_o(s)}{f(s)} = \frac{s}{(s + k_{p3})(s + \omega_o)}. \tag{24}$$

The proportional coefficient k_{p3} is set as $k_{p3} = k_{p1} = 125$. Moreover, to ensure a fair comparison, the bandwidth of the DO is tuned as $\omega_o = 200$, such that it has similar disturbance rejection ability with the proposed controller based on ESO. The bode plots of (15) and (24) are shown in Fig. 16.

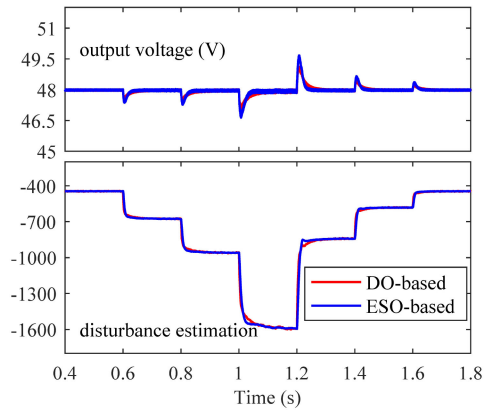

Fig. 17. Simulation results of the converter interfaced with an FC stack, without measurement noise in the output voltage.

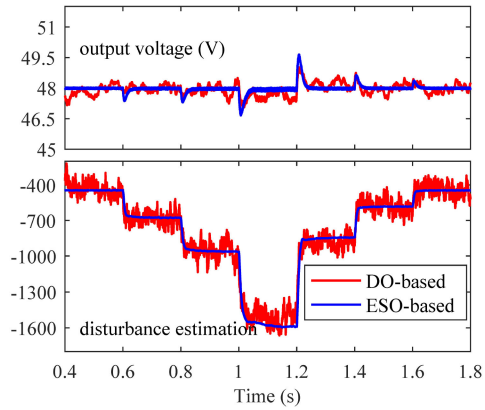

Fig. 18. Simulation results of the converter interfaced with an FC stack, with Gaussian random noise in the output voltage.

The interleaved boost converter is interfaced with the FC stack mentioned in Section VI. Applying the load current disturbance in Fig. 14 to the converter, the simulation results are obtained and shown in Fig. 17. It is observed that the two controllers can achieve almost consistent performance, including the output voltage and the disturbance estimation. However, when the output voltage contains the measurement noise, the controllers behave different. Fig. 18 shows the simulation results when the measured output voltage is polluted by a Gaussian random noise (mean = 0, variance = 0.01). It is seen that the proposed ESO-based controller still shows good performance, whereas the DO-based controller not. The DO-based controller is more sensitive to the measurement noise, due to the inclusion of the derivation in the right side of (22). The proposed ESO-based controller shows better measurement noise suppression performance.

VIII. Conclusion

In this article, a robust controller based on ESO is proposed for a dc–dc interleaved boost converter for FC application. The proposed controller treats the converter uncertainties and external disturbances as total disturbance, which is estimated

by ESO and then canceled in the control law. The PI control is also designed for comparison. By rewriting the PI control law as the same form of disturbance observer-based control, it is revealed that the PI control in fact uses the integral action to estimate the total disturbance. A theoretical study is then conducted to fairly evaluate and compare the performance of these two controllers, regarding disturbance rejection ability, step response, robustness, and stability. It is shown that the proposed controller has stronger robustness and has relatively decoupled performance between antidisturbance and step response. Thus, it is easier to tune the controller parameter. Simulation and experiment results are shown to demonstrate the effectiveness of the proposed controller. The proposed method does not need extra sensors; therefore, it can be also applied to the already fabricated converter by implementing into the available digital control system directly. The proposed method can be extended to other dc–dc converters as well.

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