Dynamic Switching of SiC Power MOSFETs Based on Analytical Subcircuit Model

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***Abstract*—Compared to silicon counterparts, silicon carbide (SiC) power MOSFETs have lower ON-state resistance and faster switching speed, which in turn makes them better candidates for high-voltage power switching applications. This creates a growing need to develop device models for such SiC power devices. The models that are currently being used are mostly physics-based models, which require all the physical parameters of the device and are not so suitable for real time hardware in loop simulations. In this article, we show a subcircuit model based on the analytical study using nonlinear curve fitting method for modeling of dynamic switching behavior. Using a 1.2 kV, 17 A MOSFET as a testbed, this subcircuit model is validated by implementing the model into Synopsys Saber in comparison with the measured dc characteristics, the Saber MOSFET Tool model, and the manufacturer's model. The switching behavior of the device at 800 V/17 A and 800 V/5.5 A based on the subcircuit model were also compared and validated with experimental measurements, the Saber MOSFET model, and manufacturer's model. Excellent agreements were achieved on both dc characteristics and switching behaviors. On the LTspice platform, the computation time of the analytical subcircuit model is 4.5 times faster than the manufacturer's model. This subcircuit model is adoptable and suitable for real time hardware in loop simulations and power converter designs.**

***Index Terms*—Device modeling, double pulse test, power switching, SIC MOSFETs.**

I. Introduction

COMPARED to silicon-based power devices, devices made of wide bandgap semiconductors materials, such as silicon carbide (SiC) and gallium nitride, have superior advantages as follows.

1) *Energy bandgap:* A wider energy bandgap results in lower leakage currents and higher operating temperatures.
2) *Critical electric field:* Wide bandgap semiconductor devices have higher critical electric fields so that the devices can have higher doping concentrations with thinner blocking layers, and resulting in lower specific on resistance.
3) *Electron saturation velocity:* These wide bandgap semiconductors also have a high electron saturation velocity, which leads to higher operating frequencies compared to equivalent silicon-based devices.
4) *Thermal conductivity:* Some wide bandgap semiconductors like SiC and diamond have a high thermal conductivity, which improves heat spreading and allows operation at higher power densities [1].

A lot of efforts have been made to improve the performance of SiC power devices recently. The basic characteristics of SiC MOSFETs and their potential utilization in power electronics and power converter systems have been deeply investigated. For applications of these power MOSFETs, fast and accurate models are also critically needed. So far, the efforts on SiC MOSFET modeling have mainly been focused on developing physics-based models for SiC MOSFETs [2]–[4] with some work done in analytic-based behavioral device models [5], [6]. To develop physics-based device models, it is necessary to be familiar with the whole device fabrication process and all device structural information like the device channel length and width, the thickness of the gate oxide layer, N-drift region and substrate, doping concentration of the junction field-effect transistor (JFET) region, P-wells, N-drift region, etc. However, such information is generally not available to chip users. Moreover, such physics-based models are not suitable for real time hardware in loop simulation because of the lengthy computation time required in such complex models. To reduce the computation time, Chen *et al*. [5], [6] used a mature Si MOSFET modeling Tool, the Synopsys Saber Power MOSFET Tool, to quickly build models for SiC MOSFETs. This tool works really well for a Level 1 model since this model is a first-order approximation of long channel devices. It does not account for short-channel effects and also assume that the threshold voltage remains constant. While this is a very attractive modeling tool for Level 1 models it turns out to be less accurate for higher level models. It simplifies the model highly and fails to recognize parameters like variable threshold voltage and effects like the short-channel effects. This method is also not compatible with other commercial simulators like Pspice or PSim as compared to the behavioral or physical models. The topology of the behavioral MOSFET model is represented by a steady-state behavior and modeled resistances. The transient state is modeled by adding modeled capacitance and inductances to the steady-state model. [7], [8].

On the other hand, analytical-based subcircuit models are generally less complex and requiring significantly less computation time. However, quite often these analytic models are less accurate. An analytical model of SiC MOSFETs developed by McNutt *et al*. [9] demonstrated a good agreement with device characteristics. While their model was straight forward and accurate, the use of multiple IMPACT programs, a compact circuit simulator, for parameter extraction was considered a quite

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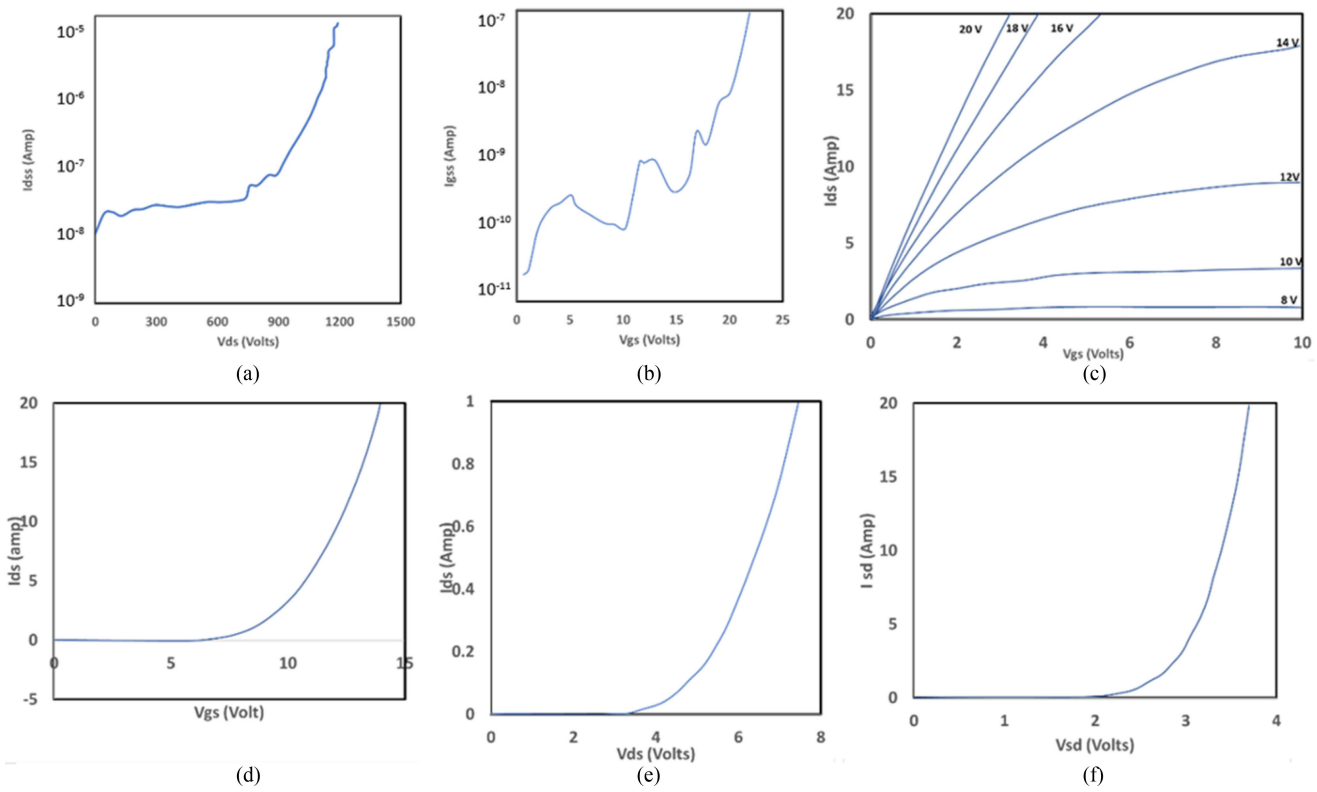

Fig. 1. Plots displaying the dc characteristics of a 1.2 kV SiC power MOSFET. (a) $I_{\rm dss}$. (b) $I_{\rm gss}$. (c) $I_{\rm ds}$–$V_{\rm ds}$ output characteristics. (d) Transfer characteristics at $V_{\rm ds} = 10$ V. (e) Transfer characteristics at $V_{\rm ds} = V_{\rm gs}$. (f) Body diode forward I–V characteristics.

complicated procedure for parameter extraction and subsequently circuit simulator coding. Another analytical model developed by Wu shows good agreement to an LTspice model but was not validated experimentally [10].

The objective of this article is to study the fast-switching-speed behavior of SiC power MOSFET using a more accurate analytical-based subcircuit model that does not require any physical or geometrical parameters from the device while providing a shorter computation time. To achieve this goal, we use SiC MOSFETs manufactured by RoHM with 1.2 kV breakdown voltage and 17 A current as a test bed. A simplified analytical model is adopted and implemented in a subcircuit model for SiC MOSFETs that can be used for real time hardware in loop simulations and power converter designs. The Synopsis Saber MOSFET model and the chip manufacturer's model will be used for comparison and validation. The extracted device parameters in the subcircuit model will be implemented in LTspice simulator platform to compare with the simulation results from Saber MOSFET model on Saber platform and the manufacturer's model on LTspice platform and measured dynamic switching behavior. In the following sections, we will present the static characteristics of the tested SiC MOSFET, followed by static modeling, dynamic characterization, and model validation.

II. Static Characterizations of SiC MOSFET

For demonstration, we used a 1.2 kV, 17 A SiC MOSFET [11] manufactured by RoHM in a package of TO-247. The device characterization is performed using an Agilent B1505A curve tracer and Agilent N1259A high power test fixture. The classical approach for device characterization is followed to measure the static characteristics for the SiC MOSFET [12], [13]. The tests were performed in pulse mode with a pulse duration of 50 ms and a duty cycle of 5%.

A. Drain–Source Leakage Current $I_{\rm dss}$

$I_{\rm dss}$, the drain–source leakage current, is shown in Fig. 1(a) plotted against the drain–source voltage. As shown in the figure, the drain–source leakage current for this device is about 8 μA at 1200 V drain–source voltage. When the drain voltage is above 1200 V, it can be clearly seen that the current increase dramatically due to the avalanche effect caused by impact ionization.

B. Gate–Source Leakage Current $I_{\rm gss}$

Fig. 1(b) shows $I_{\rm gss}$ of about 80 nA at $V_{\rm gs} = 22$ V at $V_{\rm ds} = 0$. The device has a low leakage current ($<$5 nA) if $V_{\rm gs} < 20$ V.

C. Output and Transfer Characteristics

The output characteristics were measured for different gate biases ($V_{\rm gs}$) ranging from 8 to 20 V at a 2-V interval. The transfer characteristics are obtained at a constant $V_{\rm ds}$ of 10 V. Fig. 1(c) and (d) are the output and transfer characteristics for the SiC MOSFET at room temperature. The device has a saturation current of 17 A at $V_{\rm gs} = 14$ V, and a threshold voltage of 5.28 V at the current of 10 μA.

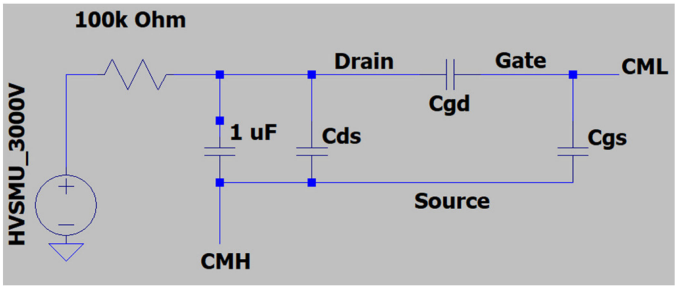

Fig. 2. Configuration scheme for $C_{\rm iss}$ measurement.

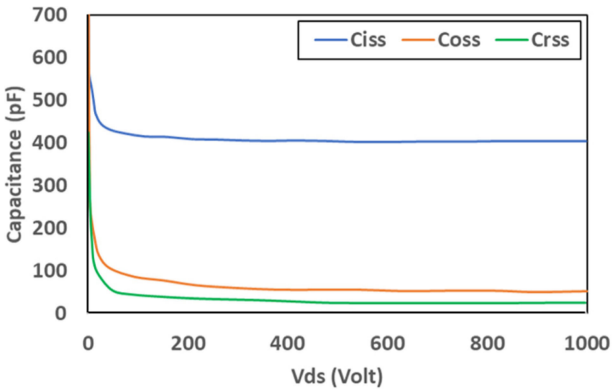

Fig. 3. Plot displaying the measured $C_{\rm oss}$, $C_{\rm rss}$, $C_{\rm iss}$ at different drain biases for the 1.2-kV SiC power MOSFET.

D. ON-State Resistance $R_{ds(on)}$

The total ON-state resistance is the sum of the eight resistances, source contact resistance, source resistance, channel resistance, accumulation resistance, JFET resistance, drift region resistance, substrate resistance, and the drain contact resistance [14]. Here, $R_{\rm ds(on)}$ is obtained to be about 0.133 Ω at $V_{\rm g} = 20$ V, and $I_{\rm d} = 15$ A. This ON-state resistance is within the expected range according to the data sheet.

E. Gate Turn-on Voltage

If the gate turn-ON voltage, $V_{\rm gs(th)}$, is defined as the gate–source voltage that produces 10 μA drain current when the drain and gate terminals are shorted ($V_{\rm gs} = V_{\rm ds}$) [15], we obtain $V_{\rm gs(th)} = 3.15$ V as shown in Fig. 1(e).

F. Body Diode I–V Characteristics

Unlike a conventional lateral structure MOSFET, a vertical device like SiC power MOSFET has an intrinsic body diode. The forward biased body diode *I–V* curve is shown in Fig. 1(f). This body diode is used by the upper device as the freewheeling diode in the dynamic switching characterizations shown later.

G. Nonlinear Junction Capacitances C_{oss}, C_{rss}, C_{iss}

To perform capacitance measurements, we used the Agilent B1505A Power Device Analyzer/Curve Tracer with the multiple frequency capacitance measurement units.

1) Output Capacitance: $C_{oss}(=C_{ds} + C_{gd})$: $C_{\rm oss}$ plotted in Fig. 3 is measured under $F = 100$ KHz, $V_{\rm ds}$ from 0 to 1000 V with 1-V step at a signal level of 20 mV. $C_{\rm oss}$ is 44 pF at 1000 V.

2) Reverse Capacitance: $C_{rss}(=C_{gd})$: $C_{\rm rss}$, equivalent to $C_{\rm gd}$, is also measured under same conditions and is shown in Fig. 3. $C_{\rm rss}$ is 20 pF at 1000 V.

3) Input Capacitance: $C_{iss}(=C_{gd} + C_{gs})$: For the input capacitance measurement, an external blocking resistor (100 kΩ) and a capacitor (1 *u*F) were used (Fig. 2). The capacitance should be much larger than C_{gd} or $C_{\rm ds}$ since the capacitor acts as a dc blocking capacitor. The measured capacitance is C_{gs} in parallel with the series combination of C_{gd} and (1 μF + $C_{\rm ds}$). Finally, we can get the measured capacitance $C_{\rm m} \approx C_{gd} + C_{gs} = C_{iss}$. In this work, C_{iss} was also measured under $f = 100$ kHz, $V_{\rm ds}$ from 0 to 1000 V with 1-V step, oscillation signal level of 20 mV. Fig. 3 shows the measured C_{iss} as a function of $V_{\rm ds}$. C_{iss} is 394 pF at 1000 V.

H. Internal Gate Resistance R_{gi}

Along with the three nonlinear capacitances, the internal gate resistance is also a vital parameter since it affects the switching speed of the device. The measurement of R_{gi} was carried out with an *LCR* Meter measuring the gate and source terminals while the drain and source terminals were shorted [8]. The R_{gi} was measured to be 0.5 Ω at 100 kHz.

I. Package Stray Inductance Measurement

The device is packaged in a TO-247 package. The stray impedances introduced by the package can be expressed as three inductances $L_{\rm G}$, $L_{\rm D}$, and $L_{\rm S}$, which are in series with the gate, drain, and source terminals, respectively [16]. Inductances were measured between the root of the leads and center of die contact. In this case, the inductances were measured to be $L_{\rm G} = 9.2$ nH, $L_{\rm D} = 6.1$ nH, and $L_{\rm S} = 7.5$ nH.

III. Static Modeling and Validation of SiC MOSFET

To make the device model adoptable and suitable in the system-level simulation for power circuit designs, a concise model is preferred to make the system-level simulation run as fast as possible. As described earlier, physics-based models generally require the physical dimensions and a lot of other parameters to build. However, most of these parameters that are needed to develop models are not directly available to circuit designers and system engineers. Apart from this, physical models also take a longer computation time, which is not suitable for real time hardware in loop simulations. To minimize the computation time, a sub-circuit model is developed that incorporates the concepts of an analytical model to describe the intrinsic dc behaviors. The advantage to build subcircuit models is that by doing characterization of devices, model parameters can be directly extracted from characterization results without knowing detailed structure information of devices [5], [6]. For validation, we implemented the subcircuit model into Saber Synopsys to simulate the dc characteristics in comparison with the Saber MOSFET model on the same platform and the manufacturer's model on the LTspice platform.

A. Analytical Subcircuit Model

The subcircuit model structure of SiC MOSFET is shown in Fig. 4. The model includes a metal–oxide–semiconductor (MOS), three junction capacitors, a reverse body diode, an internal gate resistor, and three package stray inductors. The

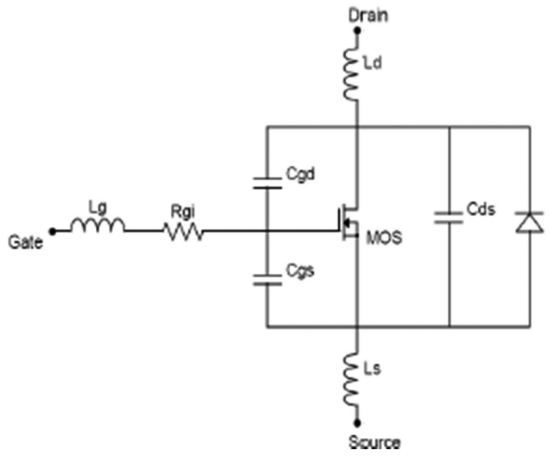

Fig. 4. Equivalent circuit diagram for a power MOSFET using the subcircuit model.

details of the main components of the SiC MOSFET subcircuit model are included in the following.

1) MOS: The MOS part is modeled as a voltage controlled current source, which can be used to describe the static *I–V* output and transfer characteristics of the device. The standard analytic model is used to describe the output characteristics at the cutoff, linear, and the saturation regime [17]

$$V_{gs} - V_{\rm th} \le 0 \ (\text{Cut} - \text{off regime}) \, I_{\rm d} = 0 \tag{1}$$

$$0 \le V_{\rm ds} \le \ V_{gs} - V_{\rm th} \, (\text{Linear regime})$$

$$I_{\rm d} = \frac{\beta}{2} V_{\rm ds} \left[2 \left(V_{gs} - V_{\rm th}\right) - \ V_{\rm ds}\right] \left(1 + \lambda V_{\rm ds}\right) \tag{2}$$

$$0 \le \ V_{gs} - V_{\rm th} \le V_{\rm ds} \, (\text{Saturation regime})$$

$$I_{\rm d} = \frac{\beta}{2} \left(V_{gs} - V_{\rm th}\right)^2 \left(1 + \lambda V_{\rm ds}\right) \tag{3}$$

where $\beta = \mu_n C_{ox} WL$, μ_n is the charge-carrier effective mobility, C_{ox} is the capacitance of the oxide layer, L is the channel length, and W is the channel width. Since the device dimensions (gate oxide thickness and channel width/length ratio are not available, the parameter β and λ (channel-length modulation parameter) were extracted using a nonlinear curve-fitting method. This behavior model was implemented into the Saber simulator. The results are shown in Fig. 6(a) and (b). A good agreement is achieved between the measurement and modeling results. The threshold voltage $V_{\rm TH,MOS,Analytical}$ is 5.2 V, β is 0.2366 $\rm AV^{-2}$, and λ is 0.03963 $\rm V^{-1}$ obtained through extraction, as shown in Table I.

2) Three Junction Capacitance: Here, the three junction capacitors $C_{\rm iss}$, $C_{\rm oss}$, and $C_{\rm rss}$ are just modeled simply as constant values based on the following relationships: $C_{\rm rss}$ $(=C_{\rm gd})$, $C_{\rm oss}$ $(=C_{\rm gd} + C_{\rm ds})$, and $C_{\rm iss}$ $(=C_{\rm gd} + C_{\rm gs})$. This assumption is valid for this work since the capacitances are essentially constants after $V_{\rm ds} = 150$ V, as shown in Fig. 3. The measured values at a drain voltage of 1000 V at 100 kHz are used. At this condition, as shown in Table I, $C_{\rm iss}$ is 394 pF, $C_{\rm oss}$ is 44 pF, and $C_{\rm rss}$ is 20 pF, respectively.

3) Body Diode: The diode is modeled in Saber as a power diode connected in antiparallel with the MOSFET. The widely known analytical model is used to design the diode along with its device characteristics ($I_{\rm ds}$–$V_{\rm ds}$) that can be tuned visually to fit the measurement result [18], [19]

TABLE I
DEVICE PARAMETERS IN THE SUBCIRCUIT MODEL

Parameter	Value	Description
	MOS	
β (A/V^2)	0.2366	Device Constant (β=$\mu_n C_{ox} WL$)
$V_{\rm TH,MOS,Analytical}$ (V)	5.2	Threshold Voltage
$\lambda_{\rm Analytical}$ ($\rm V^{-1}$)	0.03963	Channel-length Modulation Parameter
	Junction Capacitors	
$C_{\rm gs}$ (pF) at $V_{\rm ds}$=1000V	394	Gate-Source Capacitance
$C_{\rm ds}$ (pF) at $V_{\rm ds}$=1000V	44	Dain-Source Capacitance
$C_{\rm gd}$ (pF) at $V_{\rm ds}$=1000V	20	Gate-Drain Capacitance
	Power Diode	
$R_{\rm s,Analytical}$ (Ω)	0.025	Diode Series Resistance
$I_{\rm LS,Analytical}$ (A)	1.56 x 10^{-6}	Saturation Current for Low-Level Injection
$V_{\rm tll,Analytical}$ (V)	0.21	Threshold Voltage for Low-Level Injection
$I_{\rm HS,Analytical}$ (A)	1.10 x 10^{-5}	Saturation Current for High-Level Injection
$V_{\rm thl,Analytical}$ (V)	3.2	Threshold Voltage for High-Level Injection
	Internal Gate Resistor	
$R_{\rm gi,Measured}$ (Ω)	0.5	Internal Gate Resistance
	Package Stray Inductors	
$L_{\rm G,Measured}$ (nH)	9.2	Gate Terminal
$L_{\rm D,Measured}$ (nH)	6.1	Drain Terminal
$L_{\rm S,Measured}$ (nH)	7.5	Source Terminal

$$V_{\rm tll} \le \ V \le V_{\rm thl}$$

$$I_{\rm d} = I_{\rm LS} \left[\exp\left(\frac{q(V_{\rm tll} - IR_{\rm s})}{kT}\right) - 1\right] \tag{4}$$

$$V \ge V_{\rm thl}$$

$$I_{\rm d} = \ I_{\rm HS} \left[\exp\left(\frac{q(V_{\rm thl} - IR_{\rm s})}{2kT}\right) - 1\right] \tag{5}$$

where q is the electron charge, k is the Boltzmann constant, and T is the temperature in Kelvin. Other parameters that were extracted from diode *I–V* characteristics include the following:

1) $R_{\rm s}$: series resistance;
2) $I_{\rm LS}$: saturation current for low-level injection;
3) $V_{\rm tll}$: threshold voltage for low-level injection;
4) $I_{\rm HS}$: saturation current for high-level injection; and
5) $V_{\rm thl}$: threshold voltage for high-level injection.

This diode model was implemented into the Saber simulator to simulate the diode characteristics. The comparison of modeled and measured result is shown in Fig. 6(d).

4) Other Parameters: The values of internal gate resistance R_{gi} and package stray inductances $L_{\rm G,Measured}$, $L_{\rm D,Measured}$, and $L_{\rm S,Measured}$ are directly used in the model. All the parameters for the SiC MOSFET model are listed in Table I.

B. Saber Power MOSFET Model for Validation

The Power MOSFET Tool in Saber is a convenient way to develop an accurate SiC MOSFET model. The Power MOSFET Tool provides support to generate Level 1 MOSFET models intended for evaluation in power electronic circuits. These models are well suited for examining switching transients and losses in power

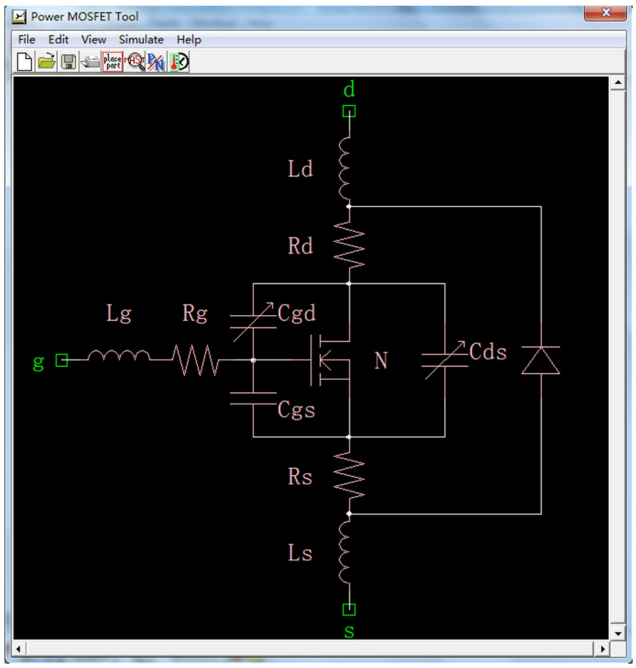

Fig. 5. Saber Power MOSFET Tool Interface demonstrating its equivalent circuit for a power MOSFET.

TABLE II
BIASING CONDITION USED IN SABER TOOL AND GENERATED PARAMETERS OF SABER MODEL FOR *I–V* CHARACTERISTICS

Parameter	Value	Description
Temp (°C)	25	Temperature at which the subsequent parameters are specified
$V_{th,MOS,Saber}$ (V)	5.2	Threshold voltage
vgs_0(V), vds_0(V), ids_0(A)	12, 6, 7.3	Coordinates of a point on the id (vds_0, vgs_0) surface located at the boundary between quasi-linear and saturation regions.
rds0(Ω)	0.035	Device resistance when drain bias is close to zero and gate bias is equal to vgs_0
Rs(Ω)	0.0041	Series resistance at the source terminal
Rd(Ω)	0.037	Series resistance at the drain terminal
Rg(Ω)	0.5	Series resistance at the gate terminal
$\lambda_{Saber}(V^{-1})$	0.039	Channel-length modulation parameter

supplies. An optimizer is also provided to help matching the model dc characteristics with experimental data. Since a Level 1 MOSFET model is good enough for this study, the Saber Power MOSFET Tool is used more as a comparison and verification to the subcircuit method of modeling developed in this work. The interface of the Power MOSFET Tool is displayed in Fig. 5.

The Power MOSFET Tool uses all the static characteristics measured in the previous section as input. The program starts with one biasing condition, shown in Table II, for optimization to generate parameters (rds0, rg, rd, rs, λ) for *I–V* characteristics. Fig. 6(a) and (b) show the measured and the modeled results of the output and transfer *I–V* characteristics.

TABLE III
CAPACITANCES AT SPECIFIC BIASING CONDITIONS AND THE PROFILE FACTOR USED IN SABER TOOL

Parameter	Value	Description
crss0(pF)	420	maximum crss value
crss1(pF)	110	crss value for reference voltage v1
crss2(pF)	20	crss value for reference voltage v2
coss0(pF)	900	maximum coss value
coss1(pF)	180	coss value for reference voltage v1
coss2(pF)	44	coss value for reference voltage v2
ciss0(pF)	800	maximum ciss value
v1(V)	9	first reference voltage
v2(V)	800	second reference voltage (v2>v1)
profile	0.46	doping profile parameter (typical values range between 0.3 and 0.6).

In the models produced by the Saber Tool, $C_{\mathrm{gd,Saber}}$ and $C_{\mathrm{ds,Saber}}$ are nonlinear, whereas $C_{\mathrm{gs,Saber}}$ is assumed to be a constant, which is commonly verified by measured data. Table III shows the list of capacitance model parameters measured from *C–V* characteristics of the SiC MOSFET at three specific biasing conditions (0, 9, 800 V) and the fitted profile factor (relevant to the doping density) that are used for modeling the capacitances at other biasing conditions. The measured and modeled C–V_{ds} characteristics of the SiC MOSFET are shown in Fig. 6(c). The body diode is modeled with the Diode Characterization Tool in Saber. Fig. 6(d) shows the modeled and measured body diode *I–V* forward characteristics.

C. RoHM Manufacturer's Model for Validation

The manufacturer (RoHM) of the SiC MOSFET chip we used provides a model publicly available on their website. We implemented that model on LTspice platform to simulate the dc characteristics of the SiC MOSFET and body diode. The results are shown in Fig. 6 for comparison.

IV. DYNAMIC CHARACTERIZATIONS OF SiC MOSFET

A. SiC Power MOSFET Switching Characteristics

SiC power MOSFETs are usually used as switches in high-power circuits due to their high breakdown voltage and fast switching capability [20], [21]. Their switching behavior is mainly affected by the three capacitances between the three device terminals, namely gate–drain capacitance, gate–source capacitance, drain–source capacitance, due to the charge and discharge phenomenon during the device turn-ON and turn-OFF process.

To have a better understanding of the power MOSFET switching behavior, a brief introduction of the power MOSFET turn-ON and turn-OFF transient [Fig. 7(a) and (b)], and a basic inductive load switching behavior test circuit is shown in Fig. 8 [22], [23].

1) Turn-ON Transient: The turn-ON transient process is illustrated in Fig. 7(a). The process starts from a turn-OFF state. When the gate bias V_{gs} increases, it begins to charge the capacitors of the SiC MOSFET.

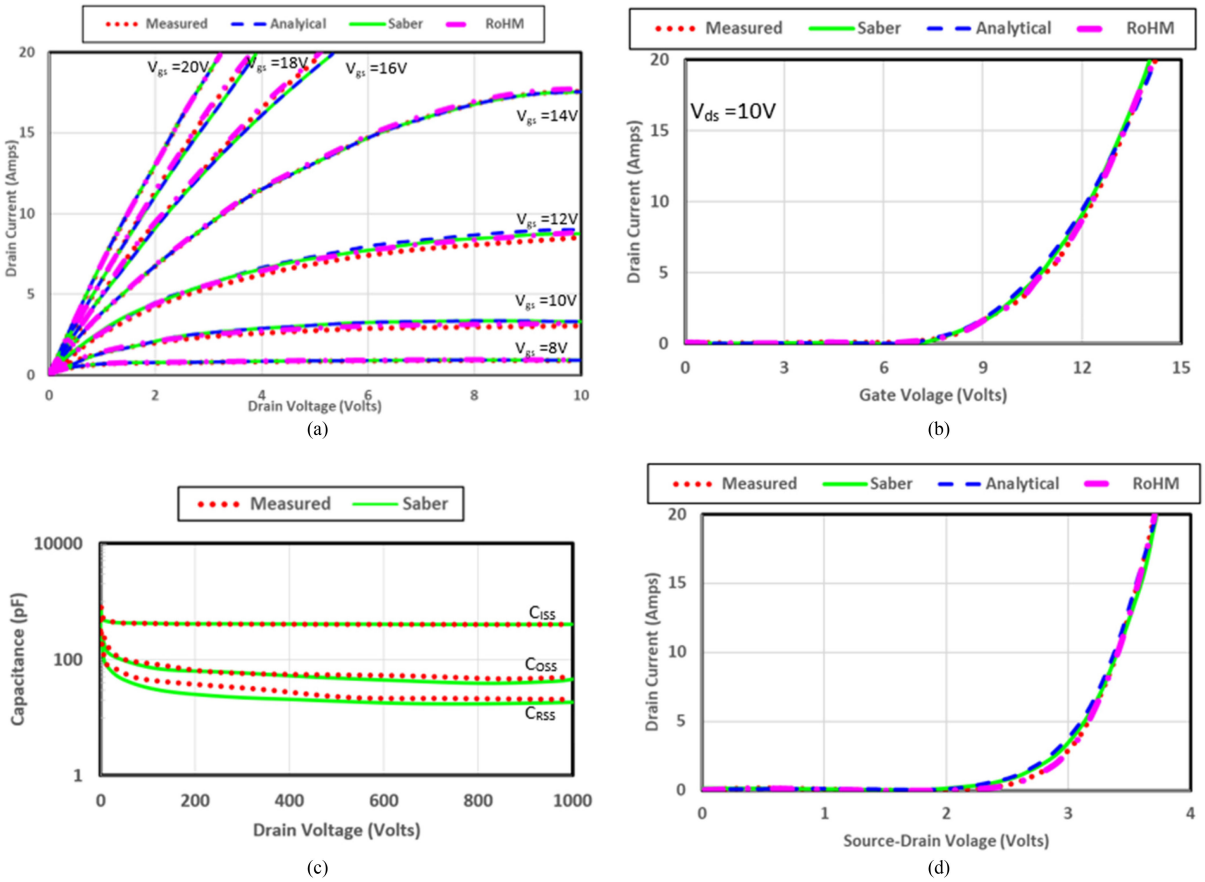

Fig. 6. Comparisons between the measured (red dots), analytical model (A) (blue dash), Saber Power MOSFET Tool (S) (green solid), and RoHM manufacturer model (pink dash) simulated results of the electrical characteristics for the 1.2-kV SiC Power MOSFET. (a) Output characteristics. (b) Transfer characteristics. (c) Capacitance–$V_{\rm ds}$ characteristics. (d) Body diode.

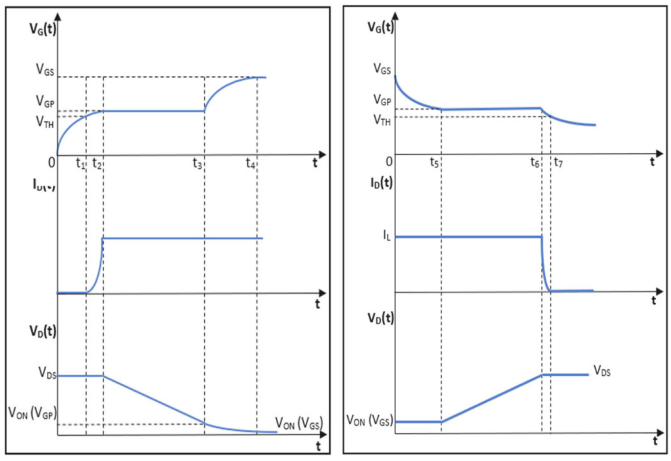

Fig. 7. Plots showing the behavior of gate voltage, drain current, and drain voltage during the (a) turn-ON transient process and (b) turn-OFF transient process.

Before the gate voltage exceeds ($V_{\rm gs}<V_{\rm th,MOS}$) the threshold voltage, no drain current flows through the SiC MOSFET device, which means $I_{\rm D}$ will remain zero and the device drain voltage $V_{\rm ds}$ also keep its initially value, which is equal to the drain bias voltage $V_{\rm ds}$. Since the gate drain capacitance $C_{\rm gd}$ varies with the applied drain voltage in accordance with the thickness of depleted region, it remains constant at this situation due to the constant $V_{\rm ds}$. When the gate bias is higher than the threshold voltage, drain current starts to flow through the SiC MOSFET device and the current increases. During this time, the drain voltage remains constant since the freewheeling diode cannot be used to provide any voltage until all the load current is transferred to the SiC MOSFET device. As a result, the gate drain capacitance $C_{\rm gd}$ still remains constant. The drain current keeps increasing until it reaches the same value as the load current $I_{\rm L}$. At time t_2, the entire load current $I_{\rm L}$ has transferred from the diode to the SiC MOSFET and the diode begin to support voltage, which means the drain voltage $V_{\rm ds}$ will begin to reduce until it reaches the ON-state voltage $V_{\rm on}$. During this time period, the gate voltage keeps increasing until it reaches the gate bias voltage. As the gate bias increases, at the same drain current level, the on-state resistance will be reduced that results in a small reduction of the drain voltage during this period.

2) Turn-OFF Transient: The turn-OFF transient process is illustrated in Fig. 7(b). As the gate bias decreases, neither drain voltage nor drain current will change until the gate voltage reaches the plateau voltage $V_{\rm gp}$, which is the voltage allows the SiC MOSFET to operate at its saturation current level equal to the load current level. During t_5–t_6 time period, the drain voltage begins to increase while the drain current remains constant because the current is not able to be transferred to the freewheeling diode until the drain voltage $V_{\rm ds}$ exceeds the drain bias and makes the

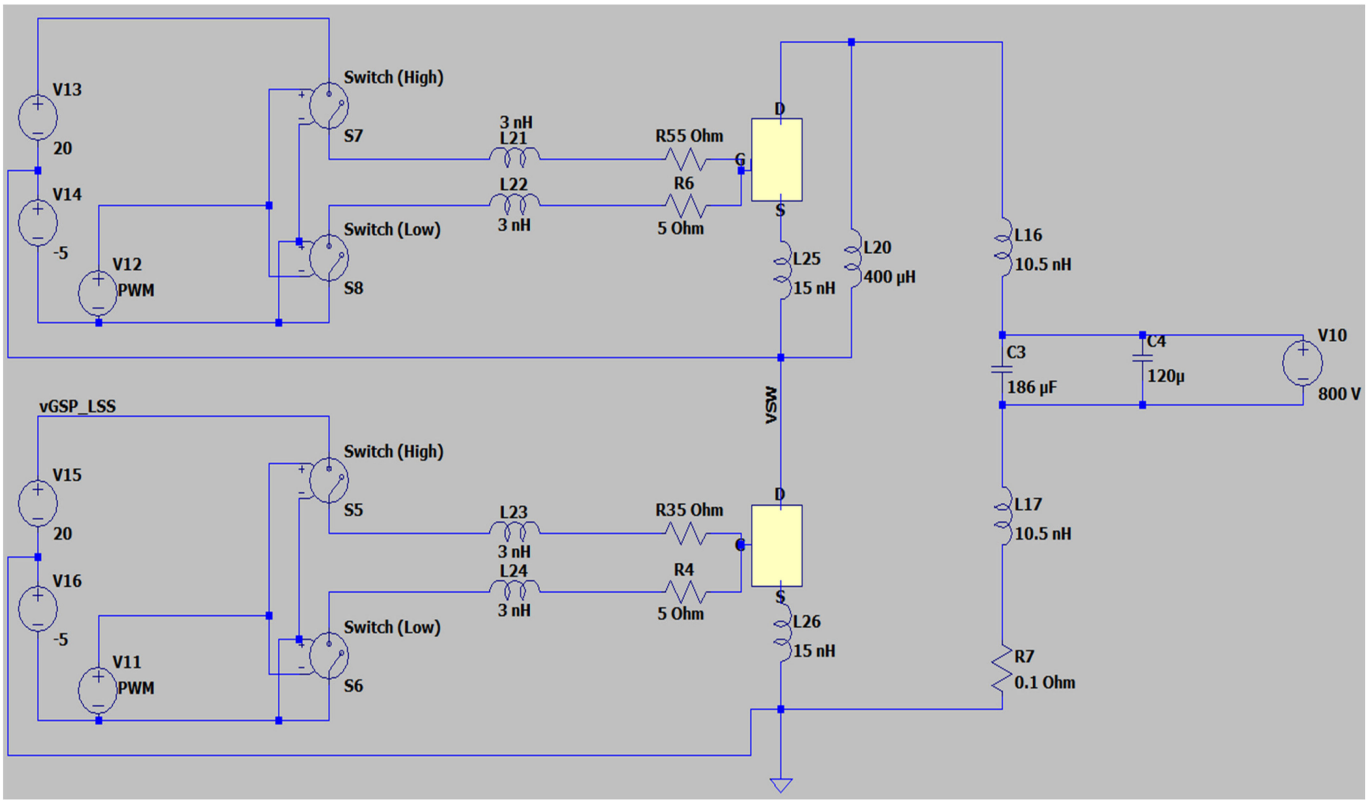

Fig. 8. Schematic circuit diagram of a clamped inductive load test circuit with an equivalent circuit for the power MOSFET used to measure/simulate the switching characteristics of the 1.2 kV SiC power MOSFET.

diode working at the forward bias condition. During this time period, the load current begins to transfer from the SiC MOSFET to the freewheeling diode, resulting in a current drop for the device. The current flowing through the gate resistance discharges both the gate-to-drain and gate-to-source capacitance, leading to a quick fall in the gate voltage. At time t_6, the gate voltage drops to the threshold and beyond that point, the drain current turns to zero and the drain voltage equals to the drain bias voltage.

B. Double Pulse Tester for Dynamic Switching Performance Characterization

To evaluate the dynamic characteristics of a SiC MOSFET, a classical double pulse tester (DPT) is built to obtain the switching waveforms and data [11]. In this article, an inductor is used for double pulse tests since the system load is inductive for a majority part of power electronics and power systems applications. The basic operation principle of the DPT is similar to that of the inductive load test circuit discussed in the previous section.

For dynamic tests, two pulses are applied to the gate of the SiC MOSFET with very low frequency, which is usually below 10 Hz to help the device under test avoid deviation caused by self-heating. During the first pulse period, appropriate dc bias and pulse width are chosen to charge the inductor to a certain load current. The second pulse is utilized for the turn ON characterization of the SiC MOSFET.

In this article, the switching characterizations was performed under two conditions: 800 V drain bias, 17 A, and 5.5 A inductive load, −5 V/20 V gate voltage with turn-ON and turn-OFF gate resistance values of 5 Ω each. Different turn-ON current values were achieved using different turn-ON times of the gate driver.

Although, the double pulse test provides a good solution for evaluating switching dynamic characteristics, there is still accuracy problem related to it.

1) For the circuit main loop, because of the high dv/dt and di/dt, the current overshoot can be high during the turn-ON process. As a result, the energy stored in the stray inductance can have oscillation with the output capacitor of MOSFET.
2) For the gate charge loop, the stray inductance can also slow down the charging time or even cause mistrigger of the MOSFET if it causes too large oscillation on gate charge signal.
3) For the measurement side, the parasitic capacitance and the stray inductance in the current shunt will affect the accuracy of measurement on $V_{\rm ds}$ and $I_{\rm d}$. This is because under high frequency resonance in the circuit, even very little change of parasitic parameters can induce relatively high impedance, which can affect the accuracy.

In this design, both the gate charge loop and the main power loop lengths have been minimized for stray inductance reduction to minimize the switching overshoot and oscillation. Also, to guarantee the measurement accuracy, the current was measured across the shunt to achieve a better switching current waveform. A Tektronix TPP0850 voltage probe with a small parasitic capacitance and 800 MHz bandwidth was used for voltage measurement. In this case, the hardware can output optimized switching characteristics and the measurement error can be reduced to an acceptable range.

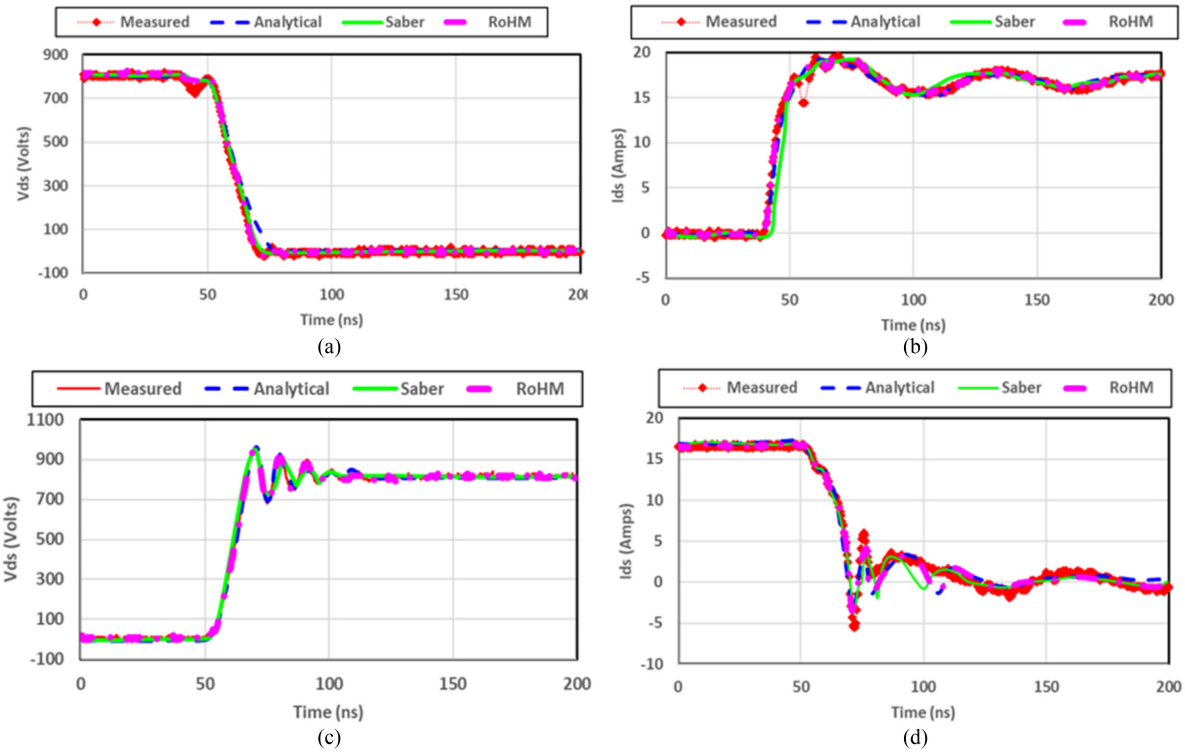

Fig. 9. Comparing the measured (red dots), analytical model (A) (blue dash), Saber Power MOSFET Tool (S) (green solid), and RoHM manufacturer model (pink dash) for the 1.2-kV SiC power MOSFET at $R_g = 5\ \Omega$ with turn-ON process in (a) and (b), and turn-OFF process in (c) and (d).

V. Dynamic Switching Simulation of SiC MOSFET

To verify the analytical subcircuit model, the same DPT circuit was used to simulate the switching behavior in LTspice platform in comparison with the cases of RoHM manufacturer model on LTspice platform and Saber MOSFET model on Saber Synopsys platform [24], [25]. In the simulations, the gate drive circuit was replaced by an ideal voltage source to generate the two pulses. All three models were plugged individually into simulator platforms to simulate the switching behavior while keeping all other conditions constant. The switching behavior measured using the DPT board and simulated using the three models are compared in Fig. 9 at 800 V, 17 A, and in Fig. 10 at 800 V, 5.5 A. We have verified that our model accurately simulated measurement waveforms in the operating ranges of $V_{\rm ds} = 400$ to 800 V, $I_{\rm d} = 5.5$ to 17 A, and Rg $= 5$ to 20 Ω. Since this is Level 1 modeling, the switching characteristics simulated using the Saber Power MOSFET model on Saber simulator platform and the RoHM model on LTspice simulator platform are used as validations for the analytical-based subcircuit model.

As seen in Figs. 9 and 10, the overall turn-ON and turn-OFF behavior for the simulations based on all three models and the measured results are in great agreements. Compared to the simulation data the measured switching behavior has a little mismatch during the oscillations also known as ringing. This is prominent for the Saber model during the turn-OFF current measurement. The high voltage switching in SiC MOSFET can lead to a higher voltage and current derivative, which is a big cause of the overshoot voltage and current. The parasitic in the closed loop circuit is a major reason why the high switching transient leads to overshoots and long-lasting ringing during the turn-ON process. Stray inductance also leads to electromagnetic interference in the circuit due to inductive coupling [26], [27].

Lastly, if the current is not shared equally between the parallel capacitors, due to the mismatch between internal parasitic, then oscillations are likely to occur between the capacitors [28]. Some of this noise can be reduced by using additional decoupling capacitors across the voltage inputs in the circuit. Parasitic extraction has been an issue in models for a long time. The accuracy of the extracted parasitic values depends highly on the model being used. The Saber MOSFET Tool that is preferred only for Level 1 modeling is used mostly for quick simulation studies just to compare the turn-ON and turn-OFF times. Overall the agreements of switching behavior between the three simulations and the measured results are considered excellent, with slightly better performance from the analytical subcircuit model and RoHM model. While the analytical subcircuit model performed equally well with the RoHM model regarding the degree of agreement with measurements, we also compared the computation time by implementing the two models into LTspice platform. The result shows that the computation time of the analytical subcircuit model is about 4.5 times faster than the RoHM model when simulated on the same simulator. Since both models are behavior based models that are generally faster than physics based models, therefore it is safe to say that the proposed subcircuit should also have a smaller computation time than physics-based models. Considering the better accuracy compared to the Saber MOSFET Tool and the shorter computation time than the RoHM and physics-based models, this analytical subcircuit model is more suitable for in-loop hardware simulations and power electronics circuit design.

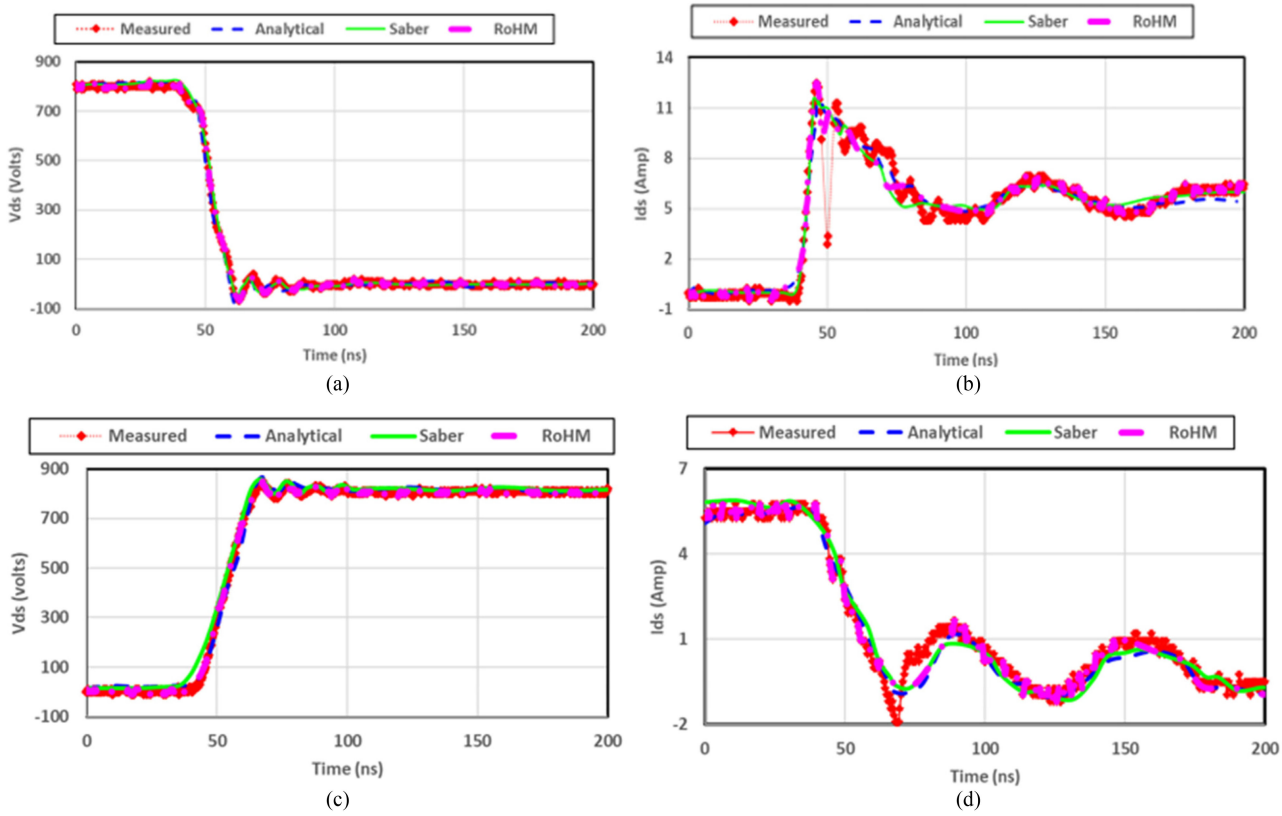

Fig. 10. Comparing the measured (red dots), analytical model (A) (blue dash), Saber Power MOSFET Tool (S) (green solid), and RoHM manufacturer model (pink dash) for the 1.2 kV SiC power MOSFET at $R_g = 5\ \Omega$ with turn-ON process in (a) and (b) and turn-OFF process in (c) and (d).

VI. Conclusion

In summary, we presented an analytical subcircuit model for SiC MOSFETs that was suitable for system-level simulations. Using a RoHM SiC MOSFET as a testbed, this subcircuit model was implemented in the Saber and LTspice programs for validation in comparison with experimental measurement results and simulation results from Saber Power MOSFET and RoHM models. The output *I–V* characteristics from the model have good agreement to the experimental results. Dynamic characterization was performed using a double-pulse tester at 800 V/17 A and 800 V/5.5 A. The simulated results from the subcircuit model have good agreement with the experimental results from the double pulse test on dynamic switching behaviors and performed slightly better than the Saber MOSFET Tool. On the same LTspice platform, the computation of the analytical subcircuit model is about 4.5 times faster than that of RoHM model. This fast but accurate subcircuit model for SiC MOSFETs can be used for real time hardware in loop simulations and power converter designs. The model can be run in other commercial simulator tools such as Pspice, Topspice, Psim, etc., besides Saber and LTspice. This analytical model solves some of the challenges faced by other models by reducing the amount of input parameters. This method can also be used to generate other generation models or advanced level models. This work presented a method to study the fast-switching-speed behavior of SiC power MOSFETs using a more accurate and nontime consuming analytical based subcircuit model that does not require any physical or geometrical parameters from the device.

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