Dual-Mode Modulation Scheme With Seamless Transition for a Tunable Immittance-Based DAB Converter Featuring High-Efficiency Performance Over Whole Output Power Range

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***Abstract*—Switching loss and conduction loss are two main loss mechanisms in dual-active-bridge (DAB) converter and the degree to which they affect the efficiency of DAB converter depends on the chosen power modulation scheme. In general, no single modulation scheme will perform optimally under all operating conditions. In this article, a hybrid modulation scheme and a new DAB converter topology designed for its realization are presented. The DAB converter is designed to switch between two operation modes—dynamic frequency matching (DFM) for medium- to full-load condition and enhanced dual-phase-shift (EDPS) modulation for light-load condition. Under DFM modulation, a switch-controlled capacitor is used to tune the resonant frequency of an LCL immittance network such that minimum rms current is guaranteed by unity-power-factor operation under different load conditions, leading to zero backflow power, zero circulating current, and zero-voltage switching (ZVS) operation of all switches. Under EDPS modulation, zero backflow power, and ZVS operation of all switches are achieved. These advantageous features are critical to ensuring a high-efficiency operation of DAB converter. The proposed solution is experimentally verified using a 1.5-kW hardware prototype with efficiency exceeding 96% for all output power levels.**

***Index Terms*—Bidirectional converter, dual-active-bridge (DAB) converter, immittance network, resonant converter, soft-switching.**

I. Introduction

ACCORDING to the Renewable Capacity Statistics 2019 released by the International Renewable Energy Agency, the total installed renewable generation capacity has increased to approximately one third of the global installed electricity capacity at the end of 2018 [1]. Renewable energy resources, such as solar and wind energy, are highly dynamic and intermittent in nature leading to imbalance between instantaneous energy generation and consumption. As a promising solution to this problem, energy storage systems, such as batteries and supercapacitors, are utilized as energy buffers which help to smooth out the power fluctuations caused by these dynamic energy sources [2]. The interfacing of these energy storage systems to the grid requires the use of bidirectional converters for charging and discharging the energy storage devices.

Dual-active-bridge (DAB) converter, which was first introduced in [3] and [4], is one of the most widely studied and applied bidirectional power converter topologies, consisting of two full-bridges interfaced by a series inductor and a high-frequency isolation transformer. Besides energy storage systems, DAB converter is also frequently employed in many emerging applications, such as vehicle-to-grid systems [5] and solid state transformers [6]. The attractiveness of DAB converter stems from its advantages of high power density, galvanic isolation, soft-switching capability, and flexibility in realizing various power modulation schemes [7]. In conventional DAB converter, the basic mechanism for power control is by generating two phase shifted high-frequency ac voltages (square-wave or quasi-square-wave) using H-bridges, and by applying them to the two ends of an energy-transfer inductor so that energy flows from the leading ac voltage to the lagging ac voltage.

The simplest method to modulate the output power of DAB converter is to apply a phase shift between two square-wave ac voltages, i.e., single-phase-shift (SPS) modulation [8]. However, DAB converter operating with SPS modulation is known to suffer from significant circulating current and backflow power, and narrow zero-voltage switching (ZVS) range since the inductor current's waveform is highly sensitive to the input-to-output voltage ratio and load condition. To reduce circulating current and backflow power and to extend ZVS range, various modulation methods have been proposed. In general, by introducing an internal phase shift between the two legs of the same H-bridge, a three-level ac voltage with adjustable duty ratio can be produced. Hence, there are in total four degrees of freedom (DoF) in the control of the output power of DAB converter, i.e., internal phase shift of the primary bridge (α_p), internal phase shift of the secondary bridge (α_s), external phase shift between two ac voltages (θ), and switching frequency (f_s). By combining some or all of these control parameters, the modulation methods for

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DAB converter can be broadly classified into the following five categories.

1) SPS modulation: Both internal phase shifts α_p and α_s are kept constant at 180° and only external phase shift θ is utilized for power control, hence SPS is a 1-DoF modulation.
2) Extended-phase-shift (EPS) modulation: One of the two internal phase shifts (α_p or α_s) is varied while the other is kept constant at 180°, and both internal phase shift (α_p or α_s) and external phase shift θ are utilized for power control, hence EPS is a 2-DoF modulation [9]–[11].
3) Dual-phase-shift (DPS) modulation: Both internal phase shifts ($\alpha_p = \alpha_s$) are varied simultaneously, and both internal phase shift ($\alpha_p = \alpha_s$) and external phase shift θ are utilized for power control, hence DPS is a 2-DoF modulation [12]–[14].
4) Triple-phase-shift (TPS) modulation: All phase-shift parameters ($\theta, \alpha_p, \alpha_s$) are varied independently, hence TPS is a 3-DoF modulation and SPS/EPS/DPS can be considered as special cases of TPS [15], [16].
5) (N + 1)-DoF modulation is obtained when the above N-DoF modulation schemes are combined with switching frequency modulation, providing an additional DoF in power control [17].

Stemming from its general form, many works have been done to optimize TPS modulation scheme to meet different performance objectives [18], such as maximizing fundamental power factor [19], minimizing the fundamental component of inductor current [20], minimizing reactive power [21], minimizing current stress (peak inductor current) [22]–[24], minimizing rms current [25]. The computational efforts involved in these optimization procedures, however, are often extensive, hence complexity is one major concern in association with the implementation of TPS modulation scheme. For some of the proposed modulation schemes, switching frequency modulation is utilized to provide an additional DoF for power control when the values of θ, α_p, and α_s are restricted by some optimization constraints [26]–[27]. Regardless of the modulation scheme used, one common drawback associated with the conventional DAB converter is the dependence of soft-switching condition on the input-to-output voltage ratio. This implies that the desired optimum operating parameters must be precalculated for each input-to-output voltage ratio, which greatly increases the complexity of its application.

In view of the limitations of the abovementioned modulation schemes, some works focused on improving the performance of DAB converter by means of modified topologies. For example, a front and rear end switch DAB converter, which has two additional switches connected in series with the input and output terminals of the converter, was proposed to eliminate the backflow power at both ends of the converter [28]. This, however, limits the maximum power transferred by the DAB converter. In [29]–[31], neutral-point-clamped (NPC) multilevel bridges are utilized in place of H-bridges to offer advantages, such as lower device stress, lower voltage and current harmonics, improved fault tolerance, and additional DoF for power control. Besides using NPC bridges, other multilevel topologies have also been proposed. For example, in [32], a hybrid-bridge-based DAB converter was proposed where the hybrid bridge can be configured as H-bridge or half-bridge by controlling two auxiliary switches to generate a four-level ac voltage to achieve ZVS operation over a wide range of input-to-output voltage ratio. In [33], a dual-transformer topology was proposed to generate a four-level ac voltage without using auxiliary switches, hence control is simplified. Other methods to improve ZVS range include series voltage injection (in series with energy-transfer inductor) [34] and the use of an auxiliary switch-controlled inductor connected between the two legs of the low-voltage-side (LVS) H-bridge for modifying the current values at the switching instances of the LVS switches for achieving ZVS [35]. Both methods, however, require additional power and control circuitries which increase the complexity of DAB converter.

Besides the series-inductor-based DAB converter described above, a growing number of works were reported on resonant DAB converters utilizing second- or higher-order resonant tanks [36]–[38]. The different structures and characteristics of various resonant tank designs provide another DoF for realizing various desirable features, such as dc blocking, extended ZVS range, reduced rms tank current, and reduction or even total elimination of backflow power in DAB converter. Recently, resonant DAB converters utilizing immittance network have attracted a significant level of attention. Several works were reported on DAB immittance converters characterized by minimum tank current and conduction loss since unity-power-factor operation are achieved at both ports of the immittance network, leading to minimization of circulating current and elimination of backflow power [39]–[42]. However, the fundamental limitation of these works is that ZVS cannot be achieved for all switches. For example, for the works reported in [41] and [42], only 50% of the switches are soft-switched.

Recently, DAB converters utilizing tuned $CLLC$ and LCL immittance networks have been proposed where the internal phase shifts of the H-bridges are modulated in synchronism with the external phase shift between two ac voltages, i.e., enhanced dual-phase-shift (EDPS) modulation [43], [44]. While ZVS range is extended with the proposed modulation scheme, the resulting DAB converter suffers from severe circulating current under light-load condition. To ensure high-efficiency operation over a wide load range, a reconfigurable modulation scheme was proposed in [45]. In this article, it was demonstrated that a fifth-order DAB immittance converter should switch between different operation modes in order to achieve high-efficiency operation under wide-range variations in output power and input-to-output voltage ratio. However, the switching boundaries between different operation modes are predicted using a loss model, which is time consuming to develop and the predicted boundaries may not fully match with the actual cases in the presence of parasitic parameter variations or component tolerances. Moreover, the results obtained were specific to the fifth-order DAB immittance converter considered in [45]. In [46], a DAB converter combining the immittance network and multilevel bridges was proposed to utilize multilevel modulation schemes for shaping the efficiency profile of the converter. With achieving full-range ZVS and wide-range zero circulating

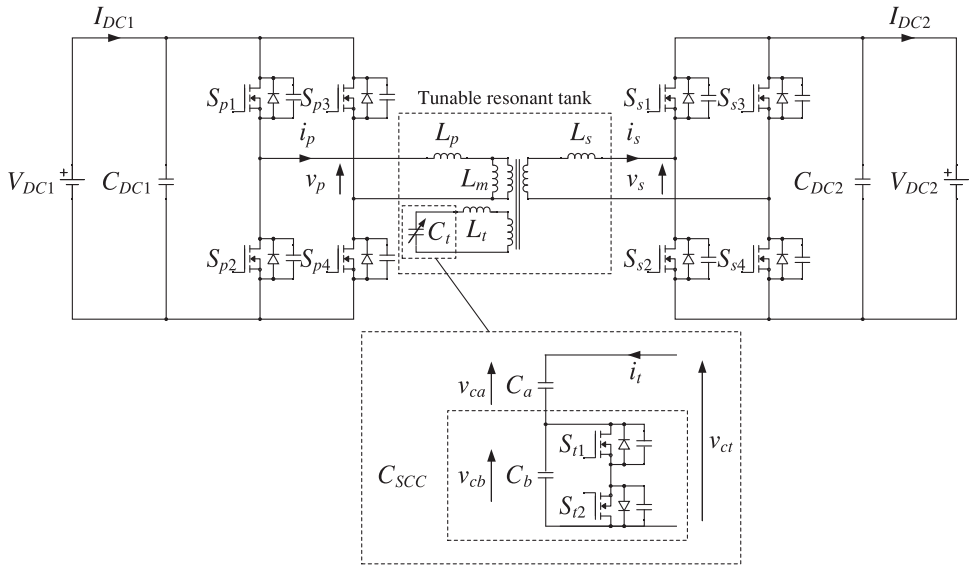

Fig. 1. Proposed DAB dc–dc converter with tunable resonant network.

current, the converter's efficiency becomes insensitive to the output power and voltage levels.

In this article, a simple modulation scheme is presented for a new reconfigurable DAB immittance converter based on tunable LCL immittance network. With the proposed modulation scheme, the DAB converter is switched between two operation modes for achieving high efficiency over a wide load range. For medium- to heavy-load conditions, the DAB converter achieves zero backflow power, zero circulating current, and full ZVS operation by adopting switching frequency modulation. To maintain zero circulating current, the immittance condition is ensured by modulating the resonant frequency of the immittance network to follow the switching frequency by means of a switch-controlled capacitor (SCC), i.e., dynamic frequency matching (DFM). For light-load condition, the DAB converter switches to EDPS modulation to achieve full ZVS operation and reduced circulating current compared to [43]–[44]. An important advantage of the proposed DAB immittance converter is that, unlike single-inductor-based and other resonant DAB converters, the established ZVS conditions are independent of the input-to-output voltage ratio which greatly simplifies its ZVS design and implementation. The effectiveness of the proposed modulation scheme is verified by experimental result obtained from a 1.5-kW hardware prototype.

II. Converter Analysis

The schematic diagram of the proposed resonant DAB dc–dc converter is shown in Fig. 1. Four complementary switch-pairs S_{p1}/S_{p2}, S_{p3}/S_{p4}, S_{s1}/S_{s2}, and S_{s3}/S_{s4} form the primary-side and secondary-side H-bridges with the input and output filter capacitors $C_{\rm DC1}$ and $C_{\rm DC2}$, respectively. Two H-bridges are connected through a tunable T-type resonant network comprising a three-port high-frequency isolation transformer with magnetizing inductance L_M, primary-side inductance L_p, secondary-side inductance L_s, tertiary-side leakage inductance L_t, and a tunable capacitor C_t. The tunable capacitor C_t is realized by connecting a fixed auxiliary capacitor C_a in series with an SCC which is composed of two switches S_{t1} and S_{t1} in parallel with a base capacitor C_b. The voltages v_p and v_s are the high-frequency ac voltages generated by the primary-side and secondary-side H-bridges, respectively. The voltages v_{ct}, v_{ca}, and v_{cb} are the voltages across C_t, C_a, and C_b, respectively, and the currents i_p, i_s, and i_t are the currents flowing through L_p, L_s, and L_t, respectively.

With this topology, four switch-pairs are controlled to commutate complementarily at a variable switching frequency f_s with a fixed duty cycle of 0.5. By introducing an internal phase shift α_p between S_{p1}/S_{p2} and S_{p3}/S_{p4}, a high-frequency pulsewidth-modulated three-level ac voltage v_p ($+V_{\rm DC1}$, 0, $-V_{\rm DC1}$) with a variable duty ratio is generated at the primary-side H-bridge as α_p varies between 0 and π. Similarly, a second three-level ac voltage v_s ($+V_{\rm DC2}$, 0, $-V_{\rm DC2}$) is generated at the secondary-side H-bridge by introducing an internal phase shift α_s between S_{s1}/S_{s2} and S_{s3}/S_{s4}. For transferring power between $V_{\rm DC1}$ and $V_{\rm DC2}$, v_s is phase shifted from v_p by an external phase shift θ, where θ is defined to be positive when v_p leads v_s and power is transferred from $V_{\rm DC1}$ to $V_{\rm DC2}$, and *vice versa*. The three-level ac voltages v_p and v_s can be represented by their Fourier series

$$v_p = \frac{4V_{\rm DC1}}{\pi} \sum_{k=1,3,\ldots}^{\infty} \frac{1}{k} \sin(k\omega_s t) \sin\left(\frac{k\alpha_p}{2}\right) \tag{1}$$

$$v_s = \frac{4V_{\rm DC2}}{\pi} \sum_{k=1,3,\ldots}^{\infty} \frac{1}{k} \sin(k\omega_s t - k\theta) \sin\left(\frac{k\alpha_s}{2}\right) \tag{2}$$

where $\omega_s = 2\pi f_s$.

Assuming that higher order voltage and current harmonics are removed by the resonant network, fundamental component analysis is applied. The fundamental components of v_p, v_s, i_p, i_s, and i_t are represented in the phasor form by $\mathbf{U}_p$, $\mathbf{U}_s$, $\mathbf{I}_p$,

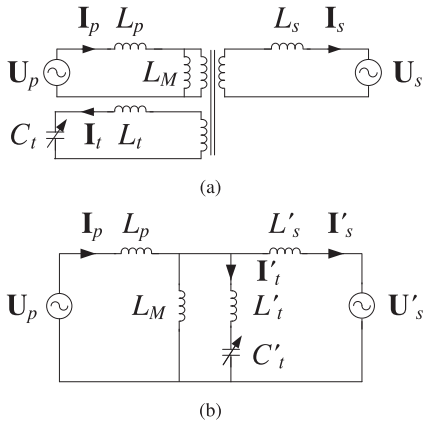

Fig. 2. (a) Equivalent circuit of the proposed resonant DAB converter. (b) Equivalent circuit referred to the primary side of the high-frequency transformer.

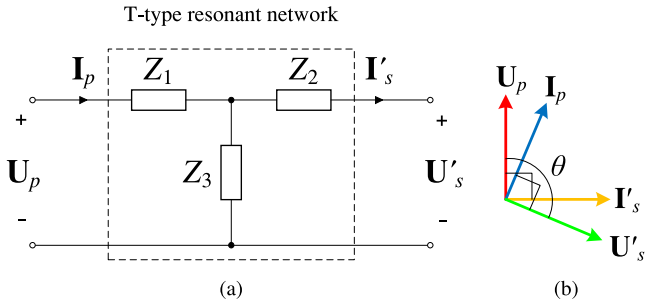

Fig. 3. (a) Two-port T-type resonant network. (b) Phasor relationships between port voltages and currents.

$\mathbf{I}_s$, and $\mathbf{I}_t$, respectively, with angular switching frequency ω_s. Hence, $\mathbf{U}_p$ and $\mathbf{U}_s$ can be written as

$$\mathbf{U}_p = U_p\angle 0 = \frac{4V_{\mathrm{DC1}}}{\pi\sqrt{2}}\sin\left(\frac{\alpha_p}{2}\right)\angle 0 \tag{3}$$

$$\mathbf{U}_s = U_s\angle -\theta = \frac{4V_{\mathrm{DC2}}}{\pi\sqrt{2}}\sin\left(\frac{\alpha_s}{2}\right)\angle -\theta. \tag{4}$$

Given that n_p, n_s, and n_t denote the number of turns in the primary, secondary, and tertiary windings, all secondary- and tertiary-side voltages, currents, and inductances/capacitances are referred to the primary side to form a transformer-less network for easier analysis. These primary-referenced variables are given by (5). Fig. 2(b) shows the resulting primary-referenced resonant network, which resembles a T-type resonant network with branch impedances Z_1, Z_2, and Z_3 shown in Fig. 3(a). By using these branch impedances, the admittance matrix Y of the T-type resonant network can be derived as

$$\begin{aligned}
\mathbf{U}'_s &= \frac{n_p}{n_s}\mathbf{U}_s \quad L'_s = \left(\frac{n_p}{n_s}\right)^2 L_s \quad C'_a = \left(\frac{n_t}{n_p}\right)^2 C_a \\
\mathbf{I}'_s &= \frac{n_s}{n_p}\mathbf{I}_s \quad\quad L'_t = \left(\frac{n_p}{n_t}\right)^2 L_t \quad C'_b = \left(\frac{n_t}{n_p}\right)^2 C_b \\
\mathbf{I}'_t &= \frac{n_t}{n_p}\mathbf{I}_t \quad\quad C'_t = \left(\frac{n_t}{n_p}\right)^2 C_t
\end{aligned} \tag{5}$$

$$\begin{bmatrix}\mathbf{I}_p \\ \mathbf{I}'_s\end{bmatrix} = Y\begin{bmatrix}\mathbf{U_p} \\ \mathbf{U}'_s\end{bmatrix} = \begin{bmatrix}y_{11} & y_{12} \\ y_{21} & y_{22}\end{bmatrix}\begin{bmatrix}\mathbf{U}_p \\ \mathbf{U}'_s\end{bmatrix} \tag{6}$$

where

$$Y = \begin{bmatrix}\frac{Z_2+Z_3}{Z_1Z_2+Z_1Z_3+Z_2Z_3} & -\frac{Z_3}{Z_1Z_2+Z_1Z_3+Z_2Z_3} \\ \frac{Z_3}{Z_1Z_2+Z_1Z_3+Z_2Z_3} & -\frac{Z_1+Z_3}{Z_1Z_2+Z_1Z_3+Z_2Z_3}\end{bmatrix}. \tag{7}$$

When the condition $Z_1 = Z_2 = -Z_3$ is fulfilled, leading to $y_{11} = y_{22} = 0$ and $y_{12} = -y_{21} = -1/Z_1$, the resonant network exhibits immittance characteristics and the port currents $\mathbf{I}_p$ and $\mathbf{I}'_s$ will become functions of the adjacent port voltages $\mathbf{U}'_s$ and $\mathbf{U}_p$, respectively. In other words, when the resonant frequency ω_r of the T-type resonant network, given by (9), is equal to the switching frequency ω_s, the voltage source at one port, e.g., $\mathbf{U}_p$, will be transformed into a current source at the adjacent port, e.g., $\mathbf{I}'_s$. By substituting Z_1, Z_2, and Z_3 from (8) into (7), the port currents $\mathbf{I}_p$ and $\mathbf{I}'_s$ can be derived as given in (10) and (11). The phasor relationships between $\mathbf{U}_p$, $\mathbf{U}'_s$, $\mathbf{I}_p$, and $\mathbf{I}'_s$ can be obtained from (3), (4), (10), (11) and shown in Fig. 3(b). Thus, under immittance conditions, there is a fixed phase difference of $\pi/2$ between $\mathbf{I}_p$ and $\mathbf{U}'_s$ and between $\mathbf{I}'_s$ and $\mathbf{U}_p$. From (12), it should be noted that the voltage across Z_3 is the summation of the port voltages $\mathbf{U}_p$ and $\mathbf{U}'_s$, which is the reason for using a tertiary winding to step down the voltage seen by L_t and C_t

$$\begin{aligned}
Z_1 &= j\omega_s L_p \\
Z_2 &= j\omega_s L'_s \\
Z_3 &= \frac{j\omega_s L_M\left(1-\omega_s^2 L'_t C'_t\right)}{1-\omega_s^2\left(L_M+L'_t\right)C'_t}
\end{aligned} \tag{8}$$

$$\omega_r = \sqrt{\frac{L_p+L_M}{C'_t\left(L_pL'_t+L_pL_M+L'_tL_M\right)}} \tag{9}$$

$$\mathbf{I}_p = -\frac{1}{Z_1}\mathbf{U}'_s = \frac{4V_{\mathrm{DC2}}}{\pi\omega_r L_p\sqrt{2}}\frac{n_p}{n_s}\sin\left(\frac{\alpha_s}{2}\right)\angle\frac{\pi}{2}-\theta \tag{10}$$

$$\mathbf{I}'_s = \frac{1}{Z_1}\mathbf{U}_p = \frac{4V_{\mathrm{DC1}}}{\pi\omega_r L_p\sqrt{2}}\sin\left(\frac{\alpha_p}{2}\right)\angle -\frac{\pi}{2} \tag{11}$$

$$\mathbf{U}_{Z_3} = \mathbf{U}_p - \mathbf{I}_pZ_1 = \mathbf{U}_p + \mathbf{U}'_s. \tag{12}$$

By taking the real part of the product of $\mathbf{U}_p$ and $\mathbf{I}_p^*$ (or $\mathbf{U}'_s$ and $\mathbf{I}'^*_s$), the active power P transferred from V_{DC1} to V_{DC2} can be derived as

$$P = \frac{8V_{\mathrm{DC1}}V_{\mathrm{DC2}}}{\pi^2\omega_r L_p}\frac{n_p}{n_s}\sin\left(\frac{\alpha_p}{2}\right)\sin\left(\frac{\alpha_s}{2}\right)\sin\theta. \tag{13}$$

III. Conventional Modulation Schemes and Their Problems

For the conventional resonant DAB converter with fixed immittance network, two modulation schemes have been proposed in the literature—namely, DPS modulation [41], [42] and EDPS modulation [43], [44]. Under DPS modulation, the output power of DAB immittance converter is regulated by varying α_p and α_s simultaneously such that $\alpha_p = \alpha_s = \alpha_{DPS}$ and $\theta = \pm\pi/2$ to achieve unity power factor at both ports. Under these conditions, $\mathbf{I}_p$ and $\mathbf{I}'_s$ are constantly in phase with $\mathbf{U}_p$ and $\mathbf{U}'_s$, respectively,

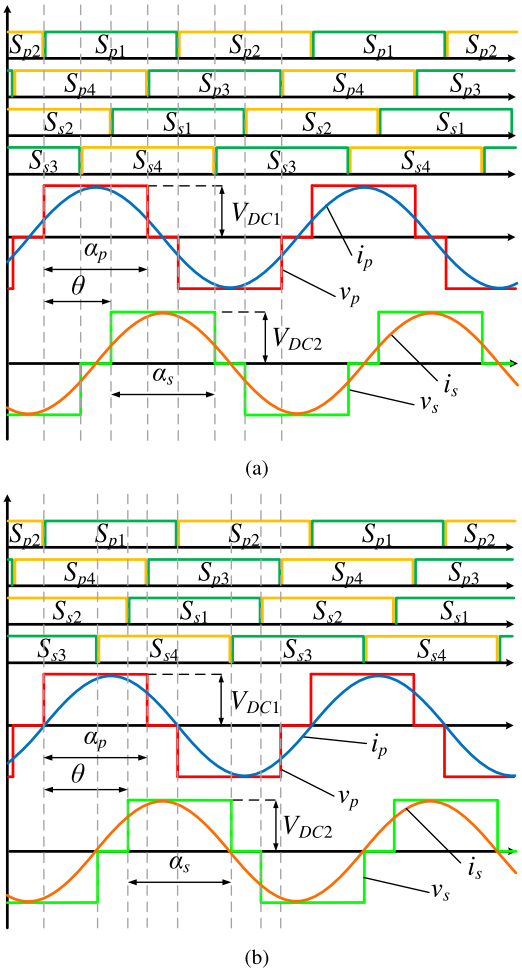

Fig. 4. Main operating waveforms of DAB immittance converter under (a) DPS modulation and (b) EDPS modulation.

as shown in Fig. 4(b), which leads to reduced rms port currents and conduction loss. The main drawback of DPS modulation, however, is that 50% of the switches suffer from hard-switching.

To mitigate the switching loss incurred by DPS modulation, EDPS modulation has been proposed recently to achieve full-range ZVS in all switches by modulating α_p, α_s, and ϕ simultaneously such that $\alpha_p = \alpha_s = \alpha_{EDPS}$ and $\theta = \pm(\pi - \alpha_{EDPS}/2)$. The main idea of EDPS modulation is to align the zero-crossings of i_p with the rising edges of v_p and the zero-crossings of i_s with the falling edges of v_s, as shown in Fig. 4(b). As a result, i_p constantly lags v_p while i_s constantly leads v_s by θ, which leads to increased circulating current and conduction loss, especially at light load.

Therefore, it is clear that wide-range high-efficiency operation cannot be achieved with these two conventional modulation schemes. In summary, DPS modulation leads to hard-switching of 50% of the switches and seriously limits the converter's switching frequency and hence its power density, while EDPS modulation incurs high circulating current and conduction loss at light load and degrades the converter's light-load efficiency. The main objective of this article is to devise a new modulation scheme to resolve these problems.

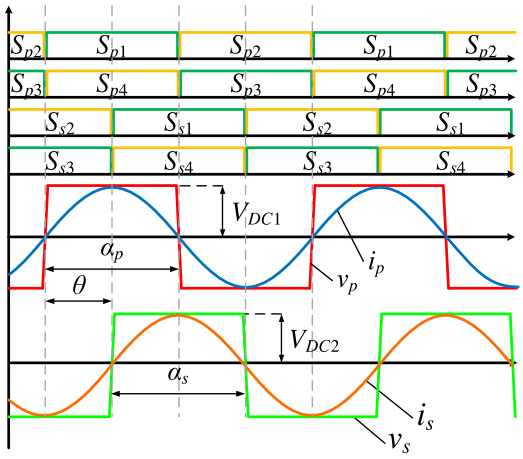

Fig. 5. Port voltage and current waveforms under DFM modulation for medium- and high-power operation.

IV. Proposed Modulation Scheme

In this section, a hybrid modulation scheme is proposed. The proposed converter will switch between two operation modes in two output power ranges. For medium- and high-power operation ($\geq$ 50% of rated load), DFM modulation is used to achieve zero backflow power, zero circulating current, and full ZVS operation. For light-load operation ($<$ 50% of rated load), EDPS modulation is used to achieve full ZVS operation with reduced circulating current compared to the case where EDPS modulation is utilized in the entire load range [43], [44].

A. Medium- and High-Power Operation

It can be inferred from (10) and (11) that when the resonant network is tuned, i.e., $\omega_s = \omega_r$, there exists a constant phase shift of $\pi/2$ between $\mathbf{U}_p$ and $\mathbf{I'}_s$ ($\mathbf{U}_p$ leads $\mathbf{I'}_s$) as well as between $\mathbf{U'}_s$ and $\mathbf{I}_p$ ($\mathbf{I}_p$ leads $\mathbf{U'}_s$). Thus, when $\alpha_p = \alpha_s$ are set to π and θ is set to $\pi/2$, the primary voltage $\mathbf{U}_p$ will be in phase with the primary current $\mathbf{I}_p$ and the secondary voltage $\mathbf{U'}_s$ will be in phase with the secondary current $\mathbf{I'}_s$. Under this condition, both $\mathbf{U}_p$ and $\mathbf{U'}_s$ are square-wave voltages that are in phase with their respective port currents, as shown in Fig. 5, and both backflow power and circulating current are fully eliminated. However, as all the frequently used modulation parameters (α_p, α_s, θ) must have specific values in order to achieve this condition, a new modulation parameter must be introduced for modulating the converter's output power.

By inspection of (13), one possible modulation parameter is the switching frequency ω_s, i.e., output power decreases with increasing switching frequency. However, when switching frequency varies while resonant frequency remains unchanged, the resonant network will no longer operate as an immittance network and zero backflow power and zero circulating conditions will be violated. To address this problem, we propose a DFM modulation scheme which will adjust the network's resonant frequency in synchronism with the switching frequency. In other words, the resonant network will always exist in a tuned state as switching frequency is increased/decreased to decrease/increase the converter's output power by ensuring that $\omega_r = \omega_s$.

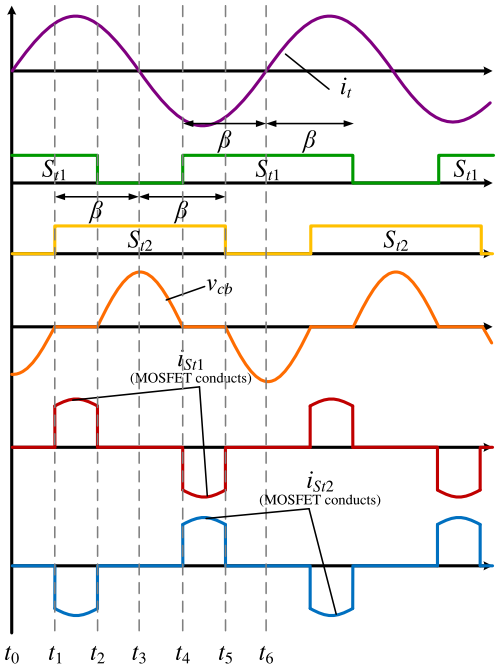

Fig. 6. Operating waveforms of switch-controlled capacitor C_{SCC}.

The DFM modulation scheme proposed in this article is based on the tuning of the resonant frequency ω_r of the T-type resonant network for matching with the varying switching frequency ω_s. In accordance with (9), ω_r can be tuned by varying the tertiary-side capacitor C'_t. As shown in Fig. 1, this is achieved by means of an SCC connected to the tertiary winding of the high-frequency isolation transformer. The SCC comprises a fixed capacitor C_a and an electronically tunable capacitor C_{SCC} consisting of a fixed capacitor C_b and two series-connected switches S_{t1} and S_{t2}. By appropriate switching of the MOSFETs S_{t1} and S_{t2} according to the pattern shown in Fig. 6, the voltage across capacitor C_b, and hence the effective capacitance C_{SCC}, can be adjusted by varying the width β of the gate drive signals. Considering only the fundamental component of v_{Cb} [50], the effective capacitance C_{SCC} can be derived as

$$C_{\text{SCC}}(\beta) = \frac{\pi C_b}{2\pi - 2\beta + \sin 2\beta} \tag{14}$$

and, hence, the effective tertiary-side capacitance C_t is given by

$$C_t(\beta) = \frac{C_a C_{\text{SCC}}}{C_a + C_{\text{SCC}}} = \frac{\pi C_a C_b}{\pi C_b + C_a(2\pi - 2\beta + \sin 2\beta)}. \tag{15}$$

For matching with switching frequency, the required value of C_t can be determined from (16), where C'_t is the primary-referenced value of C_t

$$C'_t = \frac{\pi C'_a C'_b}{\pi C'_b + C'_a(2\pi - 2\beta + \sin 2\beta)} = \frac{L_p + L_M}{\omega_s^2(L_p L'_t + L_p L_M + L'_t L_M)} \tag{16}$$

$$P = \frac{8 V_{\text{DC1}} V_{\text{DC2}}}{\pi^2 \omega_s L_p} \frac{n_p}{n_s}. \tag{17}$$

By setting $\alpha_p = \alpha_s = \pi$ and $\theta = \pi/2$, the converter's output power P in medium- and high-power operation is given by (17). The range of converter's output power that can be modulated in this way depends on the acceptable range of switching frequency variation, as P is inversely proportional to ω_s. For example, given that the switching frequency at the rated output power is $\omega_{\min}$, decreasing the converter's output power to 50% of the rated output power requires a switching frequency of $2\omega_{\min}$, and the switching frequency tends to infinity as the converter's output power decreases toward zero. Therefore, to exercise a reasonable controllability of the converter's output power at light load, a different modulation method should be used to avoid the use of extremely high switching frequency. The boundary between DFM modulation and the light-load modulation is taken as the output power level at which the maximum acceptable switching frequency $\omega_{\max} = K\omega_{\min}$ is reached. The maximum and minimum output power and the corresponding maximum and minimum value of the tunable capacitor under DFM modulation are, respectively, given by (18)–(21). Before discussing the light-load modulation, three modulation strategies for SCC are compared and their impacts on efficiency are discussed.

$$P_{\max} = \frac{8 V_{\text{DC1}} V_{\text{DC2}}}{\pi^2 \omega_{\min} L_p} \frac{n_p}{n_s} \tag{18}$$

$$P_{\min} = \frac{8 V_{\text{DC1}} V_{\text{DC2}}}{\pi^2 \omega_{\max} L_p} \frac{n_p}{n_s} = \frac{P_{\max}}{K} \tag{19}$$

$$C'_{t,\max} = \frac{C'_a C'_{\text{SCC,max}}}{C'_a + C'_{\text{SCC,max}}} = \frac{L_p + L_M}{\omega_{\min}^2(L_p L'_t + L_p L_M + L'_t L_M)} \tag{20}$$

$$C'_{t,\min} = \frac{C'_a C'_{\text{SCC,min}}}{C'_a + C'_{\text{SCC,min}}} = \frac{L_p + L_M}{\omega_{\max}^2(L_p L'_t + L_p L_M + L'_t L_M)} = \frac{C'_{t,\max}}{K^2} \tag{21}$$

B. Comparison of Modulation Strategies for SCC

In this section, two conventional modulation schemes for controlling SCC are reviewed and compared with the proposed modulation scheme as shown in Fig. 6 in order to highlight the benefit of the proposed scheme. Fig. 7(a) shows a non-complementary pulse width modulation (PWM) scheme used in [47]–[49], where the gate drive signals with a width of β (radian) are applied to S_{t1} and S_{t2} during the positive and negative half-cycle of the capacitor current i_t, respectively. It can be seen that with this modulation scheme, there exists a large dead time of $(\pi - \beta)$ during which both switches are turned OFF, giving rise to the noncomplementary nature of the gate drive signals.

Prior to $t = t_0$, S_{t2} is not conducting and its drain-source capacitance is charged to the same voltage as C_b, i.e., v_{cb}. At $t = t_0$, S_{t1} is turned ON at zero current and zero voltage, but it

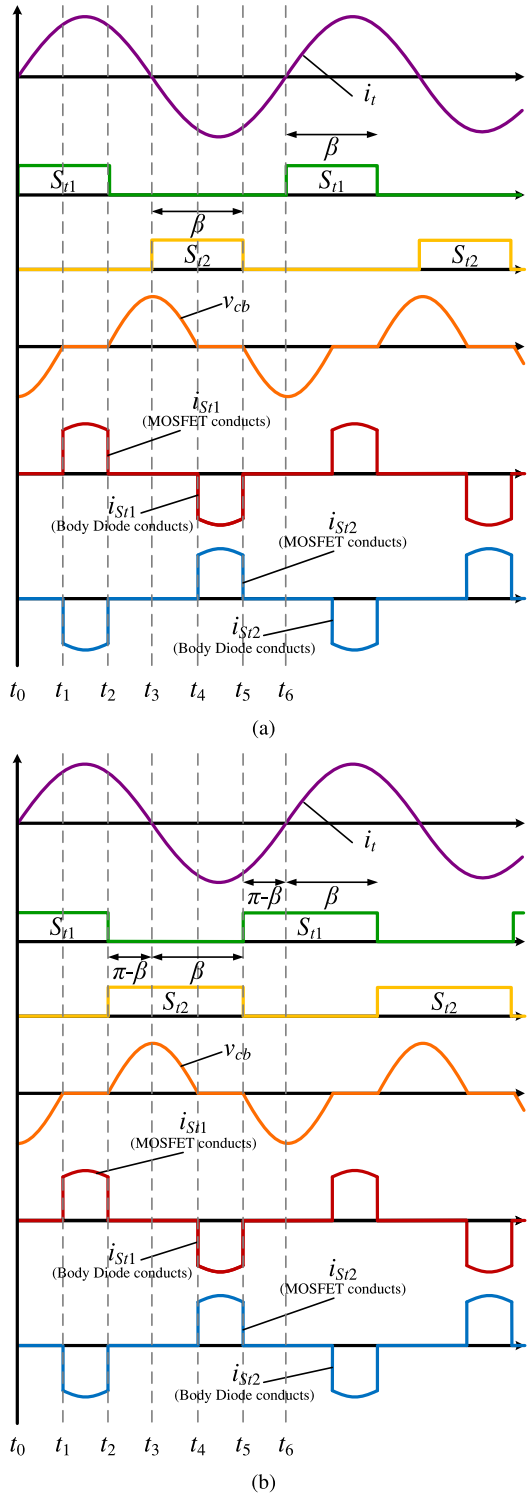

Fig. 7. (a) Noncomplementary PWM scheme. (b) Complementary PWM scheme.

will not conduct as S_{t2} is OFF and the negative v_{cb} keeps the body diode of S_{t2} in a reverse-blocking state. This forces i_t to flow through C_b, discharging it until v_{cb} reaches zero at $t = t_1$. During $t = t_1$–t_2, i_t flows through S_{t1} and the body diode of S_{t2} and maintains v_{cb} at zero level. At $t = t_2$, S_{t1} ceases to conduct (turned OFF at zero voltage) and i_t charges both C_b and the drain-source capacitance of S_{t1} in parallel. The charging process ends when i_t crosses zero at $t = t_3$.

Although S_{t2} is turned ON at the same time (at zero current and zero voltage), the positive v_{cb} keeps the body diode of S_{t1} in a reverse-blocking state, hence i_t is forced to flow through C_b, discharging it until v_{cb} reaches zero at $t = t_4$. During $t = t_4$–t_5, i_t flows through S_{t2} and the body diode of S_{t1} and maintains v_{cb} at zero level. At $t = t_5$, S_{t2} is turned OFF at zero voltage, diverting i_t to C_b and charging it up so a negative v_{cb} is established across C_b. The charging process ends when i_t decreases to zero and v_{cb} reaches its negative maximum value at $t = t_6$. From the above description, it can be concluded that no switching loss is incurred to S_{t1} and S_{t2}. However, part of i_t flows through their body diodes and gives rise to conduction loss.

Fig. 7(b) shows an alternative configuration of the gate drive signals of S_{t1} and S_{t2} proposed in [50]. Compared to the noncomplementary PWM scheme described above, the width of the gate drive signals are extended to π so that the gate drive signals of S_{t1} and S_{t2} are complementary to each other. Since i_t only flows through C_b during the extended part of the gate drive signals, i.e., $(\pi - \beta)$, the modified PWM scheme neither alters the operation of SCC nor leads to any improvement in efficiency, as part of i_t still flows through the body diodes of S_{t1} and S_{t2} and gives rise to conduction loss. ZVS of the switches remain effective with the modified PWM scheme. Under the two conventional modulation schemes for SCC, the negative current flows through the body diodes of S_{t1} and S_{t2} when they are turned OFF. Hence, the total conduction loss incurred to SCC under the two conventional modulation schemes is given by

$$P_{\text{loss}} = 2(I^2_{St(\text{rms})} R_{DS(\text{on})} + V_f I_{St})$$

$$I_{St(\text{rms})} = \sqrt{\frac{1}{2\pi}\int_{\pi-\beta}^{\beta} i_t^2 \, d(\omega t)}$$

$$I_{St} = \frac{1}{2\pi}\int_{\pi-\beta}^{\beta} |i_t| \, d(\omega t) \tag{22}$$

where $I_{St,(\text{rms})}$ is the rms value of the part of i_{St1} or i_{St2} that flows through S_{t1} or S_{t2}, I_{St} is the average value of the part of i_{St1} or i_{St2} that flows through the body diode of S_{t1} or S_{t2}, $R_{DS(\text{on})}$ is the ON-state resistance of S_{t1} or S_{t2}, and V_f is the forward voltage of the body diode of S_{t1} or S_{t2}. Motivated by the desire to reduce conduction loss and improve the efficiency of SCC, a new modulation scheme is proposed in this article as shown in Fig. 6. With the proposed modulation scheme, the width of the gate drive signals of S_{t1} and S_{t2} are further extended to $2\beta(>\pi)$ so that they overlap with each other. It can be seen that in the overlapped area $(2\beta - \pi)$ both S_{t1} and S_{t2} are turned ON, hence i_t will flow through S_{t1} and S_{t2} instead of their body diodes during the operation of SCC. Hence, the total conduction loss incurred to SCC under the proposed modulation scheme is given by

$$P_{\text{loss}} = 4I^2_{St(\text{rms})} R_{DS(\text{on})}. \tag{23}$$

Since MOSFETs commonly have very low ON-state resistance (tens of $\text{m}\Omega$ or less), the voltage drop across the ON-state

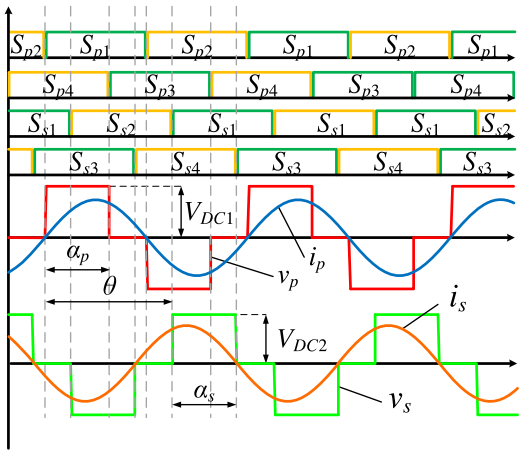

Fig. 8. Port voltage and current waveforms under EDPS modulation for light-load operation.

TABLE I
HARDWARE SPECIFICATIONS FOR CONVERTER PROTOTYPE

Parameter	Symbol	Design Value
Input voltage	V_{DC1}	400 V
Output voltage	V_{DC2}	400 V
Maximum output power	$P_{\max}$	1500 W
Switching frequency	f_s	40–80 kHz
Frequency gain	K	2
Control angle of SCC	β	90°–160°
Transformer's turns ratio	$n_p : n_s : n_t$	3:3:2
Primary-side inductance	L_p	344.0 μH
Secondary-side inductance	L_s	344.0 μH
Tertiary-side leakage inductance	L_t	5 μH
Magnetizing inductance	L_M	5 mH
Auxiliary capacitor	C_a	115.2 nF
Base capacitor	C_b	35.7 nF
Switches	S_{p1}-S_{p4}, S_{s1}-S_{s4}, S_{t1}-S_{t2}	UJC06505K

resistance of S_{t1} or S_{t2} is much lower than that across their body diodes. As a result, conduction loss is reduced and efficiency is improved. Furthermore, both switches are constantly turned ON/OFF at zero voltage, thus, switching loss can be minimized. Therefore, it can be concluded that the proposed modulation scheme leads to a more efficient operation of SCC which contributes to the overall high efficiency of the proposed tunable DAB immittance converter, as will be experimentally verified later.

C. Light-Load Operation

Under light-load condition, EDPS modulation method is selected to achieve full ZVS operation. The port voltage and current waveforms under EDPS modulation are shown in Fig. 8. The main feature of EDPS modulation is the alignment between the zero-crossings of i_p with the rising edges of v_p, and the zero-crossings of i_s with the falling edges of v_s, which leads to ZVS operation of all switches. With EDPS modulation, the converter's output power is varied by the simultaneous variations of $\alpha_p = \alpha_s = \alpha$ and $\theta = \pm(\pi - \alpha/2)$ [44]. The maximum output power is transferred when $\alpha = \pi$ and $\theta = \pm\pi/2$, and the minimum (zero) output power occurs when $\alpha = 0$ and $\theta = \pi$. With the proposed hybrid modulation scheme, the converter switches from DFM modulation to EDPS modulation at $\omega_{\max}$ and the switching frequency is kept constant $\omega_{\max}$ under EDPS modulation. Hence, the converter's output power is given by

$$P = \frac{8V_{\rm DC1}V_{\rm DC2}}{\pi^2\omega_{\max}L_p}\frac{n_p}{n_s}\sin^3\left(\frac{\alpha}{2}\right) = \frac{P_{\max}}{K}\sin^3\left(\frac{\alpha}{2}\right). \quad (24)$$

It should be noted that as there exists a nonzero phase shift between the voltage and current at each port under EDPS modulation, circulating current is incurred by this modulation method (although backflow power remains zero), and the amount of circulating current increases as output power decreases, mainly due to the shrinking pulsewidth α of the port voltages and the increased phase shift between the voltage and current at each port. Hence, if EDPS modulation is used alone over the entire output power range with the switching frequency fixed at $\omega_{\min}$, the amount of circulating current will increase rapidly as output power decreases from 100% to 0% of the rated output power, leading to rapid decrease of converter's efficiency at light load. This can be verified by (25), where $\omega_{\rm L}$ and $\omega_{\rm H}$ are two switching frequencies where $\omega_{\rm L} < \omega_{\rm H}$ and $\alpha_{\rm L}$ and $\alpha_{\rm H}$ are the corresponding internal phase shifts

$$\frac{1}{\omega_H}\sin^3\left(\frac{\alpha_H}{2}\right) = \frac{1}{\omega_L}\sin^3\left(\frac{\alpha_L}{2}\right). \quad (25)$$

It can be deduced from (25) that for equal output power, we have $\alpha_{\rm L} < \alpha_{\rm H}$ and $\theta_{\rm L} > \theta_{\rm H}$, hence v_p will lead i_p and v_s will lag i_s by a larger external phase shift, leading to a higher circulating current and conduction loss. Since EDPS modulation only becomes active starting from an intermediate output power, e.g., 50% of the rated output power, under the proposed hybrid modulation scheme, the incurred circulating current is reduced compared to the case where EDPS modulation is used alone, hence conduction loss is reduced and the converter's efficiency is improved.

V. HARDWARE DESIGN AND EXPERIMENTAL VERIFICATION

A. Design Considerations

A DAB immittance converter prototype was designed with the specifications listed in Table I. Recall that $K = \omega_{\max}/\omega_{\min} = P_{\max}/P_{\min}$. Thus, when deciding the boundary between DFM and EDPS modulation, K should be selected based on the acceptable maximum switching frequency. Fig. 9 shows the relationships between the normalized effective tank current I_n and the normalized output power P_n for different modulation schemes, where $I_n = \sqrt{(I_{pn}^2 + I_{sn}'^2)/2}$, $I_{pn} = \sin(\alpha_s/2)$ is the normalized primary port current $\mathbf{I}_p$, and $I'_{sn} = \sin(\alpha_p/2)$ is the normalized primary-referenced secondary port current $\mathbf{I}'_s$. In general, a higher effective tank current leads to a higher conduction loss, thus, a lower effective tank current is preferred for higher efficiency. For DFM modulation, three curves corresponding to $K = (1.5, 2, 3)$ are plotted for comparison.

Due to the phase displacement between the fundamental components of the voltage and current at each port, EDPS

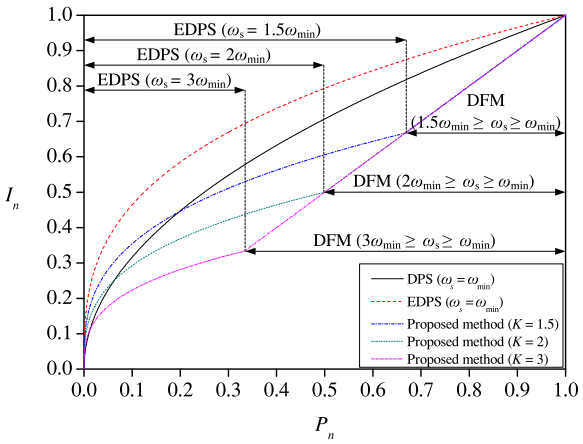

Fig. 9. Normalized effective tank current I_n versus normalized output power P_n.

modulation at $\omega = \omega_{\min}$ results in the highest effective tank current over the entire output power range. This is followed by DPS modulation at $\omega = \omega_{\min}$ which is characterized by a medium effective tank current with the fundamental components of the voltage and current at each port being in phase with each other. Although both EDPS and DPS modulation do not incur backflow power, circulating current still occurs during the zero voltage level of v_p and v_s and results in conduction loss. On the contrary, circulating current is completely eliminated by the proposed DFM modulation, where v_p and v_s are square-wave voltages (without zero voltage level) that are in phase with i_p and i'_s, respectively. Since the entire current waveforms of i_p and i'_s are involved in transferring active power, the rms values of i_p and i'_s required for transferring a given output power are the minimum compared to EDPS and DPS modulation, as shown in Fig. 9. To limit the range of switching frequency, a value of $K = 2$ is chosen for the converter prototype such that the switching frequency varies from 40 kHz at 100% to 80 kHz at 50% of the rated output power.

In choosing the transformer's turns ratio, n_p and n_s are chosen to be equal, i.e., $n_p = n_s$, since both V_{DC1} and V_{DC2} are equal to 400 V. The tertiary winding n_t should be less than n_p or n_s in order to reduce the voltage stress withstood by the SCC. Finally, $n_p : n_s : n_t$ is set to $3 : 3 : 2$. From (5) and (18), and setting $\omega_{\min} = 2\pi f_{s,\min} = 80\pi$ krad/s, the resonant inductors $L_p = L_s$ are calculated to be 344 μH. The primary-referenced magnetizing inductance L_M and tertiary winding's leakage inductance L'_t are estimated to be 5 mH and 5 μH, respectively. Based on these values, the required capacitance range of the tunable capacitor C_t can be calculated from (20) and (21) as 27–108 nF and the trend of C_t versus switching frequency f_s is shown in Fig. 10(a).

Recall that C_t is a function of C_{SCC} which in turn is a function of the control angle β. Fig. 10(b) shows the effective SCC capacitance C_{SCC}/C_b as a function of the control angle β. It can be seen that C_{SCC}/C_b increases very rapidly when the control angle exceeds approximately 160° or $8\pi/9$. To avoid the SCC from operating in this highly nonlinear region, the maximum value of β is chosen to be $8\pi/9$ which gives

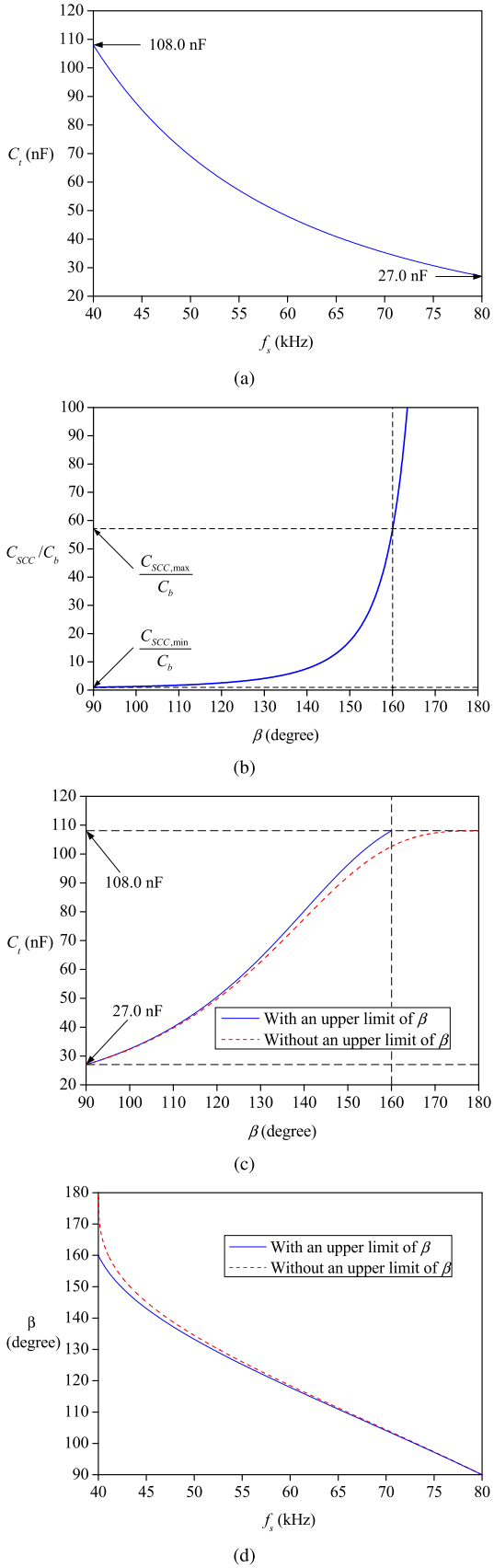

Fig. 10. (a) Effective tunable capacitance of C_t versus switching frequency f_s. (b) Effective SCC capacitance C_{SCC} versus control angle β. (c) Effective tunable capacitance of C_t versus control angle β. (d) Control angle β versus switching frequency f_s.

$C_{\mathrm{SCC,max}} = \pi C_b/[2\pi/9 + \sin(16\pi/9)]$. The minimum value of β is 90° or $\pi/2$ which gives $C_{\mathrm{SCC,min}} = C_b$. Finally, the required values of C_a and C_b can be calculated from (14) and (15) as 115.2 and 35.7 nF, respectively. Fig. 10(c) and (d) verified that the degree of nonlinearity of the relationship between C_t, β, and f_s has been effectively reduced by limiting the maximum value of β.

According to (12), high voltage ratings are required for the tertiary-side components (C_a, C_b, S_{t1}, S_{t2}). The maximum steady-state voltage of C_b is given by (26), which occurs at $\beta = \pi/2$ and $\omega = \omega_{\max}$ and can be used to determine the voltage rating of the SCC switches. However, as shown in Fig. 11(a), the voltage of C_b can still experience a large overshoot during transient process which may exceed the voltage rating of the switches. To protect these switches from overvoltage, a voltage clamp circuit as shown in Fig. 12 is placed in parallel with C_b to clamp v_{cb} to the input dc voltage V_{DC1} during transient overshoot. In comparison to the case without a voltage clamp circuit, Fig. 11(b) shows that v_{cb} and the voltages across the SCC switches (v_{st1} and v_{st2}) are kept below the dc input voltage V_{DC1} at all time.

$$V_{cb,\mathrm{peak}} = \sqrt{\left(\frac{n_t}{n_p}\right)^2 U_p^2 + \left(\frac{n_t}{n_s}\right)^2 U_s^2} \times \left(\frac{\sqrt{2}\cdot \frac{1}{\omega_{\max} C_b}}{\sqrt{\omega_{\max}{}^2 L_t^2 + \frac{1}{\omega_{\max}{}^2 C_a^2} + \frac{1}{\omega_{\max}{}^2 C_b^2}}} \right). \quad (26)$$

B. Sensitivity to Component Tolerances

To gain knowledge on the sensitivity of the network's resonant frequency to component tolerances, (9) was evaluated by Monte Carlo simulations for three nominal resonant frequencies (40, 60, and 80 kHz) when there exist ±5% tolerances in L_p, L_s, L_M, L_t, and C_t, assuming that their variations follow a normal distribution. From Fig. 13, it can be seen that the network's resonant frequency is not highly sensitive to the component tolerances. By using a two-port T-type resonant network model terminated with an equivalent load resistance R_{ac} as shown in Fig. 14, the network's transconductance $|\mathbf{I}'_s/\mathbf{U}_p|$ (current gain) are plotted as a function of switching frequency f_s for different values of R_{ac} as shown in Fig. 15, where (a), (b), and (c) corresponds to the nominal resonant frequency of 80, 60, and 40 kHz, respectively. It can be seen that the load-independent constant-current-gain characteristic of the resonant network holds over a small frequency range in the proximity of the nominal resonant frequency. Hence, some variations in the component values are not expected to alter the constant-current-gain behavior of the resonant network significantly.

C. Simulation/Experimental Results and Analysis

A DAB immittance converter prototype with the specifications listed in Table I was constructed to verify the proposed hybrid modulation scheme. The minimum switching frequency is chosen to be 40 kHz corresponding to the rated output power of 1.5 kW. For the selected value of K (=2), the maximum

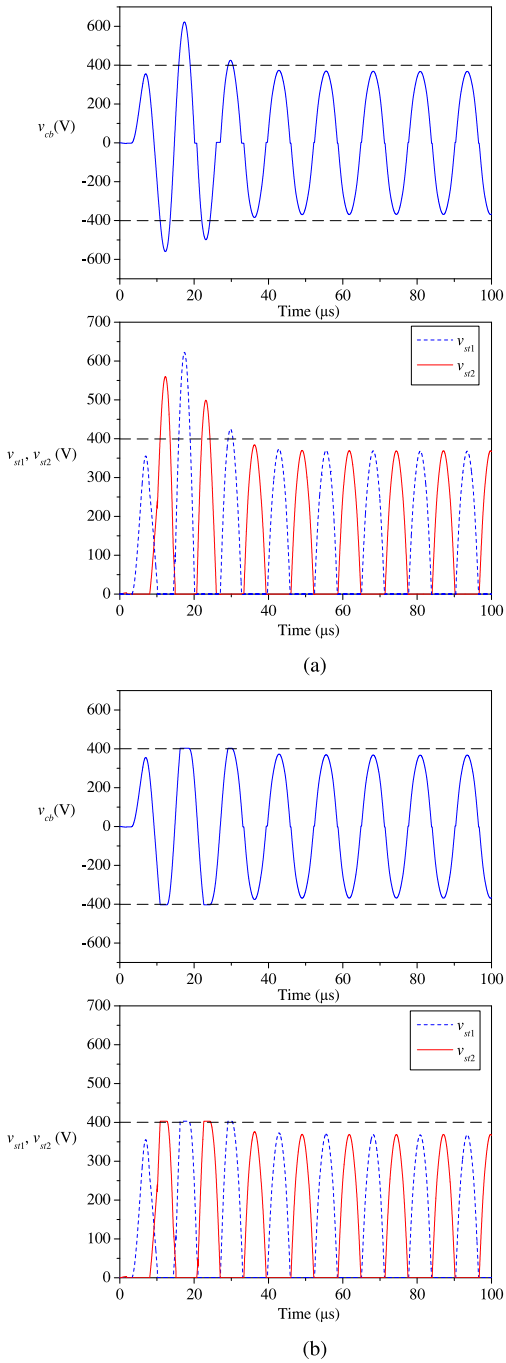

Fig. 11. Simulated waveforms of v_{cb}, v_{st1}, and v_{st2} during transient process. (a) Without a voltage clamp circuit (b) With a voltage clamp circuit.

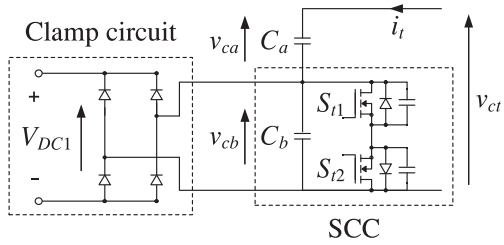

Fig. 12. Voltage clamp circuit for the protection of SCC switches.

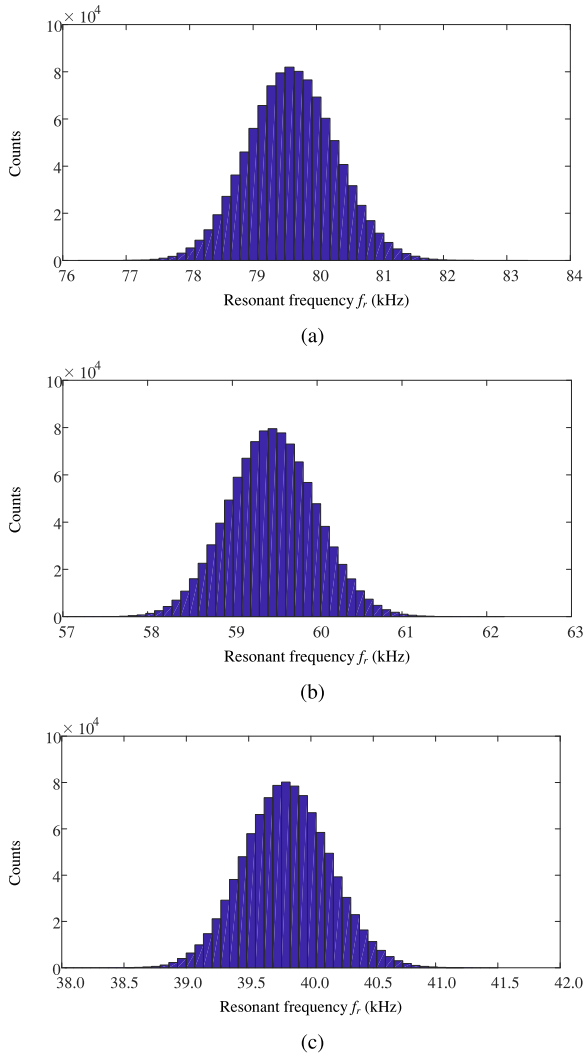

Fig. 13. Histograms showing the variations in resonant frequency f_r with $\pm 5\%$ tolerances in the parameter values of the resonant network for three nominal resonant frequencies: (a) 80 kHz; (b) 60 kHz; (c) 40 kHz.

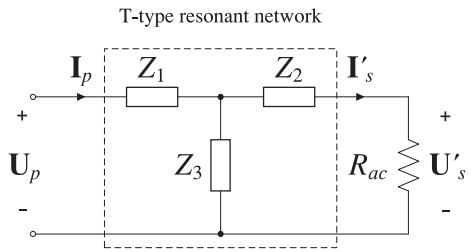

Fig. 14. Two-port T-type resonant network terminated with an equivalent load resistance R_{ac}.

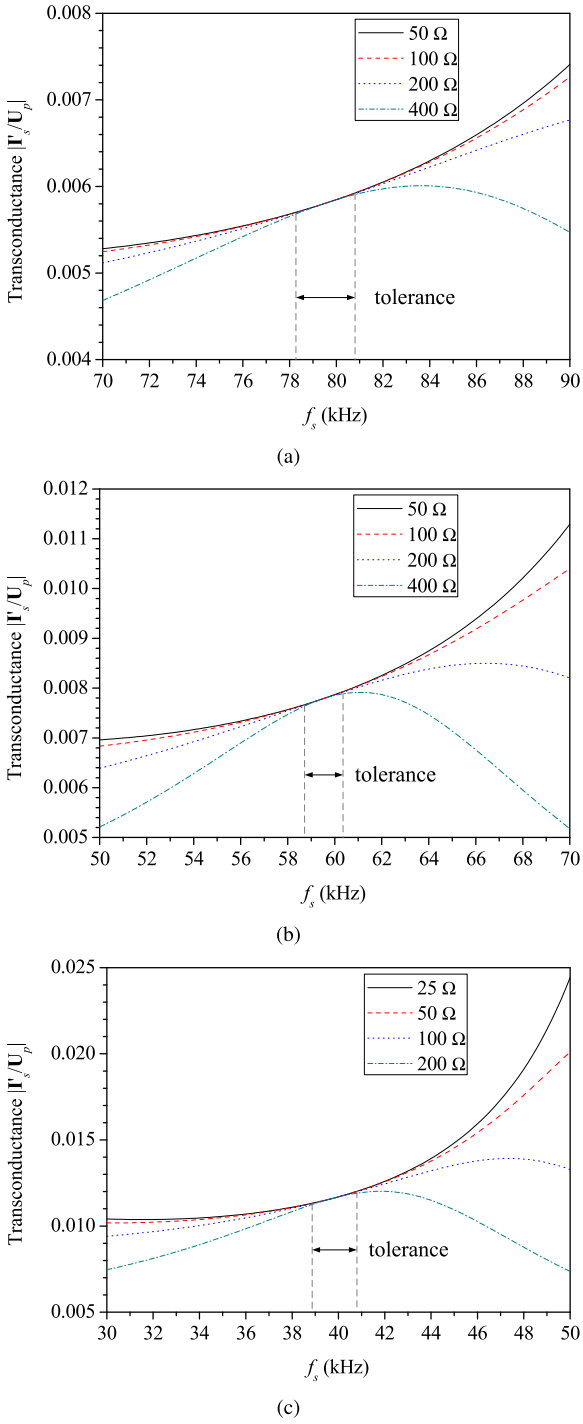

Fig. 15. Transconductance $|\mathbf{I}'_s/\mathbf{U}_p|$ (current gain) versus switching frequency f_s for three nominal resonant frequencies. (a) 80 kHz. (b) 60 kHz. (c) 40 kHz. For each nominal resonant frequency, transconductance curves are plotted for different values of R_{ac}.

frequency under DFM modulation is 80 kHz corresponding to 0.75 kW or 50% of the rated output power. In order to maintain the immittance condition of the resonant network under different output power levels, the SCC's control angle β is varied synchronously with the switching frequency f_s. Below 50% of the rated output power, the converter switches to EDPS modulation where the internal phase shifts $\alpha_p = \alpha_s = \alpha$ and external phase shift $\theta = \pm(\pi - \alpha/2)$ are varied synchronously at fixed switching frequency (=80 kHz). Fig. 16 summarizes the values of the control variables for realizing different output power levels, where P_n is the normalized output power with 1.5 kW being the base value.

It can be seen from the figure that the both DFM and EDPS modulation schemes share the same boundary at $P_n = 0.5$ with

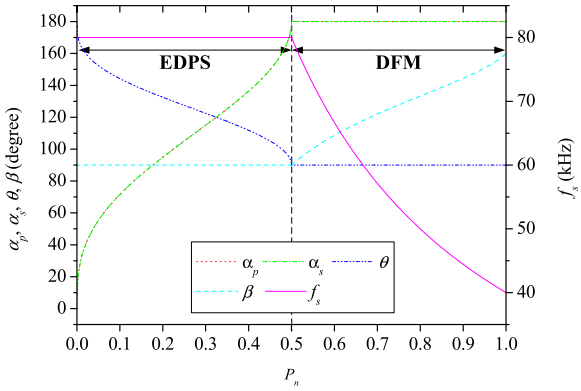

Fig. 16. Summary of control variables for realizing different output power levels.

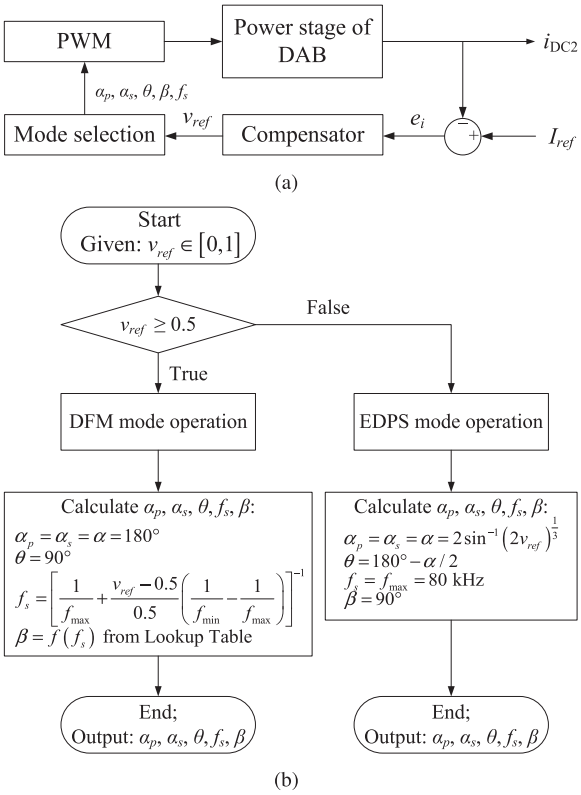

Fig. 17. (a) Closed-form implementation of the proposed DAB converter. (b) Flowchart for selection of operation mode and calculation of control variables.

$(\alpha_p, \alpha_s, \theta, \beta, f_s, P_n) = (180°, 180°, 90°, 90°, 80\text{ kHz}, 0.5)$, hence the converter will undergo smooth transition between light- and heavy-load operation. Fig. 17 shows the closed-loop design of the proposed DAB converter and the flowchart for selection of operation mode for practical implementation. In our designed hardware prototype, the proposed DAB converter is used to interface two dc voltage sources V_{DC1} and V_{DC2}, hence the control objective is to regulate the secondary-side dc current i_{DC2} at the desired (reference) value I_{ref}. The compensated error v_{ref} is used to determine the converter's operation mode, and hence the appropriate equation set for calculating the modulation parameters α_p, α_s, θ, β, and f_s. When $v_{ref} \geq 0.5$, i.e., $P_n \geq 0.5$, the converter will operate under DFM modulation, otherwise it will operate under EDPS modulation.

Fig. 18(a), (c), and (e) shows the simulated port voltages and currents at $f_s = 40$, 60, and 80 kHz, respectively, under forward power transfer, i.e., power flow from V_{DC1} to V_{DC2}. The corresponding experimental waveforms are shown in Fig. 18(b), (d), and (f) for comparison. It can be seen that both simulated and experimental waveforms are closely matched with each other. For all three output power levels, the voltage and current at each port are in phase with each other, leading to zero backflow power and zero circulating current.

Fig. 19(a)–(f) shows the measured port voltages and currents under DFM modulation at different voltage levels and switching frequencies. For a given switching frequency, the following can be observed.

1) The voltage and current at each port are constantly in-phase with each other and the relationship is unaffected by voltage level so long as the resonant network is tuned (by tuning SCC) to match with the switching frequency.
2) When V_{DC2} is reduced from 400 V (cf. Fig. 18) to 300 and 200 V, the amplitude of the primary port current i_p decreases proportionally with V_{DC2}, in agreement with (10).
3) Since V_{DC1} remains unchanged at 400 V, the amplitude of the secondary port current i_s also remains unchanged, in agreement with (11).

These observations are clear evidences of the immittance behavior of the tuned resonant network. To verify the ZVS behavior of the switches under DFM modulation, the detailed switching waveforms of S_{p1} and S_{s1} were captured and are shown in Fig. 20. It can be seen that ZVS is achieved in both switches. Due to symmetry, the switching waveforms of other switches (S_{p2}–S_{p4} and S_{s2}–S_{s4}) are similar, therefore ZVS are similarly achieved in all these switches.

To demonstrate the proper working of the SCC using the proposed modulation scheme (cf. Fig. 6), the measured waveforms of the gate drive signals of S_{t1} and S_{t2} ($v_{gs,st1}$, $v_{gs,st2}$), the terminal voltage of the SCC (v_{cb}), and the current flowing through the SCC (i_t) are shown in Fig. 21(a)–(c) for three switching frequencies (i.e., 40, 60, 80 kHz). It can be verified from these waveforms that both SCC switches are turned ON/OFF at zero voltage and they incur negligible switching loss to the converter. In practice, a turn-ON time delay of δ is introduced to the gate drive signals of the SCC switches as shown in Fig. 21(b) to ensure that the body diode of the incoming switch fully conducts before the gate drive signal is applied, hence ZVS turn-ON is achieved. In comparison to the conventional complementary PWM scheme with operating waveforms shown in Fig. 21(d), the proposed modulation scheme prevents the SCC current (i_t) from flowing through the body diodes of the switches during the zero voltage level of the SCC voltage (v_{cb}), hence the new modulation scheme is expected to improve the efficiency of SCC.

Below 50% of the rated output power, the converter switches to EDPS modulation with the switching frequency fixed at 80 kHz. Fig. 22(a) and (b) shows the measured port voltages and currents when the converter operates at 40% and 21% of the rated output power with $\alpha = 68.2°$ and 48.9°, respectively. It can be

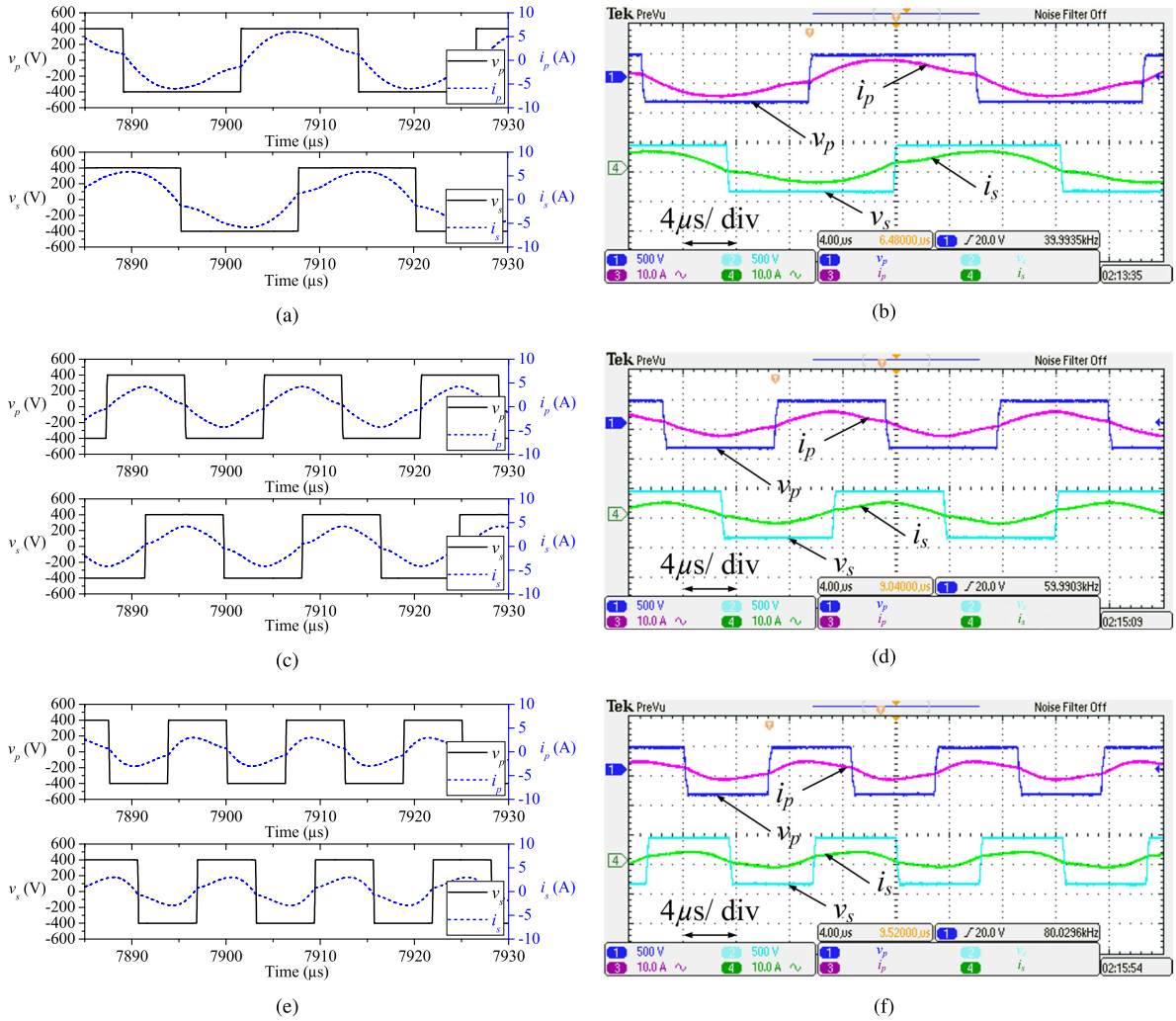

Fig. 18. Simulated [(a), (c), (e)] and measured [(b), (d), (f)] port voltages and currents under DFM modulation at different switching frequencies. (a) and (b) 40 kHz. (c) and (d) 60 kHz. (e) and (f) 80 kHz.

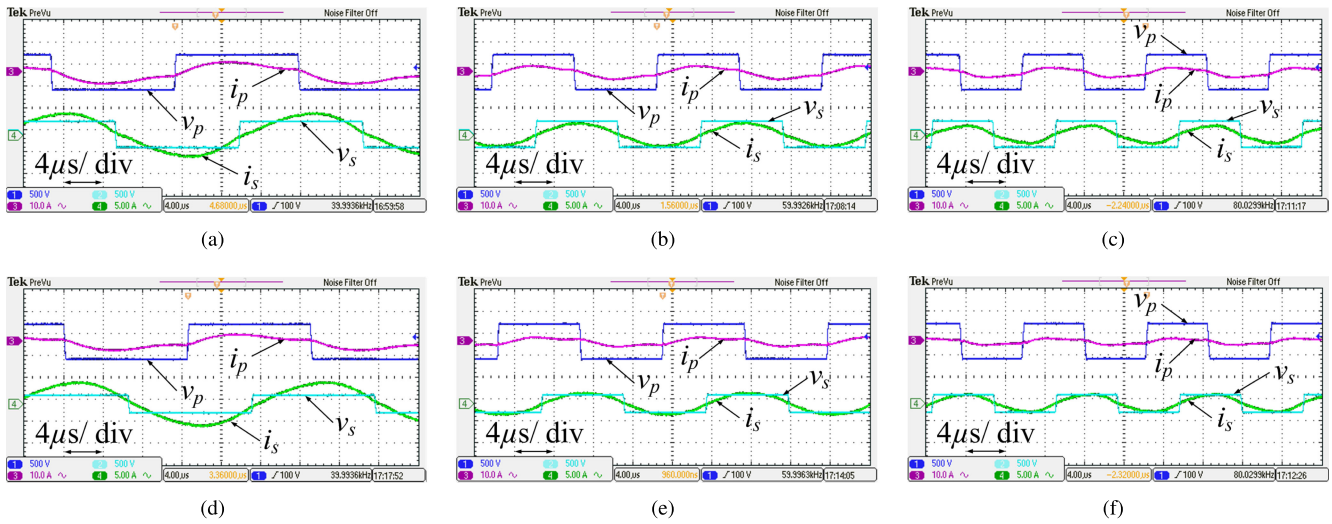

Fig. 19. Measured port voltages and currents under DFM modulation at different voltage levels [(a)–(c) $V_{DC2} = 300$ V; (d)–(f) $V_{DC2} = 200$ V] and switching frequencies [(a) and (d) 40 kHz; (b) and (e) 60 kHz; (c) and (f) 80 kHz].

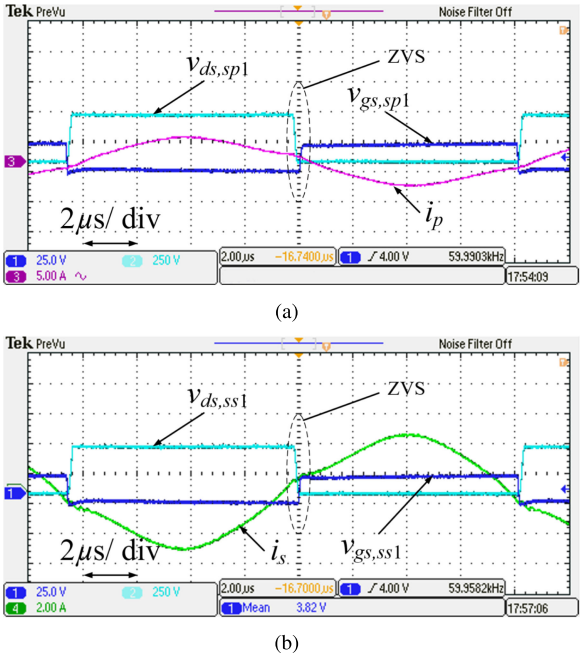

Fig. 20. Measured tank currents i_p and i_s, gate drive signals, and drain-source voltages of (a) S_{p1} and (b) S_{s1} at $f_s = 60$ kHz.

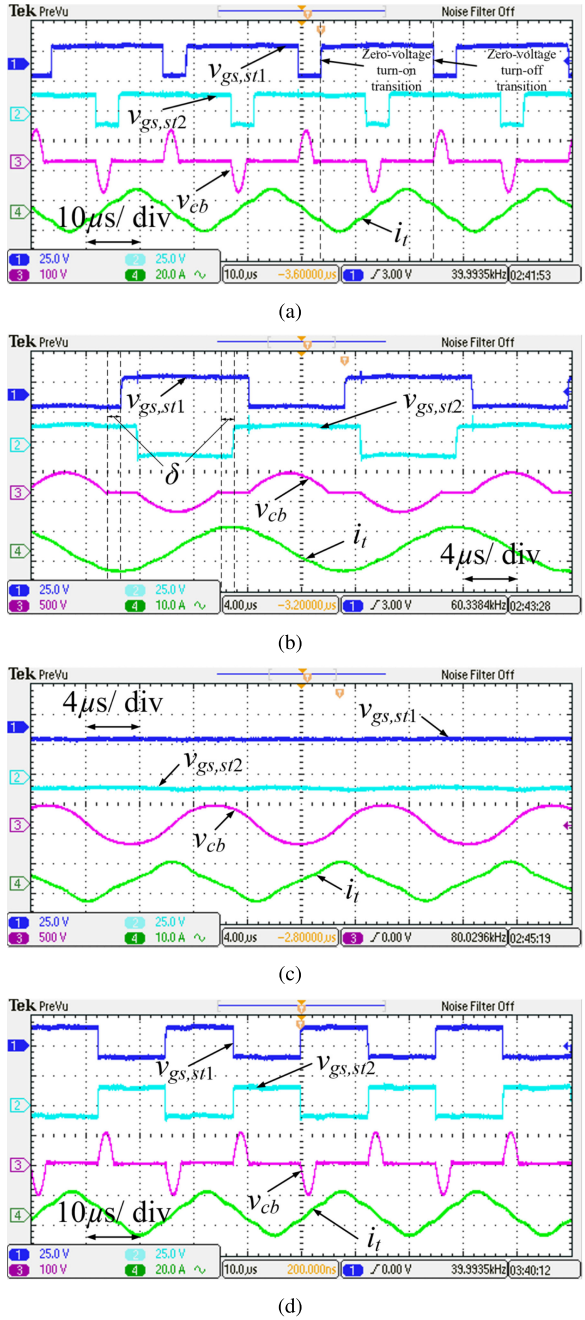

Fig. 21. Measured waveforms of $v_{gs,st1}$, $v_{gs,st2}$, v_{cb} and i_t at (a) 40 kHz ($\beta = 160^{\circ}$), (b) 60 kHz ($\beta = 117.9^{\circ}$), (c) 80 kHz ($\beta = 90^{\circ}$) (S_{t1} and S_{t2} are turned OFF), and (d) 40 kHz with conventional complementary PWM scheme.

verified from these waveforms that, under EPDS modulation and light-load condition, the zero-crossings of i_p are aligned with the rising edges of v_p and the zero-crossings of i_s are aligned with the falling edges of i_s, leading to zero backflow power and ZVS operation of all switches.

Experimental results depicting the closed-loop transient response of the proposed DAB converter under step load changes of 500 Ω → 125 Ω → 500 Ω are shown in Fig. 23. The transitions between EDPS and DFM modulations are evident from the measured gate drive signal of S_{t1} which is completely turned OFFunder EDPS modulation and is activated under DFM modulation. Furthermore, Fig. 24 shows that the closed-loop DAB converter also performed well under step input voltage changes of 400 → 350 → 400 V.

Fig. 25 shows a comparison between the measured efficiency of the proposed tunable DAB immittance converter and the efficiencies of a DAB converter with fixed immittance network under different modulation schemes. Among all the cases being compared, DPS modulation (black line with solid square marks) gives rise to the lowest efficiency due to nonzero circulating current, particularly at light load, and hard-switching in 50% of the switches. EDPS modulation with fixed switching frequency ($\omega = \omega_{\min}$) (red line with solid circle marks) results in the highest efficiency at heavy load above 73% of the rated output power. Over this output power range (73% to 100% of the rated output power), the converter's efficiency under DFM modulation with overlapped PWM scheme (pink line with solid left-pointing triangle marks) is marginally lower than that of EDPS modulation with $\omega = \omega_{\min}$. It is therefore believed that the conduction loss induced by circulating current under EDPS modulation is similar in magnitude to the conduction loss incurred by the SCC switches. As the output power is decreased from 73% to 50% of the rated output power, the circulating current under EDPS modulation further increases and the increased conduction loss leads to a lower efficiency compared to that of DFM modulation with overlapped PWM scheme. Comparing the performances of DFM modulation with overlapped PWM scheme and the conventional complementary PWM scheme (green line with solid inverted triangle marks), it can be verified that the former leads to an improved efficiency of the SCC and hence a higher overall efficiency of the DAB converter.

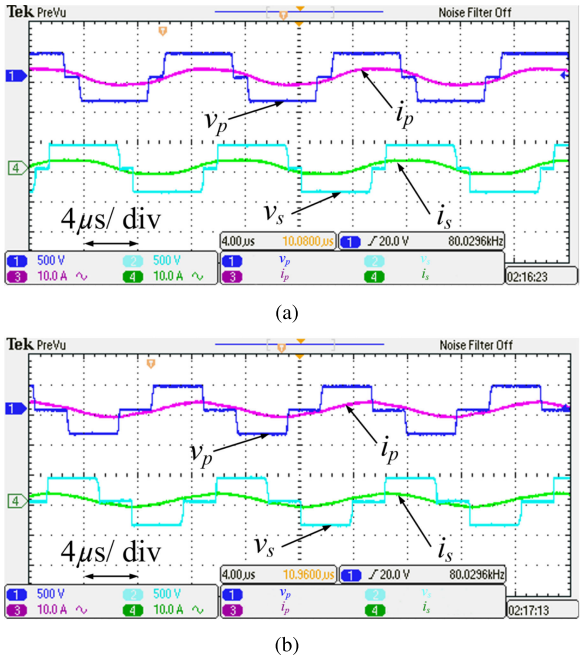

Fig. 22. Measured port voltages and currents under EDPS modulation at 80 kHz for (a) 40% and (b) 21% of the rated output power.

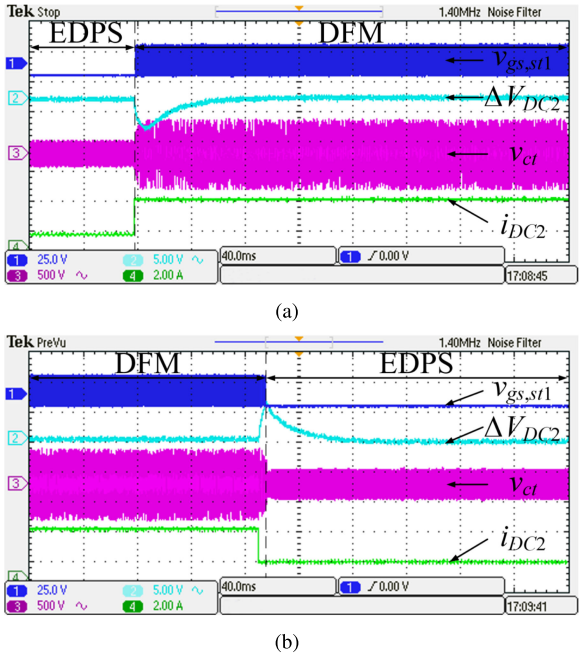

Fig. 23. Closed-loop transient response of the proposed DAB converter under step load changes. (a) 500 Ω → 125 Ω. (b) 125 Ω → 500 Ω.

For output power below 50% of the rated output power, the proposed hybrid modulation scheme switches to EDPS modulation with $\omega = \omega_{\max}$ (blue line with solid triangle marks) and consistently performs better than both DPS modulation and EDPS modulation with $\omega = \omega_{\min}$. Comparing the port voltage and current waveforms associated with these three modulation schemes at 40% of the rated output power [cf. Figs. 22(a), 26(a),

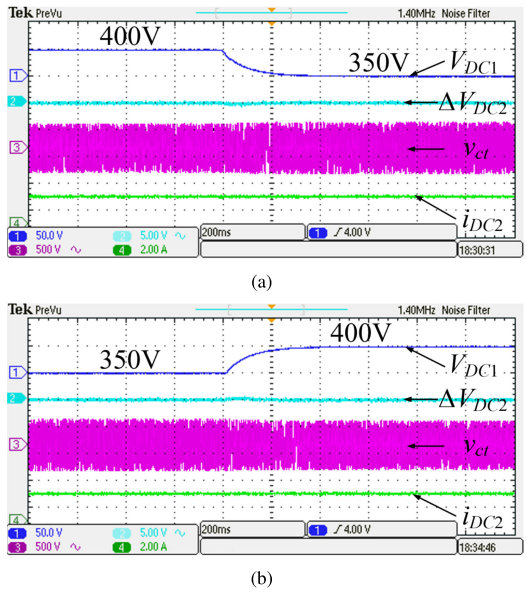

Fig. 24. Closed-loop transient response of the proposed DAB converter under step input voltage changes. (a) 400 → 350 V. (b) 350 → 400 V.

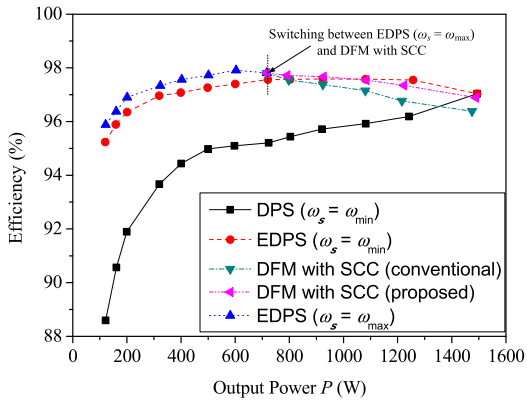

Fig. 25. Measured converter's efficiency under different modulation schemes.

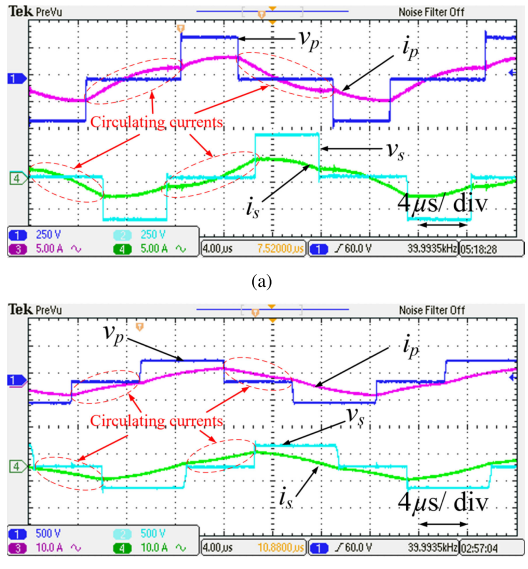

Fig. 26. Measured port voltages and currents under (a) DPS and (b) EDPS modulations at 40 kHz for 40% of the rated output power.

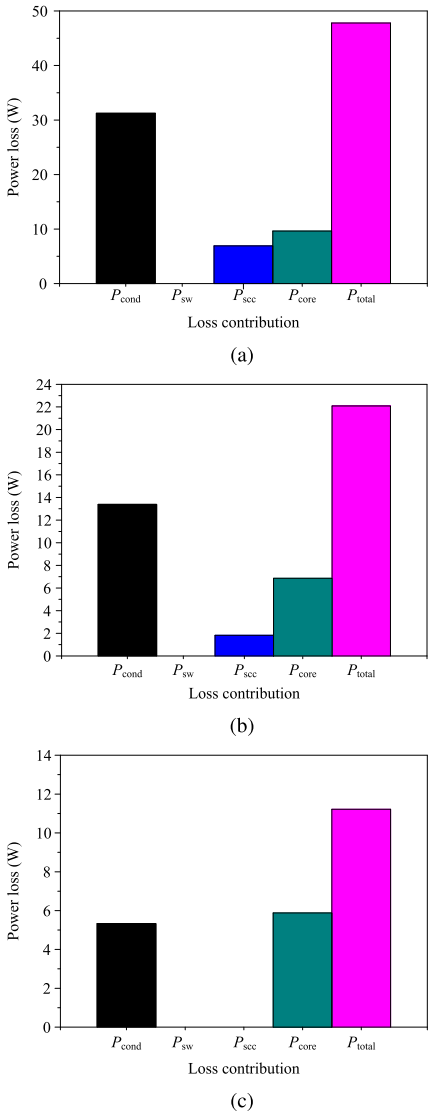

Fig. 27. Loss breakdown of the proposed DAB converter for (a) 100% of $P_{\max}$ under DFM modulation; (b) 60% of $P_{\max}$ under DFM modulation; (c) 30% of $P_{\max}$ under EDPS modulation.

and (b)], it can be concluded that the main reasons for the poor light-load performance of DPS modulation is high circulating current and hard-switching in 50% of the switches, while for EPDS modulation with $\omega = \omega_{\min}$, the high circulating current resulting from the large external phase shift between v_p and v_s explains its lower efficiency compared to EPDS modulation with $\omega = \omega_{\max}$, although ZVS is achieved in all switches in both cases.

Finally, the loss breakdown of the proposed DAB converter under DFM and EDPS modulation schemes are shown in Fig. 27 for three output power levels. The total power loss P_{total} comprises—the loss in SCC P_{scc}, conduction loss P_{cond}, magnetic core loss P_{core}, and switching loss P_{sw}. P_{scc} is caused by the ON-state resistances of the SCC MOSFETs; P_{cond} is caused by the ON-state resistances of the primary- and secondary-side H-bridge's MOSFETs, and resistive losses in the copper windings of the two resonant inductors and high-frequency transformer; P_{core} occurs in the magnetic cores of the two resonant inductors and high-frequency transformer; P_{sw} arises from MOSFETs undergoing hard-switching, which is negligible as ZVS is achieved is all switches. It can be seen from the loss breakdown that the total power loss is mainly contributed by conduction loss under medium- to heavy-load operations, and it is dominated by both conduction loss and core loss under light-load operation.

VI. Conclusion

A new LCL-based DAB immittance converter topology and a hybrid modulation scheme are collectively proposed in this article. With the proposed modulation scheme, the DAB converter is switched between two operation modes. For medium- to heavy-load conditions, the DAB converter's output power is regulated by frequency modulation while the desired conditions of zero backflow power, zero circulating current, and full ZVS operation are achieved by dynamically matching the resonant frequency of the LCL network to the switching frequency. For light-load condition, the DAB converter switches to EDPS modulation to achieve zero backflow power, full ZVS operation, and reduced circulating current compared to the case where EDPS modulation is used over the entire output power range. The effectiveness of the proposed topology and modulation scheme is verified by experimental results obtained from a 1.5-kW hardware prototype with efficiency above 96% for all output power levels.

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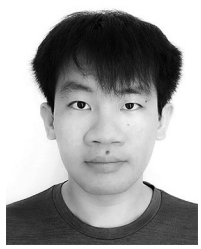

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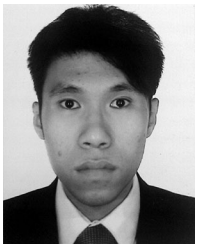

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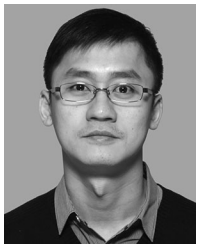

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