Conversion Efficiency of the Buck Three-Level DC–DC Converter in Unbalanced Bipolar DC Microgrids

Giel Van den Broeck, *Graduate Student Member, IEEE*, Wilmar Martinez, *Senior Member, IEEE*, Mauricio Dalla Vecchia, *Graduate Student Member, IEEE*, Simon Ravyts, *Graduate Student Member, IEEE*, and Johan Driesen, *Senior Member, IEEE*

***Abstract*—This article evaluates the power conversion efficiency of the buck three-level dc–dc converter, when operating in unbalanced bipolar dc microgrids. Bipolar dc microgrids adopt a positive, neutral, and negative wire to double the power transfer capability, reduce conduction losses, and provide two voltage levels. Additional converters are however required to balance the pole-to-neutral voltages in the presence of unbalanced loading conditions. Previous work has shown that the buck three-level dc–dc converter features voltage balancing capability and can serve, at the same time, as an interface for battery storage and photovoltaic systems for example. Nevertheless, available conversion loss models are only valid for balanced loading conditions. Therefore, this article derives a conversion loss model for a buck three-level dc–dc converter, also valid in unbalanced conditions. The model is decomposed in balanced and unbalanced components in order to separate losses arising in balanced and unbalanced conditions. Furthermore, the model accounts for nonideal common-mode currents as experimental results will reveal that they have a profound impact on the conversion efficiency in unbalanced and balanced conditions.**

***Index Terms*—Bipolar dc microgrid, common-mode current, dc–dc power conversion, energy storage, power distribution.**

I. Introduction

LOW-VOLTAGE dc (LVdc) microgrids provide a valuable alternative for ac technology, considering that future power systems will encompass a high number of distributed energy resources and energy efficient loads, all grid-interfaced by power electronic converters. LVdc microgrids are highly compatible with, for instance, battery energy storage, fuel cells, photovoltaic systems, variable speed drives, heat pumps, and LED lighting [1]. Applications for dc grid architectures range from data centers [2], commercial buildings [3], [4], industrial facilities [5], [6], electric vehicle charging infrastructure [7], public lighting [8], to all-electric aircraft [9], and shipboard power distribution systems [10]. Apart from increased compatibility, LVdc microgrids enable to transfer more power per unit conductor cross-section and they are inherently controllable [11]–[13].

Two network configurations of LVdc microgrids exist: the unipolar, two-wire LVdc configuration; and the bipolar, three-wire LVdc configuration [14]. This article considers bipolar LVdc microgrids, applying a positive, neutral, and negative conductor for power distribution, as depicted in Fig. 1. Typical voltage levels are ± 350 and ± 380 V [15], [16]. On the one hand, the bipolar LVdc configuration provides two voltage levels: The positive pole-to-neutral voltage level (350 or 380 V) and the

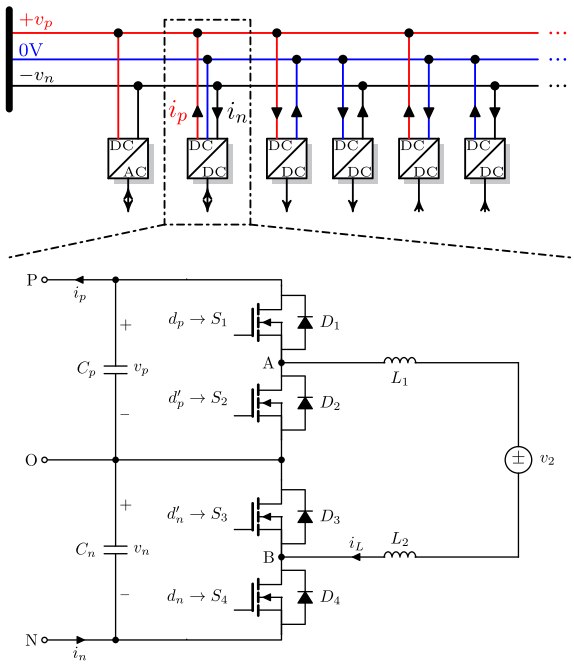

Fig. 1. Bipolar dc microgrid architecture with the buck three-level dc–dc converter balancing the pole-to-neutral voltages.

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The authors are with the Department of Electrical Engineering (ESAT), EnergyVille, Katholieke Universiteit Leuven, 3000 Leuven, Belgium (e-mail: giel.vandenbroeck@esat.kuleuven.be; wilmar.martinez@kuleuven.be; mauricio.dallavecchia@kuleuven.be; simon.ravyts@esat.kuleuven.be; johan.driesen@esat.kuleuven.be).

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positive-to-negative pole-to-pole voltage level (700 or 760 V). Therefore, devices can be connected at a suited voltage level. Electric vehicle chargers benefit from the pole-to-pole voltage level, while the end-use voltage of LED lighting and heatpumps is lower and therefore benefits from the pole-to-neutral voltage level. On the other hand, the bipolar LVdc configuration enables to transfer more power per unit conductor cross section with less conduction losses as compared to the unipolar configuration [17].

The price to pay for the advantages that bipolar LVdc (b-LVdc) yield, is the need for (additional) converters stabilizing the two pole-to-neutral voltage levels instead of a single voltage level in the unipolar configuration [18]. Although equal load distribution across the positive and the negative pole should preferably minimize the level of unbalance, unbalanced conditions may still arise during transients from one operating point to another or when a particular device on one pole would fail in operation. Should the case arise, converters with voltage balancing capability should actively control the positive and negative pole-to-neutral voltage by transferring power from the positive to the negative pole, such that the power infeed and off-take matches at each pole. If no converters with voltage balancing capability would be provided, the pole-to-neutral voltages would start deviating to such an extent that power semiconductors and passive devices can fail due to overvoltage. To avoid this situation from occurring, different possibilities exist. The first possibility is applying two separate voltage source converters for the positive and the negative pole, respectively [19]. The second possibility is applying a single voltage source converter regulating the pole-to-pole voltage, complemented with a half-bridge voltage balancer [20]. The third possibility is applying an ac/dc or dc/dc three-level converter, which is the subject of this article [21]–[24].

The buck three-level dc–dc converter (B-TLC) is a dc–dc converter that can simultaneously interface a dc device (e.g., battery storage or photovoltaic modules) and balance the pole-to-neutral voltages of a bipolar LVdc microgrid [25]. It therefore benefits from the split-capacitor dc front end, as depicted in Fig. 1. By controlling the four power semiconductor devices S_1–S_4, the B-TLC is able to asymmetrically inject current in either the positive and the negative pole. Additionally, because power is directed immediately toward the positive or negative pole, an additional voltage balancing step becomes obsolete.

The aim of this article is evaluating the power conversion efficiency and losses of the B-TLC in unbalanced conditions, for pole-to-neutral voltage balancing in bipolar dc microgrids. Thus far, available conversion loss models for three-level dc–dc converters are only valid in balanced conditions [26]. This article, therefore, proposes a conversion loss model, expressed in balanced and unbalanced components [25], which decomposes losses occurring in balanced conditions from losses occurring in unbalanced conditions. Furthermore, the presented conversion loss model accounts for common-mode currents which influence the conversion efficiency as the article will explain theoretically and prove experimentally. These common-mode currents arise due to stray capacitances, which, for instance, occur in photovoltaic installation between the electrodes and the frame [27], [28] and flow through electromagnetic interference (EMI) filter capacitors that intentionally provide return paths for common-mode currents [19].

The article starts by revisiting the operation of the B-TLC in unbalanced conditions, the governing equations and the decomposition in balanced and unbalanced components. The decomposition enables to separate loss factor which depend on the level of unbalance from loss factors that do not. Subsequently in Section III, the decomposition is used to evaluate the inductor current waveforms, in which special consideration is given to common-mode currents that profoundly affect the waveforms in unbalanced conditions. Section IV subsequently links the inductor current waveform to the core losses and derives all remaining loss components systematically as a function of the balanced and unbalanced duty cycle, yielding the proposed conversion loss model. That model is eventually validated by comparing simulation to experimental results of a B-TLC prototype in unbalanced conditions, presented in Sections V and VI, respectively. Finally, Section VII concludes this article.

II. Operation in Unbalanced Conditions

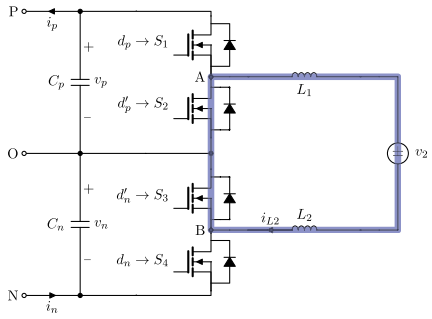
A. Circuit Description

Fig. 1 depicts the B-TLC. As shown in the figure, the B-TLC constitutes a bidirectional interface between a three-wire, bipolar LVdc microgrid at the front-end terminals (labeled P, O, and N) with the dc back end, represented by the voltage source v_2. The dc back-end can for instance be a battery storage system, a photovoltaic system, or an electric vehicle. The B-TLC consists of four power semiconductor devices S_1 to S_4 with antiparallel diodes D_1 to D_4, two stacked capacitors C_p and C_n at the dc front end and two inductors L_1 and L_2 carrying inductor current i_L. The two front end capacitors stabilize the pole-to-neutral voltages v_p and v_n, respectively. The converter supplies or withdraws currents i_p and i_n from the bipolar dc microgrid, as indicated in the figure.

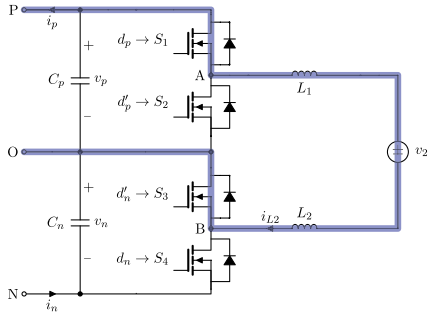
B. Circuit Operation

Power semiconductor devices S_1 and S_2 are turned ON and OFF complimentary, as well as power semiconductor devices S_3 and S_4. The two switch pairs are driven by pulsewidth modulation signals, characterized by the positive duty cycle d_p for S_1 and the negative duty cycle d_n for S_4. The complimentary switches S_2 and S_3 are then driven by complimentary pulsewidth modulation signals with duty cycles $d'_p = 1 - d_p$ and $d'_n = 1 - d_n$, respectively.

In order to understand how the B-TLC is able to balance v_p and v_n when i_p and i_n differ, consider Fig. 2 and presume that the inductor current is controlled at its setpoint value. Fig. 2 shows the four conversion stages that the B-TLC can attain. Stage 0 is the freewheeling stage, where S_1 and S_4 are both OFF, applying $-v_2$ across the inductors. In stage 1, S_1 is in the ON-state and S_4 is in the OFF-state, applying $v_p - v_2$ across the inductors. In stage 2, S_1 is in the OFF-state and S_4 is in the ON-state, applying $v_n - v_2$ across the inductors. In stage 3, S_1 and S_4 are both in the ON-state and $v_p + v_n - v_2$ is applied across



(a)



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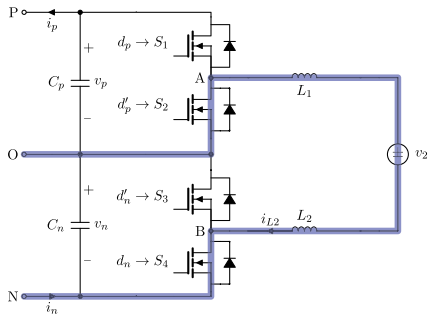

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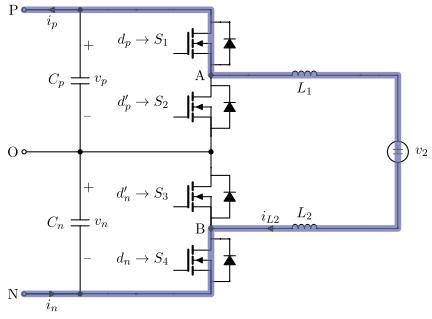
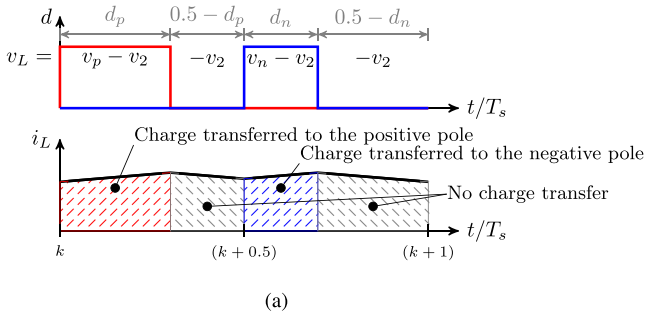


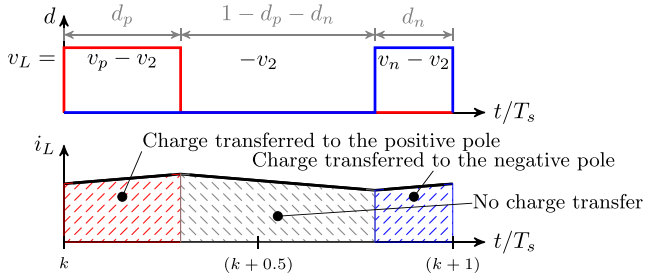
(d)

Fig. 2. Operation stages of the B-TLC. (a) Stage 0. (b) Stage 1. (c) Stage 2. (d) Stage 3.

the inductors. By altering the duration of stage 1 and stage 2 throughout a single switching period, the amount of charge injected (or withdrawn in case $i_L > 0$) from the dc front end by the inductor current is altered. If for example, stage 1 lasts longer than stage 2, more charge is exchanged with the positive capacitance C_p as compared to the negative capacitance C_n.



(a)



(b)

Fig. 3. Modulation schemes. (a) Modulation 1. (b) Modulation 2.

This difference in duration is used to balance the dc front end, connected to the bipolar LVdc microgrid.

The difference in duration is also noticeable from the modulation scheme depicted over time t in Fig. 3(a) for an arbitrary switching period k of duration T_s. As duty cycle d_p exceeds d_n, more charge will be exchanged with C_p as compared to C_n. Typically, d_p and d_n are applied at $t/T_s = k$ and $t/T_s = k + 0.5$ to minimize the inductor current ripple. But alternatively d_p and d_n can be applied at the start and at the end of a switching cycle, as in Fig. 3(b), which will be discussed further in the next section.

C. Governing Equations

Expressing the voltage-second balance for the inductors and the current-second balance for the capacitors, yields the steady-state (1)–(3), in which D_p is the steady-state positive duty cycle, D_n is the steady-state negative duty cycle, I_L is the steady-state inductor current, I_p is the steady-state load current at the positive pole and I_n is the steady-state load current at the negative pole. Given the loading conditions I_p and I_n, and the duty cycles D_p and D_n, the equations yield the steady-state operating point V_p, V_n, and I_L

$$D_p V_p + D_n V_n - V_2 = 0 \tag{1}$$

$$D_p I_L + I_p = 0 \tag{2}$$

$$D_n I_L + I_n = 0. \tag{3}$$

These equations can subsequently be decomposed in balanced (b) and unbalanced (u) components in (5)–(7). Not only V_p, V_n, I_p, and I_n but also D_p and D_n have been decomposed according to (4). This lead to the introduction of the balanced D_b and the unbalanced duty cycle D_u. Note that the balanced duty

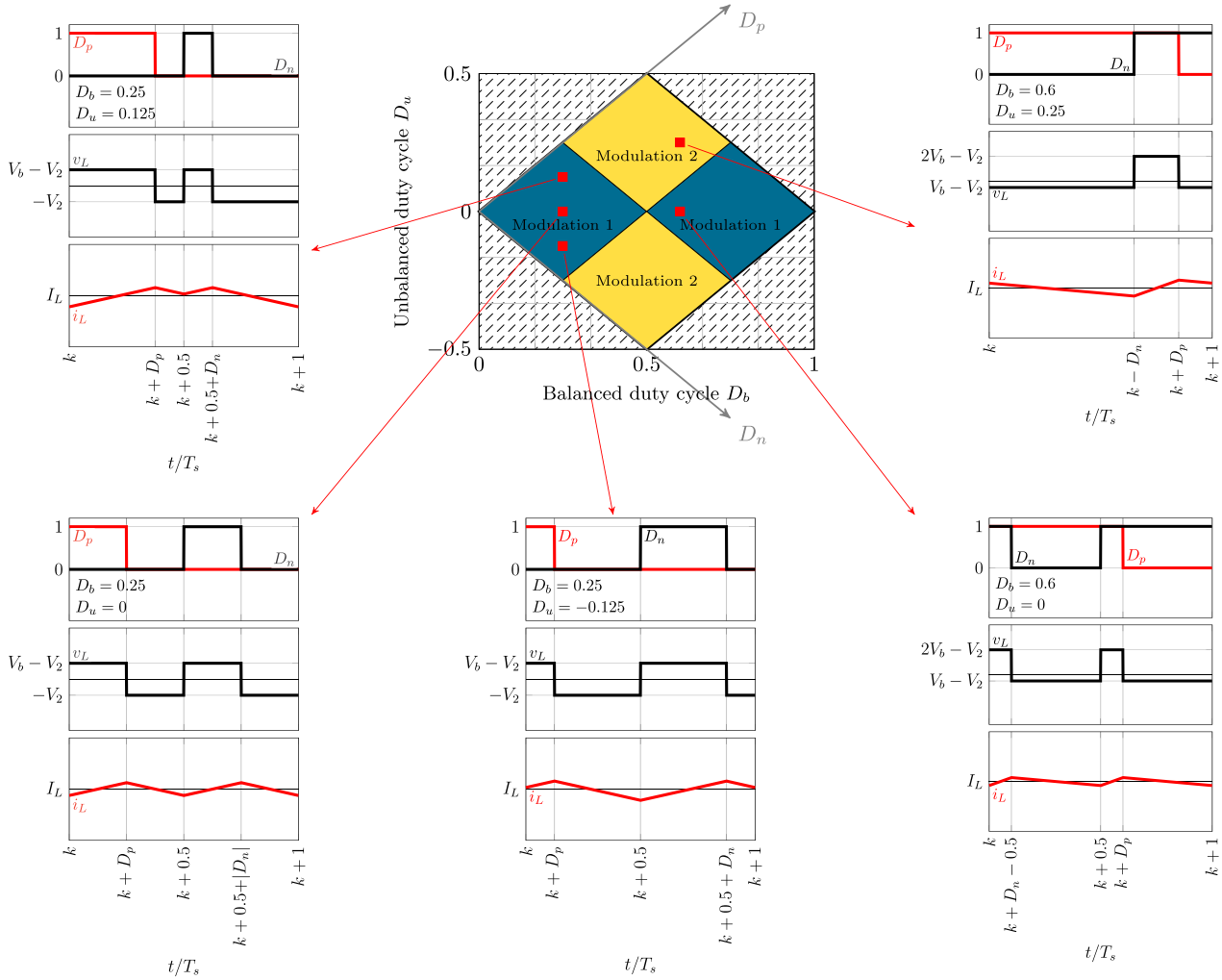


Fig. 4. Modulation of the B-TLC in unbalanced conditions.

cycle is solely a function of the input–output voltage ratio and does not depend on the level of unbalance current I_u. Hence D_b remains constant, regardless of I_u. The only quantity depending on I_u is the unbalanced duty cycle D_u, related to the ratio of I_u and I_L. In the remainder of this article, equations will be expressed in terms of the balanced and unbalanced duty cycle to distinguish loss components which depend on the level of unbalance and others which do not. A more in-depth discussion about the decomposition into balanced and unbalanced components can be found in [25], [29]

$$\forall x \in [d, v, i, D, V, I, P] : \begin{cases} x_p = x_b + x_u \\ x_n = x_b - x_u \end{cases} \tag{4}$$

$$D_b = \frac{V_2}{2V_b} \tag{5}$$

$$I_L = -\frac{I_b}{D_b} \tag{6}$$

$$D_u = -\frac{I_u}{I_L} = \frac{I_u}{I_b} D_b. \tag{7}$$

Note that, just like the original duty cycles D_p and D_n, the balanced D_b and unbalanced D_u duty cycle are limited [25]. The balanced duty cycle are absolutely limited between $[0, 1]$, meanwhile the limits of the unbalanced duty cycle depend on the balanced duty cycle D_b according to (8). This implies that the amount of unbalanced current I_u, that the B-TLC can supply, depends on the magnitude of the inductor current and the maximum unbalanced duty cycle

$$\begin{aligned} |D_u| &\leq D_b \qquad \text{if } D_b \leq 0.5 \\ |D_u| &\leq 1 - D_b \quad \text{if } D_b > 0.5. \end{aligned} \tag{8}$$

III. Inductor Current in Unbalanced Conditions

This section will investigate the shape of the inductor current waveform in unbalanced operating conditions. The inductor current waveform directly relates to the inductor core losses, described and evaluated in the next section. Because the converter is intended for bidirectional applications, only continuous conduction mode is considered.

Fig. 4 depicts the inductor current waveforms (with dc value I_L), as well as the pulsewidth modulation signals with duty

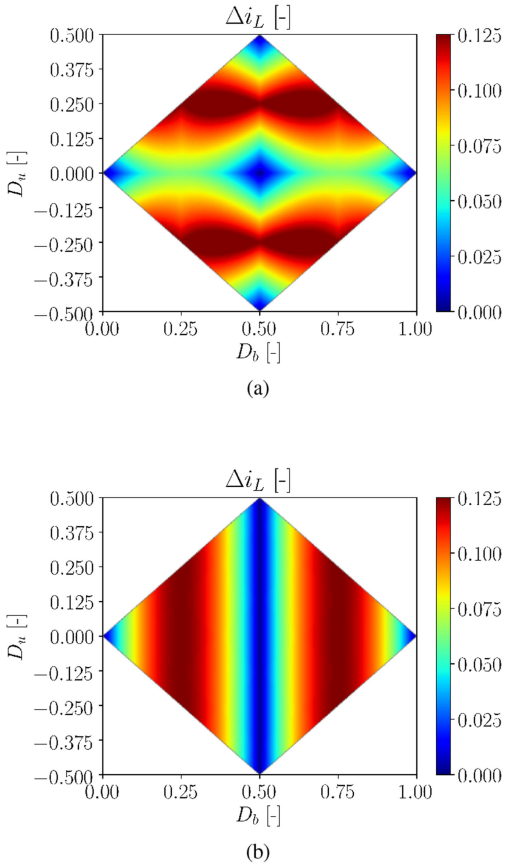


Fig. 5. Normalized inductor current ripple Δi_L as a function of the balanced D_b and unbalanced D_u duty cycle (absolute current ripple $\Delta I_L = \Delta i_L V_b[(L_1 + L_2)f_s]^{-1}$). (a) Modulation 1. (b) Modulation 2.

cycles D_p and D_n, the voltage v_L across L_1 and L_2. It depicts these waveforms for different operating points of the operating area defined by (8). Remind that in balanced, steady-state conditions the unbalanced duty cycle equals zero and that the balanced duty cycle D_b only depends on the dc back-end voltage V_2 and the balanced voltage V_b. The modulation scheme commonly adopted in the literature is modulation scheme 1 of Fig. 3(a) [26], [30], which is applied in the blue parts of the operating area, as shown in Fig. 4. In the remaining yellow part, modulation scheme 2 results in the lowest inductor current ripple, as the subsequent analysis will prove. According to the figure, the inductor current ripple not only depends on D_b but also on the level of unbalance characterized by D_u.

In order to evaluate the inductor current ripple, consider (9) and (10). These equations yield the normalized current ripple Δi_L for modulation scheme 1 and 2, respectively. The normalized inductor current ripple is proportional to the absolute inductor current ripple ΔI_L according to (11). Based upon these equations, Fig. 5 depicts the inductor current ripple for modulation scheme 1 and 2 as a function of the balanced and unbalanced duty cycle. The figure shows that, for modulation scheme 1, the inductor current ripple increases linearly with D_u up to $|D_u| = 0.25$ where it starts decreasing again. For modulation scheme 2, the inductor ripple is independent from D_u. The

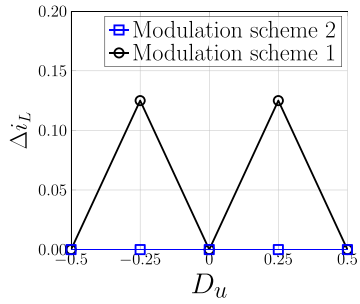


Fig. 6. Comparison of the current ripple in case of modulation scheme 1 and 2 for $D_b = 0.5$ as a function of D_u.

figure also indicates that modulation scheme 1 features a lower inductor current ripple as compared to modulation scheme 2 in certain parts of the operating area and vice versa. This is more clearly indicated in the yellow area in Fig. 4, where modulation scheme 2 features a lower ripple magnitude than modulation scheme 1. Consider for instance the inductor current ripple as a function of the level of unbalance (D_u) in Fig. 6. The figure indicates that the normalized inductor current ripple in case of modulation scheme 2 does not vary with the level of unbalance, while it does vary in case of modulation scheme 1, yielding an overall higher inductor current ripple. Therefore, this article recommends to adopt both modulation scheme 1 and 2 in specific parts of the operating area where each of them yields the lowest inductor current ripple

$$\Delta i_L = \begin{cases} (D_b + |D_u|)\,(1 - 2D_b) & D_b \in [0; 0.25] \\ (0.5 - D_b + |D_u|)\,(2D_b) & D_b \in [0.25; 0.5] \wedge |D_u| \leq 0.25 \\ (1 - D_b - |D_u|)\,(2D_b) & D_b \in [0.25; 0.5] \wedge |D_u| > 0.25 \\ (D_b + |D_u| - 0.5)\,(2 - 2D_b) & D_b \in [0.5; 0.75] \wedge |D_u| \leq 0.25 \\ (D_b - |D_u|)\,(2 - 2D_b) & D_b \in [0.5; 0.75] \wedge |D_u| > 0.25 \\ (1 - D_b + |D_u|)\,(1 - 2D_b) & D_b \in [0.75; 1] \end{cases} \tag{9}$$

$$\Delta i_L = \begin{cases} (1 - 2D_b)(2D_b) & D_b \leq 0.5 \wedge D_b - |D_u| > 0 \\ (2D_b - 1)(2 - 2D_b) & D_b > 0.5 \end{cases} \tag{10}$$

$$\Delta I_L = \Delta i_L V_b \left[(L_1 + L_2)\, f_s\right]^{-1}. \tag{11}$$

However, the analysis of the inductor current until now does not consider the presence of common-mode capacitances C_Y between the terminals of the dc back-end v_2 and the positive pole and the negative pole, respectively, as depicted in Fig. 7. These capacitances represent capacitor's of electromagnetic interference (EMI) filters and stray capacitances, which for instance occur in photovoltaic installations between the electrodes and the frame [27], [28]. Due to currents passing by C_Y, the inductor current waveforms i_{L1} and i_{L2} are no longer equal, although they share the same dc components I_L.

Accordingly, Fig. 7 indicates the three circuits the dc back-end is composed of. Apart from the main circuit considered thus far,

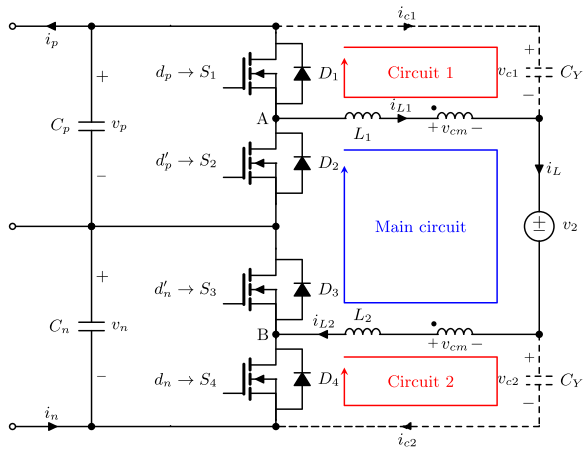


Fig. 7. B-TLC with common-mode choke and additional capacitances C_Y.

circuit 1 and 2 are introduced and governed by (12), (13). The voltages across C_Y is denoted v_{c1} and v_{c2}, respectively. v_{c1} and v_{c2} are charged by i_{c1} and i_{c2}. L_1 and L_2 are both equal to $L/2$. Furthermore, a common-mode choke is included, inducing a voltage $v_{\rm cm}$. The analysis presumes that the voltage across C_Y does not vary appreciably throughout a switching period, such that the small-ripple approximation holds [31]

$$\frac{L}{2}\frac{di_{L1}}{dt} = v_{c1} - v_{\rm cm} - (1-d_p)v_p \tag{12}$$

$$\frac{L}{2}\frac{di_{L2}}{dt} = v_{c2} + v_{\rm cm} - (1-d_n)v_n. \tag{13}$$

Expressing (12) and (13) in terms of the differential-mode and the common-mode inductor current, as defined in (14) and (15), leads to (16) and (17)

$$i_{\rm dm} = \frac{i_{L1}+i_{L2}}{2} \tag{14}$$

$$i_{\rm cm} = \frac{i_{L1}-i_{L2}}{2} \tag{15}$$

$$L\frac{di_{\rm dm}}{dt} = d_p v_p + d_n v_n - v_2 = 2d_b v_b + 2d_u v_u - v_2 \tag{16}$$

$$\begin{aligned} L\frac{di_{\rm cm}}{dt} &= v_{c1} - v_{c2} - 2v_{\rm cm} - (1-d_p)v_p + (1-d_n)v_n \\ &= v_{c1} - v_{c2} - 2v_{\rm cm} - 2(1-d_b)v_u + 2d_u v_b. \end{aligned} \tag{17}$$

For the sake of completeness, the derivation subsequently includes a common-mode choke to mitigate common-mode currents. Because a common-mode choke introduces voltages of opposite polarity in the main loop, the differential-mode current remains unaffected by the common-mode choke (16). The common-mode voltage $v_{\rm cm}$ can in turn be expressed as a function of the common-mode current $i_{\rm cm}$ and the common-mode inductance $L_{\rm cm}$, according to (18). Substituting (18) in (17), results in (19)

$$v_{\rm cm} = \frac{L_{\rm cm}}{2}\frac{di_{L1}}{dt} - \frac{L_{\rm cm}}{2}\frac{di_{L2}}{dt} = L_{\rm cm}\frac{di_{\rm cm}}{dt} \tag{18}$$

$$(L+2L_{\rm cm})\frac{di_{\rm cm}}{dt} = v_{c1} - v_{c2} - 2v_u + 2d_b v_u + 2d_u v_b. \tag{19}$$

In steady state, the voltages V_{c1} and V_{c2} across the capacitances then adhere to (20) and (21), respectively

$$V_{c1} = V_b(1 - D_b - D_u) \tag{20}$$

$$V_{c2} = V_b(1 - D_b + D_u). \tag{21}$$

In balanced conditions, $D_u = 0$, the capacitances C_Y share the same voltage $V_b(1-D_b)$, but in unbalanced conditions they start deviating. In case the unbalanced duty cycle increases, V_{c1} drops and V_{c2} rises, which causes the potentials of the dc back end to shift toward the positive pole. The opposite happens when the unbalanced duty cycle D_u is negative.

The common-mode inductor current $i_{\rm cm}$ has tacitly been assumed to be zero before. However, as Figs. 8 and 9 show for modulation scheme 1 and 2, the common-mode inductor current influences inductor currents i_{L1} and i_{L2} and their current ripple. The figures also show that the inductor current ripple of i_{L1} and i_{L2} differs in unbalanced conditions ($D_u \neq 0$). In case $D_u < 0$, V_{c2} and the inductor current ripple of i_{L2} increases, while the inductor current ripple of i_{L1} decreases with V_{c1}. The opposite occurs for $D_u > 0$.

To synthesize, this section demonstrated that the inductor current waveforms i_{L1} and i_{L2} are profoundly altered in the presence of capacitances C_Y, due to EMI capacitors and stray capacitances. In balanced conditions, they increase the inductor current ripple up to a factor 2. In unbalanced conditions, they cause an asymmetry in the inductor current waveforms.

IV. Conversion Loss Model in Unbalanced Conditions

Building further on the decomposition introduced in Section II, this section will derive the conversion loss model of the B-TLC, valid in unbalanced conditions, expressed as a function of the balanced duty cycle D_b and the unbalanced duty cycle D_u. This approach enables to distinguish losses which are unbalance dependent and independent. Furthermore, to evaluate the inductor core losses, the outcomes of Section III will be employed.

The conversion loss model of the B-TLC comprises:

1) conduction losses in the power semiconductor devices P_{Sc};
2) switching losses in the power semiconductor devices P_{Ss};
3) conduction losses in the antiparallel diodes P_D;
4) dc conduction losses in the inductor windings $P_{\rm Ldc}$;
5) ac conduction losses in the inductor windings $P_{\rm Lac}$;
6) core losses in the inductors P_{Lc}.

A. Conduction Losses in the Power Semiconductor Devices

The power semiconductor devices S_1–S_4 conduct current during part of each switching cycle. S_1 and S_4 conduct for a duty cycle D_p and D_n, respectively, while S_2 and S_3 conduct during the complimentary time intervals. As discussed in the previous section, the duty cycles D_p and D_n vary depending on the level of unbalance. According to (4), $D_p = D_b + D_u$ and $D_n = D_b - D_u$.

Hereinafter, MOSFETS are selected as power semiconductor devices. The average conduction losses of MOSFETS depend on

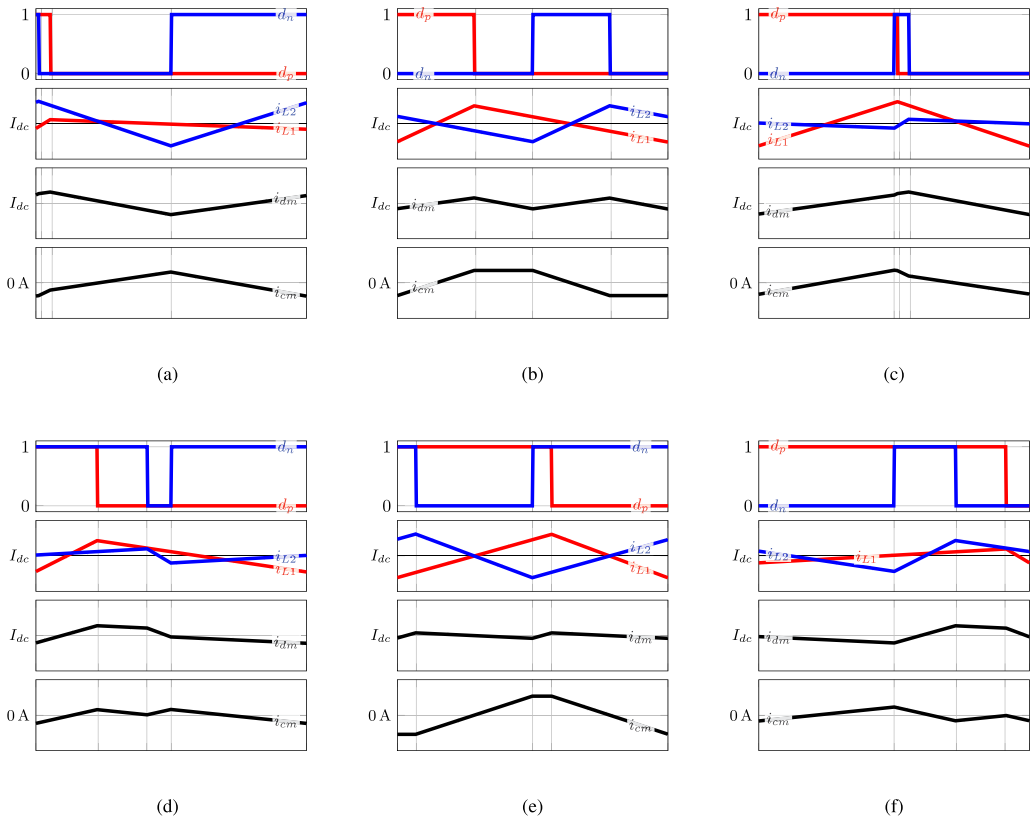


Fig. 8. Inductor current waveforms during a single switching period for varying balanced (D_b) and unbalanced (D_u) duty cycles (modulation scheme 1). (a) $D_b = 0.29$, $D_u = -0.21$. (b) $D_b = 0.29$, $D_u = 0$. (c) $D_b = 0.29$, $D_u = 0.21$. (d) $D_b = 0.57$, $D_u = -0.34$. (e) $D_b = 0.57$, $D_u = 0$. (f) $D_b = 0.57$, $D_u = 0.34$.

their ON-state resistance $R_{\mathrm{ds,on}}$ and the conducted rms current, according to (22)–(25) for the four power semiconductor devices, respectively. In the approximation in the last step of the equation, the instantaneous currents through the power semiconductor devices $i_{S1}(t)$, $i_{S2}(t)$, $i_{S3}(t)$, and $i_{S4}(t)$ can be approximated as pulse-shaped current waveforms of magnitude I_L, in case the additional losses due to the inductor current ripple are negligible

$$P_{Sc1} = R_{\mathrm{ds,on}} \frac{1}{T_s} \int_0^{T_s} i_{S1}(t)^2 dt \approx \begin{cases} 0 & \text{if } I_L < 0 \\ R_{\mathrm{ds,on}}(D_b + D_u) I_L^2 & \text{if } I_L > 0 \end{cases} \tag{22}$$

$$P_{Sc2} = R_{\mathrm{ds,on}} \frac{1}{T_s} \int_0^{T_s} i_{S2}(t)^2 dt \approx \begin{cases} R_{\mathrm{ds,on}}(1 - D_b - D_u) I_L^2 & \text{if } I_L < 0 \\ 0 & \text{if } I_L > 0 \end{cases} \tag{23}$$

$$P_{Sc3} = R_{\mathrm{ds,on}} \frac{1}{T_s} \int_0^{T_s} i_{S3}(t)^2 dt \approx \begin{cases} R_{\mathrm{ds,on}}(1 - D_b + D_u) I_L^2 & \text{if } I_L < 0 \\ 0 & \text{if } I_L > 0 \end{cases} \tag{24}$$

$$P_{Sc4} = R_{\mathrm{ds,on}} \frac{1}{T_s} \int_0^{T_s} i_{S4}(t)^2 dt \approx \begin{cases} 0 & \text{if } I_L < 0 \\ R_{\mathrm{ds,on}}(D_b - D_u) I_L^2 & \text{if } I_L > 0. \end{cases} \tag{25}$$

The total power semiconductor device conduction losses is given by (26). This equation shows that, in case the inductor current waveform approximation is valid, they are independent from the level of unbalance as the unbalanced duty cycle D_u drops out of the equation. In case the inductor current ripple needs to be accounted for, the integral formulation in (22)–(25) should be applied

$$P_{Sc} = P_{Sc1} + P_{Sc2} + P_{Sc3} + P_{Sc4} = \begin{cases} 2R_{\mathrm{ds,on}} D_b I_L^2 & \text{if } I_L \geq 0 \\ 2R_{\mathrm{ds,on}}(1 - D_b) I_L^2 & \text{if } I_L < 0. \end{cases} \tag{26}$$

B. Switching Losses in the Power Semiconductor Devices

Switching losses occur in the power semiconductor devices during device turn-ON and turn-OFF and are governed by (27) [32]. The total switching losses are then given by (28). As two power semiconductor devices conduct current during a switching period the factor $1/2$ drops out of the first term of the equation. Equation (28) shows that the switching losses do

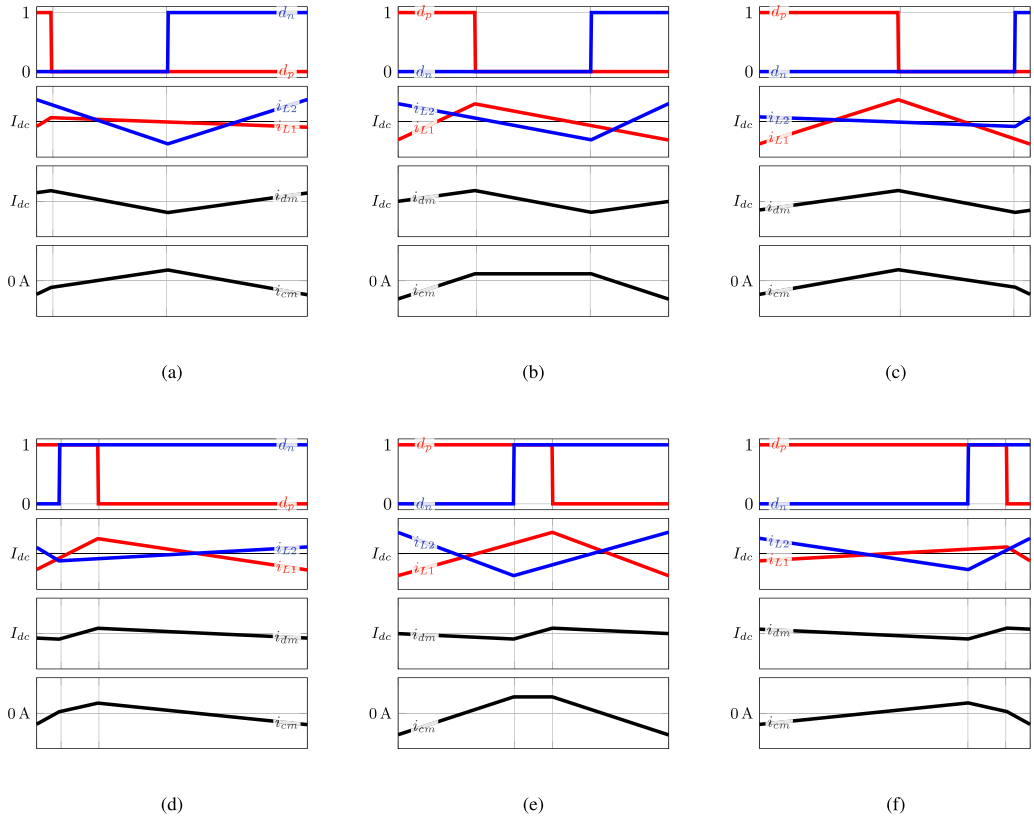


Fig. 9. Inductor current waveforms during a single switching period for varying balanced (D_b) and unbalanced (D_u) duty cycles (modulation scheme 2). (a) $D_b = 0.29$, $D_u = -0.21$. (b) $D_b = 0.29$, $D_u = 0$. (c) $D_b = 0.29$, $D_u = 0.21$. (d) $D_b = 0.57$, $D_u = -0.34$. (e) $D_b = 0.57$, $D_u = 0$. (f) $D_b = 0.57$, $D_u = 0.34$.

not depend on the level of unbalance, but only on the balanced voltage V_b, the inductor current I_L, the switching frequency f_s, the device output capacitance C_{oss} and the device turn-ON and turn-OFF time t_{on} and t_{off}

$$\forall i \in [1,4] : P_{Ssi} = \frac{1}{2} V_b |I_L| (t_{\text{on}} + t_{\text{off}}) f_s + \frac{1}{2} C_{oss} V_b^2 f_s \tag{27}$$

$$P_{Ss} = V_b |I_L| (t_{\text{on}} + t_{\text{off}}) f_s + 2 C_{oss} V_b^2 f_s. \tag{28}$$

C. Conduction Losses in the Antiparallel Diodes

Only two out of four antiparallel diodes D_1 to D_4, accompanying S_1 to S_4, will conduct according to the direction of the inductor current. The conduction losses for each diode adhere to (29)–(32). As the unbalanced duty cycle D_u increases, one diode will conduct for a longer period of time with respect to the other. However, the total diode conduction losses P_D in (33) do not depend on the level of unbalance

$$P_{D1} = \frac{1}{T_s} V_F \int_0^{T_s} i_{D1}(t) dt \tag{29}$$

$$= \begin{cases} (D_b + D_u) V_F |I_L| & \text{if } I_L < 0 \\ 0 & \text{if } I_L \geq 0 \end{cases}$$

$$P_{D2} = \frac{1}{T_s} V_F \int_0^{T_s} i_{D2}(t) dt \tag{30}$$

$$= \begin{cases} 0 & \text{if } I_L < 0 \\ (1 - D_b - D_u) V_F I_L & \text{if } I_L \geq 0 \end{cases}$$

$$P_{D3} = \frac{1}{T_s} V_F \int_0^{T_s} i_{D3}(t) dt \tag{31}$$

$$= \begin{cases} 0 & \text{if } I_L < 0 \\ (1 - D_b + D_u) V_F I_L & \text{if } I_L \geq 0 \end{cases}$$

$$P_{D4} = \frac{1}{T_s} V_F \int_0^{T_s} i_{D4}(t) dt$$

$$= \begin{cases} (D_b - D_u) V_F |I_L| & \text{if } I_L < 0 \\ 0 & \text{if } I_L \geq 0 \end{cases} \tag{32}$$

$$P_D = P_{D1} + P_{D2} + P_{D3} + P_{D4}$$

$$= \begin{cases} 2 D_b V_F |I_L| & \text{if } I_L < 0 \\ 2(1 - D_b) V_F |I_L| & \text{if } I_L \geq 0 \end{cases}. \tag{33}$$

D. DC Conduction Losses in the Inductor Windings

The dc conduction losses in the inductor are given by (34), where R_{Ldc} denotes the inductor dc winding resistance.

These losses are not a function of the level of unbalance

$$P_{\mathrm{Ldc}} = R_{\mathrm{Ldc}} I_L^2. \tag{34}$$

E. Core Losses in the Inductors

The inductor core losses are calculated using the improved generalized Steinmetz equation (iGSE) [33], [34]. The iGSE takes into account the switch-mode triangular-shaped inductor current waveform and further only relies upon the Steinmetz parameters α, β, and k, which are commonly provided by inductor core manufacturers. The inductor core losses per unit volume are expressed in (35). The equation expresses that the core losses per unit volume are obtained by integrating the time-derivative of the magnetic flux density B and the peak-to-peak magnetic flux density ΔB over the switching period T_s. The improved Steinmetz parameter k_i is obtained via (36). The overall inductor core losses P_{Lc} are subsequently obtained by multiplying P_{Lv} by the core volume V_{Lc} as in (37)

$$P_{Lv} = \frac{1}{T_s} \int_0^{T_s} k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha}\, dt \tag{35}$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{36}$$

$$P_{Lc} = V_{Lc} P_{Lv}. \tag{37}$$

The main effort for evaluating (35) lies in calculating the inductor current waveform, as outlined in the previous section, which yields the peak-to-peak magnetic flux density ΔB and the time-derivative of the magnetic flux density $\frac{dB}{dt}$. The magnetic flux density is proportional to the inductor current according to (38), provided the number of windings N and the core properties: Effective magnetic path length l_e and the relative permeability μ_r

$$B = \frac{\mu_r \mu_0\, N}{l_e} i_L(t). \tag{38}$$

F. AC Conduction Losses in the Inductor Windings

The ac conduction losses in the inductor windings are given by (39) [33]. To evaluate (39), the ac winding resistance needs to be determined according to (40), using (41), in order to obtain the skin depth δ. The ac rms current I_{Lac} is given by (42). All symbols and quantities used in the equations are defined in Table I

$$P_{Lac} = R_{Lac} I_{Lac}^2 \tag{39}$$

$$R_{Lac} = \rho \frac{l_w}{\pi r_w^2 - \pi (r_w - \delta)^2} \tag{40}$$

$$\delta = \frac{1}{\sqrt{\pi \sigma \mu_0 f_s}} \tag{41}$$

$$I_{Lac} = \sqrt{\frac{1}{T_s} \int_0^{T_s} (i_L(t) - I_L)^2\, dt}. \tag{42}$$

TABLE I
EFFICIENCY ANALYSIS PARAMETERS

	Parameter	Symbol	Value
Inductor	Inductance	L	$2 \times 700\,\mu\mathrm{H}$
	Core volume	V_c	$51800\,\mathrm{mm}^3$
	Relative permeability	μ_r	60
	Permittivity of free-space	μ_0	$4\pi \cdot 10^{-7}\ \frac{\mathrm{Tm}}{\mathrm{A}}$
	Equivalent length	l_e	$144\,\mathrm{mm}$
	Number of windings	N	60
	Conductor length	l_w	$5.7\,\mathrm{m}$
	Steinmetz Parameter	α	1.43
	Steinmetz Parameter	β	1.585
	Steinmetz Parameter	k	151.44
	Resistivity	ρ	$1.68 \cdot 10^{-8}\,\Omega\mathrm{m}$
	Conductivity	σ	$5.96 \cdot 10^{7}\,\mathrm{S/m}$
	Wire radius	r_w	$1\,\mathrm{mm}$
	DC resistance	R_{Ldc}	$30\,\mathrm{m}\Omega$
CM choke	Inductance	L_{cm}	$6\,\mathrm{mH}$
MOSFET	Switching frequency	f_s	$65\,\mathrm{kHz}$
	Switching period	T_s	$15\,\mu\mathrm{s}$
	On-state resistance	$R_{ds,on}$	$120\,\mathrm{m}\Omega$
	Turn-on time	t_{on}	$46\,\mathrm{ns}$
	Turn-off time	t_{off}	$27\,\mathrm{ns}$
Diode	Forward voltage drop	V_F	$1.5\,\mathrm{V}$

V. SIMULATION RESULTS

In this section, the conversion loss model is applied to the B-TLC depicted in Fig. 1 with parameters listed in Table I. The B-TLC balances v_p and v_n and controls the voltage level at $v_p = v_n = 350$ V. Therefore, it withdraws an amount of power P_2 from the dc back-end voltage source v_2. At the dc front-end (referring to the terminals P, O, and N) load currents i_p and i_n flow, as depicted in the figure. If the amount of power at the positive pole $P_p = v_p i_p$ is equal to the amount of power at the negative pole $P_n = v_n i_n$, the converter operates in balanced conditions. In case of a difference, the B-TLC needs to asymmetrically inject more power in one of the poles relative to the other in order to maintain the front-end voltages balanced. In that case, the B-TLC provides an amount of unbalanced power P_u, which is defined by (43). In the subsequent results, the unbalanced power will always be normalized to the maximum unbalanced power $P_{u,\max}$ that the converter can provide, given by (44)

$$P_u = \frac{P_p - P_n}{2} \tag{43}$$

$$P_{u,\max} = \begin{cases} D_b I_L V_b & \text{if } D_b \le 0.5 \\ (1 - D_b) I_L V_b & \text{if } D_b > 0.5 \end{cases}. \tag{44}$$

Fig. 10 depicts the simulated power conversion losses of the B-TLC, without a common-mode choke included ($L_{\mathrm{cm}} = 0$). The figure depicts a loss breakdown of the B-TLC for varying unbalanced power P_u for $V_2 = 200$ V, $V_2 = 300$ V, and $V_2 = 400$ V. The figure clearly shows that the losses P_{Sc}, P_{Ss}, P_D, and P_{Ldc} are quasi-independent of P_u, while the core losses P_{Lc1} (L_1) and P_{Lc2} (L_2) do significantly depend on P_u. Note that the simulation results include the inductor current ripple in the evaluation of P_{Sc}, P_{Ss}, and P_D, thereby confirming that the inductor current ripple can indeed be neglected in this case as proposed in the previous section. Furthermore, the core losses of L_1 and L_2 differ in unbalanced conditions, because of the

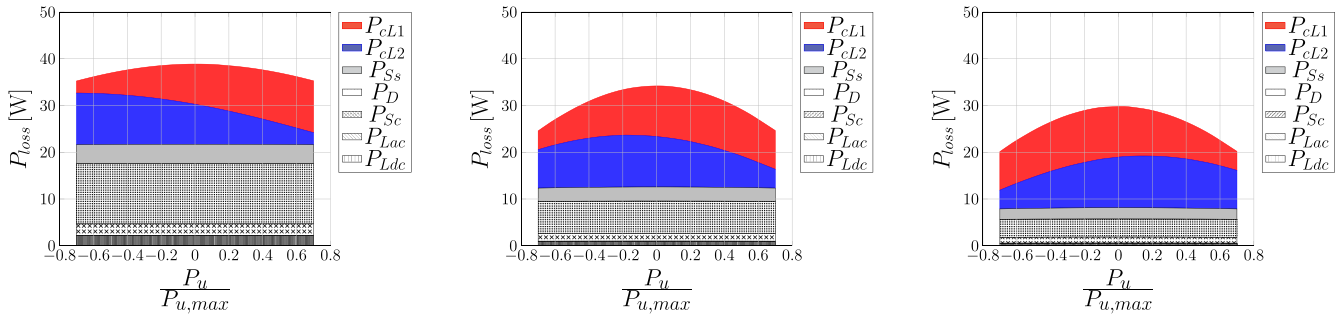


Fig. 10. Power conversion losses without common-mode choke as a function of the unbalanced power for different back-end voltages V_2 ($V_b = 350$ V, $P_2 = 1$ kW). (a) $V_2 = 200$ V. (b) $V_2 = 300$ V. (c) $V_2 = 400$ V.

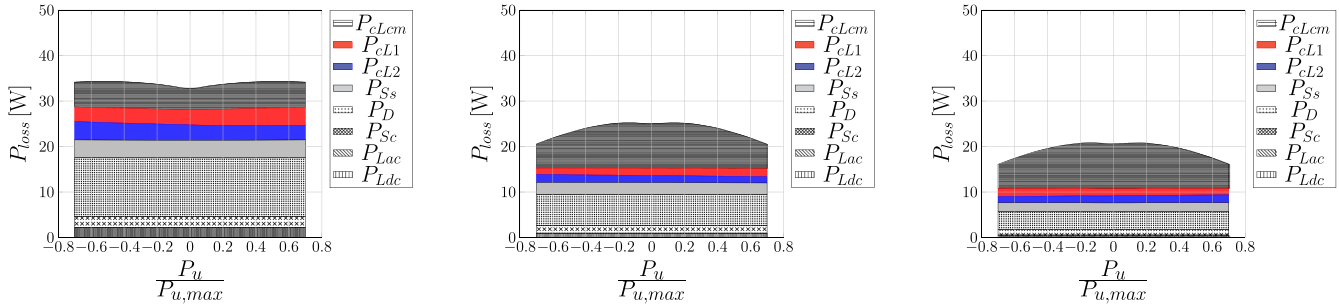


Fig. 11. Power conversion losses with common-mode choke as a function of the unbalanced power for different back-end voltages V_2 ($V_b = 350$ V, $P_2 = 1$ kW). (a) $V_2 = 200$ V. (b) $V_2 = 300$ V. (c) $V_2 = 400$ V.

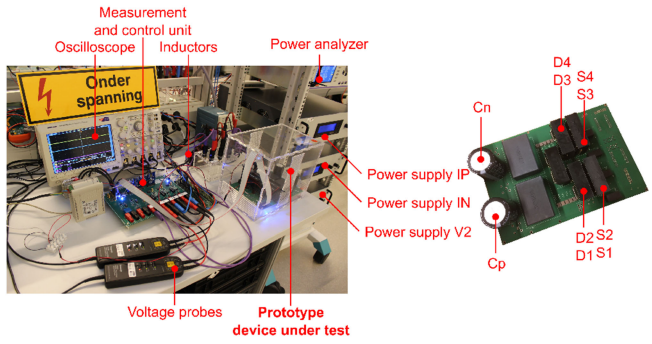


Fig. 12. Converter prototype and lab setup.

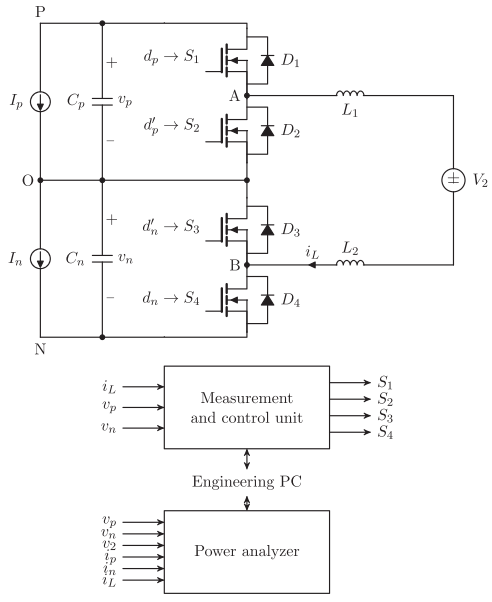


Fig. 13. Schematic overview of the lab setup.

capacitances C_Y, included in the simulations. As explained in the Section III, this loss asymmetry is due to the differing inductor current ripple arising in unbalanced conditions. Below $D_b < 0.5$, the ripple on i_{L1} (i_{L2}) increases (decreases) with D_u, while beyond $D_b > 0.5$ the opposite applies. Remarkably, the overall core losses reduce in unbalanced conditions, as the reduction of the core losses in one inductor offsets the increase in the other inductor. Therefore, the overall conversion losses decrease in unbalanced conditions, which is counterintuitive.

To mitigate the common-mode inductor currents, a common-mode (CM) choke L_{cm} is added. Introducing a common-mode choke reduces the common-mode currents to almost zero and the inductor current ripple in i_{L1} and i_{L2}. Accordingly, i_{L1} and i_{L2} are nearly equal and incur the same amount of core losses,

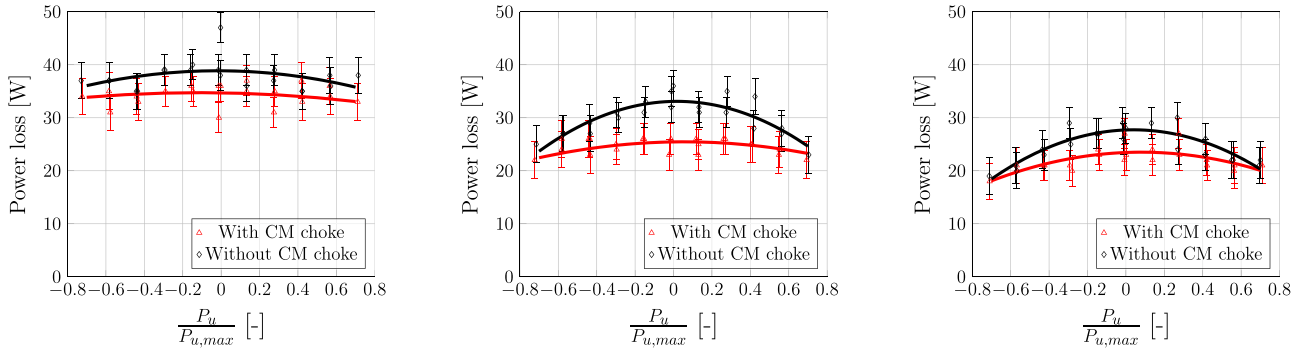


Fig. 14. Power conversion losses of the buck three-level dc–dc converter as a function of the unbalanced power for different back-end voltages V_2 ($V_b = 350$ V, $P_2 = 1$ kW). (a) $V_2 = 200$ V. (b) $V_2 = 300$ V. (c) $V_2 = 400$ V.

which in total is lower than without common-mode choke. The asymmetry in the core losses is therefore no longer visible in Fig. 11. However, core losses P_{cLcm} occur in the common-mode choke, again calculated using (37) and depicted in Fig. 11. These core losses depend on the level of unbalance, as recognized in the figure. Although the overall core losses of L_1 and L_2 strongly decrease with a common-mode choke, the decrease is offset by additional losses in the common-mode choke. Nevertheless, the total power conversion losses decrease by including a common-mode choke.

If the effect of common-mode currents arising due to the C_Y capacitances would not be accounted for, the loss distribution with common-mode choke would apply, without taking into account the losses arising in the common-mode choke. Disregarding the common-mode choke core losses, the total power conversion losses would be constant and not depend on the level of unbalance. Furthermore, the losses would be underestimated for this particular case by $25-60\%$ if C_Y capacitances would be present in practice, but not simulated.

Finally considering the unbalance independent losses, the switching losses and the diode conduction losses dominate. These losses remain unaffected by the introduction of a common-mode choke. The lowest dc back-end voltage $V_2 = 200$ V [Fig. 10(a)], results in the highest conduction and switching losses.

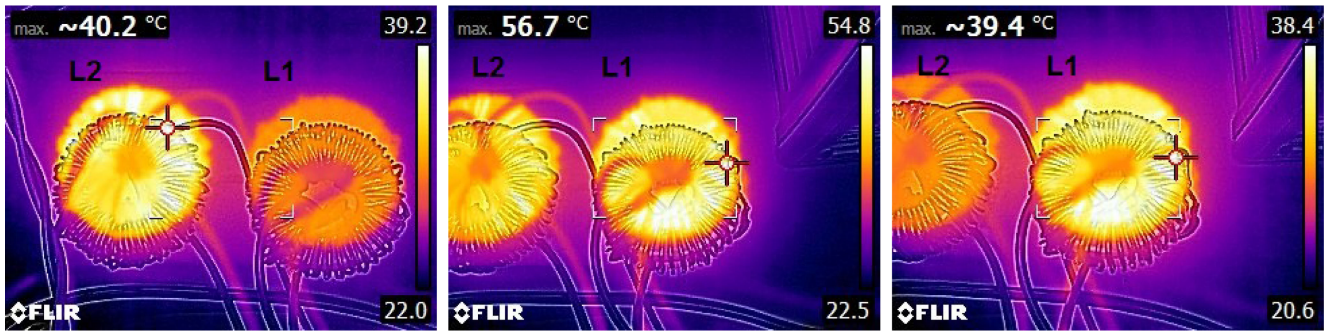
VI. Experimental Results

In this section, to validate the conversion loss model in unbalanced conditions, a 1-kW converter prototype has been realized, as depicted in Fig. 12. The converter prototype printed circuit board is depicted on the right side and contains the dc bus capacitors C_p and C_n, as well as the power semiconductor devices $S1$–$S4$ and antiparallel diodes $D1$–$D4$. The converter prototype is part of the lab setup depicted on the left side of the figure. The converter prototype is controlled by a custom measurement and control unit which measures the voltages v_p, v_n, and v_2 and the inductor current i_L. The measurement and control unit contains a Texas Instruments F28379 Digital Signal Processor, programmed to control the converter prototype. The controller adjusts the pulsewidth modulation signals sent to the converter in order to balance and control the pole-to-neutral voltages at $V_b = 350$ V, such that ± 350 V appears at the front-end terminals of the converter. At the converter terminals, three power supplies are connected, as indicated in the schematic overview in Fig. 13.

- I_p powers the positive side of the dc front end and is connected between terminal P and O. The power supply operates in constant current mode.
- I_n powers the negative side of the dc front end and is connected between terminal O and N. The power supply operates in constant current mode.
- V_2 powers the dc back-end and operates in constant voltage mode.

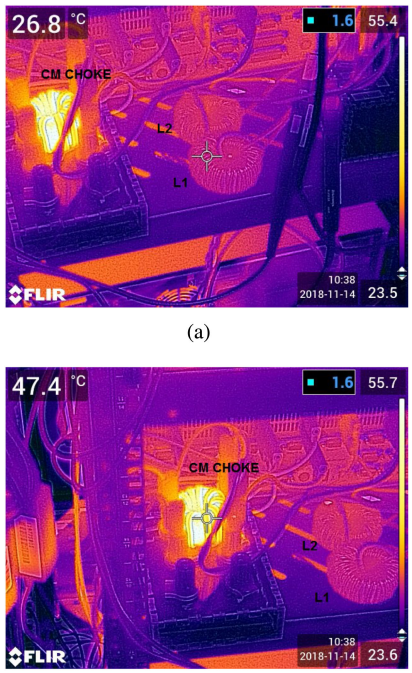
Figs. 12 and 13 also depict the power analyzer included in the setup to measure power conversion losses. The power analyzer records the power sinked by the dc backend V_2 and the power sourced by I_p and I_n. All signals are collected on the engineering PC which also sends voltage set-points to the measurement and control unit.

Fig. 14 depicts the power conversion losses at $P_2 = 1$ kW for $V_2 = 200$ V, $V_2 = 300$ V, and $V_2 = 400$ V, with and without common-mode choke. According to the simulation results, the experimental results indicate that the power conversion losses decrease in unbalanced conditions, both with and without common-mode choke. However, with common-mode choke, the power conversion losses depend less on the level of unbalance. Furthermore, the inductor current waveforms i_{L1} and i_{L2} in Fig. 18 are not equal due to common-mode currents. These common-mode currents are caused by EMI filters in the dc back-end power supply. By adding a common-mode choke, the figure shows that these common-mode currents are mitigated and that i_{L1} and i_{L2} are aligned and feature lower ripple magnitudes. The asymmetry in the inductor core losses furthermore appears from infrared thermal images of L_1 and L_2 presented in Fig. 15. A clear temperature difference exists in unbalanced conditions and the average temperature of the inductors decreases by 19 °C in unbalanced conditions. If a common-mode choke is included, as visible on the infrared thermal images in Fig. 16, the common-mode choke adds to the losses, but the



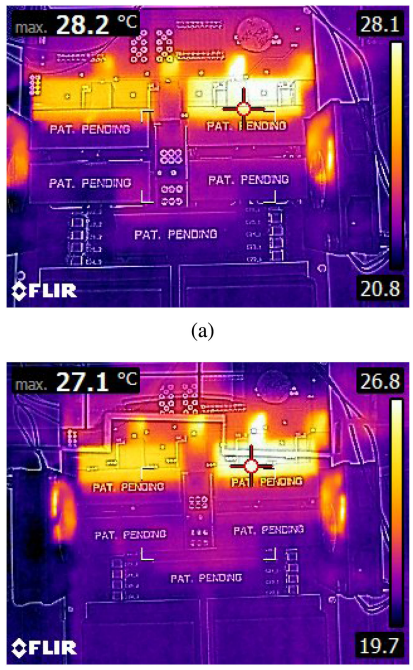
(a) (b) (c)

Fig. 15. Infrared thermal camera images of the inductors L_1 and L_2 in unbalanced conditions without common-mode choke ($P_2 = 1$ kW, $V_2 = 200$ V). (a) $P_u/P_{u,\max} = -0.7$ ($T_{L1} = 33\,^\circ$ C, $T_{L2} = 40\,^\circ$ C). (b) $P_u/P_{u,\max} = 0$ ($T_{L1} = 57\,^\circ$ C, $T_{L2} = 54\,^\circ$ C). (c) $P_u/P_{u,\max} = 0.7$ ($T_{L1} = 39\,^\circ$ C, $T_{L2} = 33\,^\circ$ C).



(a) (b)

Fig. 16. Infrared thermal camera images of the inductors L_1 and L_2 in balanced conditions with the common-mode (CM) choke ($P_2 = 1$ kW, $V_2 = 200$ V). (a) $P_u/P_{u,\max} = 0$ ($T_{L1} = T_{L2} = 27\,^\circ$ C, $T_{\rm CM} = 47\,^\circ$ C). (b) $P_u/P_{u,\max} = 0$ ($T_{L1} = T_{L2} = 27\,^\circ$ C, $T_{\rm CM} = 47\,^\circ$ C).



(a) (b)

Fig. 17. Infrared thermal camera images of the power semiconductor devices without common-mode choke ($P_2 = 1$ kW, $V_2 = 200$ V). (a) $P_u/P_{u,\max} = 0$ ($T_{S1} = T_{S2} = 28.2\,^\circ$C, $T_{S3} = T_{S4} = 27.8\,^\circ$C). (b) $P_u/P_{u,\max} = 0.7$ ($T_{S1} = T_{S2} = 27.1\,^\circ$C, $T_{S3} = T_{S4} = 26.4\,^\circ$ C).

average temperature of the inductors drops appreciably from 57 to 27 °C (−53%). Finally, Fig. 17 depicts the temperature of the power semiconductor devices at $P_u/P_{u,\max} = 0$ and at $P_u/P_{u,\max} = 0.7$. These infrared thermal images show that the power semiconductor device temperatures slightly shift with the level of unbalance, but remain constant overall with respect to the level of unbalance.

VII. Conclusion

This article derived a conversion loss model for the buck three-level dc–dc converter, which is valid in both balanced and unbalanced operating conditions experienced in bipolar dc microgrids. In order to study to which extent loss components depend on the level of unbalance, the conversion loss model has been decomposed into balanced and unbalanced components. The decomposition revealed that the conduction and switching losses occurring in the power semiconductor devices shift as a function of the level of unbalance, but that they remain constant overall, in case the losses associated with the inductor current ripple are minor relative to the losses associated with the average inductor current. Moreover, the model explicitly accounted for nonideal common-mode inductor currents, arising due to capacitive coupling between the dc back end and the positive and the negative pole. On the one hand, the theoretical and experimental analysis revealed that common-mode inductor currents result in

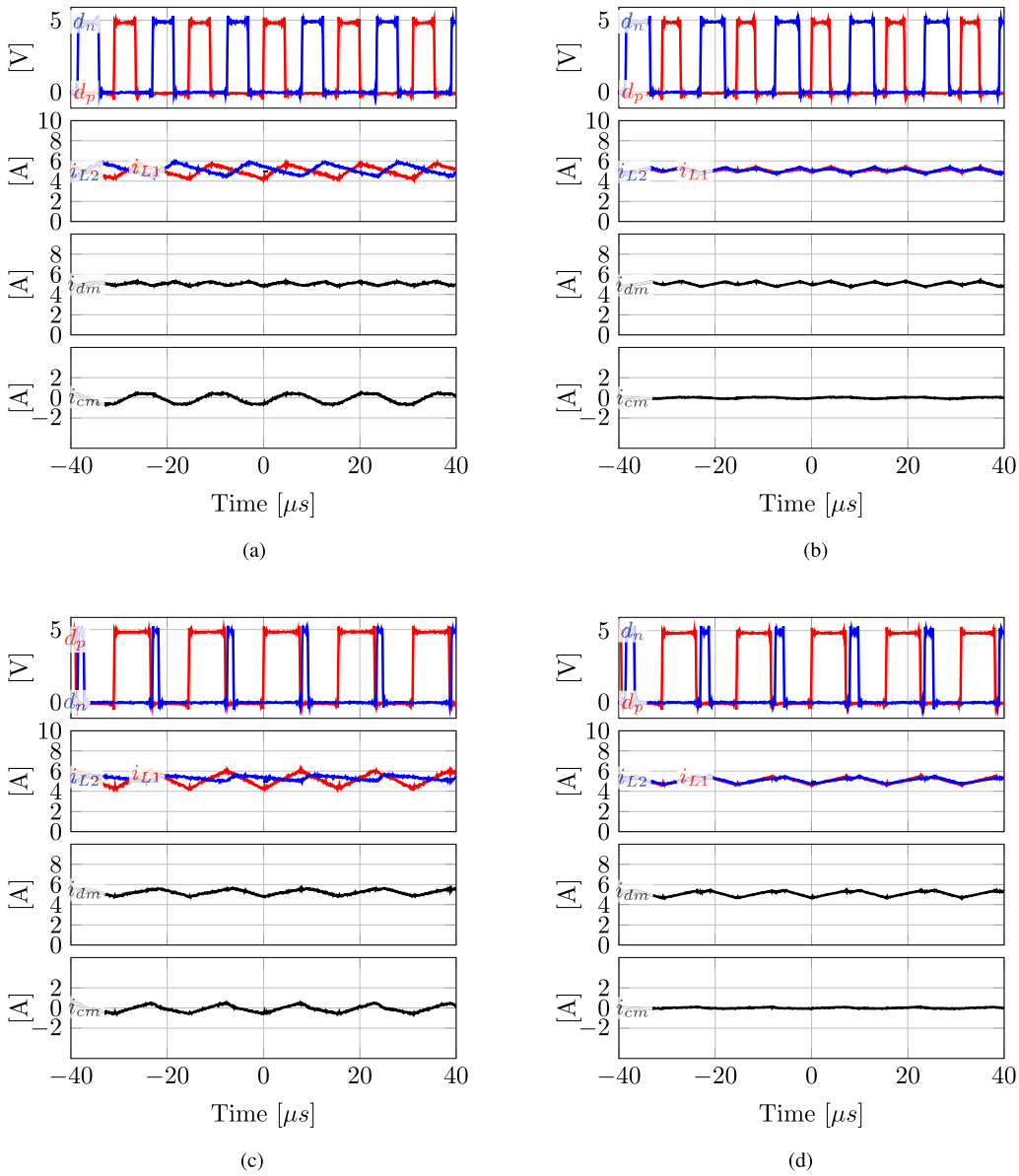


Fig. 18. Inductor current waveforms in unbalanced conditions ($P_2 = 1$ kW, $V_2 = 200$ V). (a) Without common-mode choke $P_u/P_{u,\max} = 0$. (b) With common-mode choke $P_u/P_{u,\max} = 0$. (c) Without common-mode choke $P_u/P_{u,\max} = 0.7$, $D_u = 0.21$. (d) With common-mode choke $P_u/P_{u,\max} = 0.7$, $D_u = 0.21$.

higher levels of inductor current ripple, which in turn lead to higher conversion losses. On the other hand, the inductor current waveforms and the associated core losses became asymmetrical in unbalanced conditions, which was also experimentally confirmed by the differing core temperatures. This loss asymmetry remarkably lead to lower overall conversion losses in unbalanced conditions, confirmed by the model and by experiments performed on a 1-kW converter prototype. Not considering common-mode inductor currents lead in the studied case to a loss underestimation of 25 – 60% and would render the conversion losses independent of the level of unbalance. Finally, in order to mitigate the undesired common-mode inductor currents, a common-mode choke has been included in the model and in the experimental analysis. Although the common-mode choke introduced additional conversion losses, the inductor core losses decreased significantly, yielding overall lower power conversion losses depending less on the level of unbalance.

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