An Analysis of the Thermal Interaction Between Components in Power Converter Applications

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***Abstract*—Accurately predicting the temperature of semiconductor devices is very important in the initial design of the power electronics converter. *RC* thermal models derived from the well-known methods have some ability to predict the temperature. However, the accuracy is boundary condition specific; hence, these methods cannot be used in the reliability analysis. To make the thermal model more accurate and robust, the factors contributing to discrepancies need to be analyzed carefully. These are power-module-materials' nonlinear properties, thermal grease layer, and the cooling system (i.e., liquid-cooled cold plate). In this article, the estimation of accurate *RC* parameters from the FEA thermal model is demonstrated in COMSOL. The electrical model having temperature-dependent power loss model is coupled to a refined thermal model and solved in a circuit simulator, PLECS. The proposed method is applied in two applications: assessing thermal interaction between IGBTs and antiparallel diodes in a half-bridge power module and assessing thermal interaction among the discrete switches in an interleaved bidirectional dc–dc converter. Results show that the impact of material nonlinearity, thermal grease layer, and cooling boundary conditions are significant for accurate prediction of IGBT and diode temperatures. The proposed model is consistent with FEA results and differs by 2%–6.5% compared with the experimental results.**

***Index Terms*—Circuit simulator, dc–dc converter, electrothermal model, finite-element analysis (FEA), IGBT power module.**

I. Introduction

POWER electronic converters that contain multichip power modules are widely used in applications, such as hybrid electric vehicles, automotive hybrid traction, or wind power energy conversion. In many of these applications, converters are required to handle high current and/or voltage and have to deliver power to a variable load efficiently and reliably in a harsh environment [1]–[3]. Significant improvement in semiconductor technology has accelerated the power handling capability of the converters but the design, manufacturing, and applications of these converters have to meet some new challenges, such as the stringent reliability requirements for semiconductor devices—IGBT modules, MOSFET, and diodes. Because of the changes in mission profile, large time-varying losses are produced in the power semiconductor devices and that results in high-temperature variations and degradation in the devices [4]. The failure modes in IGBT modules include bond-wire lift-off and solder fatigue, which is mainly determined by the change of the junction temperatures. Thus, detailed knowledge about the temperature behaviors of power electronic components are of great interest in the emerging field of power electronics applications, i.e., automotive hybrid traction, where the amount of power to be managed is in the order of tens of kilowatts and temperatures can exceed 100 °C [5].

Coupling the thermal model and temperature-dependent power loss models creates the basis for the electrothermal analysis of power electronic systems. There are several methods commonly used for thermal analysis. These include numerical approaches, such as computational fluid dynamics (CFD), finite-element analysis (FEA), analytical analysis, and lumped equivalent thermal resistor–capacitor (*RC*) network analysis. Numerical methods, such as FEA [6], [7] or CFD [8], are time-consuming and, therefore, not suitable for the estimation of junction temperature history for long-time load profiles. The analytical approach solves the 1-D, 2-D, and 3-D heat diffusion equations [9]–[11] and this meshless method is faster but it is only applicable for simplified structures and it has limited accuracy when modeling the heat convection between the heatsink and the coolant. Moreover, the conventional *RC*-type thermal network is faster in estimating junction temperature only. Accuracy is limited due to neglecting thermal couplings between the chips or also in the critical layers of materials in IGBT.

A well-known method of impedance determination is usually a synthesis of transient thermal impedance matrix, which is based on the step power applying on chips and recording temperatures on chips. This can be either conducted by finite-element simulations [6], [7] or by experiments [12], [13]. So far, the FEA thermal models are solved at fixed baseplate boundary

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temperatures or simplified convective boundary conditions. The impact of the thermal grease layer and cooling system is still not well studied. The experimental method involves test rig and complex hardware circuitry to perform temperature measurement. The best possible measurements can be performed to capture case temperatures by embedding either thermistors or thermocouple and IR camera [10], [14]. The synthesized *RC* network model that is based on the mathematical fitting of the measured two-end temperature profile allows a designer only to estimate chip junction temperature. Therefore, it cannot be used in determining temperatures at critical locations such as chip solder and baseplate solder.

The typical thermal *RC*-lumped network in the form of either Foster [15] or Cauer [16] network is available for a single-chip or multichip power module. For the multichip IGBT module, the Foster network is easy to construct using state-of-the-art thermal impedance measurement equipment but it is physically insignificant due to the incapability of providing the internal node temperature in the structure. Cauer network is physically significant when its parameters are derived from the geometry of IGBT-module layers and material properties. The conventional Cauer method assumes one lump in thick layers that affects the transient performance. However, for multichip IGBT module, because of the 3-D heat, spreading accurate mapping of thermal spreading on the thick layers (e.g., ceramic layer and baseplate layer) is extremely challenging [17]. The accuracy of Cauer network parameters for a multichip IGBT module is limited due to uncertainties regarding thermal interfacing and heatsinks in different systems.

In the conventional Foster and Cauer networks, the *RC* parameters are constant, which is not accurate as the behaviors of components are temperature dependent [18]–[25]. However, boundary-condition-dependent variable *RC* parameters can increase the accuracy of these models [26]. A new approach for estimating the *RC* parameters of the Cauer network using the junction temperature cooling curve has recently been presented that does not require power loss information [27]. However, the work focuses only on a single IGBT chip and ignores thermal coupling that might affect the complex heat spreading behavior from baseplate to liquid-cooled cold plate in a multichip module.

Although some thermal models [28]–[31] take into account the thermal interactions between the IGBT chips in a power module, they only provide junction temperature profile instead of the temperature profile in the critical layers of IGBT module, i.e., chip solder and baseplate solder, which are needed for reliability analysis, such as solder cracking.

Adaptive thermal models are implemented in a real-time system in estimating the junction temperature as a part of health monitoring and further used in analyzing the aging process of an IGBT module [32], [33]. A new lookup table based thermal model considering the changes in case temperatures due to aging is proposed in [34] instead of using a simplified 1-D average case temperature. The model is difficult to tune with changing boundary conditions and does not predict the temperature at critical locations of the module. In a simplified thermal coupling impedance model, Bahman *et al.* [35] considered the thermal coupling between two adjacent chips instead of taking all the chips into consideration. However, the authors did not consider the thermal grease layer in their module structure and the temperature dependence of the materials was neglected.

In the literature, no lumped *RC* model of the multichip IGBT module is found, which takes into account both material nonlinearity and variable boundary conditions at the cold plate. An important contribution of the article is that the presented thermal model is extended to the cooling system as the IGBT module is usually mounted on a liquid-cooled cold plate. The impact of not modeling the real cooling system might have a significant impact on the estimated *RC* parameters.

The novelty of the article can be summarized in the following points:

1) demonstration of accurate lumped *RC* Foster network derived from FEA thermal simulations of IGBT module and considering physical geometry, material's temperature dependence, thermal grease layer, and cooling system;
2) development of the temperature-dependent loss model and its coupling with the new *RC* network model;
3) introduction of nonlinear cooling boundary condition into the thermal model;
4) accurate prediction of temperatures at predefined nodes in a specific layer of the module.

In this article, a component thermal interaction model for a half-bridge IGBT module considering all IGBTs and diodes is developed by extracting the thermal model parameters from FEA simulations. The integration of the electrical model and the thermal model is done using the PLECS circuit simulator and the effect of thermal coupling is analyzed. The accuracy of the modeling method is also validated against the experimental results from a 12 to 48 V, 1.5 kW dc–dc converter.

The rest of this article is organized as follows. Section II describes the modeling framework, the component thermal interaction, and parameter synthesis from the FEA simulations. Section III investigates the efficacy of the model for two converter applications. Finally, Section IV draws some conclusions.

II. Methodology

A. Modeling Framework

The electrothermal analysis modeling framework is shown in Fig. 1. It consists of a circuit simulator (PLECS) and an FEA software package (COMSOL). PLECS is used to model the electrical behavior of the power converter, i.e., predicting the power losses of the converter as well as solving the derived thermal *RC* network. The modeling can be initiated by using PLECS or analytical models to calculate the power losses. The power losses are then used as heat source inputs in COMSOL for FEA thermal analysis of the components in the power electronics system under study. Based on the detailed transient temperature distribution and history in COMSOL, an enhanced *RC* network model is proposed for semiconductor devices.

B. Power Modules in an Inverter

The thermal behaviors of a half-bridge module have been analyzed using the modeling framework described above. Each

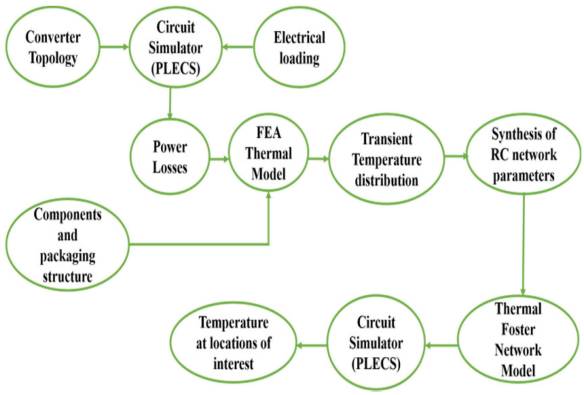


Fig. 1. Electrothermal modeling method.

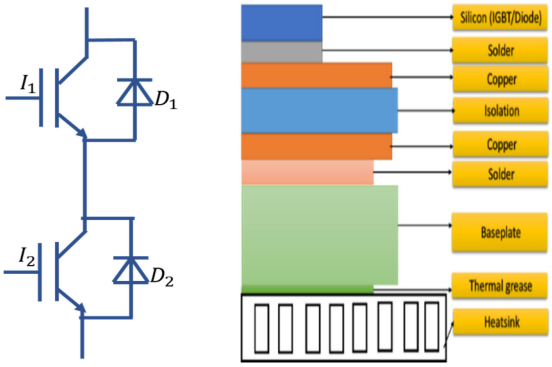


Fig. 2. (a) Schematic of a half-bridge IGBT power module. (b) Simplified cross-sectional view of an IGBT switch.

module consists of two IGBTs and two antiparallel diodes [see Fig. 2(a)]. The IGBT module is assumed to be 1200 V/75 A Semikron's SKM75GB123D [31]. The IGBT and diode chips are bonded on an aluminum oxide substrate-based direct-bond copper, which is soldered on a copper baseplate. To improve physical integrity and heat transfer, thermal interface material (TIM) (e.g., thermal grease) is applied between the baseplate and the liquid-cooled heatsink. The half-bridge circuit schematic and the cross section of the IGBT power module are shown in Fig. 2. The material properties obtained from the article presented in [31] are used in this article.

C. Modeling of Thermal Interaction: RC Parameter Extraction

The thermal interaction between the components can be analyzed using an *RC* network method. In order to extract the *RC* parameters for the *RC* Foster cells network, the thermal impedance between two thermal nodes along the thermal path of interest is needed. The extraction process of *RC* thermal parameters using FEA transient thermal responses has been demonstrated in [30] and [35]. The process uses the transformed thermal impedance responses. In this article, FEA has been conducted four times to obtain the thermal responses due to self-heating and cross

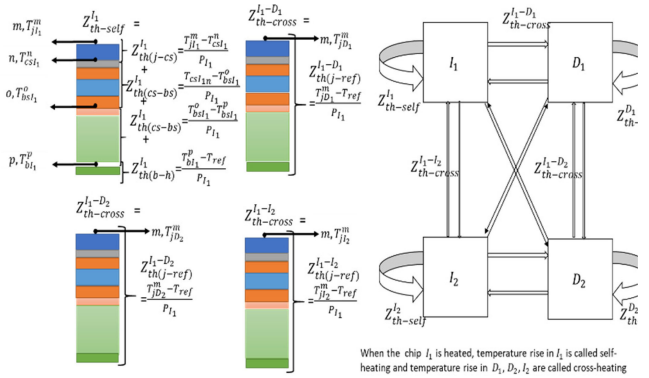


Fig. 3. Total IGBT self-heating and diode cross-heating thermal impedances and the impedances for the material layers.

heating in the two IGBT-diode pairs. IGBT1, diode1, IGBT2, and diode2 are labeled here as I_1, D_1, I_2, and D_2.

In the first simulation, only I_1 is considered to be active, i.e., no loss in the other three devices and in the second only D_1 is considered to be active. Similarly, in the third and fourth simulations, only I_2 and only D_2 are considered to be active, respectively. The self-heating and cross-heating thermal impedance at selected thermal network nodes are derived from these FEA simulation results. The selected nodes correspond to the locations at the centers of the selected material interfaces as well as the top and bottom of the whole structure. The nodes that correspond to the top of the chip, the interface of chip and chip solder, the interface of substrate solder and baseplate, and the bottom of the baseplate are denoted by letters "m," "n," "o," and "p," respectively (see Fig. 3). For the impedances (Z), upper subscripts "I" and "D" symbolize IGBT and diode, respectively. In the following, the lower subscripts "j," "cs," "bs," and "b," respectively, denote the junction, chip solder, baseplate solder, and the baseplate layers. The temperatures at these selected locations for I_1, D_1, I_2, and D_2 in simulation 1 are $T^m_{jI_1}$, $T^n_{csI_1}$, $T^o_{bsI_1}$, $T^p_{bI_1}$, $T^m_{jD_1}$, $T^m_{jI_2}$, and $T^m_{jD_2}$, respectively. Only junction temperatures are considered for investigating cross heating from D_1, I_2, and D_2 in simulation 1.

D. Thermal Impedance Network With Self- and Cross-Heating

Considering the linear-time invariant assumption of heat transfer in multichip, the junction temperature in the multichip power module can be estimated by forming the thermal impedance matrix as follows:

$$\begin{bmatrix} T_{jI_1} \\ T_{jD_1} \\ T_{jI_2} \\ T_{jD_2} \end{bmatrix} = \begin{bmatrix} Z^{I_1}_{\text{th-self}} & Z^{I_1-D_1}_{\text{th-cross}} & Z^{I_1-I_2}_{\text{th-cross}} & Z^{I_1-D_2}_{\text{th-cross}} \\ Z^{D_1-I_1}_{\text{th-cross}} & Z^{D_1}_{\text{th-self}} & Z^{D_1-I_2}_{\text{th-cross}} & Z^{D_1-D_2}_{\text{th-cross}} \\ Z^{I_2-I_1}_{\text{th-cross}} & Z^{I_2-D_1}_{\text{th-cross}} & Z^{I_2}_{\text{th-self}} & Z^{I_2-D_2}_{\text{th-cross}} \\ Z^{D_2-I_1}_{\text{th-cross}} & Z^{D_2-D_1}_{\text{th-cross}} & Z^{D_2-I_2}_{\text{th-cross}} & Z^{D_2}_{\text{th-self}} \end{bmatrix} * \begin{bmatrix} P_{I_1} \\ P_{D_1} \\ P_{I_2} \\ P_{D_2} \end{bmatrix} + \begin{bmatrix} T_{\text{ref}} \\ T_{\text{ref}} \\ T_{\text{ref}} \\ T_{\text{ref}} \end{bmatrix} \quad (1)$$

TABLE I
LIST OF THERMAL IMPEDANCES

Symbols	Meaning
$Z^{I_1}_{th(j-cs)}, Z^{D_1}_{th(j-cs)}, Z^{I_2}_{th(j-cs)}, Z^{D_2}_{th(j-cs)}$	Self-heating impedance of IGBT1 ,Diode1, IGBT2and Diode2 between junction and chip solder
$Z^{I_1}_{th(cs-bs)}, Z^{D_1}_{th(cs-bs)}, Z^{I_2}_{th(cs-bs)}, Z^{D_2}_{th(cs-bs)}$	Self-heating impedance of IGBT1 ,Diode1, IGBT2 and Diode2 between chip solder and baseplate solder
$Z^{I_1}_{th(bs-b)}, Z^{D_1}_{th(bs-b)}, Z^{I_2}_{th(bs-b)}, Z^{D_2}_{th(bs-b)}$	Self-heating impedance of IGBT1 ,Diode1, IGBT2and Diode2 between baseplate solder and baseplate
$Z^{I_1}_{th(b-h)}, Z^{D_1}_{th(b-h)}, Z^{I_2}_{th(b-h)}, Z^{D_2}_{th(b-h)}$	Self-heating impedance of IGBT and Diode between baseplate and heatsink

where T_{jI_1}, T_{jD_1}, T_{jI_2}, and T_{jD_2} are the junction temperatures in I_1, D_1, I_2, and D_2, respectively, $Z^{I_1}_{\text{th-self}}$, $Z^{D_1}_{\text{th-self}}$, $Z^{I_2}_{\text{th-self}}$, and $Z^{D_2}_{\text{th-self}}$ are the total self-heating impedances of I_1, D_1, I_2, and D_2, respectively, $Z^{I_1-D_1}_{\text{th-cross}}$, $Z^{I_1-I_2}_{\text{th-cross}}$, $Z^{I_1-D_2}_{\text{th-cross}}$, $Z^{D_1-I_1}_{\text{th-cross}}$, $Z^{D_1-I_2}_{\text{th-cross}}$, $Z^{D_1-D_2}_{\text{th-cross}}$, $Z^{I_2-I_1}_{\text{th-cross}}$, $Z^{I_2-D_1}_{\text{th-cross}}$, $Z^{I_2-D_2}_{\text{th-cross}}$, $Z^{D_2-I_1}_{\text{th-cross}}$, $Z^{D_2-D_1}_{\text{th-cross}}$, and $Z^{D_2-I_2}_{\text{th-cross}}$ are the total cross-heating thermal impedances of I_1-D_1, I_1-I_2, I_1-D_2, D_1-I_1, D_1-I_2, D_1-D_2, I_2-I_1, I_2-D_1, I_2-D_2, D_2-I_1, D_2-D_1, and D_2-I_2, respectively, P_{I_1}, P_{D_1}, P_{I_2}, and P_{D_2} are the power losses in I_1, D_1, I_2, and D_2, respectively, and T_{ref} is the reference temperature of the liquid-cooled heatsink.

The self-heating impedances of the IGBT1, diode1, IGBT2, and diode2 can be expressed by (2)–(5) and the cross-coupling impedances can be represented as a simplified form of the junction to reference equivalent impedance. Details of the impedances are provided in Fig. 3 and Table I

$$Z^{I_1}_{\text{th-self}} = Z^{I_1}_{\text{th}(j-cs)} + Z^{I_1}_{\text{th}(cs-bs)} + Z^{I_1}_{\text{th}(bs-b)} + Z^{I_1}_{\text{th}(b-h)} \tag{2}$$

$$Z^{D_1}_{\text{th-self}} = Z^{D_1}_{\text{th}(j-cs)} + Z^{D_1}_{\text{th}(cs-bs)} + Z^{D_1}_{\text{th}(bs-b)} + Z^{D_1}_{\text{th}(b-h)} \tag{3}$$

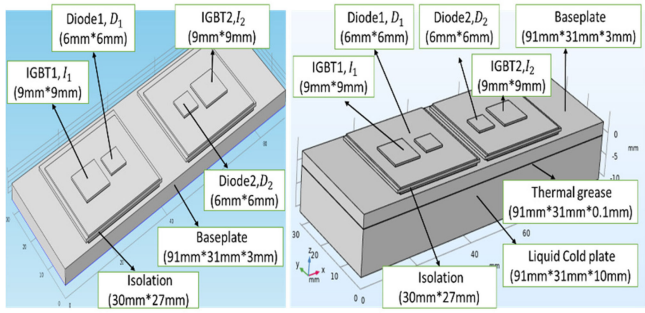
$$Z^{I_2}_{\text{th-self}} = Z^{I_2}_{\text{th}(j-cs)} + Z^{I_2}_{\text{th}(cs-bs)} + Z^{I_2}_{\text{th}(bs-b)} + Z^{I_2}_{\text{th}(b-h)} \tag{4}$$

$$Z^{D_2}_{\text{th-self}} = Z^{D_2}_{\text{th}(j-cs)} + Z^{D_2}_{\text{th}(cs-bs)} + Z^{D_2}_{\text{th}(bs-b)} + Z^{D_2}_{\text{th}(b-h)}. \tag{5}$$

The extraction process of the *RC* network parameters from the FEA-simulated transient thermal impedance responses is described in detail in Section III.

E. FEA and Thermal Impedance Curves

Two FEA thermal models are constructed in COMSOL. The first one, as shown in Fig. 4(a), considers the IGBT module without thermal grease and liquid cold plate, while the second one, as shown in Fig. 4(b), considers the IGBT module extended to liquid cold plate through the thermal grease layer. The following assumptions are made in solving FEA thermal models.



(a) (b)

Fig. 4. Internal structure of power module in FEA software. (a) Without liquid cold plate. (b) With liquid cold plate.

TABLE II
DIMENSION AND MATERIAL PROPERTIES OF THE IGBT MODULE

Material	Density $\rho, kg/m^3$	Temperature T, °C	Specific heat capacity c, $J/(kg.K)$	Thermal Conductivity $k, W/(m.K)$
IGBT (Si)	2329	25	705	148
Diode (Si)		75	757.7	119
		125	788.3	98.9
		225	830.7	76.2
		325	859.9	61.9
Solder1 Solder2	9000	All	150	35
Copper layer1(Cu)	8700	25	385	401
		75	392.6	396
Copper layer2(Cu)		125	398.6	393
		225	407.7	386
Baseplate(Cu)		325	416.7	379
Isolation	3260	All	740	100
Thermal grease	1180	All	1044	1

1) All sides are kept adiabatic conditions except the top surface of chips and bottom of the either baseplate or cold plate.
2) Convective boundary conditions are applied at the bottom of the either baseplate or cold plate,
3) The liquid-cooled cold plate material is made up of aluminum and coolant is ethylene glycol and water mix (50%/50%).
4) The reference coolant temperature is assumed to be constant.

In order to derive the thermal impedance values at selected layers, transient FEA simulations were performed four times in which the power loss of either the IGBTs or the diodes was used as the only heat source in the studied structure, as shown in Fig. 4(a). The material properties used in this FEA model are listed in Table II. The power loss values were considered 110 W and 60 W for the IGBT and the diode, respectively, which are adapted from the article presented in [31]. These power loss values are chosen to benchmark the thermal model by comparing the thermal resistance value with the thermal resistance reported in [31]. The loss was applied at the top surface of the IGBT/diode chips. It is assumed that the module is mounted on a liquid-cooled cold plate through the thermal grease layer, and in this simulation, a convective heat transfer

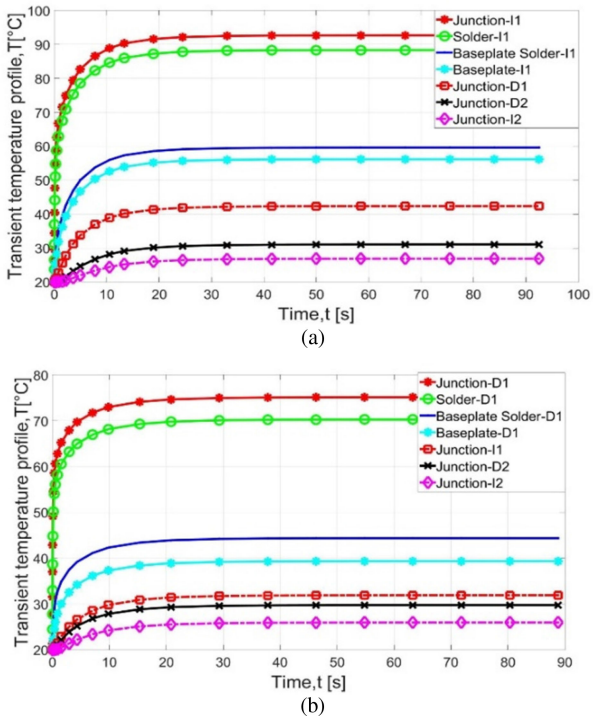


Fig. 5. (a) Transient temperature profile of IGBT, I_1. (b) Transient temperature profile of diode, D_1.

boundary condition is applied at the bottom of the liquid-cooled cold plate. The total estimated losses were estimated to be 1020 W for the inverter having six IGBTs and six diodes. The equivalent heat transfer coefficient was estimated approximately as $3000\,\mathrm{W/(m^2K)}$ from (6) for the considered cold plate area $0.017\,\mathrm{m^2}$, baseplate temperature $40\,^{\circ}\mathrm{C}$, and coolant reference temperature $20\,^{\circ}\mathrm{C}$. The estimated heat transfer coefficient of the liquid cooling cold plate was applied at the bottom of the cold plate in the FEA simulations [36]

$$h = \frac{6 * P_{\mathrm{loss-IGBT}} + 6 * P_{\mathrm{loss-diode}}}{(T_{\mathrm{baseplate}} - T_{\mathrm{ref-coolant}}) * A} \tag{6}$$

where $P_{\mathrm{loss-IGBT}}$ is the power loss in IGBT, $P_{\mathrm{loss-diode}}$ is the power loss in the diode, $T_{\mathrm{baseplate}}$ is the baseplate temperature, $T_{\mathrm{ref-coolant}}$ is the coolant reference temperature, and A is the heat spreading area of the liquid cooling cold plate.

The recorded step transient responses at selected locations from the two FEA simulations for I_1 and D_1 are shown in Fig. 5. The temperature responses are converted to thermal impedance curves using

$$Z^{\mathrm{self}}_{\mathrm{th}(m-n)} = \frac{T_m(t) - T_n(t)}{P_{\mathrm{self}}} \tag{7}$$

$$Z^{\mathrm{cross}}_{\mathrm{th}(m-n)} = \frac{T_m(t) - T_n(t)}{P_{\mathrm{cross}}} \tag{8}$$

where "m" and "n" correspond to any two consecutive nodes, and P_{self} and P_{cross} describe the power dissipation in the same chip and in the neighbor chip, respectively.

F. Thermal Parameter Extraction

By fitting the step response equation (9) to the transient thermal impedance curves, third-order thermal equivalent Foster *RC* pair parameters can be obtained. The particle swarm optimization curve fitting algorithm [37] has been used to fit (9) to the simulated impedance data

$$Z_{\mathrm{th}}(t) = \sum_i Rth_i * \left(1 - e^{\frac{-t}{Rth_i * Cth_i}}\right) \tag{9}$$

where $R_{\mathrm{th}i}$ and $C_{\mathrm{th}i}$, respectively, correspond to the thermal resistance and thermal capacitance at the ith term.

The analysis of thermal coupling has been carried out using a simplified thermal network in which the cross-heating network is modeled using the two nodes at the junction and at the heatsink, and the third-order *RC* pair for this network is extracted to represent all the layers between the two nodes.

Typically, power modules are connected to a heatsink through thermal grease. Adding heatsink to the power module introduces nonlinearity due to the heat convection process occurred in the heatsink. In addition, thermal spreading and temperature-dependent material properties also generate an error if a linear assumption is applied. Before applying the Foster thermal model, the impact of nonlinear factors on the linear assumption has been demonstrated in [24]. The use of temperature-dependent material properties, as shown above in the simulations, gives 5%–7% difference in predicting junction temperature compared with the conventional linear thermal model, where material properties are considered to be constant. However, if average temperature-dependent thermal properties are used in the simulations to linearize the system, the difference in the prediction of junction temperatures becomes 2%–5%. In this article, the nonlinearity of the cooling system is modeled by considering the IGBT structure with a liquid-cooled cold plate and thermal grease and temperature-dependent material properties. This is outlined in Section II-G.

G. Modeling the Nonlinearity of Cooling System

In this section, a new thermal network is introduced to translate the nonlinearity of the cooling system and *RC* parameters are expressed as a function of convective heat transfer coefficient. Converters in real applications do not operate in fixed load and, thus, produce varying power losses due to varying load. As a part of the thermal management, the cooling system is tuned accordingly to maintain the cooling capability by adjusting the flow rate and the pressure drop in the flow channel at varying load. Therefore, the use of fixed *RC* parameters obtained for a fixed convective thermal boundary condition is no longer appropriate for varying thermal boundary conditions. To circumvent these problems, a generic compact *RC* thermal model is required that can adapt the changes in the boundary conditions. Although some recent literature discussed the impact of the various cooling boundary conditions on thermal impedance network [24], [25], [35], they failed to include either the temperature-dependent material properties [24], [25] or the thermal grease layer [35] in their models. This article shows that these simplifications

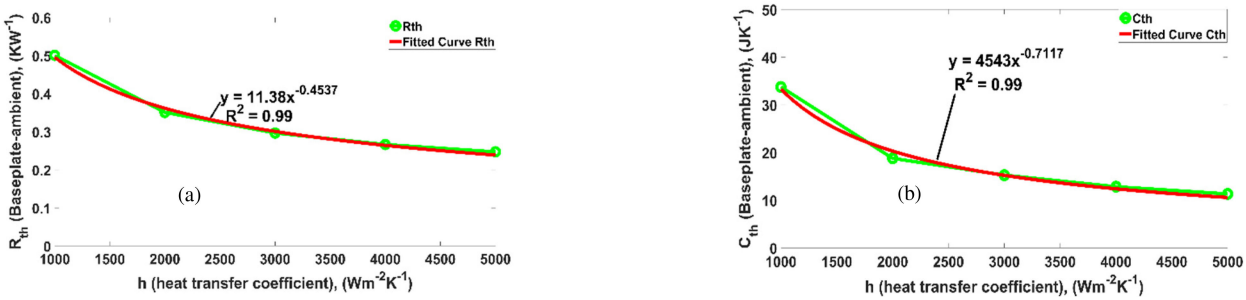


Fig. 6. Curve-fitted thermal resistance and thermal capacitance for varying heat transfer coefficient. (a) I_1, baseplate to ambient thermal resistance. (b) I_1, baseplate to ambient thermal capacitance.

affect the temperature prediction accuracy in electrothermal simulations.

To tackle the nonlinearity of thermal boundary conditions, two cases are studied. In case 1, temperature-constant material properties are used, and in case 2, temperature-dependent material properties are used. To model the capability of the cold plate for varying loading conditions, the heat transfer coefficient is estimated by (6) based on the losses occurred in the inverter due to each loading condition. In both cases, the heat transfer coefficient h is varied, h ranges from 1000 to 5000 $\mathrm{Wm^{-2}K^{-1}}$ and five simulations are conducted for each case. Gathering the FEA step response in each case and by processing, these data are fitted to generate the compact thermal model.

The most influential thermal path for the device under consideration is baseplate-to-ambient due to the proximity of the baseplate layer to the cooling system. For case 1, transient thermal impedance curves for I_1, D_1, D_2, and I_2, the thermal path starting is extracted according to varying heat transfer coefficient values. Then, the first-order *RC* parameters are extracted by fitting (9) to each thermal impedance curve. The choice of first-order *RC* parameter is due to make the thermal network simple. Afterward, the derived *RC* parameters are further fitted to obtain a mathematical function of h. For self-heating of I_1, the curve-fitted expression of thermal resistance and thermal capacitance as a function of h (only for baseplate-to-ambient thermal path) is shown in Fig. 6. Similarly, for cross heating, the curve-fitted expressions of thermal resistance and thermal capacitance as a function of h for D_1, D_2, and I_2 are shown in Fig. 7 (only for junction-to-ambient thermal paths). The method for developing the model for case 2 (temperature-dependent material properties in FEA) is exactly the same.

III. Applications

The method detailed above has been implemented to analyze the thermal behaviors of an IGBT-diode pair in an IGBT module that is used in a conventional three-phase voltage-source inverter, as shown in Fig. 8. The figure illustrates the 5 Hz inverter's electrical circuit that is coupled to the thermal network circuit for the IGBT-diode pair. The power loss in each IGBT is estimated from the conduction and switching losses.

To facilitate the high accuracy of temperature prediction by the electrothermal model, it is important to construct an accurate loss model. The studied IGBT module is considered in a three-phase voltage-source converter system. The converter circuit is built in PLECS. One of the salient features of PLECS is its capability of providing accurate estimation of losses in the power converter. This has been demonstrated by a few recent works in converter loss modeling [23]–[25], [38]. A similar approach is applied here to develop a lookup table based loss model to estimate power losses based on loading conditions, various operating temperatures, and other electrical parameters.

For the thermal analysis, the obtained *RC* parameters are used in the thermal network circuit model, which is shown in Fig. 9 for both noncoupled and coupled conditions. For the IGBT (or diode), the thermal circuit consists of four branches of third-order *RC* Foster cells that are connected in series. The thermal branches correspond to the junction to solder, chip solder to baseplate solder, baseplate solder to baseplate, and the baseplate to heatsink thermal impedance, respectively. The cross heating of other chips has been represented by a third-order *RC* Foster cell for the junction to ambient impedance. As shown in Fig. 9(b), the junction temperature of the IGBT or the diode consists of the contribution from self–heating, cross heating, and the ambient temperature.

To study the impact of nonlinear cooling boundary on the thermal model, *RC* network parameters are expressed as a curve-fitted equation of heat transfer coefficient h. A new cooling boundary dependent thermal network is illustrated in Fig. 10. As shown in Fig. 10(a) and (b), the cooling boundary dependent *RC* parametrized network of the IGBT1 (I_1) and the diode1 (D_1) consists of the contribution from self–heating, cross heating, and the ambient temperature. The model parameters can be tuned by varying h.

Pulsed power loss profiles (frequency 5 Hz) for the IGBTs and diodes in the IGBT module in the above-mentioned power inverter have been generated using PLECS. Fig. 11 describes the power loss profiles for IGBT1 (I_1) and diode1 (D_1), respectively. These profiles are then used in the power module thermal network circuit for the analysis of the thermal coupling effect among I_1, D_1, I_2, and D_2. The thermal circuit has also been analyzed using PLECS and the total simulation time is 25 s.

Three cases have been analyzed. In case 1, the thermal network *RC* parameters are derived from FEA simulation using temperature-dependent material properties of silicon and copper. In case 2, the *RC* parameters are derived from FEA simulation using fixed material properties. In both cases, the cross-heating impedance terms (for D_1, I_2, and D_2) are included in the IGBT1 (I_1) thermal network model. In case 3, the *RC* parameters do not contain cross-heating thermal impedance terms (conventional approach).

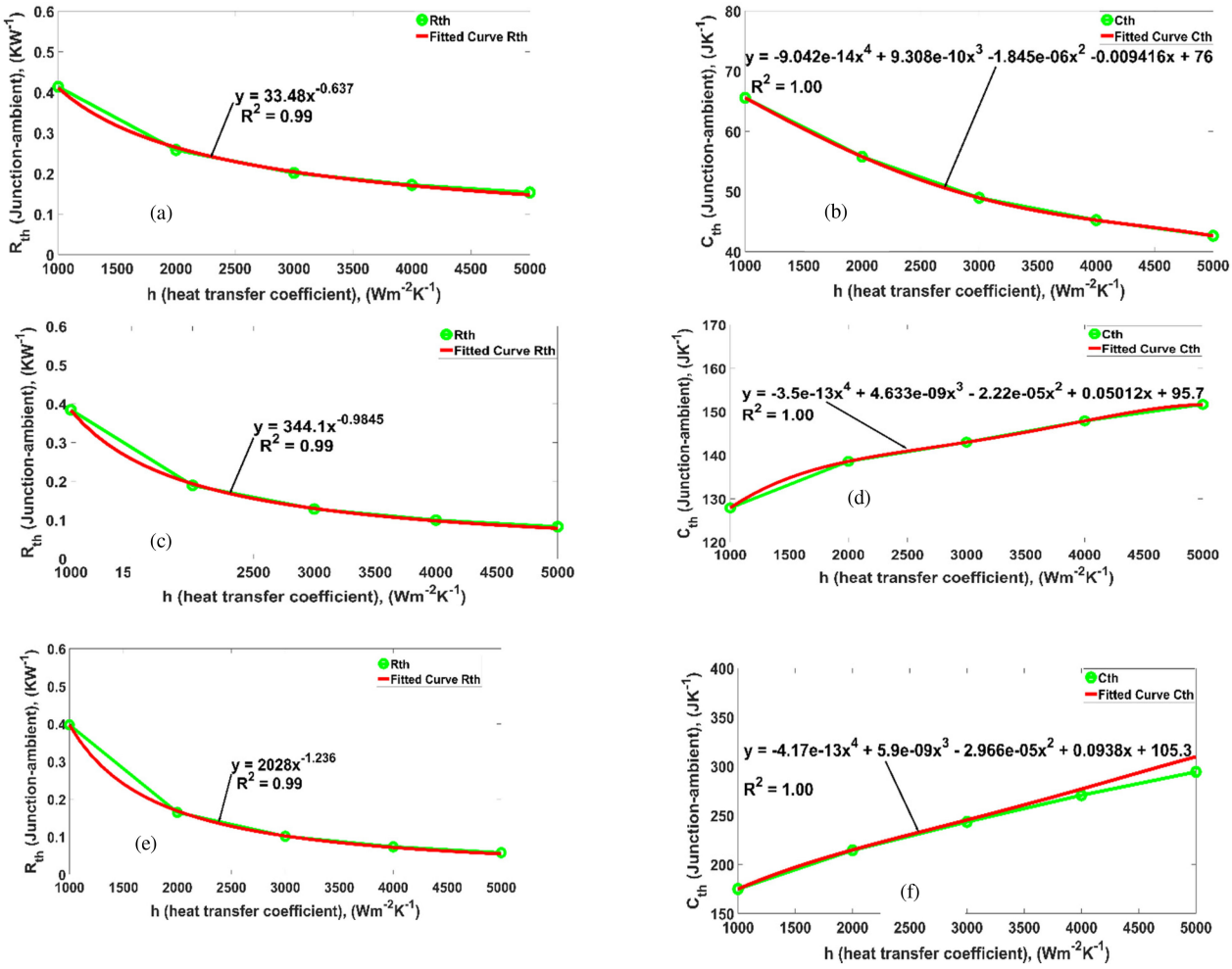


Fig. 7. Curve-fitted thermal resistance and thermal capacitance for varying heat transfer coefficient. (a) $D_1, R_{\mathrm{th}(j-a)}$. (b) $D_1, C_{\mathrm{th}(j-a)}$. (c) $D_2, R_{\mathrm{th}(j-a)}$. (d) $D_2, C_{\mathrm{th}(j-a)}$. (e) $I_2, R_{\mathrm{th}(j-a)}$. (f) $I_2, C_{\mathrm{th}(j-a)}$.

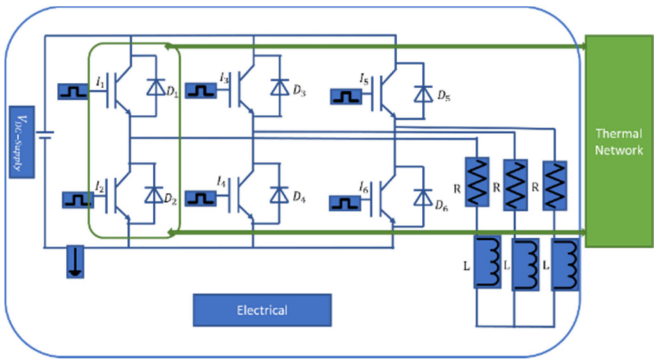


Fig. 8. Coupled electrothermal network circuit for an inverter in PLECS.

A. Thermal Interaction and Temperature-Dependent Material Properties Effect in the Temperature Estimation of a Half-Bridge Module

A transient power loss profile is applied to the inverter's thermal model in Fig. 8 to investigate the impact of the coupling effect and material nonlinearity on temperature prediction by the proposed method. Squared power pulses of 160 W in the IGBT and 30 W in the diode are applied to understand better thermal dynamics. The applied frequency is 5 Hz. Fig. 12 shows the IGBT1 I_1 and diode D_1 temperatures for the three cases analyzed in this article. The time period was considered between 22 and 22.2 s when the steady state has been reached.

As can be seen in Fig. 12(a), the IGBT1 junction temperatures for case 1 (temperature-dependent) and case 2 (temperature-independent) differ by about 1.95 °C, and case 1 and case 3 (noncoupled) differ by about 9.8 °C. This shows that both the thermal coupling and the temperature-dependent material properties affect the temperature predictions, but the thermal coupling has a greater effect. A similar discrepancy is also observed at chip solder, baseplate solder, and baseplate temperatures. The predicted temperature difference between cases 1 and 3 is about 12.16 °C, 12.14 °C, and 11.8 °C, respectively, at chip solder, baseplate solder, and baseplate, respectively. Fig. 12(b) shows the junction temperature of the diode. Once again, the effects of material property and thermal coupling are significant. However, for diode D_1, the temperature difference between cases 1 and 3 is about 24.7 °C, which is much greater than for the IGBT I_1. The difference is about 24.8 °C, 25.9 °C, and 24.8 °C, respectively, at chip solder, baseplate solder, and baseplate, respectively. This

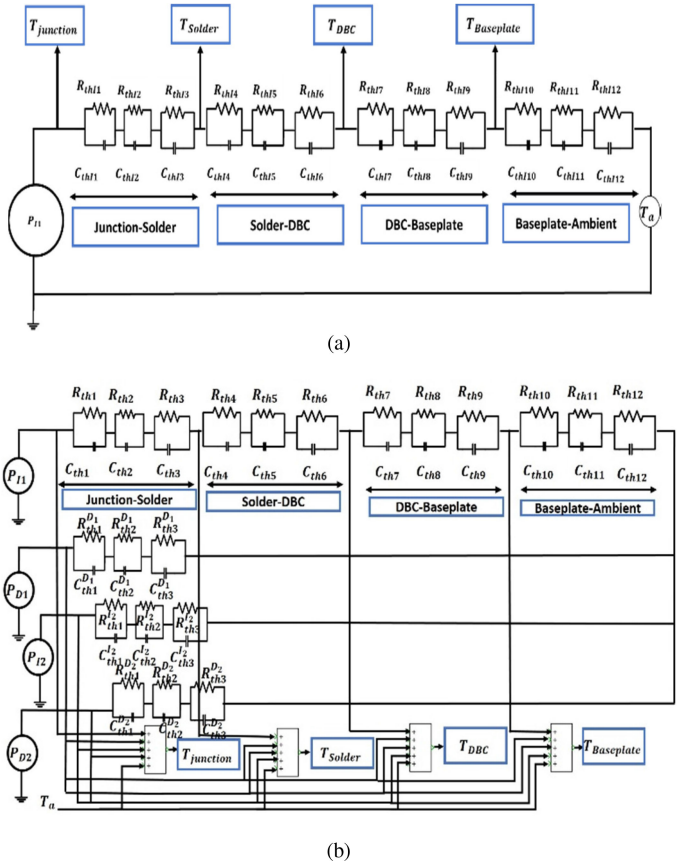


Fig. 9. (a) Noncoupled thermal network of igbt1 (I_1). (b) Coupled thermal network of igbt1 (I_1), diode1 (D_1), IGBT2 (I_2), and diode2 (D_2).

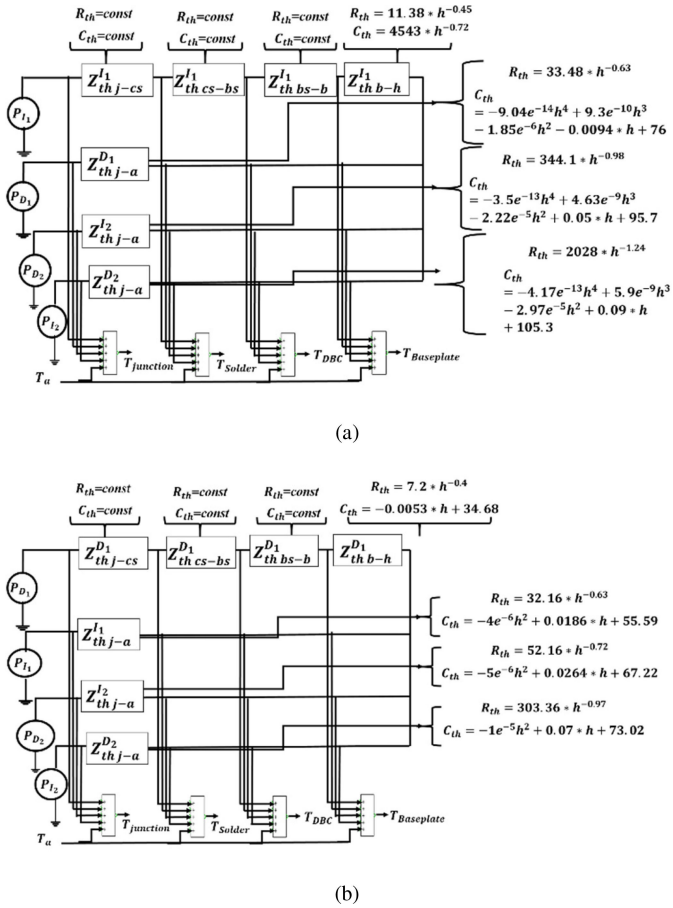


Fig. 10. (a) Cooling boundary dependent coupled thermal network of IGBT1 (I_1) including cross-heating effect of diode1 (D_1), diode2 (D_2), and IGBT2 (I_2). (b) Cooling boundary dependent coupled thermal network of diode1 (D_1) including cross-heating effect of IGBT1 (I_1), diode2 (D_2), and IGBT2 (I_2).

can be attributed to the fact that high dissipated power loss in I_1 causes the heat flux to spread and interact with adjacent D_1, D_2, and I_2, and thereby influencing the temperature of a closely adjacent diode D_1.

The temperature predicted by this proposed model was also compared with our previous work that did not include the thermal grease layer [39]. Neglecting the thermal grease layer in the model causes the temperature difference of I_1 at junction, solder, baseplate solder, and baseplate by 10.23 °C, 11.08 °C, 13.64 °C, and 11.14 °C, respectively, compared with the case 1 results. For D_1, temperature differs at the junction, solder, baseplate solder, and baseplate by 10.97 °C, 11.38 °C, 12.05 °C, and 11.92 °C, respectively, compared with the case 1 results. It can be seen that the impact of the thermal grease layer and material nonlinearity is significant for predicting temperatures in the IGBT modules. This is due to the fact that the thermal grease layer contributes to increase the thermal resistance and thermal capacitance in the baseplate to the ambient layer.

B. Cooling Boundary Dependent Material Nonlinearity Effect in the Temperature Estimation of a Half-Bridge Module

With the new thermal network presented in Fig. 10, the transient load profile is applied to the inverter in Fig. 8. Similar three cases are studied by the proposed *RC* thermal model considering the nonlinear material properties, constant material properties, and thermal noncoupling. The purpose of this article is to identify the impact of material nonlinearity, cooling boundary, and the errors of the thermal model due to applying the boundary condition at the bottom of baseplate instead of the heatsink. The results, as shown in Fig. 13, have clearly demonstrated that the case 2 still underestimates the junction temperature of IGBT1 and diode1 by 11.2 °C and 3.42 °C, respectively, comparing with the case 1, and the impact of thermally noncoupling is glaringly obvious on the temperature prediction. The discrepancies in case of prediction of the junction temperature of IGBT1 and diode1 are about 12.72 °C and 25.24 °C, respectively, between case 1 and case 3. The estimation errors in junction temperatures are 12.92% and 45% for the IGBT1 and the diode1, respectively, due to not considering the thermal coupling effect. The higher thermal coupling effect is more pronounced in diode 1 due to high power losses in IGBT1, and thus, the prediction error is significant.

In order to verify the accuracy of the proposed cooling boundary dependent *RC* network method, a test case scenario is set up in both FEA and proposed circuit method. In both cases, a similar dynamic loss profile obtained from the converter loading

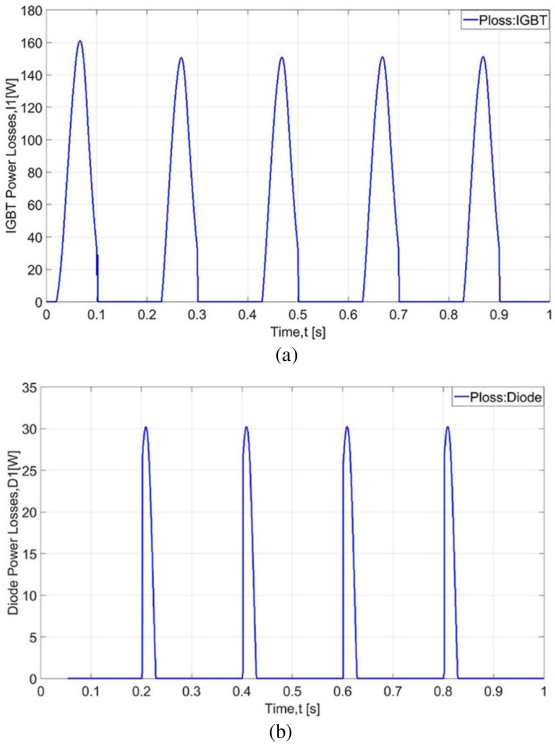


Fig. 11. Average power loss profiles of (a) IGBT1 (I_1) and (b) diode1 (D_1).

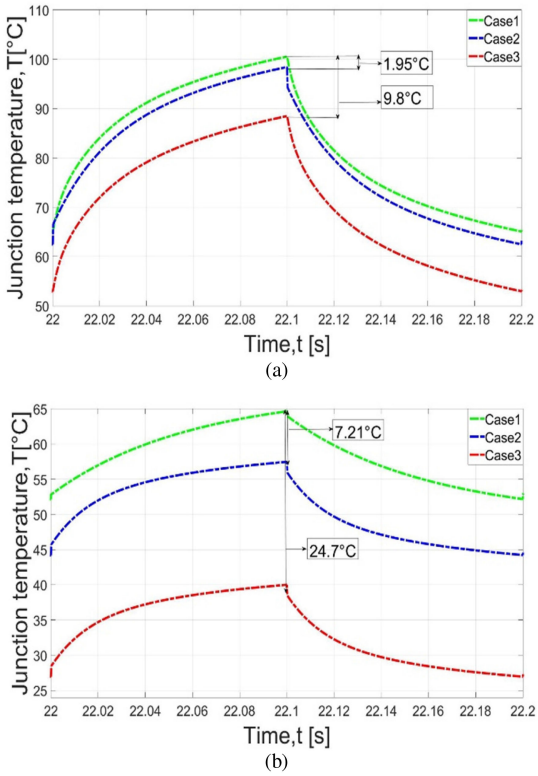


Fig. 12. Dynamic junction temperature profile of (a) IGBT1 and (b) diode1. Case 1—Temperature-dependent material properties. Case 2—Fixed material properties. Case 3—No thermal coupling.

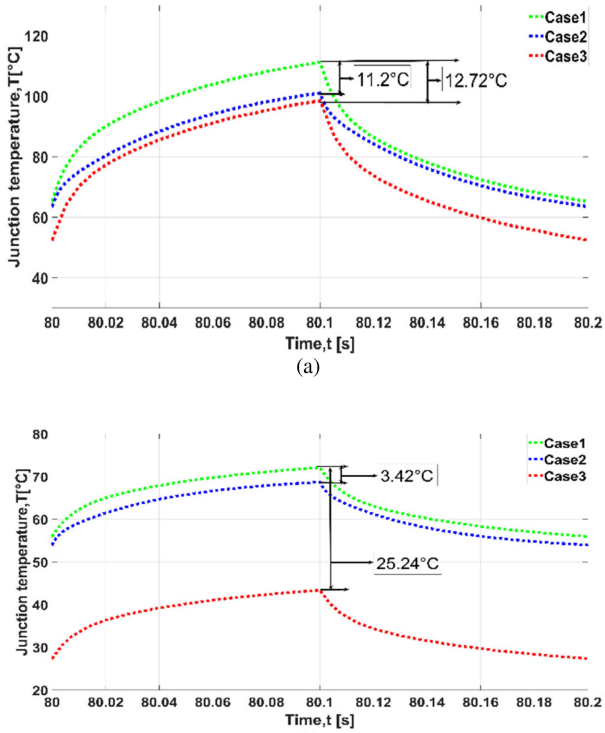


Fig. 13. Estimated dynamic junction temperature profile of (a) IGBT1 and (b) diode1. Case 1—Improved cooling boundary dependent model @ temperature-dependent material properties. Case 2—Improved cooling boundary dependent model @ temperature-independent material properties. Case 3—No thermal coupling.

is applied and h is considered $2500\,\mathrm{Wm^{-2}K^{-1}}$. The predicted temperature responses from the proposed method are compared with the FEA results. As it is shown in Fig. 14, FEA results are consistent with the proposed method and the maximum peak-to-peak temperature error between two methods is 3% and 4% for the IGBT1 and the diode1, respectively. It is worth to mention that FEA takes 40 min to solve a 100 s dynamic loss profile with a desktop computer with a Core i7 processor system, while the proposed method only takes 10 s to solve in the circuit-simulation platform. In practice, converter design experiences a long mission profile (i.e., a yearly mission profile for a wind turbine system). FEA will not be a suitable tool to handle the long mission profile due to memory and processing speed concerns.

C. Comparison Between Experiments and Simulation for a DC–DC Converter

In order to evaluate the accuracy of the proposed modeling method, the experimentally observed temperature profile in a power electronic converter [40] is compared with the results from the electrothermal analysis of the converter. The thermal interactions caused by the conduction and switching losses in the power semiconductor devices are validated using the proposed modeling approach. A high-bandwidth infrared thermal camera (FLUKE TiS 10) is used to observe the temperature distribution between four MOSFETs (Si CoolMOS, IRF7759L2TRPBF)

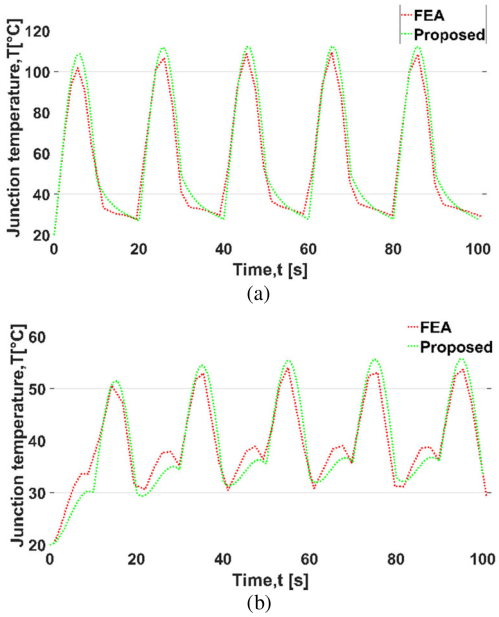


Fig. 14. Estimated dynamic junction temperature profile of (a) IGBT1 and (b) diode1 by proposed and FEA.

during the operation of the converter. The circuit topology and the experimental setup are illustrated in Fig. 15. The converter is a bidirectional interleaved dc–dc converter (1.5 kW, 12 to 48 V) with an interphase transformer (IPT). A dc power supply is used to feed the converter with a constant dc voltage as input and a variable resistive load is connected at the output; thereby, the current loading of the device can be adjusted. In Fig. 15(a), all the capacitors are multilayer ceramic capacitors and L_{in} is an amorphous alloy core-based filter inductor. T1–T4 are Si CoolMOS (MOSFET) from Infineon, IRF7759L2TRPBF in the DirectFET L8 package. The switching frequency of the converter was 40 kHz. During the boost-mode operation of the converter, T1 and T3 are turned OFF using zero gate bias, so the body diodes D1 and D3 are active in the converter. T2 and T4 work as the main MOSFETs in the boost cells. Only the temperature distribution during boost-mode experiments is shown in this section.

The MOSFETs were soldered on top of an insulated metal substrate board (TCLAD board) with 2oz copper and 1.02 mm Al base plate. The TCLAD board was screwed on top of an air-cooled Al heatsink. Silicone grease was used as TIM between the TCLAD board and the heatsink. On the top side of the MOSFETs, two *L*-shaped copper heatsinks were connected. A silicone polymer thermal pad (1 mm) is used between the Can and the copper heatsink for each MOSFET. Both filter inductor and IPT were placed above the TCLAD board. Therefore, the effect of their losses on the TCLAD board and the heatsinks can be considered negligible.

At the rated operating condition of the converter, 1.5 kW and 12–48 V, the power loss (switching plus conduction) in each of T2 and T4 was 13.7 W. Power loss in each of T1 and T3 was 9.8 W [40]. Ambient temperature was varied in the range of 21–25 °C. Two FEA models are constructed. In the first FEA model, material properties (Si, Cu) are temperature

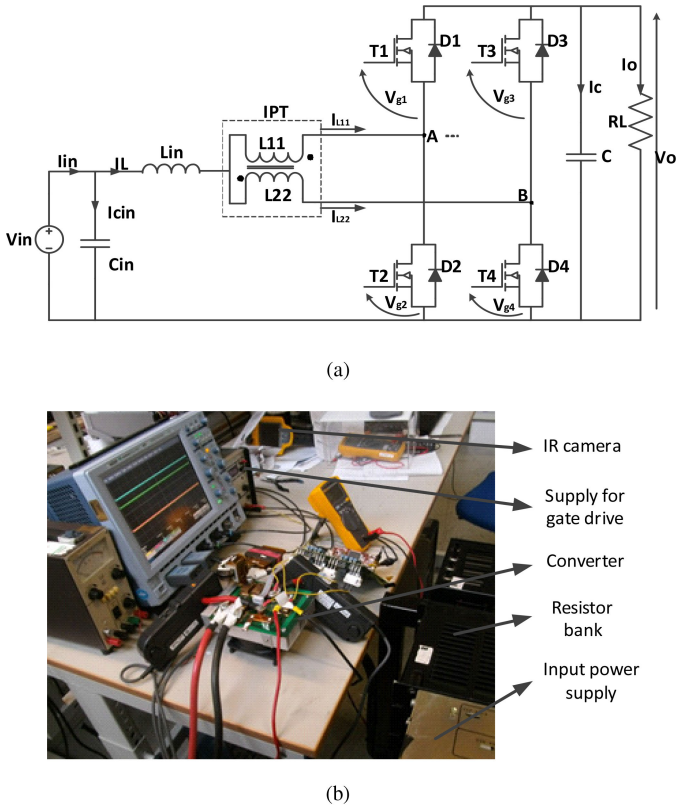


Fig. 15. Experimental validation of the electrothermal analysis of a dc–dc converter. (a) Circuit topology (IPT-based dual-interleaved bidirectional converter). (b) Experimental setup.

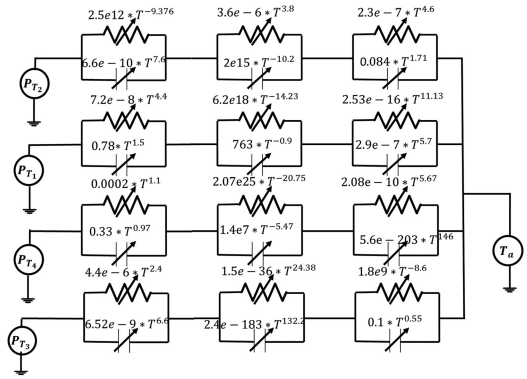


Fig. 16. Proposed *RC*-lumped thermal network for MOSFET.

dependent, while in the second FEA model, material properties are constant. The proposed *RC*-lumped thermal network that establishes the temperature dependence of the thermal resistance and capacitance is shown in Fig. 16. The power losses for T1–T4 are applied in both FEA thermal models of the converter and the temperature problem is solved. The self-heating and cross heating have been considered. Fig. 17 shows the temperature distribution of the MOSFETs, heatsinks, TCLAD, and interface materials in the converter. Using the FEA derived transient thermal responses, thermal network parameters have been extracted (similar to the process explained in Section II-E). Then, later three thermal models (coupled_$T_{\text{dependent}}$, coupled_T_{constant},

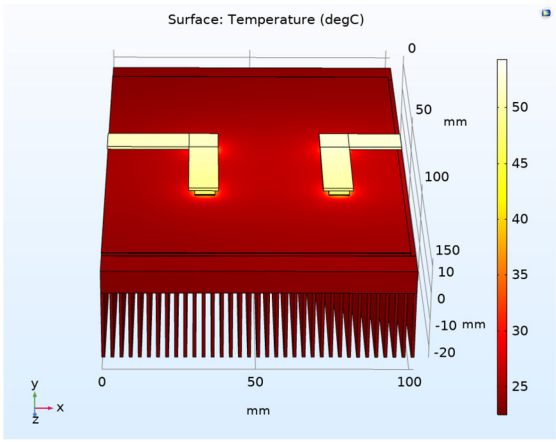


Fig. 17. FEA modeling of IPT-based dual-interleaved bidirectional dc–dc converter.

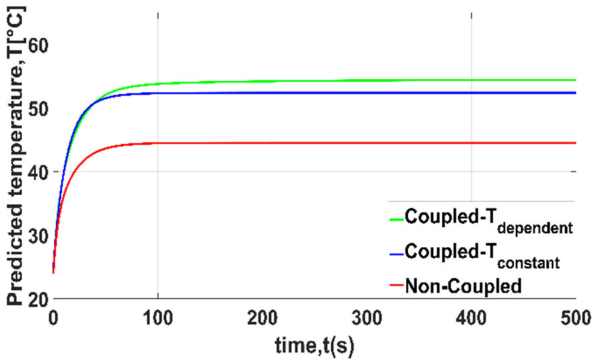


Fig. 18. Predicted temperature on the top surface of the copper heatsink where T2 is connected—Difference between the proposed coupled and conventional noncoupled approaches.

and noncoupled) have been analyzed in PLECS by integrating converter electrical model with a thermal model. For simplicity, to demonstrate the coupling effect, only T2 is modeed considering self-heating and cross heating. The coupled model includes all the MOSFET interactions, while the noncoupled considers only the self-heating of T2. The temperature profiles for T2 (top of copper heatsink) using coupled_$T_{dependent}$, coupled_$T_{constant}$, and noncoupled model are plotted in Fig. 17. The steady-state temperature difference is 9.9 °C between the coupled_$T_{dependent}$ and the noncoupled model. The steady-state temperature difference is 7.9 °C between the coupled_$T_{constant}$ and the noncoupled model. As in the noncoupled model, only a self-heated heat source is considered and the heat flux spreading contributed by the other MOSFETs is ignored; it provides inaccurate result.

A thermal image of the MOSFETs taken by the infrared camera is shown in Fig. 19 at the rated operating condition of the converter (1.5 kW, 12 V input–48 V output). The temperatures on the top surface of the copper heatsink, where the MOSFETs are connected, can be clearly observed. High emissivity white paint was put on the top surface of the heatsink, where the MOSFETs are connected to allow accurate temperature measurement using the infrared camera. The observed temperatures for T4, T3, T2,

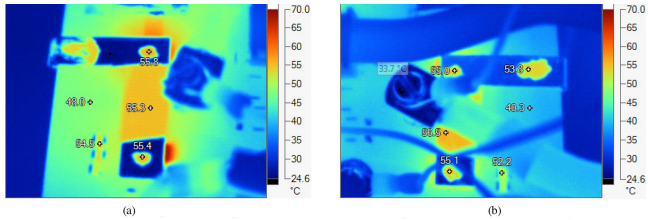


Fig. 19. Temperature of different components. (a) Temperature of T3 (bottom) and T4 (top) and (b) temperature of T1 (bottom) and T2 (top) when the dc–dc converter is running at 1.5 kW.

TABLE III
STEADY-STATE TEMPERATURE OF MOSFET, T2 IN AN INTERLEAVED DC–DC CONVERTER

Temperature (°C)	Proposed model	FEA	Experimental
	53.4°C	54.8°C	55°C

and T1 are 55.8 °C, 55.4 °C, 55 °C, and 55.1 °C, respectively. In Fig. 19(a), at the edge of *L*-shaped copper heatsink positioned at T3, the temperature is slightly higher, around 68.6 °C. This is due to the improper use of white paint. The thickness of white paint at that particular edge was higher, which may have worsened the surface emissivity in that particular location. Also, reflection from nearby components (copper connectors on the TCLAD) and thermal radiation of the surroundings can affect the measurement.

The steady-state temperature of the top surface of the copper heatsink, where T2 is connected, obtained by two methods (proposed modeling and FEA) is listed in Table III along with the experimental result. The observed steady-state temperatures from FEA simulations for T4, T3, T2, and T1 are 54.01 °C, 52.18 °C, 54.8 °C, and 51.39 °C, respectively. It is worth to note that the temperatures agree well, although a small variation of 1.2 °C is observed for T2 switch between the proposed model and the experiment. Predicted T2 temperature from the proposed circuit method differs by 0.7% and 3% compared with the FEA simulation and the experiment, respectively. The FEA result agrees well with the experimental results for other switches (i.e., T4, T3, and T1) and it differs by 1.8%, 5.1%, and 6.5% compared with the experiment, respectively. This discrepancy might generate due to neglecting the effect of the thermal coupling of other components and the simplification of the converter setup and the simplified MOSFET package used in the FEA simulation. The DirectFET package was simplified in this analysis. Also, the current density in the copper tracks of the TCLAD board was very high causing around 18 W loss in them during the experiment at the rated operating condition [37]. This loss was neglected in the FEA simulation that can influence the thermal equivalent Foster network parameters in the proposed model.

IV. CONCLUSION

The accuracy of any thermal model depends on the precise modeling of component thermal interaction, module or device geometry, material nonlinearity, accurate measurement of critical layers, and cooling system (i.e., liquid-cooled cold plate and

extruded air-cooled fin heat sink). In this article, a methodology for solving the electrothermal problems of power electronics components (IGBT power module and discrete FET package) is proposed using an enhanced *RC* network model. The *RC* thermal network parameters are extracted from FEA simulations considering the impact of nonlinear cooling boundary conditions and self- and cross-coupling thermal impedances.

The analysis presented in this article has demonstrated that the estimated temperatures of IGBT and diode using the proposed *RC* network is more accurate compared with the traditional *RC* network, which is derived by applying the convective cooling boundary conditions at the bottom of baseplate instead of at the bottom of liquid-cooled cold plate or heat sink. To further validate the accuracy of the proposed modeling approach, estimated temperatures of the MOSFETs in a dual interleaved dc–dc converter are compared with the experiments and FEA simulation. The predicted temperature of the MOSFETs is very close to the FEA results but differs by 2%–6.5% from the experimental result. This is thought to be caused by the simplification of the MOSFET package in the FEA model due to the lack of detailed structural and material information of the can-to-drain layer of the MOSFET package. The analysis shows that the proposed approach can increase the accuracy of the temperature prediction for a specific component if the geometrical and material details of the component are known. Because of the fast and accurate simulation, the proposed method could enable more accurate reliability assessment at the initial design stage of a power electronics converter resulting in a more effective guide to reliable hardware prototyping and further qualification test. Additionally, it can help develop a model-based observer that can be implemented in real-time health monitoring purpose.

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