A Wire Bondless SiC Switching Cell With a Vertically Integrated Gate Driver

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***Abstract*—In this article, an SiC half-bridge module with an integrated gate driver is demonstrated. A physically and electrically compact integration scheme produces a decrease in the parasitic inductance of the critical switching loops in the circuit. Furthermore, a wire bondless integration scheme was devised for the power devices to keep the interconnect parasitic inductance to very low levels. This was realized by converting a bare die SiC power device into a flip-chip capable chip-scale package. This article provides a description of the implementation of the novel wire bondless chip-scale device packages in a switching cell with an integrated gate driver. The electrical performance of the module was evaluated, and very high slew rates of 24 V/ns were demonstrated with $<$5% overshoot. These results were encouraging for realizing high-frequency switching in SiC power electronic systems.**

***Index Terms*—High-frequency switching, integrated power module, low parasitic, silicon carbide, switching cell, wire bondless.**

I. Introduction

SILICON carbide power devices are superior to conventional silicon power devices in several ways [1]–[5]. Some of the notable benefits are a very low ON-state resistance, lower switching losses, and high-temperature capability. These properties of SiC devices make efficient and high-frequency switching a viable possibility in power electronics systems. This will enable a significant volumetric decrease since high-frequency systems require physically smaller passive devices. Passive devices account for the most weight and volume in a contemporary power electronics system—thermal management being the only other significant contributor. High-frequency switching, therefore, has great potential to realize smaller and lighter power electronics systems, combined with a reduction in cost [6], [7]. Intuitively this seems simple, but prevailing packaging techniques prevent this.

SiC power devices require novel system integration methods to realize their full potential. Even today, a power electronics system using SiC devices resembles a Si system. This has to change, and it is encouraging to see changes in the right direction. There have been several notable efforts in which the gate driver and/or the decoupling capacitor have been integrated within the power module to reduce parasitic elements for fast switching [8], [9]. These approaches were able to demonstrate the benefit of reducing parasitics in an SiC system. However, integrating gate drivers within a module may not always be possible. SiC power devices and modules are often rated for maximum junction temperatures of 175 °C. However, commercial gate drivers will not be able to operate reliably at these temperatures. The reliability of the module or system will be limited by this. Moreover, these approaches still use wire bonding as the interconnection method.

One of the major roadblocks to high-frequency switching is the presence of wire bonds in a power electronics module. Wire bonds possess an inherent parasitic inductance which leads to undesired overshoots during fast switching events. Despite this fact, we need to consider that wire bonding processes are well understood and a standard process in the industry. Hence, there has been a number of research efforts focused toward achieving low inductance layouts employing wire bonded interconnections. Several studies from Arkansas Power Electronics International (now Cree Wolfspeed) demonstrated high-frequency operation (500 kHz to 1 MHz) at $>$93% efficiency by using innovative layout designs [10], [11]. A recent study demonstrated a 40% decrease in loop inductance in a wire bonded module as compared with the state-of-the-art [8]. However, high-frequency switching is still not common with wire bonded modules despite these efforts. A technology gap needs to be bridged to realize a reliable increase in switching frequency, and wire bondless solutions are the way forward.

Wire bondless technologies will enable (electrically) shorter vertical signal loops with low parasitic inductances. This concept has been implemented with great success in low-voltage GaN power electronics systems [12], [13]. In a previous study, the authors successfully realized a wire bondless switching cell using SiC power devices [14], [15]. Wire bonds are also one of the first components to fail during reliability testing [16]. There is also a limit to the number of wire bonds per die. With the shrinking sizes of SiC die, this is going to be an even greater challenge in the near future. The die will be capable of sourcing high current densities, but the number of wire bonds will become the limiting factor. It will be essential to maximize the contact area on the drain and source terminals of an SiC MOSFET, and one of the most effective ways of realizing this is flip-chip bonding. For example, the area of a single source pad of the MOSFET used for this article is about 1.5 sq.mm. Each of the pads has six solder balls of 15 mil (0.4 mm) diameter, which covers a total area of 0.75 sq.mm. This amounts to 50% coverage. A typical heavy aluminum wire bond is about 10 mil (0.25 mm) in diameter. With

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a 10 mil bond, the maximum number of wire bonds that can be accommodated on the source pad would be five. Approximately, this would be 0.25 sq.mm., which is third of the area covered by the solder ball array. One of the main reasons why a dense pitch is not possible for power wire bonding is because the layout design has to allow space and clearance for the loop geometry. In contrast, for the solder ball array, the connection is vertical and enables a higher pitch and more coverage.

An ancillary advantage of flip-chip bonding is the scope for implementing double-sided cooling. This is impossible to realize with contemporary wire bonded modules. In fact, wire bondless packaging has proven to be very effective even for Si power modules in the past, and examples may be found both in industry and academia [17]–[28]. The motivation for this was either to implement double-sided cooling or enhance the current density. These benefits will only be magnified in case of SiC devices. This is straightforward to understand but wire bondless SiC modules are not commercially available yet. One of the major reasons for this is that the top side metallization of commercial SiC power devices is aluminum. This is to support top side wire bonding. Commercial SiC module manufacturers still employ aluminum wire bonding. Most of these manufacturers are tooled for Si IGBT modules, and still use the same processes for manufacturing SiC power modules. However, an aluminum top side metallization is neither solderable nor sinterable. The topside metal of commercially available SiC devices needs to be remetallized to achieve flip-chip bonding. The SiC device manufacturers can provide a simple solution by producing devices with a solderable top side. However, until the benefit of flip-chip SiC modules is demonstrated, the paradigm shift required for this change will not occur.

In this article, a commercially available bare die SiC MOSFET was reconfigured into a chip-scale package, which was flip-chip bonded onto a substrate/interposer. This approach eliminates the need for wire bonds and enables fast signal slew rates with minimized overshoots. This article extends this concept to a system through a novel and compact integration of the gate driver circuit and the power circuit. In Section II, the concept of chip-scale SiC power device is summarized. Section III describes, in concept, how the chip-scale device was manufactured and was then used to realize a highly compact integrated system. The feasibility and performance estimation of the novel approach is demonstrated in Section IV. Finally, after the evaluating the design in software, a prototype was constructed and tested. The results are presented in Section V.

II. Flip-Chip SiC Power MOSFET

A. Description of the Power Device Package

The concept of a flip-chip power device was demonstrated in an earlier study by the authors [14]. This article described the method of reconfiguring a commercial bare die power device into a flip-chip capable surface mount package. A SiC bare die typically has a pair of source pads and a gate pad on the top surface, and a drain pad on the bottom surface. The bottom pad connector as shown in Fig. 1, was used to convert the bottom drain pad of the MOSFET to a top side pad—thus enabling flip-chip bonding. It was also demonstrated that the switching performance of the novel power device surpassed that of through hole packages and conventional wire bonded

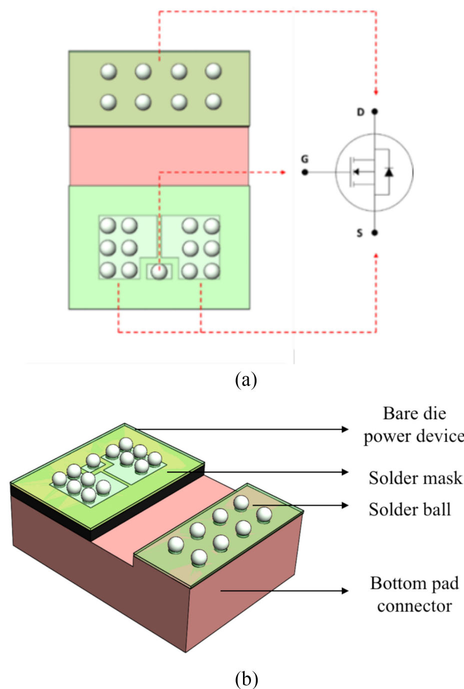


Fig. 1. Flip-chip power MOSFET showing (a) isometric view of the various components and (b) description of the electrical contacts.

packages containing the same die. Fig. 1 shows the flip-chip MOSFET and its circuit implementation as demonstrated in [14].

The demonstrated concept did not, however, contain an integrated gate driver. The gate signals were fed into the switching cell through an off-board, traditional gate driver. Although using an off-board gate driver circuit is standard practice, there are many benefits of closely integrating the gate driver with the power MOSFET. As system power density increases, efficiently integrating the gate drive as part of the power module will enable high-frequency switching, improve signal quality, and reduce part count.

The concept proposed in this article offers a solution to this issue. It electrically integrates the gate driver circuit to the power device, while thermally isolating them from each other. This is realized by using the flip-chip MOSFET chip-scale device. This approach strives to improve upon some previous forms of wire bondless packaging like direct lead bonding, planar interconnect bonding, etc. First, the flip-chip approach uses a solder ball array to distribute the thermo-mechanical stresses in the system. Historically, the reliability of this approach is very well-understood in numerous microelectronics applications [29]–[34]. Flip-chip BGA technology has remained a strong package choice in the microelectronics industry. Second, the flip-chip MOSFET is a chip-scale discrete device. This makes creative system architectures easily achievable without a highly customized power module. It combines the easy implementation of a discrete device while increasing the electro-thermal performance as compared with contemporary power modules. This is also what sets this approach apart from integrated power modules (IPMs). Today's IPMs do not employ wire bondless integration and/or 3-D integration for lowering parasitics and enabling double sided cooling.

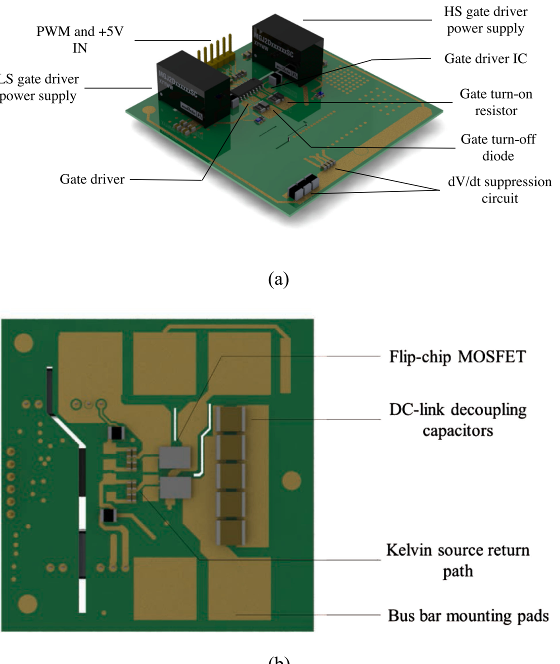


Fig. 2. Artistic renderings of the 3-D wire bondless integrated power module showing (a) 3-D view of the top side of the module and (b) bottom view of the same.

III. 3-D Integrated Wire Bondless Switching Cell

The concept of the proposed integrated power module is presented in Fig. 2. It represents a half-bridge power module, with a single flip-chip MOSFET per switching position. The device used was a 1200 V ROHM MOSFET with an integrated Schottky barrier diode. The top side of the module contained the gate driver circuit, and the bottom side contained the power devices and the decoupling capacitors. In Fig. 2(a), a 3-D view of the power module is presented. A six-pin male header served as the input for the pulsewidth modulation (PWM) signals and 5 V gate driver supply voltage from the DSP board to the module. Each of the signals—PWM1, PWM2, and 5 V—were provided with individual adjacent ground connections. The gate driver for the module was the UCC21520DW gate driver from Texas Instruments, with rated rise and fall times of 6 and 7 ns, respectively, and a rated propagation delay of 5 ns. This half-bridge driver also had the provision for including a hardware dead time to prevent a shoot-through condition. This was a desirable feature for a fast gate driver. The specifications and layout considerations can be found in the manufacturers' datasheet.

To reduce the risk of a possible false turn-ON event under fast switching, there are a few proven approaches that have been demonstrated in the past. Some of these recommended methods were employed in this module as well for protecting against switching transients. A +20 V/–5 V gate voltage was used to trigger the power devices where the negative voltage rail ensured that the device remained completely turned OFF, without the risk of a false turn-ON event. An asymmetric turn-ON/OFF time was realized using a 5-Ω gate resistor during turn-on, and a low resistance Schottky barrier diode at turn-off. This is also a recommended practice which is widely used in the gate drive circuits of wide bandgap power modules. The proposed module also contains integrated power supplies for the gate driver input/output. The gate driver output is routed to the gate of the MOSFET using a through via. Fig. 2(b) shows a rendering of the bottom side of the board. It shows the flip-chip type power MOSFETs bonded to a matching land pattern on the bottom surface of the interposer. A separate trace was provided for the Kelvin source terminal. The decoupling capacitors were placed as close to the MOSFETs as possible to reduce the power loop inductance. In conventional power modules, the power loop is planar, hence offering a large parasitic inductance. In the proposed module, the power loop only extends from the bottom plane of the module to the next available interior plane. This resulted in a loop thickness of only 0.28 mm. A *dV/dt* suppression circuit is also included on the PCB to protect against possible electromagnetic interference (EMI) issues resulting from the expected high signal slew rates. This is achieved by inductively isolating the heatsink/chassis and prevents the noise from corrupting the gate drive circuit [35]. This was included as a safeguard against potential conducted EMI issues, but was not employed during testing.

IV. Simulation Results: Parasitic Estimation and Thermal Feasibility

The power loop and gate loop parasitic inductances were simulated, and the results are presented in Fig. 3. The simulation was performed in the ANSYS Q3D software environment. For the power loop inductance estimation, the signal net encompassed the bottom drain connector of the device, the solder ball array on the source and drain pads of the device, and all the power loop metal traces and vias in the interposer. The frequency was swept from 0.1 to 10 MHz. Fig. 3(a) shows a schematic of the cross-sectional view of the module. The figure shows how low-inductance vertical signal loops may be obtained using the novel flip-chip MOSFET design. Fig. 3(b) shows the power signal net for the simulation. $V_{\mathrm{DC+}}$ and $V_{\mathrm{DC-}}$ refer to the positive and negative rails of the bus voltage. $V_{\mathrm{OUT+}}$ and $V_{\mathrm{OUT-}}$ refer to the positive and negative reference points of the output voltage in the half bridge (the voltage across the low-side switch position). The total power loop inductance was <11 nH and the total power loop resistance was ~ 21 mΩ.

For the gate–source loop, the signal net encompassed the gate solder ball, the source solder ball array, and all the internal gate loop traces in the interposer from the device signal pads to the gate driver output pads. The frequency was swept from 0.1 to 10 MHz. Fig. 3(c) shows the gate signal net for the simulation. The gate–source loop inductance was estimated to be ~ 1.8 nH, with a parasitic resistance <9 mΩ. While these values are very low, it must be noted that they are capable of being further optimized. The goal of this article was to implement a system using wire bondless integration of SiC MOSFETs. The optimization of the board parasitics was beyond the scope. More stress was placed on being able to position probes to enable accurate measurements of the switching events in the critical switching loops. The inductance and resistance values, presented in Fig. 3, can be lowered much further by optimizing the traces in the interposer. Fig. 3(d) and (e) show the variation of the parasitic inductance (and resistance) of the power and gate loops as a function of frequency.

The thermal considerations for this module were evaluated as a next step. The heat removal strategy for the proposed module involved a direct contact to a heat sink through the metallic drain

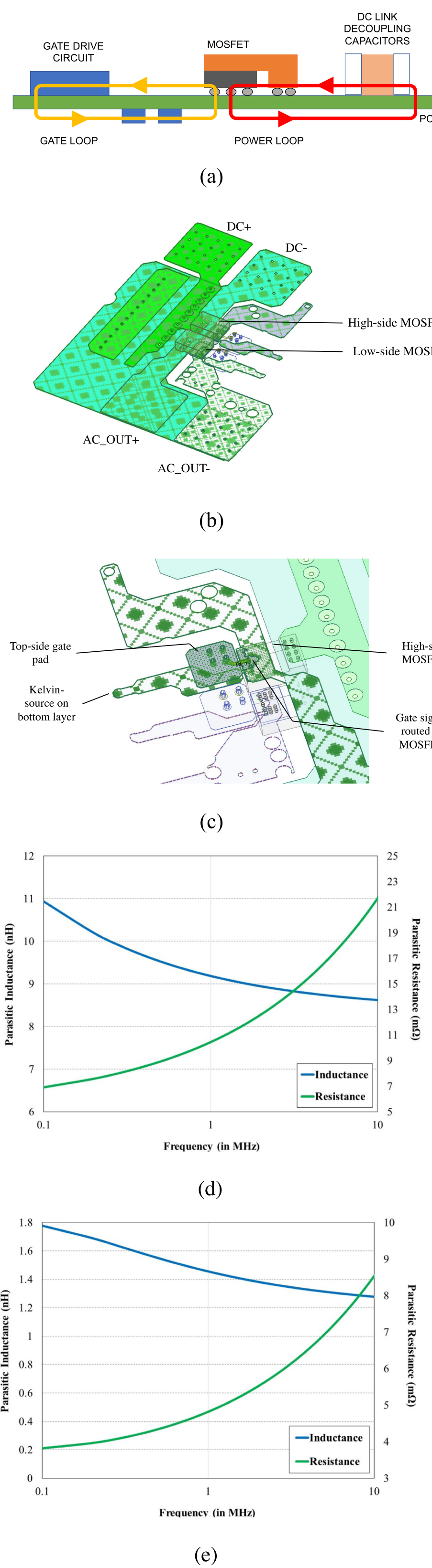


Fig. 3. Results of the parasitic estimation of the integrated half-bridge showing (a) schematic representation of the lateral view of the signal loops, (b) power loop net in ANSYS, (c) signal loop net in ANSYS, (d) variation of the parasitic inductance and resistance of the power loop with frequency, and (e) variation of the parasitic inductance and the resistance of the gate–source loop with frequency.

TABLE I
MATERIAL PROPERTIES USED FOR THERMAL SIMULATION

Material	Density (kg/m3)	Thermal Conductivity (W/m.K)	Specific Heat Capacity (J/g-°C)
Copper	7764	385	0.385
SiC	3100	120	0.750
Solder	8400	50	0.167
FR4	2000	0.3	1.300
AlN	3260	160	0.74

connector. This was expected to provide a low resistance path to the heat sink. However, the drain connector was a live electrical component. To ensure adequate voltage isolation, a spacer was introduced between the drain connector and heat sink. The spacer was required to be electrically insulating but thermally conducting. In this design, a 25 mil thick aluminum nitride (AlN) spacer was used to achieve this. This may be realized in one of two ways: 1) the spacer is bonded to the drain connector ad heat sink using a silver loaded epoxy compound, or 2) a DBC substrate with 25 mil AlN is bonded to the drain connector and heat sink using solder, sintering paste, or silver loaded epoxy. Fig. 4(a) shows a schematic depicting the implementation of the spacer. A thermal simulation was conducted to estimate the viability of the proposed method of thermal management for the flip-chip devices. A thermal load of 32 W was applied to one of the power MOSFETs to simulate the conduction and switching losses in the device during electrical operation. Care was taken to ensure that the decoupling capacitors were thermally and electrically isolated. The rated continuous operating temperature for these modules is 150–175 °C. In the proposed approach, the ceramic capacitors stay very close to room temperature as a result of the thermally isolated design. Fig. 4(b) shows the direction of heat spreading along the heat spreader and the thermal path.

In this article, solder material used could provide reliable operation for up to 90 °C. Fig. 4(c) shows that the maximum temperature of the power MOSFET under 32 W power dissipation is 90 °C. This maximum temperature target was dictated chiefly by the choice of solder balls used for the flip-chip device. This article used a commonly available and inexpensive solder, which loses structural integrity at temperatures beyond 100 °C. However, the demonstrated technology is not limited to operating at 100 °C. Using high-temperature solder spheres, high-temperature PCB material, and a better heat sink will allow 175 °C operation. The simulations were performed in ANSYS Workbench. The interposer was hidden from the active view in Fig. 4 to easily visualize the other components, but it was included in the simulation. The material properties used for the simulation are shown in Table I. Fig. 4(d) shows the temperature distribution across the flip-chip package. A temperature difference of about

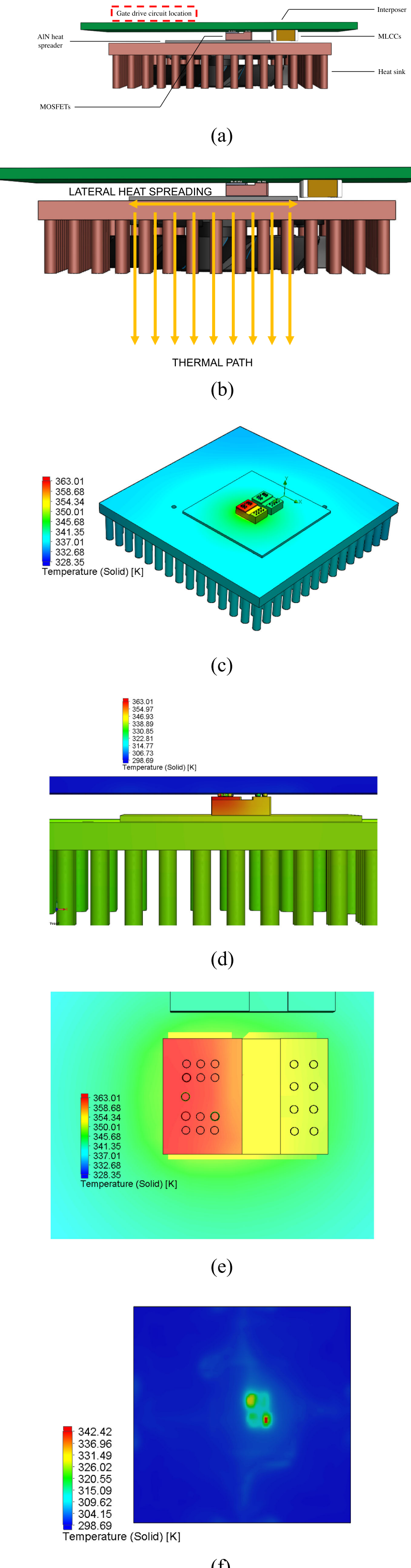


Fig. 4. Results of the thermal simulation showing (a) 3-D model used for this article, (b) thermal path, (c) thermal profile across the module (interposer hidden from active view), (d) zoomed-in view of the thermal profile across the flip-chip package, (e) side view of the module showing the vertical temperature distribution, and (f) top view of the temperature distribution across the interposer.

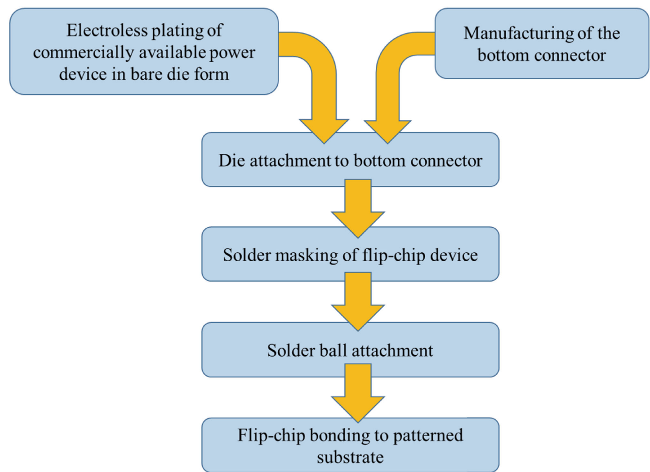


Fig. 5. Flowchart depicting the process flow for reconfiguring a bare die power device to a flip-chip capable component.

10°C indicated good heat spreading across the entire package. In addition, Fig. 4(e) shows that the dissipated heat was not transferred to the interposer, thus protecting the interposer and the components on the interposer from thermal damage. Fig. 4(f) shows a top view of the interposer and the maximum temperature of its top surface was found to be <70 °C. These results validated the choice of low-cost FR-4 material as the interposer in the proposed module. From the thermal simulation, the package junction-to-case thermal resistance was estimated to be 0.34 °C/W.

V. Prototyping and Electrical Testing

A. Device Prototyping

The prototyping of the flip-chip MOSFET device was developed as part of this article. Known-good processes for chip remetallization and solder bumping were reviewed, and the processes were customized for the existing package configuration. This section describes the detailed processes used to convert a bare die MOSFET into a flip-chip capable power package.

The fabrication followed the following five major steps:

1) remetallization of the aluminum top pads of the commercial power device in bare die form;
2) attachment of the remetallized die to the copper drain connector;
3) solder masking of the top surface to expose circular pads for solder ball bumping;
4) solder ball bumping;
5) flip-chip bonding to a patterned interposer/substrate.

The sequence of the process flow in depicted in Fig. 5.

The preliminary step in this process was remetallization. Commercially available SiC power devices are tailor-made for wire bonding. Hence, the top pads of these devices are aluminum for all commercial die manufacturers. An electroless nickel gold finish has been well established as a preferred remetallization process for aluminum bond pads as evidenced by the literature [36]. For this article, an electroless nickel finish was used. Adding the gold finish was found to be cost-prohibitive and would not add substantially to the results presented herein. However, for reliability studies using this approach it is highly

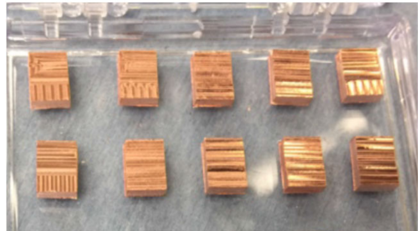


Fig. 6. Photograph showing a batch of CNC milled copper bottom connectors.

recommended that the top gold layer be included. Some process variations were necessary to form a uniform and highly adherent coating, but the underlying philosophy was identical to a standard electroless nickel plating process on an aluminum device pad. The process involved the stripping of the native oxide layer of the aluminum bond pad, followed by the deposition of a very thin zinc adhesion layer known as a zincate layer. The nickel layer was then deposited atop the zinc layer.

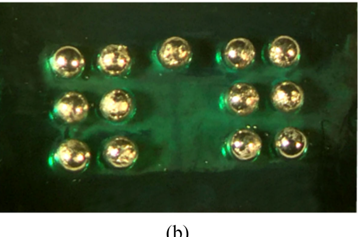
The bottom contact of the device was already plated with a solderable silver finish and needed to be protected from the electroless process for the top side. This was achieved by masking the bottom pad of the devices using an adhesive Kapton film. After the plating process was completed, the Kapton layer was removed, and the bottom pad was cleaned thoroughly using IPA. An interesting feature of choosing electroless plating was the self-patterning nature of the process. No additional photolithography (or masking) step and lift-off process was required—thus reducing the cost and complexity of the process. The die that went through the remetallization process were curve traced, and it was verified that the device characteristics remained unchanged.

The next step in the process was the attachment of the remetallized die to the metallic bottom connector. The connector was milled out of a 1.5-mm sheet of copper. The machined bottom connectors are shown in Fig. 6. The die attach material was SAC305 solder paste with a peak reflow temperature of 249 °C. A Sikama zone reflow oven was used for the die attachment process. The soak times in each zone were assigned to be 90 s.

The assembly was solder-masked using a UV-patternable dry film solder resist. The exposure time varies with the intensity of the UV light source and was optimized for the UV-source used for this article. The dry film was laminated on to the surface of the chip-scale package using a thermal laminator. A photolithography step was conducted on the sample through a photo-mask containing the solder ball array pattern. The development time was kept fixed at 6 min. It was found through a simple optimization that a 20 s exposure time yielded the desired 12 mil opening. Using a larger exposure time overexposed the solder masked and constricted the bond pad openings. Fig. 7(a) shows a photograph of a developed sample. It must be noted that the die is a dummy silicon chip with a metallization pattern matching the MOSFET used for this article.

Solder ball attachment was the next step of the process. A squeegee was used to stencil solder paste into the circular open pad areas on the chip-scale package. About 15 mil solder spheres were hand-placed on to the wet solder paste. The assembly was reflowed in a Sikama reflow oven. The melting temperature of the attachment solder paste was lower than the solder spheres. Hence, the spheres retained their shape but attached securely

(a)



(b)

Fig. 7. Pictorial representation of the ball-bumping process showing (a) bare die dummy die and (b) ball-bumped sample.

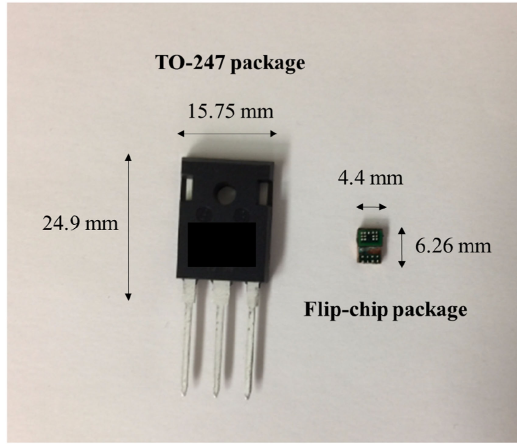
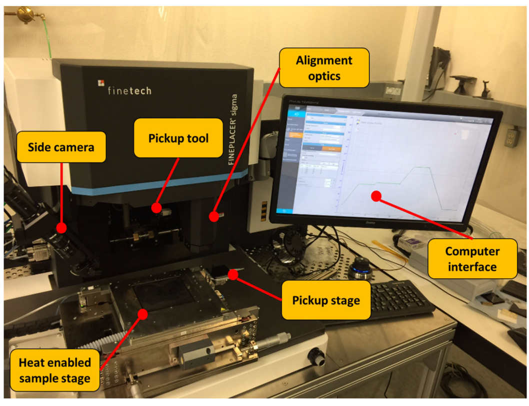


Fig. 8. Photograph of a ball-bumped sample alongside a TO-247 MOSFET package for comparison.

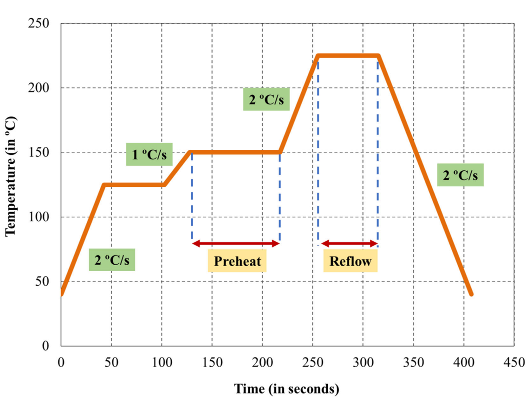
to the bond pads on the chip-scale package. The reflow step for the ball-attachment was accomplished using a Sikama zone reflow oven. The melting temperature of the low-temperature solder used for ball attachment (Sn42Bi58) was around 160 °C, with a prescribed reflow time of 60–80 s. However, process optimization using this solder paste revealed that 170 °C for 90 s was a satisfactory dwell time and temperature for the process. A photograph of a solder ball bumped sample is shown in Fig. 7(b).

The assembly was now capable of being flip-chip bonded on to a substrate with matching bond pads, much like a discrete MOSFET. However, the footprint of this device is approximately 14× smaller as compared with a discrete TO-247 device. Fig. 8 shows a photograph comparing a commercial TO-247 package with a finished and functional flip-chip package to illustrate this fact.

A Finetech Fineplacer flip-chip bonder was used for both die placement and reflow, and a labeled diagram depicting the same is presented in Fig. 9(a). Fig. 9(b) shows the reflow profile and Fig. 9(c) shows a photograph of the flip-chipped components after the reflow process. As a next step, the flip-chipped devices



(a)



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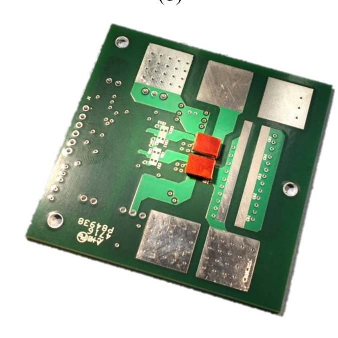
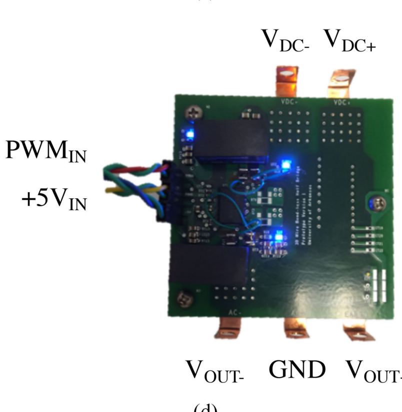


(c)



(d)

Fig. 9. (a) Photograph showing the Finetech Fineplacer used for assembly. (b) Reflow profile used for the process. (c) Photograph of the bottom of the interposer showing the flip-chip MOSFET packages bonded to the interposer. (d) Photograph of top of the interposer showing the gate drive circuit in operating condition.

were underfilled to provide additional mechanical support and electrical isolation. The underfill material was chosen so that it could provide adequate isolation between the gate and source solder balls. The gate leakage was less of a concern since the voltage across the gate and source solder balls experienced a very small voltage difference of 25 V. The isolation between the drain and the source and gate pads on the chip was a much greater concern since the voltage difference was equal to the maximum bus voltage. This could be as high as 900 V while using 1200 V power MOSFETs. To test the isolation capability of the stack, the drain and source terminals for each switch position were connected to a HiPOT tester set at 0.6 kV for 15 min to make sure that the devices blocked the rated voltage. Neither switch position showed any increase in the drain leakage current. This validated both the choice of materials and the electrical layout of the interposer to be able to block the desired dc bus voltage.

In the figure, $V_{\mathrm{OUT}+}$ and $V_{\mathrm{OUT}-}$ refer to the drain and source terminals of the low-side switch, across which the output waveforms are measured. The GND terminal refers to the chassis ground. The remaining components were then soldered on to the interposer. The gate driver circuit on the top side of the interposer was verified by powering the gate drive circuit with a 5-V signal and the respective PWMs. A photograph showing the gate drive circuit in working condition is presented in Fig. 9(d). The gate driver was capable of very fast rise and fall times of the order of 10 ns according to the datasheet, and also had the provision for a hardware adjusted dead-time to prevent a shoot-through condition. A 5-Ω gate drive resistor was used with an antiparallel Schottky diode to achieve an asymmetric turn OFF. This is a standard practice to reduce switching artifacts at high signal slew rates [37].

B. Electrical Testing

Once the gate drive circuit was verified, the switching characteristics of the module were evaluated using a double-pulse test. The gate and source terminals of the high-side MOSFET were electrically shorted. This effectively reduced the functionality of the high-side device to a diode. The switching pulses were then applied to the low-side devices, and switching responses were measured during the turn-ON and turn-OFF events. A schematic showing the circuit diagram is presented in Fig. 10(a), and a photograph of the test setup is shown in Fig. 10(b). A Tektronix TPS 2024, four-channel digital storage oscilloscope was used for this article. The probes were P5120 200 MHz passive high-voltage probes. The ground loop was shortened by using a short ground-probe torsion spring. This allowed for the capture of fast switching events with maximum precision. Low-bandwidth differential probes would not be able to capture switching artifacts which occurred on a nanosecond scale. In addition, the high bandwidth probes were fitted with a grounding coil spring to enable a very short measurement loop. The parasitic inductance of the power loop in the module is extremely low. Any additional stray inductance in the measurement circuit would show up as undesired erroneous spikes in the measured waveforms. Five 1 kV, 0.47 μF X7R 2220 ceramic capacitors were used across the dc bus. The *dV/dt* suppression circuit was not connected to the test circuit. There was no chassis connected to the module during testing, and the expectation of interference due to conducted EMI was low. The results of the double-pulse test are presented in Fig. 10.

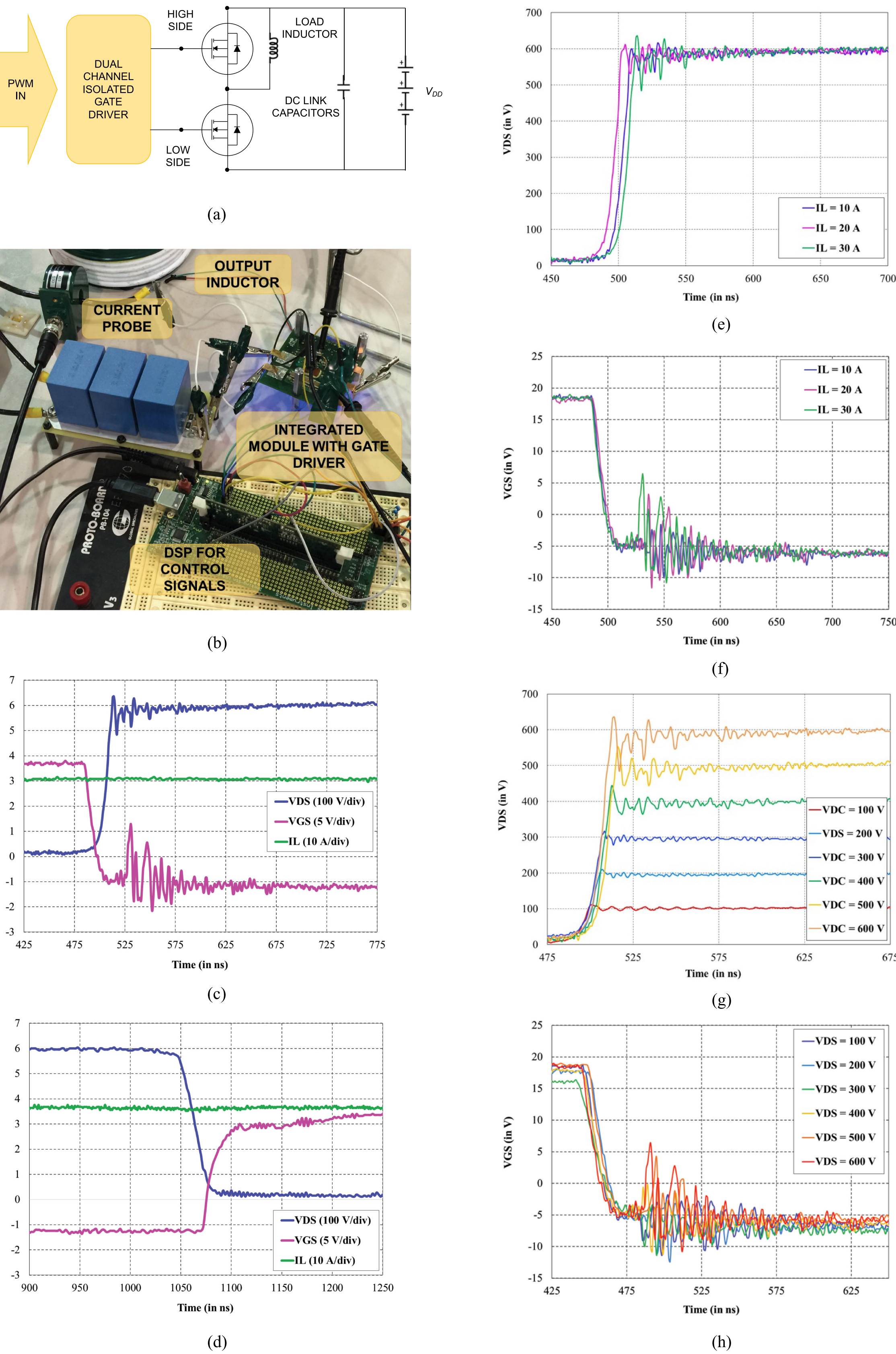
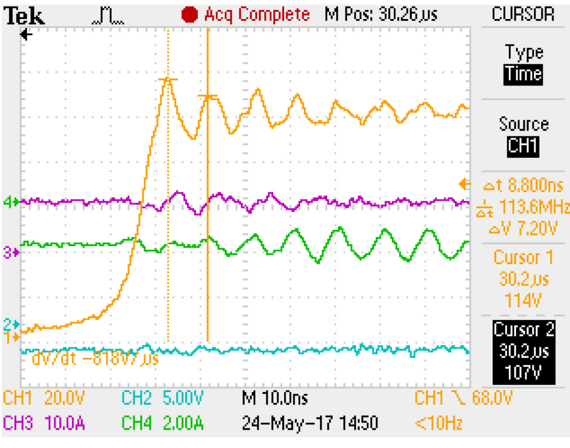
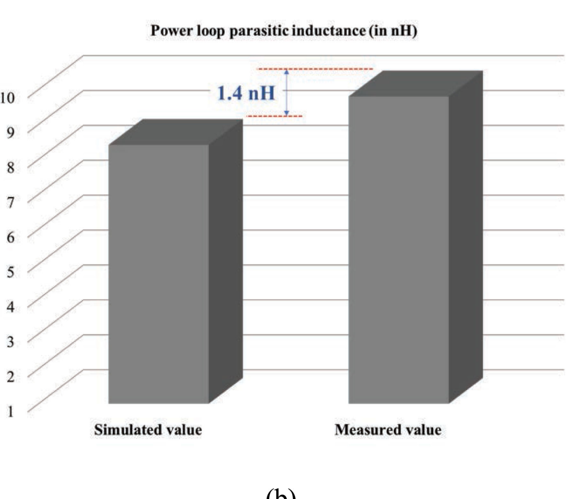


Fig. 10. Results of the double pulse test showing (a) schematic of the test circuit, (b) photograph of the test circuit, (c) turn-OFF event, (d) turn-ON event, (e) variation of V_{DS} with load current during the turn-OFF event, (f) variation of V_{GS} with load current during the turn-OFF event, (g) variation of V_{DS} with the dc bus voltage during the turn-OFF event, and (h) variation of V_{GS} with the dc bus voltage during the turn-OFF event.



(a)



(b)

Fig. 11. (a) Oscilloscope waveform showing the measurements for power loop inductance estimation. (b) Graph showing a comparison between the predicted and measured value.

Fig. 10(c) and (d) show the waveforms of the circuit operating at 600 V, while supplying a load current of 30 A. The turn-ON time for the MOSFET was only 28 ns, which corresponds to a *dv/dt* of 17 V/ns. It must be noted that the turn-ON for the MOSFET was controlled by a 5-Ω gate resistor. The turn-OFF time for the drain–source voltage was measured to be 20 ns, corresponding to a *dv/dt* of 24 V/ns. The turn-OFF is quicker since the gate signal bypasses the gate resistor through the anti-parallel diode. As mentioned before, the asymmetric turn-ON/OFF is a good practice for minimizing switching losses in SiC MOSFETs. However, despite intentionally slowing down the turn-ON event, there was no significant penalty in terms of time. It was very encouraging that the gate drive circuit remained stable under these aggressive *dv/dt* rates.

As a next step, the effect of increasing the load current was explored. For a particular voltage level, the current was controlled by varying the pulsewidth of the first pulse of the double-pulse signal using a LabVIEW interface. This allowed for controllably energizing the inductor to supply a desired load current. The bus voltage was set at 600 V, and the load current was varied between 10 and 30 A in steps of 10 A. The effect of increasing the load current is presented in Fig. 10(e) and (f). The effect of increasing *di/dt* was clearly apparent in the voltage waveforms. It must be noted here that the *di/dt* overshoot was dictated by the parasitic loop inductance as well as the measurement loop inductance. At these rapid slew rates, the inductance of the measurement probe may dominate the observed waveforms. Even though appropriate measures were taken to reduce the measurement loop inductance, it was a challenge to measure a gate–source loop with parasitics of the order of 1 nH. The overshoot may also be controlled by optimizing the resistance of the gate source loop, but this is beyond the scope of this article. Adding more resistance would also slow down the signal slew rate. The goal of this article was to determine the fastest slew rate possible with the proposed technology and achieving this safely by adding minimum gate–source resistance.

TABLE II
POWER LOOP PARASITIC INDUCTANCE ESTIMATION

Output capacitance of the S2301UCSF MOSFET at 100 VDC (Coss) (pF)	**Measured time-period of ringing (Δt) (ns)**	**Parasitic loop inductance (L_{loop}) = $\frac{(\Delta t/2\pi)^2}{C_{oss}} \times 10^3$ (nH)**
200	8.8	9.8

The effect of an increase in the dc bus voltage was also investigated. Fig. 10(g) shows the waveforms at bus voltages ranging from 100 to 600 V in steps of 100 V. The load current was fixed at 30 A. The drain–source voltage overshoot increased at 600 V but was still confined to 4.67%. The gate–source overshoot levels were confined to <0 V up to a bus voltage of 400 V, but increased at 500 and 600 V. The gate loop parasitic inductance was estimated to be <1.5 nH. As mentioned earlier, the inductance of the measurement loop and an unoptimized gate–source resistance gave rise to the artifacts observed in Fig. 10(h).

The estimated parasitic inductance of the power loop was verified by measuring the time period of the drain–source waveform [see Fig. 11(a)]. The oscillation in the drain–source waveform is dictated chiefly by the output capacitance of the MOSFET and the parasitic inductance in the drain–source loop. It was found that the estimated parasitic inductance was within 1.4 nH of the measured value [see Fig. 11(b)]. The details of this calculation are presented in Table II.

VI. CONCLUSION

In this article, a novel concept of an integrated wire bondless power module was demonstrated. A gate driver was closely integrated with the power devices, forming low inductance switching loops. The thermal performance of the module was also evaluated. Direct heat removal from the power device through the drain connector appeared to greatly decrease the thermal resistance compared with commercially available discrete packages. The benefit of the low parasitics manifested itself directly in the switching waveforms of the module. Very high

signal slew rates of ~24 V/ns were realized with <5% overshoot in the output voltage.

Wire bondless integration is the next major step forward for SiC power electronics. High parasitics and reliability concerns aside, wire bonding will be challenging as the current rating of SiC die increases. It is essential that the entire metallization area of the bare die be utilized to maximize the switching performance, current capacity and reliability of a power module. The demonstrated concept proposes a possible way forward for the wire bondless packaging of SiC devices and presents some of the major performance benefits.

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