A Universal Controller Under Different Operating States for Parallel Inverters With Seamless Transfer Capability

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***Abstract*—A universal controller is proposed in this article to operate parallel inverters in both grid-connected (GC) state and standalone (SA) state and ensure seamless transfer between them without reconfiguring the control structure. The universal controller is mainly composed of frequency-locked-loop and three cascaded control loops: a grid current loop, capacitor voltage loop, and inductor current loop. A proportional-integral regulator is adopted in the grid current loop, and a limiter is inserted after the integrator. In the GC state, the proposed controller accurately regulates the grid current of an individual inverter. When islanding occurs, the proposed controller can automatically convert from grid current control to v_C–i_g-based droop control; critical islanding detection is not needed. This universal controller has several advantages. First, it can realize seamless transfer of parallel inverters; microgrid reliability can be guaranteed in the SA state, and power sharing can be achieved among parallel inverters without communication lines. Second, compared with droop control, it can regulate the grid current accurately and output constant power when the grid voltage fluctuates in the GC state. Third, the grid current harmonics in the GC state and capacitor voltage harmonics in the SA state can be mitigated. Simulation and experimental results verify the effectiveness of the controller.**

***Index Terms*—Current droop control, grid-connected (GC) state, seamless transfer, standalone (SA) state.**

I. Introduction

DISTRIBUTED energy resources (DERs) have attracted increasing scholarly attention because they can alleviate stress in main transmission systems, improve system power quality, and reduce environmental pollution. The expansive penetration of DERs interfaced via power converters has introduced the concept of microgrids (MGs). An MG is a small-scale grid consisting of multiple DERs; electrical energy storage devices; and loads that are electrically interconnected and hierarchically controlled, which can operate in both grid-connected (GC) and standalone (SA) states.

The output voltage and output power of DERs are controlled by controlling inverters to achieve the following goals under different MG operating states according to grid availability.

1) Controlling the output power of inverters in the GC state according to set points determined by the MG central controller (MGCC).
2) Maintaining the stability of MG and load voltage via load tracking (i.e., maintaining a balance between production and consumption) when transitioning from the GC state to SA state.
3) Voltage regulation and accurate power sharing in the SA state [1].

Compared with objectives (1) and (3) in a steady state, a primary challenge involves seamless transfer from the GC state to SA state. The control targets in GC and SA states are noticeably different, which may burden interstate transfers with inrush currents and potential system crashes [2].

Therefore, two major control strategies have been proposed to realize seamless transfer from the GC state to SA state. The first approach is the hybrid current and voltage mode (HCVM) control method, and the second is the droop control method.

In the HCVM control method, the DER inverter operates under a current control mode (CCM) in the GC state but a voltage control mode (VCM) in the SA state [3]–[11]. In the GC state, these inverters can operate in parallel with other inverters based on active and reactive power (PQ) control. Most inverters belonging to DER systems operate in CCMs, as in photovoltaic (PV) or wind power systems. These inverters can participate in the control of the MG ac voltage amplitude and frequency by adjusting, at a higher level control layer, the references of active and reactive powers to be delivered [1]; however, inverters with CCM cannot operate in the SA state if there is no inverter to set the MG voltage amplitude and frequency. At least one inverter should therefore change to VCM in the SA state, and it is necessary to switch between two controller sets depending on the state. This task calls for a critical islanding detection scheme, which increases system complexity; the islanding detection requires time, varying from 20 ms to a few hundred ms. From the moment a utility outage begins (i.e., islanding occurs)

Manuscript received August 17, 2019; revised November 7, 2019 and January 8, 2020; accepted January 21, 2020. Date of publication February 3, 2020; date of current version May 1, 2020. This work was supported by the National Natural Science Foundation of China under Grant 51437007. Recommended for publication by Associate Editor M. Su. *(Corresponding authors: Zeng Liu; Jinjun Liu.)*

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Digital Object Identifier 10.1109/TPEL.2020.2970971

to the moment the controller is switched to VCM (i.e., islanding is detected), the load voltage is neither fixed by the utility nor regulated by the inverter. Accordingly, the load voltage quality may worsen during this period [12].

Various improved HCVM control methods have been proposed to overcome this drawback by switching the inverter from a CCM to a VCM without relying on islanding detection. When the grid is broken, some limiters in the control structure of the inverter will become saturated [13]–[19] or desaturated [12] to realize automatic switching of the control mode; therefore, the load voltage quality can be improved during the transition from the GC state to SA state. However, many of these improved HCVM control methods mainly focus on the seamless transfer of a single inverter. If an improved HCVM control method is applied to parallel inverters, they cannot operate normally in the SA state. They will change to constant amplitude and constant frequency (*V-f*) controlled voltage sources in the SA state, which will elicit a circulating current and prevent power sharing among them.

Under the droop control method, including virtual synchronous generator control as a special case, the parallel inverters in DERs operate in VCMs in GC and SA states. The droop control method is suitable for inverters in energy storage (ES) systems or for PV or wind power systems with ES equipment. These inverters can help regulate MG frequency and voltage by delivering appropriate active and reactive power values in GC and SA states. They can achieve seamless transfer from the GC state to SA state and realize power sharing in the SA state. However, if grid voltage fluctuates in the GC state, the objective (1) may fail and the inverter output power could deviate from its set point. Moreover, the droop control method does not control the inverter grid current directly; hence, its dynamics may be slow and distortion could follow from grid voltage harmonics.

Several improved droop control methods have been devised to solve these issues [2], [20]–[28]. An enhanced power flow control for droop-controlled inverters was suggested in [20], where the feedforward of grid frequency and voltage magnitude was adopted to mitigate the effects of grid fluctuation; however, reference switching occurred in different operating states. Control strategies for multimode operations of an online uninterruptible power supply (UPS) system were proposed [21], where UPS system inverters were based on droop control. The transfer between different operating modes was achieved by adjusting the reference value and control structure of droop control. Yet, the reference switching in [20] and adjustment to the reference and control structure in [21] both relied on islanding detection. If islanding occurs but has not yet been detected and the reference and control structure remain constant, undesirable transients may result. Karimi-Ghartemani *et al*. [22] presented a controller that was flexible in combining real and reactive power control with voltage and frequency support, which did not rely on islanding detection, but the grid current was still not controlled directly.

This article tries to address the above-mentioned research gaps by proposing a universal controller for parallel inverters. The universal controller is mainly composed of frequency-locked-loop (FLL) and three cascaded control loops: a grid current loop, capacitor voltage loop, and inductor current loop. A proportional-integral (PI) regulator is adopted in the grid current loop, and a limiter is inserted after the integrator. A PI regulator is adopted in the capacitor voltage loop, and a proportional (P)-regulator is adopted in the inductor current loop.

The proposed universal controller offers three advantages.

1) In the GC state, parallel inverters are controlled as current sources, and the grid current of an individual inverter is regulated by a PI regulator in the grid current loop to follow its reference value. Compared with the droop control method, the universal controller can regulate the grid current accurately and output constant power when the grid voltage fluctuates in the GC state.
2) When islanding occurs, the integrator in the grid current loop will be saturated, but the P-regulator will continue working and the inverters will transfer automatically from current sources to voltage sources based on v_C–i_g droop control without relying on islanding detection. The droop relationship is established between the inverter output capacitor voltage v_C and grid current i_g in the *dq* synchronous reference frame (SRF). Seamless transfer of parallel inverters is achieved, and uninterruptible load voltage is realized during the state transition. In the SA state, the combination of v_C–i_g droop control and an FLL block can realize power sharing among parallel inverters without communication lines.
3) Additionally, quasi-resonant (QR) controllers are adopted in the grid current loop and capacitor voltage loop. Compared with the droop control method, in the GC state, harmonics in the grid current caused by grid voltage distortion can be mitigated, and grid current quality can be improved. In the SA state, capacitor voltage harmonics caused by nonlinear loads connected at the point of common coupling (PCC) can be suppressed.

The rest of this article is organized as follows. In Section II, the control principle of the universal controller is introduced. Section III presents the design and analysis of the control parameters. Simulation and experimental results are summarized in Sections IV and V, respectively, to verify the effectiveness of the proposed controller. Finally, conclusions are given in Section VI.

II. Control Principle of the Universal Controller

In this section, the control principle of inverters with a universal controller is introduced in detail.

A. System Structure

A schematic diagram of parallel inverters and the main control block appear in Fig. 1. The dc voltage of the individual inverter is controlled by the front-end power electronic converter, both represented by the dc voltage source. The inverter output connects with an *LC* filter. $Z_{\rm line}$ denotes the line impedance between the DER and PCC. The transfer switch S_i is controlled by the MGCC, and the circuit breaker S_u is governed by the relay protection device. When the grid is normal, S_i and S_u are each closed. When the grid is broken, S_u turns OFF immediately, and

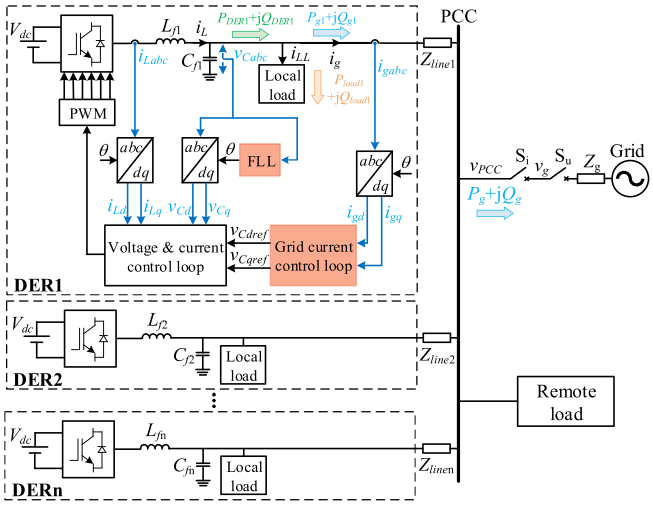


Fig. 1. Schematic diagram and control block of the universal controller.

an island forms. Once islanding is confirmed, S_i turns OFF. When the grid is restored, the circuit breaker S_u closes automatically. The PCC voltage should presynchronize with the utility voltage first, after which the transfer switch S_i turns ON to reconnect the MG with the utility. The inductor current i_{Labc}, capacitor voltage v_{Cabc}, and grid current i_{gabc} are sensed and used in the control loops. The PCC voltage $v_{\rm PCC}$ and grid voltage v_g of both sides of S_i are sensed to realize presynchronization.

The average model of power stage in SRF can be derived according to [15]. With the decoupling approach, the average model can be simplified into three single input single output systems, as shown in (1)–(3) and the subscript d and q are neglected

$$\frac{V_{\rm dc}}{2}\cdot d = L_f\cdot\frac{di_L}{dt} + R_{\rm ESR}\cdot i_L + v_C \tag{1}$$

$$i_L = C_f\cdot\frac{dv_C}{dt} + i_{LL} + i_g \tag{2}$$

$$v_C = L_{\rm line}\cdot\frac{di_g}{dt} + R_{\rm line}\cdot i_g + v_{\rm PCC} \tag{3}$$

where $V_{\rm dc}$ is the dc voltage, d is the average duty cycle, and $R_{\rm ESR}$ is the equivalent series resistance of the filter inductor L_f; i_L and v_C represent the inductor current and capacitor voltage, respectively; C_f is the capacitance of filter capacitor; i_{LL} is the local load current; i_g represents the grid current; $L_{\rm line}$ is the inductance component of $Z_{\rm line}$, $R_{\rm line}$ is the resistance component of $Z_{\rm line}$, and $v_{\rm PCC}$ is the PCC voltage. The transfer function from capacitor voltage v_C to grid current i_g can be represented as (4), and the grid current can be controlled by regulating the capacitor voltage in d- and q-axes, respectively

$$G_{ig\_v}(s) = \frac{i_g(s)}{v_C(s)} = \frac{1}{s\cdot L_{\rm line} + R_{\rm line}}. \tag{4}$$

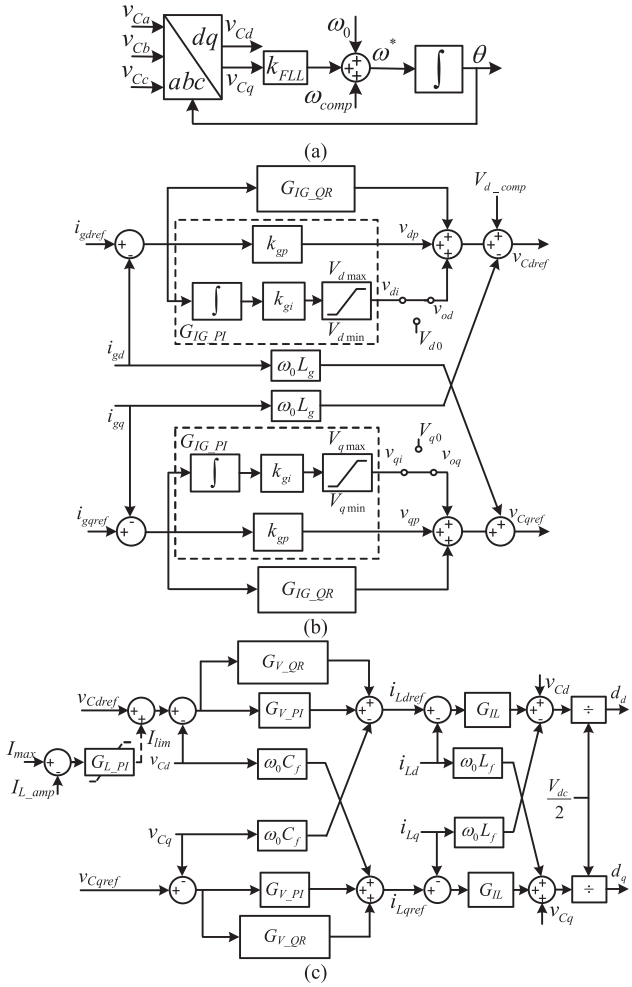


Fig. 2. Overall control diagram of the proposed controller. (a) FLL block. (b) Grid current loop. (c) Capacitor voltage loop and inductor current loop.

B. Control Scheme

The overall control block of the individual inverter is shown in Fig. 2, including the FLL block, grid current loop, capacitor voltage loop, and inductor current loop.

1) FLL Block: The FLL block is presented in Fig. 2(a); it is used instead of the phase-locked-loop (PLL) to estimate the frequency. On one hand, the FLL combines with the v_{Cq}–i_{gq} droop equation to form negative feedback control in the SA state; on the other hand, because the frequency is more stable than the phase angle, FLL is more robust against grid disturbance than PLL [29]. The compensation term $\omega_{\rm comp}$ is used to realize phase angle presynchronization of the PCC voltage $v_{\rm PCC}$ and grid voltage v_g, which will be introduced later. If the grid voltage is heavily polluted by the harmonics, the second-order generalized integrator—quadrature signal generators (SOGI-QSGs) can be used to extract the fundamental positive sequence components of capacitor voltage [30], as shown in the Appendix, which can improve the FLL performance.

2) Grid Current Loop: As indicated in Fig. 2(b), in the grid current loop, $i_{gd\rm ref}$ and $i_{gq\rm ref}$ denote grid current references, i_{gd} and i_{gq} are the actual grid currents on the d- and q-axes,

respectively; and $\omega_0 L_g$ is the decoupling item. A PI regulator G_{IG_PI} and QR regulator G_{IG_QR} are also used, where k_{gp} represents the coefficient of the P-regulator, and k_{gi} represents the coefficient of the integrator.

One noteworthy improvement is that a limiter is inserted after the integrator rather than after the PI regulator. In the GC state, the limiter does not restrict the output of the integrator, and v_{od} connects with v_{di} while v_{oq} connects with v_{qi}; therefore, the regulator G_{IG_PI} serves as a PI regulator to regulate the grid current to track its reference, and the inverters operate in CCMs. When the grid is broken, the limiter after the integrator becomes saturated and outputs the limiting value. The regulator G_{IG_PI} changes to a P-regulator to form v_C–i_g droop control, which will be explained in detail later.

The most common harmonics in grid voltage are the –5th and 7th harmonics [31], these change in the three-phase coordinating system to the –6th and 6th harmonics, respectively, in the SRF with rotating speed of fundamental angular frequency. The ±6th harmonics in the grid current are regulated to zero by the QR regulator with a resonance angular frequency of 6ω in the GC state. If harmonics of other times occur in the grid voltage, more QR regulators with different resonance angular frequencies can be added to the grid current loop. The QR regulator has been presented in many studies [32]–[34] and is not detailed here.

The compensation term V_{d_comp} on the *d*-axis is used to realize voltage amplitude presynchronization of the PCC voltage v_{PCC} and grid voltage v_g, which will be addressed later.

3) Capacitor Voltage Loop and Inductor Current Loop: Detailed structures of capacitor voltage loop and inductor current loop are depicted in Fig. 2(c), where v_{Cd} and v_{Cq} are actual capacitor voltages on the *d*- and *q*-axes, respectively; and $\omega_0 C_f$ is the decoupling item. Here, the voltage regulator also adopts a PI regulator G_{V_PI} and QR regulator G_{V_QR}. The current limitation term I_{lim} is added to the capacitor voltage reference to limit the inverter output current when the overload happens, where $I_{\max}$ is the maximum allowed output current of inverter and I_{L_amp} is the amplitude of output current of inverter. G_{L_PI} is a PI controller, and its upper limiting value is set as zero.

i_{Ld} and i_{Lq} are the actual inductor currents on the *d*- and *q*-axes, respectively; $\omega_0 L_f$ is the decoupling item; and the current regulator G_{IL} adopts a P-regulator. The capacitor voltage $v_{Cd,\,q}$ is added to the *d*- and *q*-axes to implement voltage feedforward control.

C. Operating Principle

The operating principle of an individual inverter with a universal controller will be introduced in four states: the GC state, the transition from the GC state to SA state, the SA state, and the transition from the SA state to GC state.

1) GC State: If the utility is ideal, the grid voltage is purely sinusoidal and only includes the fundamental component. If the utility is not ideal, the grid voltage may include the fundamental component and harmonics, which will lead to harmonics in the grid current.

The fundamental component in the three-phase coordinating system changes to a dc component in the SRF with a rotating speed of fundamental angular frequency. When the utility is normal, the regulator G_{IG_PI} operates as a PI regulator to regulate the dc components i_{f_gd} and i_{f_gq} of the grid current to follow their references $i_{gd\mathrm{ref}}$ and $i_{gq\mathrm{ref}}$, respectively, as shown in (5). The QR regulator G_{IG_QR} regulates the ±6th harmonics in grid current $i_{h6\_gd,q}$ to zero, as shown in (6)

$$\begin{cases} v_{f\_Cd\mathrm{ref}} = (k_{gp} + \frac{k_{gi}}{s}) \cdot (i_{gd\mathrm{ref}} - i_{f\_gd}) \\ v_{f\_Cq\mathrm{ref}} = (k_{gp} + \frac{k_{gi}}{s}) \cdot (i_{gq\mathrm{ref}} - i_{f\_gq}) \end{cases} \tag{5}$$

$$\begin{cases} v_{h\_Cd\mathrm{ref}} = \frac{2k_{ir6}\omega_c s}{s^2+2\omega_c s+(6\omega)^2} \cdot (0 - i_{h6\_gd}) \\ v_{h\_Cq\mathrm{ref}} = \frac{2k_{ir6}\omega_c s}{s^2+2\omega_c s+(6\omega)^2} \cdot (0 - i_{h6\_gq}) \end{cases} \tag{6}$$

where k_{ir6} is the integral coefficient, ω_c is the cutoff angular frequency, and 6ω is the resonance angular frequency of the QR regulator.

The voltage reference for the capacitor voltage loop is as follows:

$$\begin{cases} v_{Cd\mathrm{ref}} = v_{f\_Cd\mathrm{ref}} + v_{h\_Cd\mathrm{ref}} \\ v_{Cq\mathrm{ref}} = v_{f\_Cq\mathrm{ref}} + v_{h\_Cq\mathrm{ref}}. \end{cases} \tag{7}$$

For the capacitor voltage loop, the PI regulator G_{V_PI} regulates the dc component of capacitor voltage $v_{f\_Cd,q}$ to follow their references $v_{f\_Cd,q\mathrm{ref}}$, and the QR regulator G_{V_QR} is used to regulate the ±6th harmonics in capacitor voltage $v_{h\_Cd,q}$ to follow their reference $v_{h\_Cd,q\mathrm{ref}}$.

For the inductor current loop, the P-regulator G_{IL} is adopted to regulate the dc component and harmonics.

To simplify analysis, the grid voltage is assumed as purely sinusoidal. The exchanging power between the DER and PCC can be expressed as follows:

$$P_{dg} = \frac{3}{2} \cdot (v_{Cd} \cdot i_{gd} + v_{Cq} \cdot i_{gq}) \tag{8}$$

$$Q_{dg} = \frac{3}{2} \cdot (v_{Cq} \cdot i_{gd} - v_{Cd} \cdot i_{gq}). \tag{9}$$

As shown in Fig. 2(a), the phase angle of capacitor voltage is as follows:

$$\theta = \frac{1}{s} \cdot \omega^* = \frac{1}{s} \cdot (\omega_0 + k_{\mathrm{FLL}} \cdot v_{Cq}). \tag{10}$$

The power angle δ, namely the phase-angle difference between the capacitor voltage and PCC voltage is (11). If the grid is ideal, then the angular frequency of PCC voltage ω_{PCC} equals the nominal angular frequency ω_0

$$\begin{aligned} \delta &= \frac{1}{s} \cdot (\omega^* - \omega_{\mathrm{PCC}}) \\ &= \frac{1}{s} \cdot (\omega_0 + k_{\mathrm{FLL}} \cdot v_{Cq} - \omega_{\mathrm{PCC}}) = \frac{1}{s} \cdot (k_{\mathrm{FLL}} \cdot v_{Cq}). \end{aligned} \tag{11}$$

Because of the function of the PI regulator G_{IG_PI} in the grid current loop, the actual grid current i_{gd} and i_{gq} follow their respective references $i_{gd\mathrm{ref}}$ and $i_{gq\mathrm{ref}}$. According to (5), the voltage references $v_{Cd\mathrm{ref}}$ and $v_{Cq\mathrm{ref}}$ also remain constant. The actual capacitor voltages v_{Cd} and v_{Cq} are regulated to follow $v_{Cd\mathrm{ref}}$ and $v_{Cq\mathrm{ref}}$ and remain unchanged. According to (8) and (9), the exchanging power between the DER and PCC is kept constant. Therefore, v_{Cq} must be zero; otherwise, δ will continue

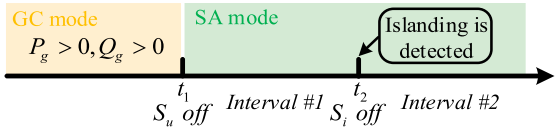


Fig. 3. Detailed transition process from the GC state to SA state.

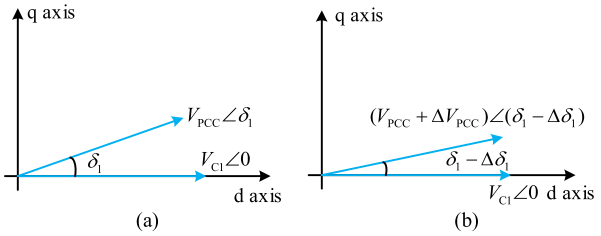


Fig. 4. (a) Phasor relationship before the utility outage. (b) Phasor relationship after the utility outage.

changing according to (11), and P_{dg} and Q_{dg} will keep changing as well.

Then, (8) and (9) can be simplified as follows:

$$P_{dg} = \frac{3}{2} \cdot v_{Cd} \cdot i_{gd} \tag{12}$$

$$Q_{dg} = -\frac{3}{2} \cdot v_{Cd} \cdot i_{gq}. \tag{13}$$

2) Transition From GC State to SA State: It is assumed that the MG injects real and reactive power into the utility in the GC state; that is, $P_g > 0$ and $Q_g > 0$, as shown in Fig. 1. The detailed transition process from the GC state to SA state is illustrated in Fig. 3. When the grid is broken and S_u turns OFF at t_1, P_g and Q_g each decline to zero. At this point, the output power of DERs remains nearly unchanged, and the remote load power is imposed on the output power of all DERs. Therefore, the amplitude and frequency of the remote load voltage rises and falls, respectively.

Before time t_1, the phasor relationship of the capacitor voltage of DER1 and the PCC voltage are shown in Fig. 4(a). The phase angle of the capacitor voltage is assumed to be 0°; thus, the phase angle of the PCC voltage is δ_1. The grid current of DER1 $i_{gd1} + ji_{gq1}$ can be calculated as (14), where X_{line1} is the reactance of Z_{line1}, and R_{line1} is the resistance of Z_{line1}

$$\begin{aligned} i_{gd1} + ji_{gq1} &= \frac{V_{C1}\angle 0 - V_{\text{PCC}}\angle\delta_1}{R_{\text{line1}} + jX_{\text{line1}}} \\ &= \frac{V_{C1} - V_{\text{PCC}}\cos\delta_1 - jV_{\text{PCC}}\sin\delta_1}{R_{\text{line1}} + jX_{\text{line1}}} \end{aligned} \tag{14}$$

$$i_{gd1} = \frac{(V_{C1} - V_{\text{PCC}}\cos\delta_1)R_{\text{line1}} + V_{\text{PCC}}X_{\text{line1}}\sin\delta_1}{R_{\text{line1}}^2 + X_{\text{line1}}^2} \tag{15}$$

$$i_{gq1} = \frac{-R_{\text{line1}}V_{\text{PCC}}\sin\delta_1 - X_{\text{line1}}(V_{C1} - V_{\text{PCC}}\cos\delta_1)}{R_{\text{line1}}^2 + X_{\text{line1}}^2}. \tag{16}$$

At time t_1, the amplitude and frequency of the remote load voltage will rise and fall; therefore, the phasor relationship changes to Fig. 4(b). The grid current $i_{gd1} + ji_{gq1}$ is then calculated as in (17) shown at the bottom of this page

$$\begin{aligned} i_{gd1} = &\frac{(V_{\text{PCC}} + \Delta V_{\text{PCC}})X_{\text{line1}}\sin(\delta_1 - \Delta\delta_1)}{R_{\text{line1}}^2 + X_{\text{line1}}^2} \\ &+ \frac{[V_{C1} - (V_{\text{PCC}} + \Delta V_{\text{PCC}})\cos(\delta_1 - \Delta\delta_1)]R_{\text{line1}}}{R_{\text{line1}}^2 + X_{\text{line1}}^2} \end{aligned} \tag{18}$$

$$\begin{aligned} i_{gq1} = &-\frac{R_{\text{line1}}(V_{\text{PCC}} + \Delta V_{\text{PCC}})\sin(\delta_1 - \Delta\delta_1)}{R_{\text{line1}}^2 + X_{\text{line1}}^2} \\ &- \frac{X_{\text{line1}}[V_{C1} - (V_{\text{PCC}} + \Delta V_{\text{PCC}})\cos(\delta_1 - \Delta\delta_1)]}{R_{\text{line1}}^2 + X_{\text{line1}}^2}. \end{aligned} \tag{19}$$

In the MG application with low voltage, the *R/X* ratio of line impedance is close to 7.7 [1]. Therefore, comparing (15) and (18), the *d*-axis grid current i_{gd1} declines when the grid is broken at t_1. Similarly, the *q*-axis grid current i_{gq1} increases at t_1 by comparing (16) and (19). As shown in Fig. 2(b), the input of the *d*-axis integrator in the grid current loop is larger than zero, and the output of the integrator increases. The input of the *q*-axis integrator in the grid current loop is smaller than zero, and the output of the integrator declines.

Whether the output of the integrator reaches the limiting value of the limiter depends on the amount of P_g and Q_g in the GC state. If the respective exchanging power P_g and Q_g are large, then the reduction in i_{gd} is large when the grid is disconnected, and the output of the integrator will continue increasing until reaching the upper limiting value $V_{d\max}$. At that point, v_{di} will be fixed at $V_{d\max}$ and v_{qi} will be fixed at $V_{q\min}$. Then, the voltage references will change to the following equation:

$$\begin{cases} v_{Cd\text{ref}} = k_{gp} \cdot (i_{gd\text{ref}} - i_{gd}) + V_{d\max} \\ v_{Cq\text{ref}} = k_{gp} \cdot (i_{gq\text{ref}} - i_{gq}) + V_{q\min}. \end{cases} \tag{20}$$

Conversely, if the respective amount of P_g and Q_g are small, then the reduction of i_{gd} is small when the grid is disconnected, i_{gd} is regulated to equal $i_{gd\text{ref}}$ before the output of the integrator reaches $V_{d\max}$. Regardless of the case, the output of the integrator is always between the lower and upper limiting values of the

$$\begin{aligned} i_{gd1} + ji_{gq1} &= \frac{V_{C1}\angle 0 - (V_{\text{PCC}} + \Delta V_{\text{PCC}})\angle(\delta_1 - \Delta\delta_1)}{R_{\text{line1}} + jX_{\text{line1}}} \\ &= \frac{V_{C1}}{R_{\text{line1}} + jX_{\text{line1}}} - \frac{(V_{\text{PCC}} + \Delta V_{\text{PCC}})\cos(\delta_1 - \Delta\delta_1) - j(V_{\text{PCC}} + \Delta V_{\text{PCC}})\sin(\delta_1 - \Delta\delta_1)}{R_{\text{line1}} + jX_{\text{line1}}} \end{aligned} \tag{17}$$

limiter. The output of the integrator on the *q*-axis can be analyzed similarly, and it consistently remains between $V_{q\min}$ and $V_{q\max}$. By designing appropriate limiting values, during the transition from the GC state to SA state, the capacitor voltage amplitude can be controlled within the allowable operation range.

3) SA State: As indicated in Fig. 3, after islanding has been confirmed at time t_2, S_i turns OFF. There are several islanding detection methods, which can be classified into two groups, namely, remote and local. In this proposed control method, because the voltage amplitude and frequency are always controlled within the allowed range, the local passive methods are failed; the local active method, such as the method proposed in [35], can be used in the universal controller. The inverter operates in a VCM in the SA state; the P-regulator is adopted in the grid current loop, forming v_{cd}–i_{gd}, v_{cq}–i_{gq} droop control. To improve the voltage quality in the SA state, once islanding is detected at t_2, v_{od} switches from v_{di} to V_{d0} and v_{oq} switches from v_{qi} to V_{q0}, as shown in Fig. 2(b). Here, V_{d0} is the nominal value of the capacitor voltage amplitude, and V_{q0} is zero. The QR regulator G_{IG_QR} in the grid current loop is also deactivated at t_2, and the control formula of the grid current loop changes to (the following equation:

$$\begin{cases} v_{Cd\text{ref}} = V_{d0} + k_{gp} \cdot (i_{gd\text{ref}} - i_{gd}) \\ v_{Cq\text{ref}} = V_{q0} + k_{gp} \cdot (i_{gq\text{ref}} - i_{gq}). \end{cases} \tag{21}$$

The real and reactive power can be shared approximately among DERs based on v_c–i_g droop control [36]–[38]. The output angular frequency ω^* of FLL is determined by v_{cq}, as shown in (10). The steady-state voltage error will be zero with the PI regulator G_{V_PI} in the capacitor voltage loop; therefore, v_{cq} serves as an intermediary between i_{gq} and ω^*. The relationship between ω^* and i_{gq} is presented in (22), and negative feedback results

$$\omega^* - \omega_0 = k_{\mathrm{FLL}} \cdot k_{gp} \cdot (i_{gq\text{ref}} - i_{gq}). \tag{22}$$

If i_{gq} is not equally shared among DERs, according to (22), the angular frequency ω^* of each inverter will differ, leading to a varying power angle δ. i_{gq} will also vary with varying power angle δ. Finally, ω^* of each inverter converge to the same value, and equal sharing of i_{gq} can be achieved.

The sharing of i_{gd} depends on grid line impedance. If the grid line impedances Z_{line} of different DERs are the same, then i_{gd} can be shared equally. However, if Z_{line} are different, then the v_{Cd}–i_{gd} droop relationship is useful for sharing i_{gd}. Even so, sharing error will persist due to unequal line impedance.

For the capacitor voltage loop, the QR regulator G_{V_QR} remains functional in the SA state to mitigate harmonics in the capacitor voltage. Because the QR regulator G_{IG_QR} in the grid current loop is deactivated, the reference $v_{h\_Cd,q\text{ref}}$ changes to zero. Harmonics in the capacitor voltage can be regulated to zero via the QR regulator G_{V_QR}.

4) Transition From SA State to GC State: If the grid returns to normal and S_u is closed, before turning ON S_i, the PCC voltage v_{PCC} should presynchronize with the grid voltage v_g first. Three steps are adopted in the reconnection process to reduce the inrush grid current.

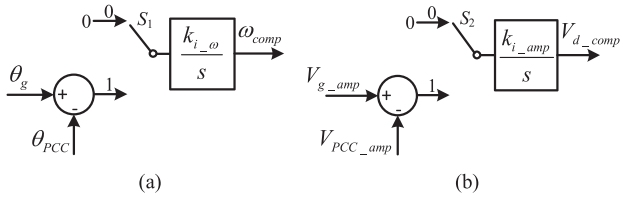


Fig. 5. Control block of (a) phase presynchronization and (b) voltage amplitude presynchronization.

First, when the grid returns to normal and switch S_u turns ON, v_{od} reconnects with v_{di} and v_{oq} reconnects with v_{qi}, see Fig. 2(b).

Second, the control switches S_1 and S_2 in Fig. 5 are connected with Channel 1 to realize amplitude and phase-angle presynchronization, where θ_g is the phase angle of the grid voltage, and θ_{PCC} is the phase angle of the PCC voltage; V_{g_amp} is the grid voltage amplitude, and $V_{\mathrm{PCC}\cdot\mathrm{amp}}$ is the PCC voltage amplitude; and k_{i_ω} and k_{i_amp} are the integral coefficients. Except for during the presynchronization process, the control switches S_1 and S_2 always connect with Channel 0.

Third, S_i turns to reconnect the MG with the utility. After some time, the limiter output in the grid current loop becomes desaturated, and the PI regulator G_{IG_PI} functions again. The QR regulator G_{IG_QR} in the grid current loop is then activated, and the compensation terms ω_{comp} and V_{d_comp} are reset to zero after the switch S_i turns ON.

D. Discussion of the Effect of Load Change on Control Mode Switching

When the load brings a large step change in the GC state, the output of the integrator in the grid current loop can reach the limiting value of limiter, and the control method will switch from grid current control to v_C–i_g droop control. This occurrence may result in an undesirable transient process as explained.

First, the influence of the local load change of one inverter on switching the control mode of parallel inverters is discussed. As displayed in Fig. 1, multiple inverters with the universal controller connect in parallel. When the local load of DER1 brings a large step change, the switching control mode of the inverters in DER1 and DER2 is analyzed.

The local active load of DER1 brings a large step change, increasing at instant t_1. The *d*-axis capacitor voltage v_{Cd1}will then decline, as well the *d*-axis grid current i_{gd1} at instant t_1. As shown in Fig. 2(b), the input of the *d*-axis integrator in the grid current loop is larger than zero, and the output of the integrator increases. If the local load increase is large enough, the decline in i_{gd1} is large and the output of the integrator will continue increasing to the upper limiting value $V_{d\max}$. Then, the capacitor voltage reference will change to (23). The reduction in i_{gd1} will cause an increase in $v_{Cd\text{ref}\ 1}$

$$v_{Cd\text{ref}1} = k_{gp} \cdot (i_{gd\text{ref}1} - i_{gd1}) + V_{d\max}. \tag{23}$$

Due to regulation of the PI regulator in the capacitor voltage loop, the *d*-axis capacitor voltage v_{Cd1} increases to follow $v_{Cd\text{ref}1}$. The relationship between the capacitor voltage

$v_{Cd1}+jv_{Cq1}$ and PCC voltage $v_{\mathrm{PCC}d}+jv_{\mathrm{PCC}q}$ can also be represented as follows:

$$v_{Cd1}+jv_{Cq1}=(R_{\mathrm{line1}}+jX_{\mathrm{line1}})\cdot(i_{gd1}+ji_{gq1})+v_{\mathrm{PCC}d}+jv_{\mathrm{PCC}q} \tag{24}$$

$$v_{Cd1}=R_{\mathrm{line1}}i_{gd1}-X_{\mathrm{line1}}i_{gq1}+v_{\mathrm{PCC}d} \tag{25}$$

$$v_{Cq1}=R_{\mathrm{line1}}i_{gq1}+X_{\mathrm{line1}}i_{gd1}+v_{\mathrm{PCC}q}. \tag{26}$$

Similarly, because in the MG application low voltage, the *R*/*X* ratio of line impedance is large, (25) and (26) can be simplified as follows:

$$v_{Cd1}=R_{\mathrm{line1}}i_{gd1}+v_{\mathrm{PCC}d} \tag{27}$$

$$v_{Cq1}=R_{\mathrm{line1}}i_{gq1}+v_{\mathrm{PCC}q}. \tag{28}$$

The increase in v_{Cd1} will stop the decline in i_{gd1} and then cause an increase in i_{gd1} according to (27). Therefore, the input of the *d*-axis integrator will decline, and the output of the integrator will reduce and gradually desaturate. The control method will ultimately return to grid current control from v_C–i_g droop control automatically. If the local reactive load of DER1 brings a large step increase, then the process is similar and is thus omitted here.

The step change in the local load of DER1 has no influence on the control mode of the inverter in DER2; the power consumed by the local load of DER1 is provided by DER1, and the local load change is undertaken by DER1. The capacity of DER1 and its local load size should be designed carefully to ensure DER1 can provide the power consumed by the local load plus the power injected into the PCC.

Second, the influence of the remote load change on switching the control mode of parallel inverters is analyzed. If the grid is strong (i.e., the grid line impedance Z_g in Fig. 1 is zero or small), when the remote load brings a large step change, it will be undertaken by the grid. Thus, it has no influence on the control mode of inverters in DER1 and DER2. While if the grid is weak (i.e., the grid line impedance Z_g in Fig. 1 is large), the remote load change will influence the control mode of inverters in DER1 and DER2. When the remote load brings a large step increase at time t_1, the output power of DERs remains nearly unchanged and is insufficient to meet remote load demand. Therefore, the amplitude and frequency of the remote load voltage falls and rises, respectively. Then, the analysis is similar with that during the transition from the GC state to SA state. It is easy to find that the *d*-axis grid current i_{gd1} increases and i_{gq1} declines at t_1. As shown in Fig. 2(b), the input of the *d*-axis integrator in the grid current loop is smaller than zero, and the output of the integrator declines. If the increase of remote active load is large, the increase of i_{gd1} is large and the output of the integrator will continue decreasing until reaching the lower limiting value $V_{d\min}$. Then, the analysis is similar with the condition of local active load change, but the change direction of variables is reverse. The control method will ultimately return to the grid current control from the v_C–i_g droop control.

Above all, no matter the local load of inverter or remote load brings a large step change in the GC state, if the control mode of inverter switches from the grid current control to v_C–i_g droop control, it can return to the grid current control automatically in the end, i.e., the control mode of inverters in DERs can achieve seamless switchover.

III. Analysis and Design of Control Parameters

In this section, the inverter with a proposed universal controller is analyzed and designed.

A. Analysis of Operating Points

In the GC state, the inverter is controlled as a current source by the grid current loop. The steady-state error of the fundamental component of the grid current is zero with the PI regulator in the grid current loop, and grid current harmonics are controlled to zero by QR regulators in the grid current loop and capacitor voltage loop; accordingly, the grid current in a steady state can be expressed by the following:

$$\begin{cases} i_{gd}=i_{gd\mathrm{ref}} \\ i_{gq}=i_{gq\mathrm{ref}}. \end{cases} \tag{29}$$

In the SA state, the inverter is controlled as a voltage source, and the voltage reference is produced by v_C–i_g droop control. The steady-state error of the fundamental component of the capacitor voltage is zero with the PI regulator in a capacitor voltage loop, and capacitor voltage harmonics are controlled to zero by the QR regulator in the capacitor voltage loop; as such, the capacitor voltage in a steady state is as follows:

$$\begin{cases} v_{Cd}=V_{d0}+k_{gp}\cdot(i_{gd\mathrm{ref}}-i_{gd}) \\ v_{Cq}=V_{q0}+k_{gp}\cdot(i_{gq\mathrm{ref}}-i_{gq}). \end{cases} \tag{30}$$

B. Limiter Design

During the transition from the GC state to SA state, the outputs of the *d*- and *q*-axes limiters $v_{d,qi}$ in the grid current loop can be different values according to the power flow direction of P_g and Q_g in Fig. 1. According to the analysis in Section II-C, if the exchanging power P_g and Q_g between the MG and utility in the GC state is small, then the output of the integrator may not reach the limiting values of limiter when the grid is disconnected. It is assumed that the exchanging power between the MG and utility is sufficient.

When the MG disconnects from the utility, the output of the *d*-axis limiter v_{di} in the grid current loop is determined by P_g, as shown in (31); similarly, v_{qi} is determined by Q_g, as in (32), where v_{Cd_GC} and v_{Cq_GC} are output values of the *d*- and *q*-axes limiters at the moment when the MG is disconnected from the utility, respectively

$$v_{di}=\begin{cases} V_{d\max}, & P_g>0 \\ v_{Cd\_\mathrm{GC}}, & P_g=0 \\ V_{d\min}, & P_g<0 \end{cases} \tag{31}$$

$$v_{qi}=\begin{cases} V_{d\min}, & Q_g>0 \\ v_{Cq\_\mathrm{GC}}, & Q_g=0 \\ V_{q\max}, & Q_g<0. \end{cases} \tag{32}$$

TABLE I
EXTREME VALUES DURING THE TRANSITION PROCESS FROM GC STATE TO SA STATE

The direction of power flow	$P_g>0$, $Q_g>0$	$P_g>0$, $Q_g<0$	$P_g<0$, $Q_g>0$	$P_g<0$, $Q_g<0$
Extreme value of v_{di}	V_{dmax}	V_{dmax}	V_{dmin}	V_{dmin}
Extreme value of v_{qi}	V_{qmin}	V_{qmax}	V_{qmin}	V_{qmax}
Extreme value of i_{gd}	i_{gdmin} A	i_{gdmin} A	i_{gdmax} A	i_{gdmax} A
Extreme value of i_{gq}	i_{gqmax} A	i_{gqmin} A	i_{gqmax} A	i_{gqmin} A
Extreme voltage amplitude	$\sqrt{\left(V_{dmax}-k_{gp}\cdot(i_{gdmin}-i_{gdref})\right)^2+\left(V_{qmin}-k_{gp}\cdot(i_{gqmax}-i_{gqref})\right)^2}$	$\sqrt{\left(V_{dmax}-k_{gp}\cdot(i_{gdmin}-i_{gdref})\right)^2+\left(V_{qmax}-k_{gp}\cdot(i_{gqmin}-i_{gqref})\right)^2}$	$\sqrt{\left(V_{dmin}-k_{gp}\cdot(i_{gdmax}-i_{gdref})\right)^2+\left(V_{qmin}-k_{gp}\cdot(i_{gqmax}-i_{gqref})\right)^2}$	$\sqrt{\left(V_{dmin}-k_{gp}\cdot(i_{gdmax}-i_{gdref})\right)^2+\left(V_{qmax}-k_{gp}\cdot(i_{gqmin}-i_{gqref})\right)^2}$

If the MG injects real or reactive power into the utility in the GC state, then the DERs should reduce their output power when the MG disconnects from the utility, When the grid currents i_{gd} and i_{gq} of DER are each zero, the output power of DER reaches its minimum value ($i_{gd\min}=0$ and $i_{gq\max}=0$). Conversely, if the MG absorbs real or reactive power from the utility in the GC state, the DERs shall output more real or reactive power when the MG disconnects from the utility. The maximum value of the d-axis grid current $i_{gd\max}$ and minimum value of the q-axis grid current $i_{gq\min}$ are determined by the inverter power rating. Combing (20), (31), and (32), extreme values during the transition from the GC state to SA state can be calculated as listed in Table I.

According to the IEEE standard 1547-2018 [40], the allowed voltage operating range is 0.88–1.1$V_{\rm nom}$, where $V_{\rm nom}$ is the nominal value of the capacitor voltage amplitude. Therefore, to ensure that the voltage magnitude is within the allowable range, the chosen limiting values shall comply with the following rules:

$$\sqrt{\begin{aligned}&(V_{d\max}-k_{gp}\cdot(i_{gd\min}-i_{gd\rm ref}))^2\\&+(V_{q\min}-k_{gp}\cdot(i_{gq\max}-i_{gq\rm ref}))^2\end{aligned}}\le 1.1\cdot V_{\rm nom} \quad (33)$$

$$\sqrt{\begin{aligned}&(V_{d\max}-k_{gp}\cdot(i_{gd\min}-i_{gd\rm ref}))^2\\&+(V_{q\max}-k_{gp}\cdot(i_{gq\min}-i_{gq\rm ref}))^2\end{aligned}}\le 1.1\cdot V_{\rm nom} \quad (34)$$

$$\sqrt{\begin{aligned}&(V_{d\min}-k_{gp}\cdot(i_{gd\max}-i_{gd\rm ref}))^2\\&+(V_{q\min}-k_{gp}\cdot(i_{gq\max}-i_{gq\rm ref}))^2\end{aligned}}\ge 0.88\cdot V_{\rm nom} \quad (35)$$

$$\sqrt{\begin{aligned}&(V_{d\min}-k_{gp}\cdot(i_{gd\max}-i_{gd\rm ref}))^2\\&+(V_{q\max}-k_{gp}\cdot(i_{gq\min}-i_{gq\rm ref}))^2\end{aligned}}\ge 0.88\cdot V_{\rm nom} \quad (36)$$

The d-axis upper limiting value $V_{d\max}$ should exceed the nominal value $V_{\rm nom}$, and the lower limiting value $V_{d\min}$ should be below the nominal value $V_{\rm nom}$, as shown in (37). In the GC state, v_{Cq} in a steady state is 0; thus, $V_{q\min}$ and $V_{q\max}$ should be symmetric, as indicated in (38)

$$\begin{cases}V_{d\max}>V_{\rm nom}\\V_{d\min}<V_{\rm nom}\end{cases} \quad (37)$$

$$V_{q\max}=-V_{q\min}>0. \quad (38)$$

The droop coefficient (proportional coefficient) k_{gp} is set to 0.4; the design procedure will be introduced later. The nominal phase-neutral capacitor voltage amplitude $V_{\rm nom}$ is 141.4 V. The d-axis grid current reference $i_{gd\rm ref}$ is set to 5 A, and $i_{gq\rm ref}$ is set to 0 A. The minimum of the d-axis grid current $i_{gd\min}$ is zero, and the maximum $i_{gd\max}$ is 10 A; the minimum of the q-axis grid current $i_{gq\min}$ is –5 A, and the maximum $i_{gq\max}$ is 0 A. Therefore, upon combining (33)–(38), we can select the limiting values as follows:

$$\begin{cases}V_{d\max}=1.08\cdot V_{\rm nom}=152.7\ \text{V}\\V_{d\min}=0.89\cdot V_{\rm nom}=125.8\ \text{V}\\V_{q\max}=0.09\cdot V_{\rm nom}=12.7\ \text{V}\\V_{q\min}=-0.09\cdot V_{\rm nom}=-12.7\ \text{V}.\end{cases} \quad (39)$$

C. Controller Design

1) Design of Voltage Loop PI Regulator $G_{V\_\rm PI}$: The voltage loop is used to regulate the capacitor voltage in GC and SA states, and the inner inductor current loop is used to improve the dynamic performance and damp the *LC* filter. For the inductor current loop, the small-signal model of the control-to-inductor current can be calculated as shown in (40). The transfer function of the delay introduced by digital control is represented by (41). The dual-updated operation mode of the program and pulsewidth modulation is adopted in digital control, such that the delay time T_d in (41) is set to one switching cycle [15]

$$G_{id}(s)=\frac{\hat{i}_L(s)}{\hat{d}(s)}=\frac{V_{dc}}{2}\cdot\frac{sC_f}{s^2L_fC_f+sR_{\rm ESR}C_f+1} \quad (40)$$

$$H_d(s)=\frac{s^2\frac{T_d^2}{12}-s\frac{T_d}{2}+1}{s^2\frac{T_d^2}{12}+s\frac{T_d}{2}+1}. \quad (41)$$

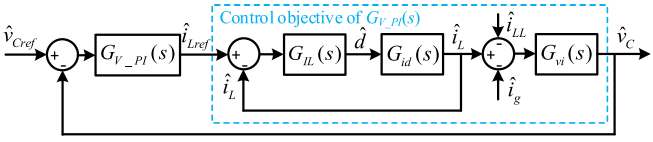


Fig. 6. Block diagram of the capacitor voltage loop and inductor current loop.

TABLE II
POWER STAGE PARAMETERS

Parameter	Value	Parameter	Value
DC voltage V_{DC}	400 V	Rated power of DER P_{DER}	10 KW
Filter inductor L_f	3 mH	R_{ESR}	0.019 Ω
Filter capacitor C_f	30 uF	Rated angular frequency of grid	50·2π rad/s
Grid-tied inductor	1 mH	Delay time T_d	$1\cdot10^{-4}$ s
Grid-tied resistor	1 Ω	Switching frequency	10 KHz

To simplify the design of inductor current loop, the delay is not considered in the derivation but will be covered in the final Bode plot. The P-regulator is adopted for G_{IL}, as shown in (42). The transfer function from the capacitor current to capacitor voltage is presented in (43). Then, the control object of the voltage compensator (i.e., the transfer function from the inductor current reference to the capacitor voltage, see Fig. 6) can be gained, which is expressed in (44)

$$G_{IL} = k_{GII} \tag{42}$$

$$G_{vi}(s) = \frac{\hat{v}_C}{\hat{i}_C} = \frac{1}{sC_f} \tag{43}$$

$$G_{v\_i\mathrm{Lref}}(s) = \frac{V_{\mathrm{dc}}}{2} \cdot \frac{k_{GII}}{s^2 L_f C_f + s(R_{\mathrm{ESR}} C_f + \frac{V_{\mathrm{dc}}}{2} C_f k_{GII}) + 1}. \tag{44}$$

It is clear that (44) is a typical second-order system, and the damping factor ζ is related to k_{GII}. k_{GII} can be calculated as (45). Therefore, k_{GII} can be designed according to the optimized damping factor ζ and is set at 0.0707

$$k_{GII} = \frac{2\xi\sqrt{\frac{L_f}{C_f}} - R_{\mathrm{ESR}}}{\frac{V_{\mathrm{dc}}}{2}} \approx \frac{4\xi}{V_{\mathrm{dc}}} \cdot \sqrt{\frac{L_f}{C_f}}. \tag{45}$$

Power stage parameters are shown in Table II, and the Bode plot of the control object of the voltage compensator is illustrated in Fig. 7 considering the delay (41).

Next, the voltage compensator G_{V_PI} can be designed conveniently. A PI regulator, expressed by (46), is used for the voltage compensator G_{V_PI}. The Bode plot of the voltage loop is shown

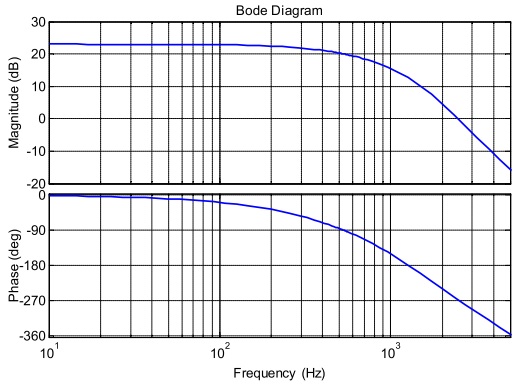


Fig. 7. Bode plot of the control object of voltage compensator.

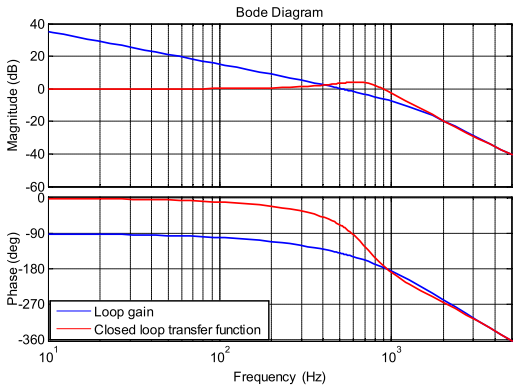


Fig. 8. Bode plot of the loop gain and closed-loop transfer function of the capacitor voltage loop.

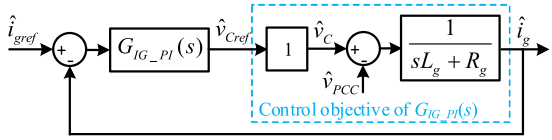


Fig. 9. Block diagram of the grid current loop.

in Fig. 8, where k_{PV} equals 0.058 and k_{IV} equals 254. The phase margin is set to approximately 40°, and the crossover frequency is roughly 510 Hz

$$G_{V\_\mathrm{PI}}(s) = k_{\mathrm{PV}} + \frac{k_{IV}}{s}. \tag{46}$$

2) Design of Grid Current Loop PI Regulator G_{IG_PI}: Because the bandwidth of the capacitor voltage loop is much larger than that of the external grid current loop, the grid current loop can be designed based on the ideal voltage loop, in which the gain of the closed-loop transfer function is in unity within full frequency range. The control object of the grid current compensator can be simplified as (4), as illustrated in Fig. 9.

The compensator G_{IG_PI} of the grid current loop adopts different forms in the GC state and SA state, respectively. In the

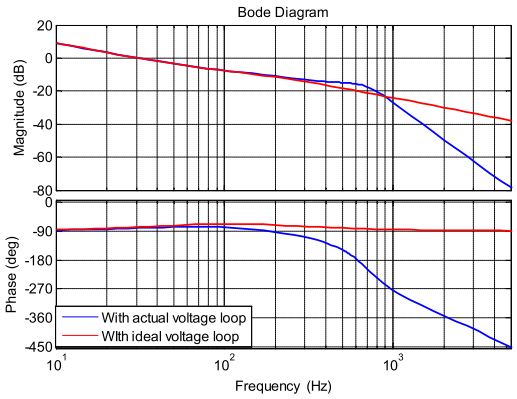


Fig. 10. Bode plot of the loop gain of grid current loop with ideal and actual voltage loop.

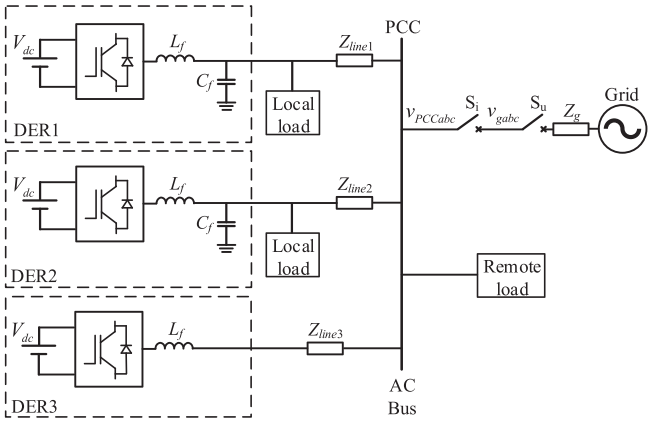


Fig. 11. Simulation circuit.

GC state, G_{IG_PI} operates as a PI regulator, where k_{gp} equals 0.4 and k_{gi} equals 180; the Bode plot of the loop gain of the grid current loop is shown in Fig. 10. The crossover frequency is 30.6 Hz, and the phase margin is approximately 102°. The Bode plot of the loop gain of the grid current loop with the actual voltage loop is also presented in Fig. 10. The Bode plots of these cases are nearly identical up to 300 Hz, larger than the bandwidth of the grid current loop. Therefore, simplification of the grid current loop design is reasonable.

In the SA state, the compensator G_{IG_PI} changes to a P-regulator, as shown in (21). To ensure that the load voltage magnitude is within the allowable range, the following rule should be obeyed:

$$\begin{cases} 0.88 \cdot V_{\text{nom}} \le v_{Cd} = V_{d0} + k_{gp} \cdot (i_{gd\text{ref}} - i_{gd}) \\ \qquad\qquad\qquad\quad \le 1.095 \cdot V_{\text{nom}} \\ -0.1 \cdot V_{\text{nom}} \le v_{Cq} = V_{q0} + k_{gp} \cdot (i_{gq\text{ref}} - i_{gq}) \\ \qquad\qquad\qquad\quad \le 0.1 \cdot V_{\text{nom}}. \end{cases} \tag{47}$$

Therefore, according to the setting values of $V_{d,q0}$, $i_{gd,q\text{ref}}$, the extreme values of $i_{gd,q}$ and (47), the proportional coefficient k_{gp} should comply with the following equation:

$$k_{gp} \le 2.68. \tag{48}$$

If k_{gp} is selected to be larger, according to (33)–(36), to ensure the voltage amplitude remains within the allowable range during the transition from the GC state to SA state, the limiting values of the limiter on the d- and q-axes should be set closer to the nominal values. However, to maintain normal functioning of the integrator in the GC state, the limiting range of the limiter cannot be too narrow. There is a tradeoff when selecting the proportional coefficient k_{gp}, which is ultimately set to 0.4 in this case.

The relationship between the angular frequency ω^* and q-axis grid current i_{gq} is shown in (22). To ensure the angular frequency is within the allowable range [39], the following rule should be obeyed:

$$2\pi \cdot 49.8 \le \omega^* = \omega_0 + k_{FLL} \cdot k_{gp} \cdot (i_{gq\text{ref}} - i_{gq}) \le 2\pi \cdot 50.2 \tag{49}$$

$$k_{\text{FLL}} \cdot k_{gp} \le 0.08 \cdot \pi \approx 0.25. \tag{50}$$

According to (50), when k_{gp} is 0.4, the maximum of k_{FLL} is 0.625. In this article, k_{FLL} is set as 0.6.

3) Design of QR Regulator G_{IG_QR} and G_{V_QR}: In the grid current loop and capacitor voltage loop, the QR regulator is used to mitigate grid current harmonics in the GC state and capacitor voltage harmonics in the SA state; see the following equation:

$$G_{\text{IG}(V)\_\text{QR}}(s) = \frac{2k_{ir6}\omega_c s}{s^2 + 2\omega_c s + (6\omega)^2}. \tag{51}$$

In the GC state, the QR regulator G_{IG_QR} is used to regulate the $\pm$6th harmonics in grid current to zero, and G_{V_QR} is used to regulate the $\pm$6th harmonics in capacitor voltage to follow its reference $v_{h\_Cd,q\text{ref}}$ when the grid voltage including harmonics. In the SA state, $G_{\text{IG\_QR}}$ in grid current loop is deactivated, the reference $v_{h\_Cd,q\text{ref}}$ changes to zero. The harmonics in capacitor voltage can be regulated to zero by the QR regulator G_{V_QR}.

The detailed design and analysis of the QR regulator have been discussed in [32]. With an increasing integral coefficient k_{ir6}, the gain of QR regulator at the resonance angular frequency increases. With a growing cutoff frequency ω_c, the gain and bandwidth of the QR regulator increase. Yet, an excessively large k_{ir6} will deteriorate the stability and convergence of the system, and an overly large ω_c will influence the frequency-selection characteristic of the regulator. Thus, there is a trade-off when selecting the integral coefficient k_{ir6} and cutoff frequency ω_c. In this article, k_{ir6} is set to 30 and ω_c is set to 5 rad/s.

IV. Simulation Verification

The simulation circuit is shown in Fig. 11 and the simulation parameters are listed in Table III. The first simulation is conducted to investigate the influence of a large load step change on switching the control mode of the inverters.

Initially, the local loads of master DER1 and DER2 are 80 Ω, and a 5 Ω resistor is added to the local load of master DER1 at 2 s. The d-axis grid current i_{gd1} and d-axis capacitor voltage v_{Cd1} each decline at 2 s, as shown in Fig. 12(a) and (b). Because the local load increase is sufficiently large, the reduction in i_{gd1} is also large, and the output of the integrator continues

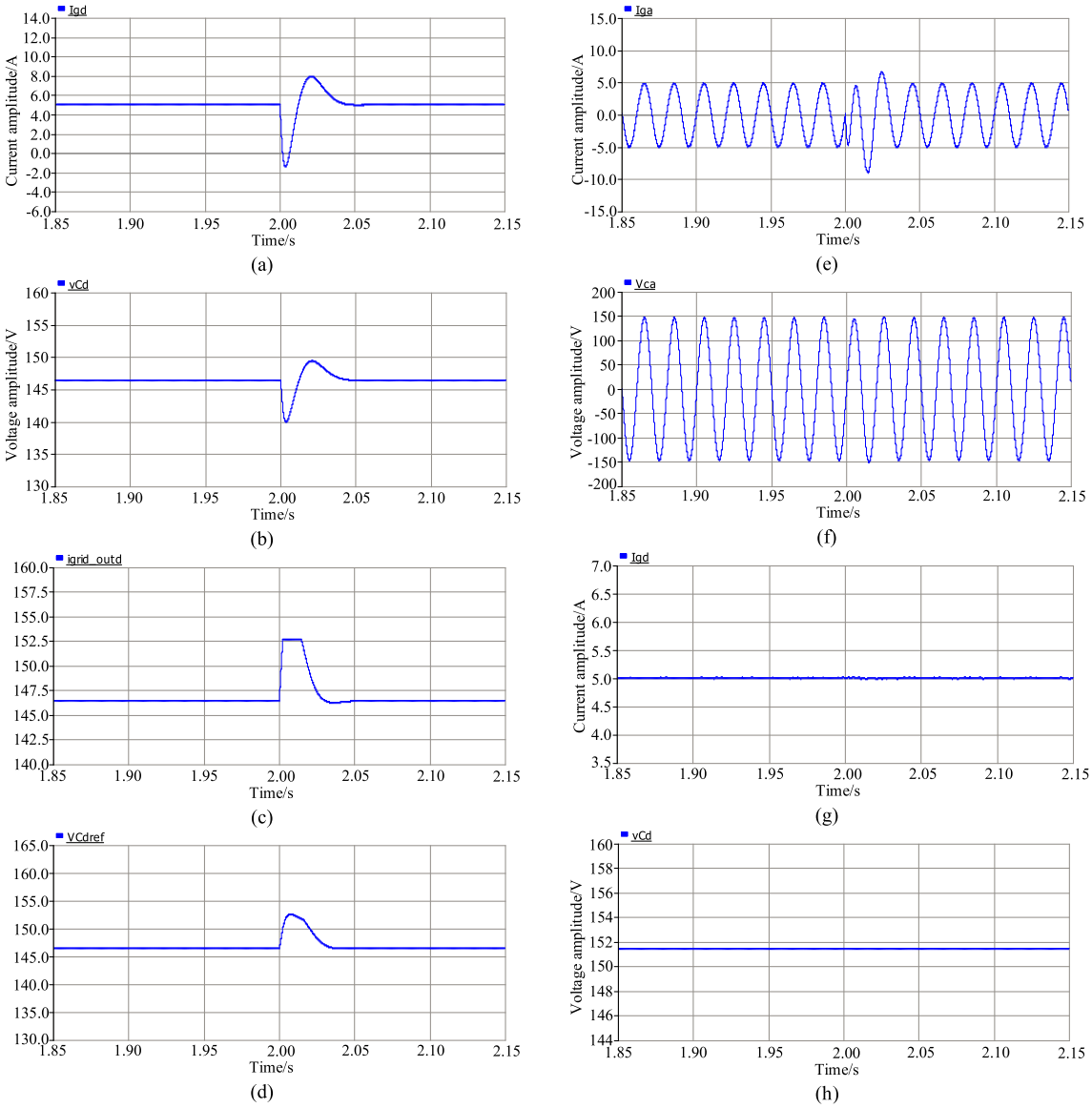


Fig. 12. Simulation results of master DER1 and DER2 when the local active load of master DER1 brings a large step increase at 2 s. (a) d-axis grid current i_{gd1} of master DER1. (b) d-axis capacitor voltage v_{Cd1} of master DER1. (c) Output of the d-axis limiter in grid current loop of master DER1. (d) d-axis capacitor voltage reference $v_{Cd\mathrm{ref}1}$ of master DER1. (e) Phase A grid current i_{ga1} of master DER1. (f) Phase A capacitor voltage v_{Ca1} of master DER1. (g) d-axis grid current i_{gd2} of master DER2. (h) d-axis capacitor voltage v_{Cd2} of master DER2.

increasing until reaching the upper limiting value $V_{d\max}$; see Fig. 12(c). Then, the capacitor voltage reference changes to (23), and the reduction in i_{gd1} causes an increase in $v_{Cd\mathrm{ref}1}$, as shown in Fig. 12(d). Due to regulation of the PI regulator in the capacitor voltage loop, the d-axis capacitor voltage v_{Cd1} increases to follow $v_{Cd\mathrm{ref}1}$. Additionally, the increase in v_{Cd1} stops the decline in i_{gd1} and leads to an increase in i_{gd1}. The input of the d-axis integrator will then reduce, and the output of the integrator will decline and desaturate gradually.

The grid current fluctuates at 2 s but can return to its reference ($i_{gd\mathrm{ref}1} = 5$ A, $i_{gq\mathrm{ref}1} = 0$ A) quickly; see Fig. 12(e). Although the capacitor voltage amplitude has some oscillations, the capacitor voltage is always controlled within the allowed range, as shown in Fig. 12(f).

The step change of the local load of master DER1 has no influence on the control mode of the inverter in master DER2. Due to length limitation, only simulation waveforms of the d-axis grid current i_{gd2} and capacitor voltage v_{Cd2} of the inverter in master DER2 are included in Fig. 12(g) and (h); both remain constant at 2 s. Above all, when the local load of DER brings a large step change, the control mode of inverters in DERs can achieve seamless switchover.

When the remote load brings a large step change at 2 s (initially, the remote load is 20 Ω, and a 3 Ω resistor is added to the remote load at 2 s), if the grid is strong (i.e., Z_g in Fig. 1 is zero), the d-axis grid current i_{gd1} and capacitor voltage v_{Cd1} of the inverter in master DER1 remain constant. If the grid is weak (i.e., Z_g in Fig. 1 is 3.5 mH), simulation results of i_{gd1},

TABLE III
SIMULATION PARAMETERS

Parameter	Value	Parameter	Value
DC voltage V_{DC}	400 V	Switching frequency	10 KHz
Filter inductor L_f	3 mH	Rated power of DER unit P_{DER}	10 KW
Filter capacitor C_f	30 uF	Rated angular frequency of grid	50·2π rad/s
DER1 line impedance Z_{line1}	1 Ω	DER2 line impedance Z_{line2}	2 Ω
DER3 line impedance Z_{line3}	1 Ω	Remote load	20 Ω
d-axis upper limiting value V_{dmax}	152.7 V	d-axis lower limiting value V_{dmin}	125.8 V
q-axis upper limiting value V_{qmax}	12.7 V	q-axis lower limiting value V_{qmin}	-12.7 V
Rated line-line voltage amplitude of utility	141.4 V		

v_{Cd1}, the output of the d-axis limiter, and the d-axis capacitor voltage reference are illustrated in Fig. 13(a)–(d), which is in accordance with the theoretical analysis. Similarly, the grid current fluctuates at 2 s but returns to its reference quickly; see Fig.13(e); and the capacitor voltage is always controlled within the allowed range, as shown in Fig. 13(f). Therefore, when the remote load brings a large step change, the control mode of inverters in DERs can also achieve seamless switchover.

The second simulation is conducted to verify that if the grid is heavily polluted by the harmonics, the SOGI-QSGs can be used in the FLL block to improve the FLL's performance. In the GC state, the 7th harmonic voltage with an amplitude of 10 V is added to the grid voltage at 2.2 s. As shown in Fig. 14, the angular frequency produced by the original FLL fluctuates heavily, while the fluctuation of angular frequency produced by the SOGI-QSG-based FLL decreases a lot.

V. EXPERIMENTAL VERIFICATION

To investigate the effectiveness of the universal controller, an experimental platform is established, as illustrated in Fig. 15. Experimental parameters are listed in Table IV.

The three-phase inverter has no neutral point; therefore, the line-to-line voltage is measured using a Tektronix DPO4014 oscilloscope. The MG platform includes four DERs, remote inductor and resistor loads, and an electrical load and grid simulator. The internal structure of the DER includes three layers: the three-phase inverter MWINV-9R144 and its I/O control board are in the top layer; the dc source, *LC* filters and switches are in the middle layer; and the transfer switch, line impedance, line impedance short-circuit switches, local load, and cooling fans are placed in the bottom layer.

The first experiment is conducted to verify the effectiveness of the proposed universal controller, which can realize the seamless transfer of parallel inverters with guaranteed uninterruptible load voltage during the state transition. Power sharing can be achieved among parallel inverters in the SA state. Three DERs are used in the first experiment: DER1 and DER2 operate with

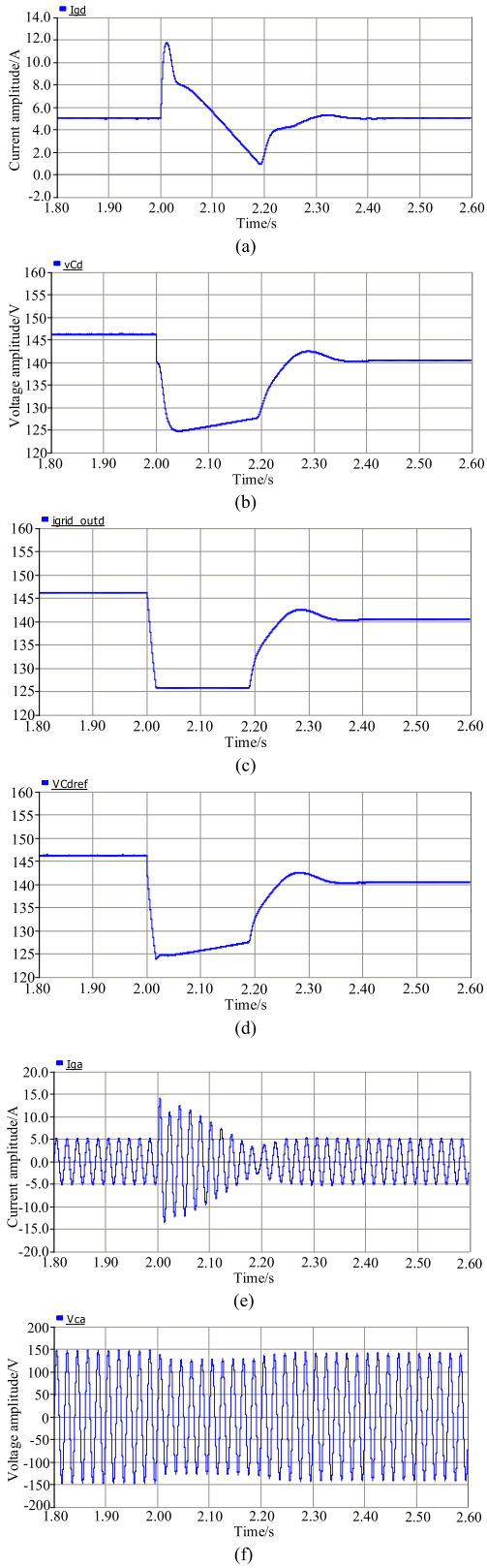


Fig. 13. Simulation results of master DER1 when the remote active load brings a large step increase at 2 s (a) d-axis grid current i_{gd1}. (b) d-axis capacitor voltage v_{Cd1}. (c) Output of the d-axis limiter in grid current loop. (d) d-axis capacitor voltage reference v_{Cdref1}. (e) Phase A grid current i_{ga1}. (f) Phase A capacitor voltage v_{Ca1}.

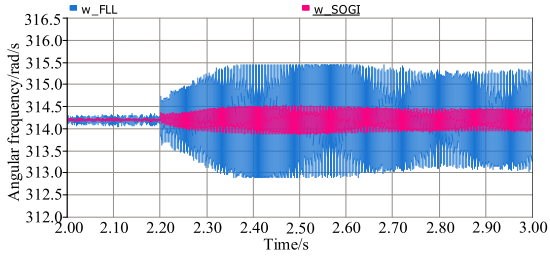
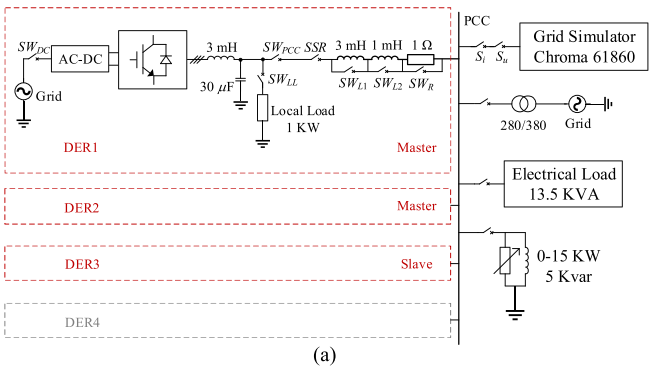
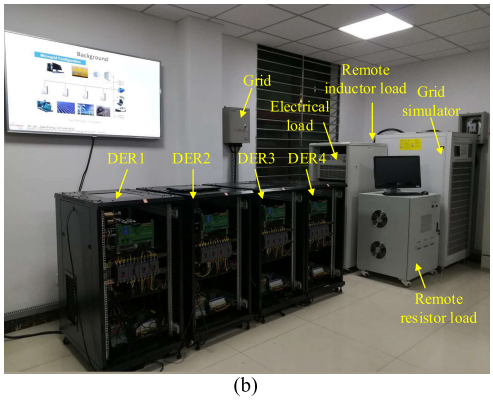


Fig. 14. Simulation waveforms of angular frequency produced by original FLL (blue line) and SOGI-QSG-based FLL (red line).



(a)

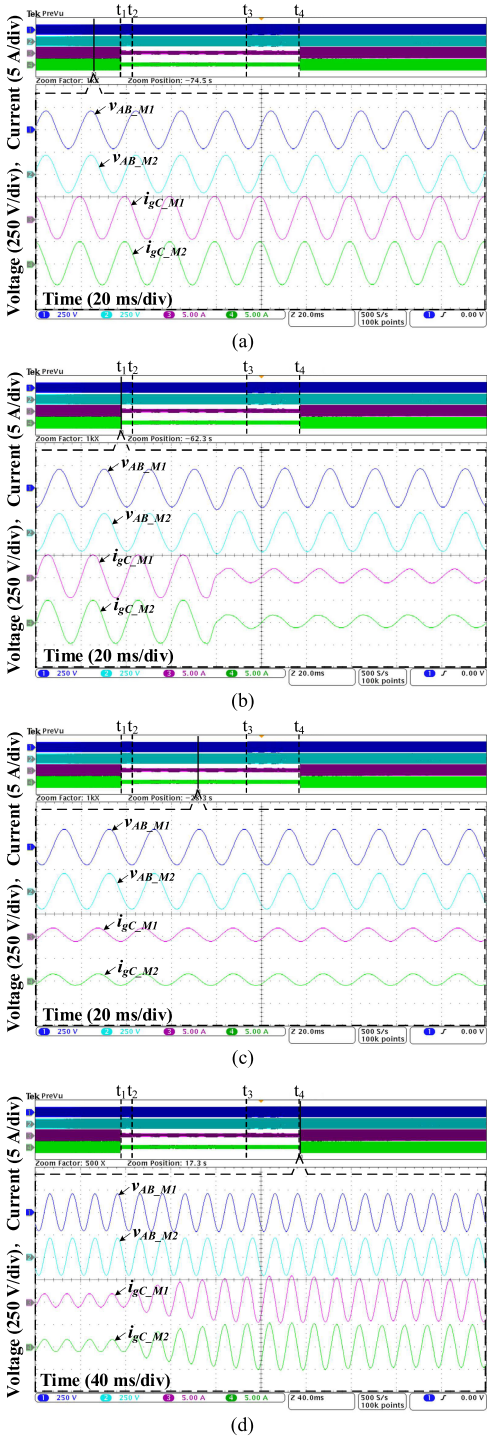


(b)

Fig. 15. Experimental platform. (a) Diagram. (b) Photograph.

TABLE IV
EXPERIMENTAL PARAMETERS

Parameter	Value	Parameter	Value
DC voltage V_{DC}	400 V	Switching frequency	10 KHz
Filter inductor L_f	3 mH	Rated power of DER unit P_{DER}	10 KW
Filter capacitor C_f	30 uF	Rated angular frequency of grid	50·2π rad/s
DER1 and 2 line impedance $Z_{line1,2}$	1 Ω + 4 mH	Remote load	20 Ω
DER3 line impedance Z_{line3}	3 mH	Rated line-line voltage amplitude of utility	141.4 V
d-axis upper limiting value V_{dmax}	152.7 V	d-axis lower limiting value V_{dmin}	125.8 V
q-axis upper limiting value V_{qmax}	12.7 V	q-axis lower limiting value V_{qmin}	-12.7 V



(a) (b) (c) (d)

Fig. 16. Experimental results of the capacitor voltage and grid current of DER1 and DER2 with the universal controller. (a) In the GC state. (b) During the transition from GC state to SA state. (c) In the SA state. (d) During the transition from SA state to GC state.

the universal controller, and DER3 is based on PQ control, as shown in Fig. 15(b). Experimental results are shown in Fig. 16.

The experimental scenario throughout the operating process is as follows.

1) Initially, the grid is normal, and the MG is connected to the grid.

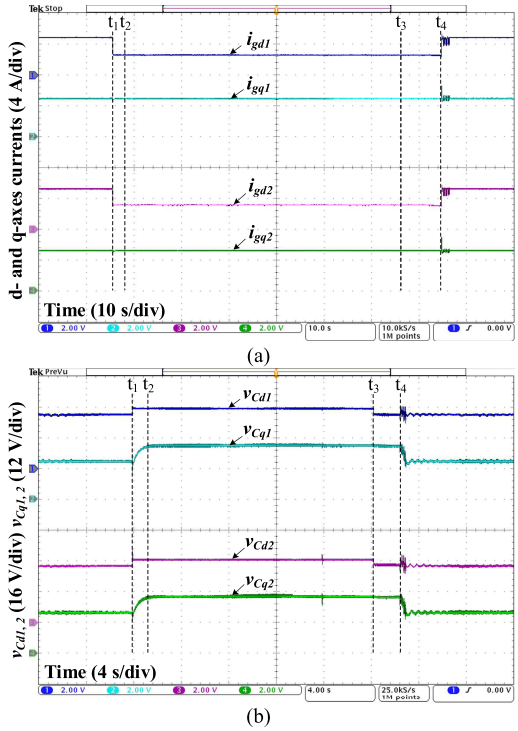


Fig. 17. Experimental results of DER1 and DER2 with the universal controller in the whole operation process (a) d- and q- axes grid currents. (b) d- and q-axes capacitor voltages.

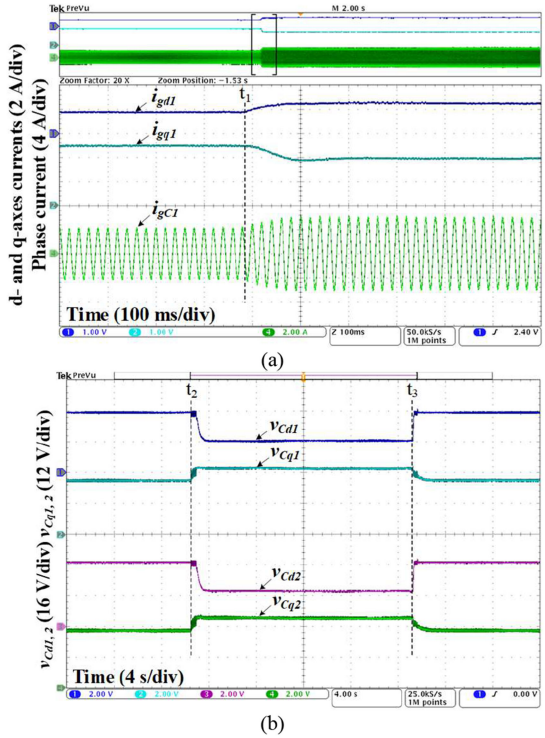


Fig. 18. Experimental results of DER1 and DER2 with the universal controller. (a) d-axis, q-axis, and Phase C grid currents in the GC state. (b) d- and q-axes capacitor voltages in the SA state.

2) At time t_1, the grid simulator stops outputting to indicate that the grid is broken, and S_u turns OFF.
3) At time t_2, islanding is confirmed and the transfer switch S_i turns OFF.
4) At time t_3, the grid simulator restarts outputting to indicate that the grid has been restored, and S_u is turned ON. At the same time, v_{od} switches from V_{d0} to v_{di} and v_{oq} switches from V_{q0} to v_{qi}.
5) At time t_4, the transfer switch S_i is turned ON. Presynchronization of the PCC voltage of the MG and grid voltage is completed during period t_3–t_4.

As shown in Fig. 16(a), DER1 and DER2 operate in CCMs before t_1. The magnitude of the grid current is 5 A and follows its reference value ($i_{gd\text{ref}} = 5\,\text{A}$, $i_{gq\text{ref}} = 0\,\text{A}$). During period t_1–t_2, the capacitor voltage quality is guaranteed during the transition from the GC state to SA state, as depicted in Fig. 16(b).

In the SA state, DER1 and DER2 are based on v_C–i_g droop control to provide voltage support. Because the line impedances are identical, real and reactive power are shared equally between the DERs, as shown in Fig. 16(c). No apparent inrush current or voltage distortion manifests during the reconnection process from the SA state to GC state; see Fig. 16(d).

Experimental results of the d- and q-axes capacitor voltages and grid currents of DER1 and DER2 are depicted in Fig. 17. Due to the oscilloscope channel limitation, the waveforms of grid current are shown in Fig. 17(a) first, and then the waveforms of capacitor voltage are shown in Fig. 17(b). The d- and q-axes components are the output analog signals of controller DSP28335.

The relationship between i_{gd} and analog signal is: 0–10 A correspond to 0–5 V, and the relationship between i_{gq} and analog signal is: –5–5 A correspond to 0–5 V. The relationship between v_{Cd} and analog signal is: 121.4–161.4 V correspond to 0–5 V, and the relationship between v_{Cq} and analog signal is: –15–15 V correspond to 0–5 V. In the GC state (before time t_1), the d- and q-axes grid currents $i_{gd1,2}$ and $i_{gq1,2}$ are 3 and 0 A, respectively, and follow their references ($i_{gd\text{ref}} = 3\,\text{A}$, $i_{gq\text{ref}} = 0\,\text{A}$). The d-axis capacitor voltage $v_{Cd1,2}$ increases at t_1 due to the decline in $i_{gd1,2}$; $v_{Cq1,2}$ also increases at t_1 because of the coupling caused by resistive and inductive line impedance. When the MG reconnects with grid at t_4, the d- and q-axes capacitor voltages and grid currents return to their original values before time t_1.

In the GC state, as illustrated in Fig. 18(a), when the d-axis grid current reference $i_{gd\text{ref}}$ changes from 2 to 3 A, and $i_{gq\text{ref}}$ changes from 0 to –1 A at t_1, the actual grid current of the inverter can follow the change accurately. In the SA state, as shown in Fig. 18(b), when the remote load changes from 20 to 10 Ω at t_2, v_{Cd1} and v_{Cd2} decline due to the increase in i_{gd1} and i_{gd2}; v_{Cq1} and v_{Cq2} increase because of the coupling. When the remote load changes conversely at t_3, the d- and q-axes capacitor voltages return to their original values.

In the SA state, as illustrated in Fig. 19(a), when the grid returns to normal at t_1, the control switches S_1 and S_2 in Fig. 5 connect with Channel 1. The output of integrator ω_{comp} and V_{d_comp} change to regulate the output voltage frequency and amplitude of inverters in DER1 and DER2. The relationship between ω_{comp} and analog signal is: –1–1 rad/s correspond to 0–5 V, and the relationship between V_{d_comp} and analog signal

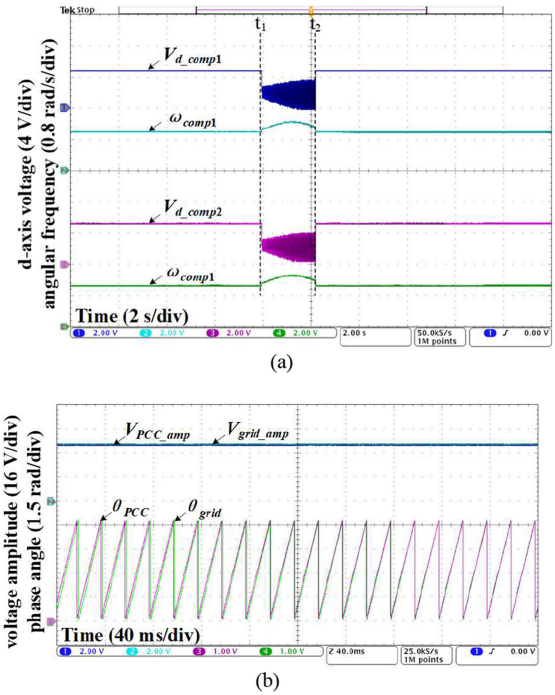


Fig. 19. Experimental results during the reconnection process. (a) Output of integrator in pre-synchronization control block. (b) Amplitude and phase angle of MG PCC voltage and grid voltage.

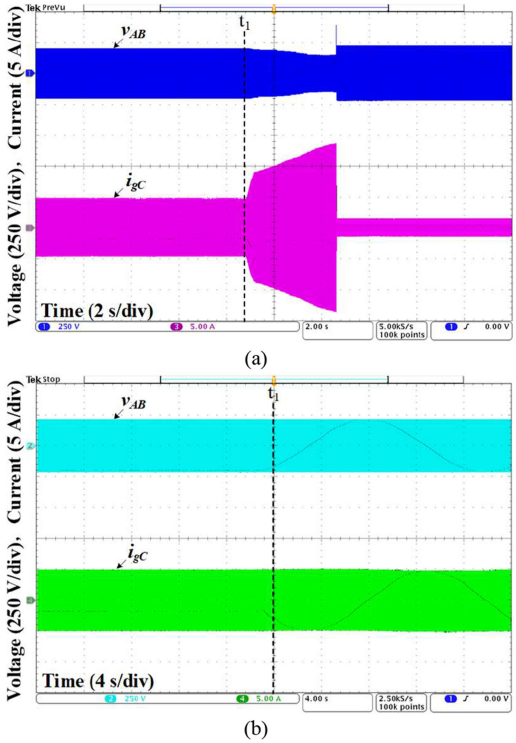


Fig. 20. Capacitor voltage and grid current of DER1 when the grid voltage frequency changes from 50 to 49.95 Hz at t_1 in the GC state. (a) Conventional droop control. (b) Proposed control method.

is: –5–5 V correspond to 0–5 V. The amplitude and phase-angle of the PCC voltage of the MG and the grid voltage during the reconnection process are illustrated in Fig. 19(b). It is easy to find that the amplitude and phase-angle are each getting closer. The relationship between $V_{\mathrm{PCC\_amp}}$ ($V_{\mathrm{grid\_amp}}$) and analog signal is: 121.4–161.4 V correspond to 0–5 V, and the relationship between θ_{PCC} (θ_{grid}) and analog signal is: 0–7.5 rad correspond to 0–5 V.

The second experiment is conducted to verify that compared with droop control, the proposed controller can regulate the grid current accurately and output constant power when the grid voltage fluctuates in the GC state. Experimental results appear in Fig. 20.

In the first case, DER1 and DER2 are based on droop control, and DER3 is based on PQ control. In the second case, DER1 and DER2 operate via the universal controller, and DER3 is based on PQ control. In the GC state, when the gird frequency drops from 50 to 49.95 Hz at t_1, the grid current of DER1 increases substantially under traditional droop control (pink line), as shown in Fig. 20(a), thus triggering inverter protection. However, the grid current of DER1 remains constant with the universal controller (green line), as shown in Fig. 20(b).

The third experiment is conducted to verify that when the grid voltage includes harmonic in the GC state, compared with the inverter based on droop control, grid current harmonics can be mitigated and the grid current quality of the inverter with the proposed controller can be improved. Experimental results are depicted in Fig. 21.

Similarly, for the first time, DER1 and DER2 are based on droop control, and DER3 is based on PQ control. For the second time, DER1 and DER2 operate with the universal controller, and DER3 is based on PQ control. In the GC state, the 7th harmonic voltage with an amplitude of 5 V is added to the grid voltage at time t_1. As shown in Fig. 21(a) and (b), the grid current is distorted and includes harmonics with traditional droop control (pink line). As shown in Fig. 21(c), the grid current is also distorted at t_1 with the proposed universal controller. However, after some time, harmonics in the grid current are regulated to zero, and the grid current approximates a pure sinusoidal wave, as indicated in Fig. 21(d).

The fourth experiment is also conducted to verify that when the grid voltage includes harmonics in the GC state, harmonics in the grid current can be mitigated by the proposed controller. Experimental results appear in Fig. 22. As the 7th harmonic grid voltage amplitude increases, the corresponding grid current amplitude of the inverter based on droop control increases clearly, whereas the 7th harmonic grid current amplitude of the inverter based on the proposed controller is suppressed.

The fifth experiment is conducted to verify that in the SA state, capacitor voltage harmonics caused by nonlinear loads connected at the PCC can be suppressed by the proposed controller. An uncontrolled rectifier load is connected at the PCC, and the capacitor voltage mainly includes –5th, 7th, –11th, and 13th harmonics. Experimental result is presented in Fig. 22. As shown in Fig. 23(a) and (c), the –5th and 7th harmonics in the capacitor voltage of the inverter based on droop control are large.

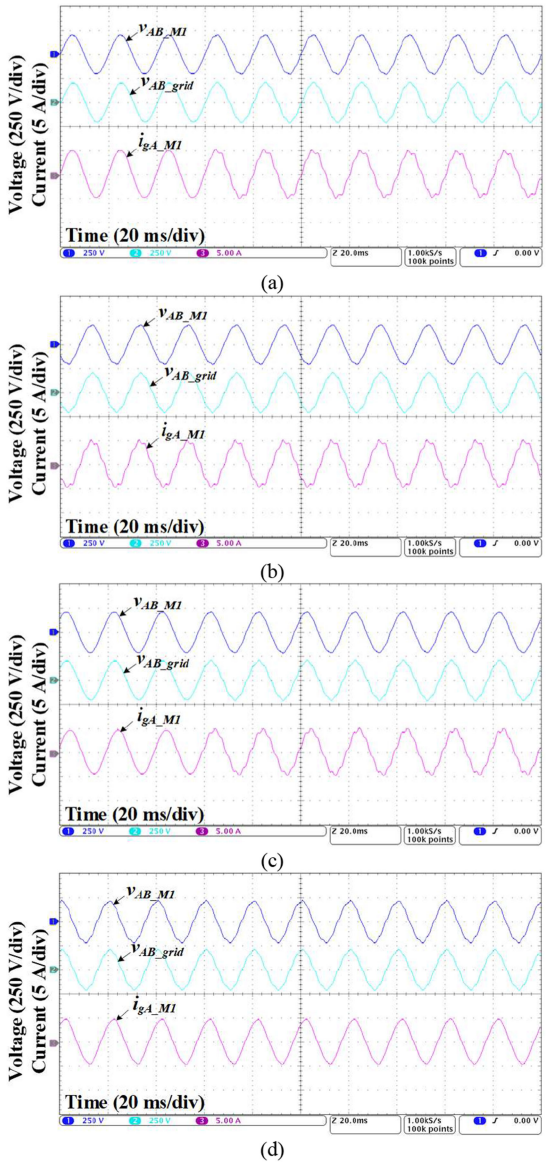


Fig. 21. Capacitor voltage and grid current of DER1 when the seventh harmonic voltage is added in the grid voltage at t_1 in the GC state. (a) Waveforms of droop control-based inverter at t_1. (b) Waveforms of droop control-based inverter after t_1. (c) Waveforms of inverter with universal controller at t_1. (d) Waveforms of inverter with universal controller after t_1.

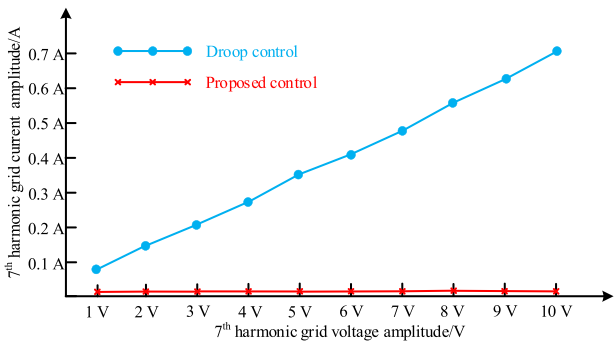
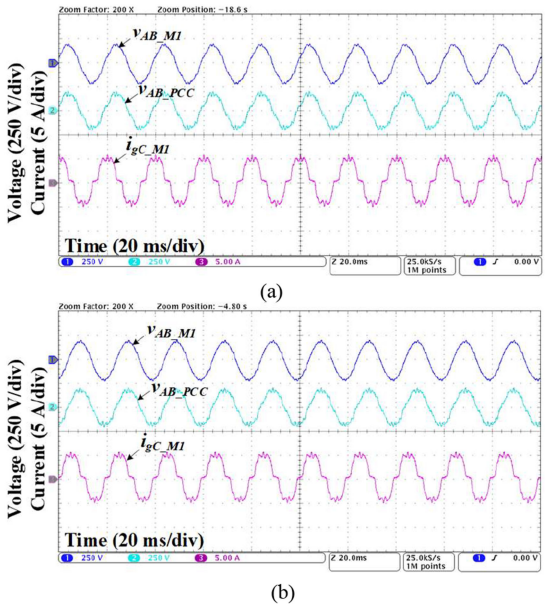


Fig. 22. Grid current harmonic of inverter based on droop control and proposed control with the increasing of seventh harmonic grid voltage amplitude.



Order	U1 [V]	hdf[%]	Order	U1 [V]	hdf[%]	Order	U1 [V]	hdf[%]	Order	U1 [V]	hdf[%]
Total	142.9		dc	----------	-------	Total	142.9		dc	----------	-------
1	142.8	99.88	2	0.2	0.14	1	142.9	99.98	2	0.2	0.16
3	1.5	1.03	4	0.0	0.03	3	1.5	1.03	4	0.1	0.04
5	5.1	3.55	6	0.1	0.04	5	0.3	0.22	6	0.0	0.03
7	3.3	2.32	8	0.1	0.09	7	0.2	0.13	8	0.1	0.05
9	0.1	0.07	10	0.1	0.09	9	0.2	0.15	10	0.1	0.05
11	1.5	1.02	12	0.1	0.05	11	1.5	1.07	12	0.0	0.03
13	2.1	1.45	14	0.1	0.05	13	1.6	1.13	14	0.1	0.07
15	0.5	0.38	16	0.2	0.15	15	0.6	0.43	16	0.2	0.13

(c) (d)

Fig. 23. Experimental results in the SA state with nonlinear load. (a) Capacitor voltage and grid current of inverter based on droop control. (b) Capacitor voltage and grid current of inverter with proposed controller. (c) THD of capacitor voltage of inverter based on droop control. (d) THD of capacitor voltage of inverter with proposed controller.

Yet, the universal controller can mitigate these harmonics in the capacitor voltage, as shown in Fig. 23(b) and (d).

The sixth experiment is conducted to verify that the proposed controller can achieve seamless switchover no matter the local load or the remote load brings a large step change in the GC state. The relationship between v_{Cd} and analog signal is: 0–200 V correspond to 0–5 V, and the relationship between i_{Ld} and analog signal is: 0–20 A correspond to 0–5 V. As shown in Fig. 24, when the local load or remote load changes from no load to 20 Ω at t_1, the capacitor voltage has some oscillations, but it is always controlled within the allowed range. The grid current fluctuates slightly but it can return to its reference (3 A) quickly.

The last experiment is conducted to verify the function of current limitation term in Fig. 2(c). When the grid is broken at t_1 and the local critical load of DER1 changes from no load to 10 Ω at t_2, if there is no current limitation term, the output current amplitude of the inverter can reach 9.3 A, as shown in Fig. 25(a). It is assumed that the allowed maximum output current amplitude of the inverter is 7 A. If the current limitation term is adopted, the output current amplitude of the inverter is controlled within 7 A, as shown in Fig. 25(b).

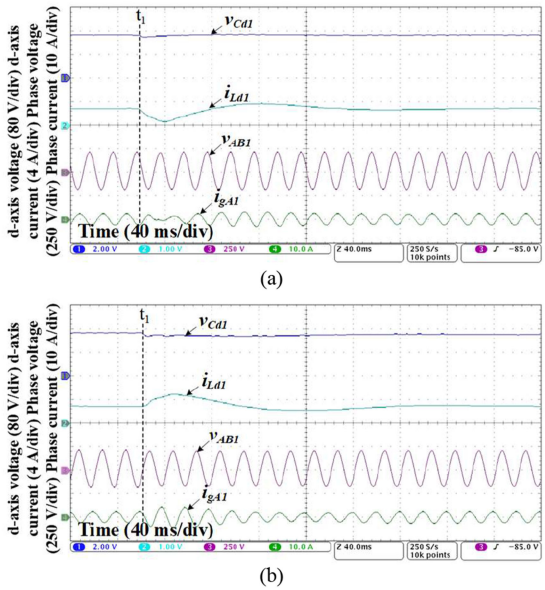


Fig. 24. Experimental results of DER1 when the load brings a large step change in the GC state. (a) Local load change. (b) Remote load change.

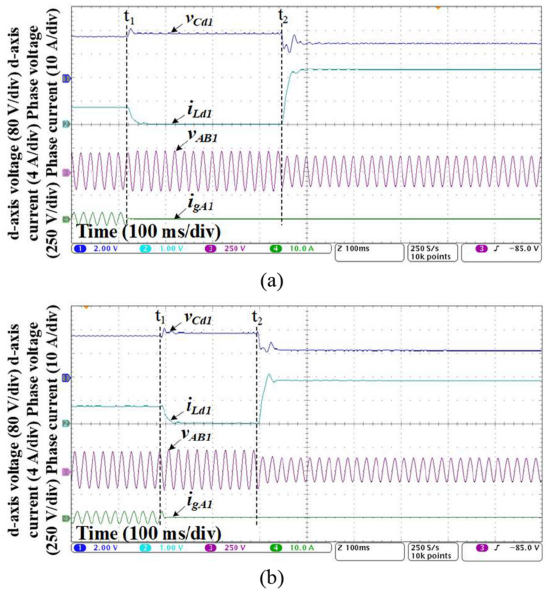


Fig. 25. Experimental results of DER1 when the grid is broken at t_1 and the local critical load brings a large increase at t_2. (a) Without current limitation term. (b) With current limitation term.

VI. Conclusion

A universal controller under different operating states for parallel inverters is proposed, which can achieve different goals in the GC state and SA state and ensure seamless transfer between these states. By implementing such a controller, the need to switch between two sets of controllers can be avoided. In the GC state, the proposed controller can realize accurate grid current regulation of the inverter. When islanding occurs, the proposed controller can automatically convert from grid current control to v_C–i_g-based droop control; islanding detection is thus unnecessary.

The advantages of this universal controller are multifold. First, it can realize seamless transfer of parallel inverters. The reliability of MG can therefore be guaranteed in the SA state, and power sharing can be achieved among parallel inverters without communication lines. Second, compared with droop control, the proposed controller can regulate the grid current accurately and output constant power when the grid voltage fluctuates in the GC state. Lastly, grid current harmonics in the GC state and capacitor voltage harmonics in the SA state can be effectively mitigated.

Appendix

See Fig. 26.

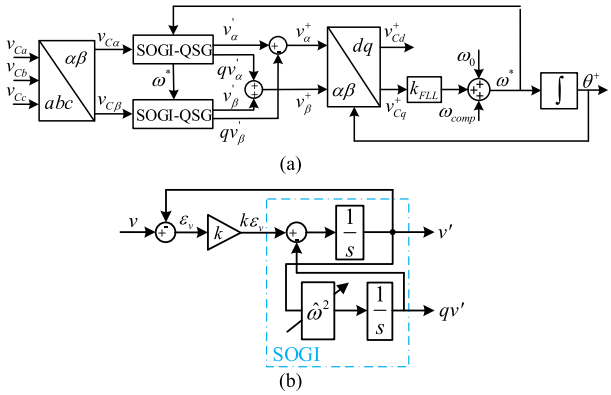


Fig. 26. (a) SOGI-QSG-based FLL block. (b) Second-order generalized integrator—quadrature signal generator (SOGI-QSG).

References

[1] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodríguez, "Control of power converters in AC microgrids," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4734–4749, Nov. 2012.

[2] H. Liu *et al.*, "Seamless transfer scheme with unified control core for paralleled systems," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6286–6298, Jul. 2019.

[3] G. G. Talapur, H. M. Suryawanshi, L. Xu, and A. B. Shitole, "A reliable microgrid with seamless transition between grid connected and islanded mode for residential community with enhanced power quality," *IEEE Trans. Ind Appl.*, vol. 54, no. 5, pp. 5246–5255, Sep./Oct. 2018.

[4] S. Huang, Y. Konishi, Z. Yang, and M. Hsieh, "Observer-based capacitor current sensorless control applied to a single-phase inverter system with seamless transfer," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2819–2828, Mar. 2019.

[5] O. V. Kulkarni, S. Doolla, and B. G. Fernandes, "Mode transition control strategy for multiple inverter-based distributed generators operating in grid-connected and standalone mode," *IEEE Trans. Ind Appl.*, vol. 53, no. 6, pp. 5927–5939, Nov./Dec. 2017.

[6] B. Singh, G. Pathak, and B. K. Panigrahi, "Seamless transfer of renewable-based microgrid between utility grid and diesel generator," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8427–8437, Oct. 2018.

[7] X. Li, H. Zhang, M. B. Shadmand, and R. S. Balog, "Model predictive control of a voltage-source inverter with seamless transition between islanded and grid-connected operations," *IEEE Trans. Ind Electron.*, vol. 64, no. 10, pp. 7906–7918, Oct. 2017.

[8] H. Kim, E. Shin, Y. Lee, J. Kim, and B. M. Han, "Smooth operation transition scheme for stand-alone power system with EG and BESS-PV panels," *IEEE Trans. Smart Grid*, vol. 8, no. 4, pp. 2042–2044, Jul. 2017.

[9] T. Tran, T. Chun, H. Lee, H. Kim, and E. Nho, "PLL-based seamless transfer control between grid-connected and islanding modes in grid-connected inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5218–5228, Oct. 2014.

[10] D. Das, G. Gurrala, and U. J. Shenoy, "Linear quadratic regulator-based bumpless transfer in MGs," *IEEE Trans. Smart Grid*, vol. 9, no. 1, pp. 416–425, Jan. 2018.
[11] S. Kumar and B. Singh, "Seamless operation and control of single-phase hybrid PV-BES-utility synchronized system," *IEEE Trans. Ind Appl.*, vol. 55, no. 2, pp. 1072–1082, Mar./Apr. 2019.
[12] Z. Liu, J. Liu, and Y. Zhao, "A unified control strategy for three-phase inverter in distributed generation," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1176–1191, Mar. 2014.
[13] S. S and L. Umanand, "A unified controller for utility-interactive uninterruptible power converters for grid connected and autonomous operations," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3871–3887, Apr. 2019.
[14] S. Buso, T. Caldognetto, and Q. Liu, "Analysis and experimental characterization of a large-bandwidth triple-loop-regulator for grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1936–1949, Feb. 2019.
[15] Z. Liu and J. Liu, "Indirect current control based seamless transfer of three-phase inverter in distributed generation," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3368–3383, Jul. 2014.
[16] S. Yoon, J. Kwon, J. Park, and S. Choi, "Indirect current control for seamless transfer of three-phase utility interactive inverters," in *Proc. 26th IEEE Appl. Power Electron. Conf. Expo.*, 2011, pp. 625–632.
[17] J. Kwon, S. Yoon, and S. Choi, "Indirect current control for seamless transfer of three-phase utility interactive inverters," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 773–781, Feb. 2012.
[18] S. Yoon, H. Oh, and S. Choi, "Controller design and implementation of indirect current control based utility-interactive inverter system," in *Proc. 3rd IEEE Energy Convers. Congr. Expo.*, 2011, pp. 955–960.
[19] S. Yoon, H. Oh, and S. Choi, "Controller design and implementation of indirect current control based utility-interactive inverter system," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 26–30, Jan. 2013.
[20] Y. Deng, Y. Tao, G. Chen, G. Li, and X. He, "Enhanced power flow control for grid-connected droop-controlled inverters with improved stability," *IEEE Trans. Ind Electron.*, vol. 64, no. 7, pp. 5919–5929, Jul. 2017.
[21] J. Lu, M. Savaghebi, S. Golestan, J. C. Vasquez, J. M. Guerrero, and A. Marzabal, "Multimode operation for on-line uninterruptible power supply system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1181–1196, Jun. 2019.
[22] M. Karimi-Ghartemani, S. A. Khajehoddin, P. Piya, and M. Ebrahimi, "Universal controller for three-phase inverters in a microgrid," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1342–1353, Dec. 2016.
[23] X. Hou *et al.*, "Distributed hierarchical control of AC microgrid operating in grid-connected, islanded and their transition modes," *IEEE Access*, vol. 6, pp. 77388–77401, 2018.
[24] W. R. Issa, A. H. E. Khateb, M. A. Abusara, and T. K. Mallick, "Control strategy for uninterrupted microgrid mode transfer during unintentional islanding scenarios," *IEEE Trans. Ind Electron.*, vol. 65, no. 6, pp. 4831–4839, Jun. 2018.
[25] W. R. Issa, M. A. Abusara, and S. M. Sharkh, "Control of transient power during unintentional islanding of microgrids," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4573–4584, Aug. 2015.
[26] P. Rodríguez, C. Citro, J. I. Candela, J. Rocabert, and A. Luna, "Flexible grid connection and islanding of SPC-based PV power converters," *IEEE Trans. Ind Appl.*, vol. 54, no. 3, pp. 2690–2702, May/Jun. 2018.
[27] X. Meng, J. Liu, and Z. Liu, "A generalized droop control for grid-supporting inverter based on comparison between traditional droop control and virtual synchronous generator control," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5416–5438, Jun. 2019.
[28] G. Lou, W. Gu, J. Wang, J. Wang, and B. Gu, "A unified control scheme based on a disturbance observer for seamless transition operation of inverter-interfaced distributed generation," *IEEE Trans. Smart Grid*, vol. 9, no. 5, pp. 5444–5454, Sep. 2018.
[29] T. Rump and H. Eckel, "Comparison between different power system frequency measurement methods for converter applications providing ancillary services," in *Proc. IEEE 8th Int. Symp. Power Electron. Distrib. Gener. Syst.*, 2017, pp. 1–7.
[30] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. Ind Electron.*, vol. 58, no. 1, pp. 127–138, Jan. 2011.
[31] Z. Wang, J. Yang, and J. Liu, *Harmonic Suppression And Reactive Power Compensation*, 2nd ed. Beijing, China: China Mach. Press, 2006.
[32] H. Zhang, H. Xu, C. Fang, and C. Xiong, "Torque ripple suppression method of direct-drive permanent magnet synchronous motor based on proportional-integral and quasi resonant controller," *Trans. China Electrotech. Soc.*, vol. 32, no. 19, pp. 41–51, Oct. 2017.
[33] C. Qin, C. Zhang, A. Chen, X. Xing, and G. Zhang, "Circulating current suppression for parallel three-level inverters under unbalanced operating conditions," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 480–492, Mar. 2019.
[34] H. Chen and X. Xing, "Circulating current analysis and suppression for module grid-connected inverters under unbalanced conditions," *IEEE Access*, vol. 6, pp. 69120–69129, 2018.
[35] F. Briz, D. Díaz-Reigosa, C. Blanco, and J. M. Guerrero, "Coordinated operation of parallel-connected inverters for active islanding detection using high-frequency signal injection," *IEEE Trans. Ind Appl.*, vol. 50, no. 5, pp. 3476–3484, Sep./Oct. 2014.
[36] T. Wu, Z. Liu, J. Liu, B. Liu, and R. An, "A decoupled current droop control method for parallel inverters in microgrids," in *Proc. IEEE 3rd Int. Future Energy Electron. Conf. ECCE Asia*, 2017, pp. 2117–2122.
[37] P. P. Das, S. Chattopadhayay, and M. Palmal, "A d–q voltage droop control method with dynamically phase-shifted phase-locked loop for inverter paralleling without any communication between individual inverters," *IEEE Trans. Ind Electron.*, vol. 64, no. 6, pp. 4591–4600, Jun. 2017.
[38] Y. Guan, J. M. Guerrero, X. Zhao, J. C. Vasquez, and X. Guo, "A new way of controlling parallel-connected inverters by using synchronous-reference-frame virtual impedance loop—part I: Control principle," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4576–4593, Jun. 2016.
[39] *IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces*, IEEE Standard 1547-2018, 2018.
[40] *Power Quality-Frequency Deviation for Power System*, GB/T 15945, 2008.

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