# Letters

## The Three-Terminal Converter Cell, Graphs, and Generation of DC-to-DC Converter Families

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***Abstract*—With the use of graphs, the three-terminal converter cell concept was extended into a systematic topology generation method for two-stage PWM dc-to-dc power converters. The converter cell may include any number of reactive elements and switches. Any operable dc-to-dc converter (a seed) generates a family of operable converters by flipping converter-cell terminals. General conversion ratio formulas were proposed depending on the flipping operation: inversion, input, or output flipping. The positive super-lift (SL) converter served as a synthesis example, deriving the negative SL converter, and four new operable converters, one of which was verified experimentally.**

***Index Terms*—Converter cell, conversion ratio formulas, dc-to-dc converter synthesis, graphs, node flipping, operable converter.**

### I. Introduction

THE systematic generation of PWM dc-to-dc power converter topologies have attracted the attention of the power converter community [1]–[5]. To generate converter families, which are composed of six converters (or three, depending on symmetry), Tymmerski and Vorperian [4] considered a three-terminal converter cell and six "configurations" of these three terminals. In this letter, we revisit these terminal flips [4] as a process of *node flipping* in graphs.

We consider the converter cell approach and its node flipping a powerful tool for converter generation, which, in our opinion, has been underappreciated and underdeveloped. Tymmerski and Vorperian chose only 14 converter cells as basic and dismissed, for example, a cell which was recognized later by Williams to generate sequence Q [6], as shown in Fig. 1(a). They also ignored the cell depicted in Fig. 1(b), which corresponds to the quadratic buck converter $a_2$ in [5]. Many other cases were also avoided, such as one- and second-order cells comprising, for example, switched-capacitor configurations. The number of possible topologies for higher order cells is unrealistic, even for third-order cells (two inductors and one capacitor), as there are also degenerated cases. We argue, however, that this problem is tractable by using node flipping on an operable converter. A plethora of voltage-sourced dc-to-dc converters has been developed in the last 30 years. Many of them can be subject to node flipping, but, to the authors' knowledge, few references exist that report the use of the converter cell concept in the generation of new converters [6], [7]. For example, the quadratic boost converter in [8] could have been generated from converter $a_2$ [5] by inversion.

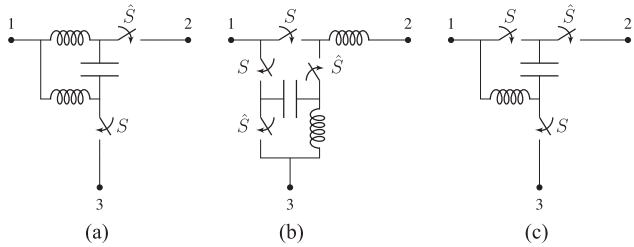


Fig. 1. Converter cells not included in [4]. Duty cycle $D$ is governed by $S$. Its complementary switch $\hat{S}$ relates to the $1-D$ cycle.

The purpose of this letter is twofold. First, it is to show that node flipping can be applied to an operable seed converter, therefore generating a family of operable converters. The second aim is to propose simple, but general formulas for the voltage conversion ratio of derived converters in terms of the seed transfer function.

We depart from a two-stage operable converter, translate it into a directed graph (we refer interested readers to [1], [3], [9], [10]), including switches, and to a pair of subgraphs where switches are open- or short-circuited. We identify the three-terminal converter cell in the netlists obtained from subgraphs. Symmetry can be identified by inversion (see Section II). We then apply node flipping and generate five (or two, depending on symmetry) other pairs of netlists. We also propose voltage converter ratio formulas for the generated converter family, which, moreover, are linked to the type of flip involved (see Section III). In this article, we treat, as an example, the second-order three-switch cell depicted in Fig. 1(c) (not considered in [4]). This converter cell corresponds to the positive output super-lift converter [11] (see Section IV), which includes an algebraic voltage constraint (via voltage lift/switched capacitor). We explain how to reinstate a derived converter graph, a step-down converter $M(D) = D/(1+D)$, into a switched circuit. We implement its experimental prototype and obtain actual waveforms, validating its operability. We finish this letter with the conclusion and avenues for further research.

Manuscript received October 13, 2019; revised November 16, 2019 and December 12, 2019; accepted December 29, 2019. Date of publication January 6, 2020; date of current version April 22, 2020. This work was supported by SEP-PRODEP under Grant UTMIX-PTC-057/DSA/103.5/16/10481. *(Corresponding author: Richard Marquez.)*

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Digital Object Identifier 10.1109/TPEL.2020.2964700

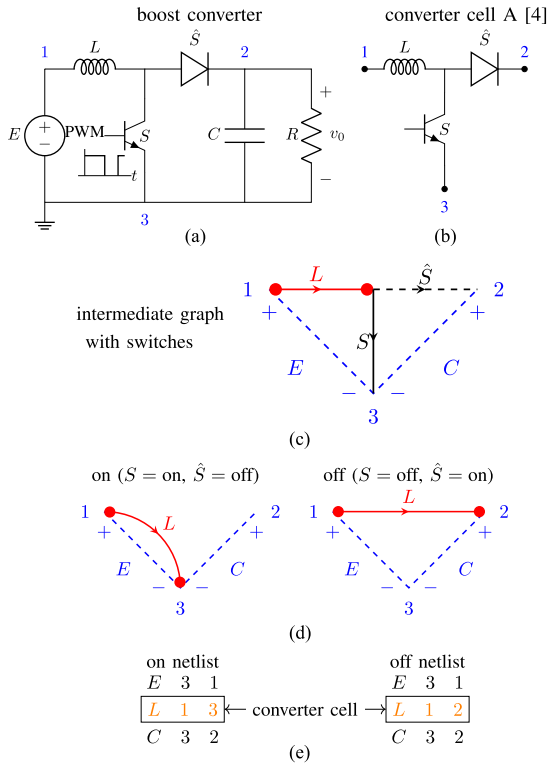


Fig. 2. Boost converter and its graph representation. (a) Circuit diagram $C$. (b) Converter cell. (c) Equivalent graph of boost converter. (d) ON and OFF graphs. (e) ON and OFF netlists. Voltage conversion ratio $M(D) = \frac{1}{1-D}$.

## II. Graphs/Netlists of a dc-to-dc Converter Cell

The converters considered here operate in two alternated stages, named "ON" and "OFF" after the controlled switch operation. These two stages may refer to continuous conduction mode in the case of a single-switch converter operation.[1] A dc-to-dc converter can be transformed into a *directed graph* and two (ON and OFF) subgraphs, and their corresponding netlists. See the boost converter example in Fig. 2(a). We consider a three-terminal converter cell, as shown in Fig. 2(b), and two fixed edges, which represent the constant, unipolar input source $V$ and the output sink (parallel connection of $C_o$ and $R_L$, seen as one edge). To obtain the converter graph [3], each circuit element is replaced by a graph edge. Union of edges at a graph node represents circuit connections, as shown in Fig. 2(c). Both input and output ports are common grounded (node 3). Voltage source $E$ and capacitor $C_o = C$ are dashed edges. Inductor $L$ corresponds to a solid edge. An arrow gives $L$ direction, edges $E$, $C$, which are connected between nodes 3 and 1, respectively, nodes 3 and 2, have the direction of positive (+) terminal. The direction of an edge in a graph corresponds to an assumed measurement polarity of a physical quantity.

We assume that switch elements $S$ and $\hat{S}$ are ideal short circuits in one stage (e.g., ON) and ideal open circuits in the opposite stage (respectively, OFF). Open and short circuits are then related to edge operations. Therefore, the resulting intermediate graph splits into two subgraphs by edge deletion (open circuit) and contraction (short circuit). In the on-stage of boost example, the diode edge $\hat{S}$ is deleted in the "ON" subgraph while the transistor edge is contracted into a node; ON and OFF subgraphs of boost converter are illustrated in Fig. 2(d). Based on edge direction, each subgraph yields a netlist, as illustrated in Fig. 2(e).

The three-terminal converter cell, as shown in Fig. 2(b), can be readily identified from the derived netlists. It corresponds to the connections of the internal converter elements. In the example, boost converter cell is given by the nodes of edge $L$ in Fig. 2(e) (highlighted). Consequently, the first and last lines of netlists (input source and output sink) are not taken into account in the flipping operations that follow.

To each operable converter, then, we associate a pair of ON and OFF subgraphs, two netlists, and a voltage conversion ratio $M(D)$, which depends on the duty cycle $D$ of the PWM controlled switch. Letting $T_s$ be the PWM switching period, $DT_s$ is the fraction of period when $S$ is ON, and $\hat{S}$ is OFF. An operable converter, i.e., a seed for family generation, exhibits $M(D) \neq 0$ and $M(D) \neq 1$.

*Remark 1:* The inverse process, i.e., constructing a converter graph from a pair of netlists, yields a clue on how to reinstate a converter circuit. The union of both subgraphs by edge expansion and addition, evidencing $S$ and $\hat{S}$ switches, results in the necessary intermediate graph for converter realization.

*Remark 2:* The conversion ratio depends on the placement of ON and OFF graphs. The conversion ratio of the boost converter is $M(D) = 1/(1-D)$, which is linked to the position of its graphs, as shown in Fig. 2. If the ON and OFF graphs are interchanged, as in Fig. 3, the conversion ratio now yields $M(D) = 1/D$, i.e., $D$ is replaced by $1-D$ (cf., the transistor-diode interchange, T⇔D, in [6]). This result is critical to understand the following node flips and conversion ratio formulas. In particular, a converter is symmetric if inversion (flip of nodes 1 and 2) changes the placement of ON and OFF graphs.

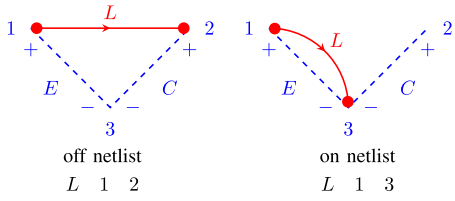


Fig. 3. Interchange of ON and OFF graphs in the boost converter. Voltage conversion ratio $M(D) = 1/D$.

## III. Generation of a Converter Family and Conversion Ratio Formulae

As in [4], terminal flipping of the converter cell then consists of an interchange of node numbers in both ON and OFF netlists. We recognize three types of flips: inversion (interchange of nodes 1 and 2, denoted $1 \Leftrightarrow 2$), input flipping or flip of input and common nodes ($1 \Leftrightarrow 3$), and output flipping or flip of output and common nodes ($2 \Leftrightarrow 3$).

Inversion ($1 \Leftrightarrow 2$) of boost converter then results in the netlists (only the converter cell is flipped)

$$\overbrace{L\ 1\ 3\quad 1\ 2}^{\text{Boost}\quad M(D)=\frac{1}{1-D}} \xleftrightarrow{1\Leftrightarrow 2} \overbrace{L\ 2\ 3\quad 2\ 1}^{\text{Buck}\quad M(D)=1-D}$$

$$D \text{ is replaced by } 1-D \longrightarrow \overbrace{L\ 2\ 1\quad 2\ 3}^{\text{Buck}\quad M(D)=D}.$$

[1] In this letter, while interesting, we avoid the inductor discontinuous current conduction mode.

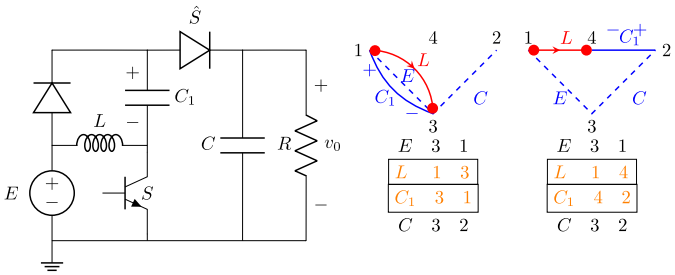


Fig. 4. Positive super-lift converter (SL1) and its graph representation. Voltage conversion ratio $M(D) = \frac{2-D}{1-D}$. Polarity of edge $C_1$ (solid) is indicated.

By inversion, the boost conversion ratio $M(D) = 1/(1-D) = A/B$ yields the reciprocal

$$M(D) = B/A = 1 - D\big|_{D \text{ by } 1-D}^{\text{Replace}} = D,$$

i.e., the buck converter, a well-known result [2].

Input flipping ($1 \Leftrightarrow 3$) of boost converter results in the buck–boost converter

$$\overbrace{\begin{matrix} L & 1 & 3 & & 1 & 2 \end{matrix}}^{\text{Boost } M(D)=\frac{1}{1-D}} \overset{1\Leftrightarrow 3}{\longleftrightarrow} \overbrace{\begin{matrix} L & 3 & 1 & & 3 & 2 \end{matrix}}^{\text{Buck–boost } M(D)=-D/(1-D)} .$$

The buck–boost conversion ratio results in $M(D) = (B - A)/B = -D/(1-D)$. Notice the symmetry of the buck–boost can be readily checked by inversion $1 \Leftrightarrow 2$.

Output flipping ($2 \Leftrightarrow 3$) yields again a boost

$$\overbrace{\begin{matrix} L & 1 & 3 & & 1 & 2 \end{matrix}}^{\text{Boost } M(D)=\frac{1}{1-D}} \overset{2\Leftrightarrow 3}{\longleftrightarrow} \overbrace{\begin{matrix} L & 1 & 2 & & 1 & 3 \end{matrix}}^{\text{Boost } M(D)=\frac{1}{D}} .$$

The boost conversion ratio results in $A/(A-B) = 1/(1-(1-D)) = 1/D$, as expected (ON and OFF graphs appear inverted).

These node flips and formulas apply to any voltage-sourced dc-to-dc power converter provided the converter is operable, as we have tested in numerous examples, including those cases in [4], [6], and [7]. Therefore, we obtain the following conversion ratios and reciprocals from the conversion ratio $A/B$ of converter seed:

$$\overbrace{\frac{A}{B}}^{\text{seed}}, \overbrace{\frac{B}{A}}^{\text{inversion}}, \overbrace{\frac{B-A}{B}}^{\text{input flipping}}, \frac{B}{B-A}, \overbrace{\frac{A}{A-B}}^{\text{output flipping}}, \frac{A-B}{A}. \quad (1)$$

These formulas can be verified for all the sequences in [6, Fig. 9]. Notice $D$ is replaced by $1 - D$ in the reciprocals.

By using (1), nonoperable converter families in [6] can also be checked. In this way, a converter must satisfy $A \neq B$ to be operable. That is, the seed conversion ratio (and, consequently, those voltage ratios of the generated converter family) must be $M(D) \neq 0$ or $M(D) \neq 1$.

## IV. Family Generation Example

The elementary positive super-lift converter [11], SL1, is depicted in Fig. 4, along with its subgraphs and netlists. Its second-order converter cell is highlighted in the netlists, as shown in Fig. 1(c). This converter is operable, $M(D) = \frac{2-D}{1-D} = \frac{A}{B}$.

We choose this converter because it was not considered in [4], [6] due to the algebraic constraint $V_{C_1} = E$, and the inclusion of a switched capacitor.

The SL family of converters, obtained by node flipping, consists of the following converter cells (type of flipping, converter label, and conversion ratio are indicated):

$$\overbrace{\begin{matrix} L & 3 & 1 & & 3 & 4 \\ C_1 & 1 & 3 & & 4 & 2 \end{matrix}}^{\text{SL2 [12], } M(D)=-\frac{1}{1-D}} \overset{1\Leftrightarrow 2}{\longleftrightarrow} \overbrace{\begin{matrix} L & 3 & 4 & & 3 & 2 \\ C_1 & 4 & 1 & & 2 & 3 \end{matrix}}^{\text{SL5 (new), } M(D)=-D}$$
$$\updownarrow 1 \Leftrightarrow 3 \qquad\qquad \updownarrow 2 \Leftrightarrow 3$$
$$\overbrace{\begin{matrix} L & 1 & 3 & & 1 & 4 \\ C_1 & 3 & 1 & & 4 & 2 \end{matrix}}^{\text{SL1 (seed) [11], } M(D)=\frac{2-D}{1-D}} \overset{1\Leftrightarrow 2}{\longleftrightarrow} \overbrace{\begin{matrix} L & 2 & 4 & & 2 & 3 \\ C_1 & 4 & 1 & & 3 & 2 \end{matrix}}^{\text{SL4 (new,implemented), } M(D)=\frac{D}{1+D}}$$
$$\updownarrow 2 \Leftrightarrow 3 \qquad\qquad \updownarrow 1 \Leftrightarrow 3$$
$$\overbrace{\begin{matrix} L & 1 & 2 & & 1 & 4 \\ C_1 & 2 & 1 & & 4 & 3 \end{matrix}}^{\text{SL3 (new), } M(D)=2-D} \overset{1\Leftrightarrow 2}{\longleftrightarrow} \overbrace{\begin{matrix} L & 2 & 4 & & 2 & 1 \\ C_1 & 4 & 3 & & 1 & 2 \end{matrix}}^{\text{SL6 (new), } M(D)=\frac{1}{1+D}} .$$

Input flipping of SL1 yields the negative output SL converter (SL2) [12], $M_{\text{SL2}} = \frac{B-A}{B} = \frac{1-D-(2-D)}{1-D} = -\frac{1}{1-D}$; output flipping of SL1 yields SL3, a step-up converter $M_{\text{SL3}} = \frac{A}{A-B} = 2-D$; inversion of SL1 yields a step-down converter SL4, $M_{\text{SL4}} = \frac{B}{A} = \frac{1-D}{2-D}\big|_{D \text{ by } 1-D}^{\text{Replace}} = \frac{D}{1+D}$; inversion of SL2 yields a negative buck converter $M_{\text{SL5}} = -D$; and, inversion of SL3 results in $M_{\text{SL6}} = \frac{1}{1+D}$. All converters in this sequence are operable, as expected from (1). Efficiencies in this family are similar to those of SL1 and SL2. Step-down converters SL4, SL6, and SL5, work, respectively, in the range $M(D) \in (0, 0.5)$, $(0.5, 1)$, and $(-1, 0)$, which should be useful for systems-on-chip power applications. Two converters, SL3 and SL5, have a linear relationship between the duty cycle and transfer gain, as the buck converter. In particular, the SL3, $M(D) = 2 - D$, is a candidate for potential step-up applications, where a linear response and conversion ratio $M(D) \in (1, 2)$ are desirable.

A converter SL4 prototype is used to check our findings, as shown in Fig. 5(c). This converter confirms the operability of designs based on inversion in the case, where algebraic constraints appear (e.g., switched capacitors). To realize the SL4, we first translate the netlists into the pair of graphs shown in Fig. 5(a), and those into the converter graph, as shown in Fig. 5(b). This graph yields both subgraphs by edge contraction and deletion, as mentioned above, and also brings the actual circuit. Converter realization, Fig. 5(d), results from adding electrical components into a circuit, including semiconductor switches, directly from this graph. Therefore, SL4 has, as shown in Fig. 5(b), one switch of type $S$ ($u = D$, solid) and two $\hat{S}$ ($\bar{u} = 1 - D$, dashed). Deciding which one is a transistor or a diode comes from electrical conditions. In this case, transistor $S$ and diode $\hat{S}_1$ were easily obtained. However, switch $\hat{S}_2$, which at first sight was a diode, was finally chosen to be a transistor governed by $\bar{u} = 1 - D$, after a PSIM simulation. Experimental waveforms are shown in Fig. 5(e) along with their average values and deviations. We use a duty cycle $D = 0.67$. Voltage $V_{C_1}$ equals output capacitor voltage, $v_o = -V_{C_1} = 8$V, for an input voltage $E = 20$ V. The measured output voltage is $v_o = 7.3 \pm 0.1$ V, close to the ideal value and to voltage $-V_{C_1} = 8.1 \pm 0.2$ V, as expected. SL4

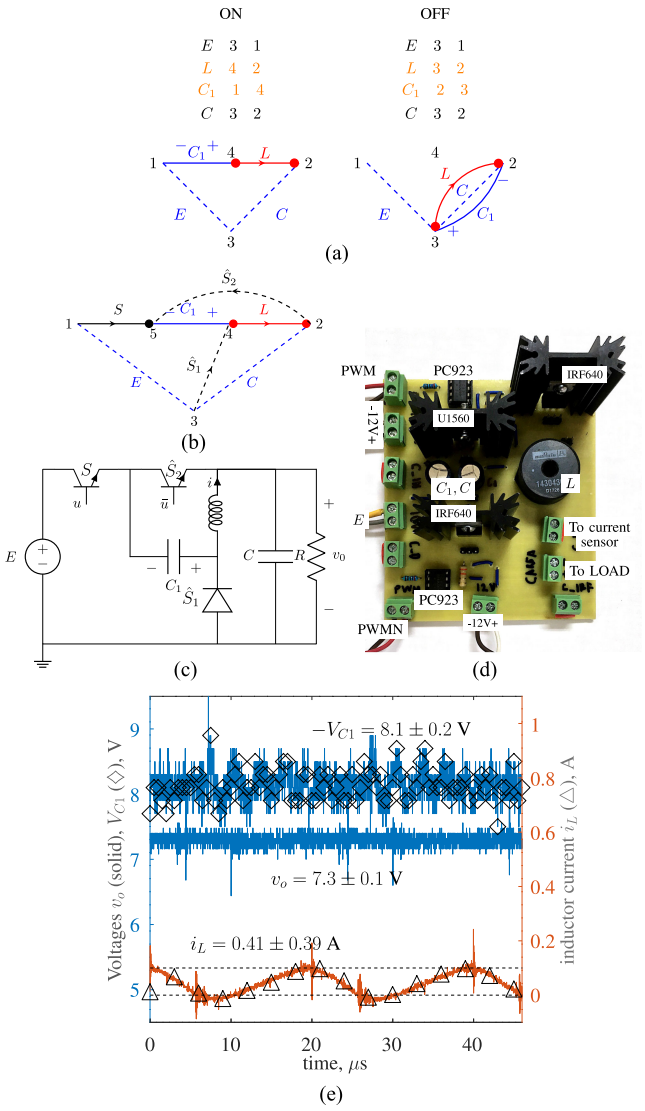


Fig. 5. Converter SL4. (a) Graphs and netlist. (b) Intermediate graph. (c) Schematic. (d) Implementation. (e) Actual waveforms. Component values: $C, C_1 = 220\,\mu$F, $L = 300\,\mu$F, load $R = 50\,\Omega$, PWM frequency $f = 50$ kHz, voltage source $E = 20$ V, MOSFET IRF640, Diode U1560. PWM duty cycle $D$ is governed by switch $S$, $u =$ PWM, and $1 - D$ by $\hat{S}_1$, $\hat{S}_2$, $\bar{u} =$ PWMN.

efficiency yields $\eta = 89\%$ at $D = 0.67$, exceeding 80% for $D > 0.3$.

## V. Conclusion

The three-terminal converter cell is an integral part of any common-grounded PWM dc-to-dc power converter, both electrically and from a graph-theoretic point of view. Based on the converter cell, this letter presents a graph-based method for the generation of a dc-to-dc converter family from an operable converter, along with its dc conversion ratio formulas (1). The designer can apply these formulas before converter derivation, guiding her/his decision on converter design and construction. We review the converter cell as netlists of a pair of graphs. Our approach, therefore, simplifies the use of circuit transformations, now seen as computable node interchange on netlists. Node flipping can be applied to any operable dc-to-dc converter, independent of the number of reactive elements and switches (e.g., quadratic boost, switched-capacitor converters). This approach is useful for topology generation from old and new dc-to-dc converters or to evaluate degenerated cases (nonoperable) directly from netlists.

The proposed conversion ratio formulas and the graph-oriented technique unify under the same approach the analysis of seemingly different dc-to-dc converters (including reactances with coupled inductors, cf., [7], or switched capacitors, or both). To test the synthesis method, we derived the negative output super-lift converter and generated four new converters of super-lift type, one of which was verified experimentally (SL4). As pointed out in [6], converter families share similar properties. In our opinion, those properties can be computed via available graph-theory and matrix algorithms using netlists. For example, generated family from zero (input) ripple converter in [13] also exhibits zero (input or output) ripple. Finally, using graph-based algorithms for comparing netlists [14], a dc-to-dc converter database can be developed.

## Acknowledgment

The authors would like to thank anonymous reviewers for their fruitful remarks; and Dr. N. Castañeda-Roldan for discussions on graph theory, and U. Hernández-Barrios for his help during prototype development.

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