Power Loss Model and Device Sizing Optimization of Si/SiC Hybrid Switches

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***Abstract*—Si/SiC hybrid switches of parallel Si insulated-gate bipolar transistor (IGBT) and SiC metal–oxide–semiconductor field-effect transistor (MOSFET) offer most of the SiC benefits but at a much lower cost in comparison to a full SiC solution. The hybrid switch can be optimized to achieve a minimum total power loss while utilizing the smallest SiC chip size without exceeding the specified maximum junction temperature. In this article, we first develop a generalized power loss model for Si/SiC hybrid switches with total power loss and junction temperature as outputs and SiC device size as a continuous input variable, and then develop a methodology to minimize SiC device size while optimizing total IGBT/MOSFET power loss and ensuring maximum junction temperature still below 150 °C. The power loss model is experimentally validated through both simple double pulse testing and a dc–dc buck converter case study. Using the model and optimization methodology, a minimum SiC device size can be obtained with optimized power loss and safe operation temperature.**

***Index Terms*—Hybrid switch, insulated-gate bipolar transistor (IGBT), loss model, MOSFET, SiC, size optimization.**

I. Introduction

SiC power metal–oxide–semiconductor field-effect transistors (MOSFETs) have been increasingly adopted into power electronic applications, demonstrating significant improvements in efficiency and power density mainly due to much reduced switching losses [1]–[4]. However, SiC MOSFETs are currently still five times more expensive than their silicon insulated-gate bipolar transistor (IGBT) counterparts [5]. This cost barrier remains one of the major reasons why SiC is not enjoying even larger scale market acceptance.

Recently, a Si/SiC hybrid switch concept featuring a Si IGBT and a SiC MOSFET in parallel was proposed to offer most of the SiC benefits but at a much lower cost in comparison to a full SiC solution [6]–[11]. In a Si/SiC hybrid switch, the total current is shared proportionally between the IGBT and MOSFET depending on their respective device size. The two separate gates of the IGBT and MOSFET are controlled in such a manner that the SiC MOSFET is responsible for facilitating hard switching while the silicon IGBT benefits from zero-voltage switching (ZVS), thus resulting in lower switching losses. Since the conduction and switching losses of the SiC MOSFET are relatively small under normal operation conditions, it is possible to use a small SiC MOSFET in the hybrid switch to improve its cost-effectiveness. In [7] and [8], a 6.5-kV hybrid switch prototype demonstrated 70% switching loss reduction comparing to a pure Si IGBT solution. In [9] and [10], the current sharing behavior in a 3.3-kV hybrid switch was analyzed via simulation. It also showed lower switching losses and suppressed oscillations comparing to an all-Si IGBT and all-SiC MOSFET package layouts, respectively. A T-type three-level solar inverter based on 1.2-kV Si/SiC hybrid switches was reported in [11], which achieved an optimized efficiency by using specific gate control patterns that allow the SiC MOSFET to turn ON shortly before and turn OFF shortly after the IGBT. In these studies, the current rating of the SiC MOSFETS is comparable to that of the IGBTs.

The main goal of Si/SiC hybrid switch design optimization is to achieve a minimum total power loss while utilizing the smallest SiC chip size without exceeding the specified maximum junction temperature on either device. On one hand, a hybrid switch of a SiC MOSFET and an IGBT of comparable current ratings is considerably more expensive than a single IGBT solution. On the other hand, an aggressively downsized SiC MOSFET may lead to overheating of the SiC chip and/or a higher total power loss. In [12], a Si/SiC current ratio of 6 was selected in an EV boost converter application. In [13] and [14], a Si/SiC current ratio of 3 was selected in a 15-kW single-phase H-bridge inverter application. In [15], a 1200 V/200 A hybrid switch phase-leg module with a Si/SiC current ratio of 4 was developed for a 10-kW converter application. These studies experimentally investigated the influence of Si/SiC current ratio (discrete values in all cases) on loss reduction and efficiency improvement without considerations on SiC die overheating. In [16], the thermal aspect of a Si/SiC hybrid switch in dc–dc buck converter applications was experimentally studied for three Si/SiC current ratios. The authors of this article proposed a thermal balance gate control strategy for a hybrid switch with a Si/SiC current ratio of 4 to improve its maximum output current capability in a 10.5-kW dc–dc boost converter application [17]. The impact of the Si/SiC current ratio on cost was studied in [18] and [19] based on 1.2-kV-rated commercial Si MOSFETs and IGBTs. It shows that the cost of a hybrid switch with a

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Si/SiC current ratio of 4 is only 50% that of a full SiC MOSFET with the same current rating.

While the electrical and thermal performances of the hybrid switches were experimentally demonstrated and/or compared in the prior work, they were limited to case studies of a few discrete Si/SiC current ratios. No generalized optimization methodology has been reported so far to achieve comprehensive optimization among SiC device size, total power loss, and maximum operating junction temperature. This may be due to two reasons. First, this is a very complex multivariable optimization problem, which involves not only SiC die size but also gate control parameters (i.e., turn-ON and turn-OFF delay times between the IGBT and the MOSFET). Second, there is a lack of analytical power loss model for the hybrid switch that takes into consideration SiC die size and junction temperature.

The objective of this article is to develop a generalized power loss model for Si/SiC hybrid switches with total power loss and junction temperature as outputs and SiC device size as a continuous input variable, and then develop a methodology to minimize SiC device size while optimizing total IGBT/MOSFET power loss and ensuring maximum junction temperature still below a specified value (e.g., 150 °C). The remainder of the article is organized as follows. The power loss model is introduced in Section II. In Section III, electrical and thermal characteristics of the power loss model are experimentally validated through both simple double pulse testing and a dc–dc buck converter. In Section IV, the SiC device sizing optimization method based on the power loss model calculation is proposed. The influence of the turn-ON and turn-OFF gate control delay times between the IGBT and MOSFET on total switch power loss for a range of SiC device size is first studied. The turn-ON and turn-OFF delay times are then optimized to a narrow range, which offers a minimum total power loss (within a margin of 5%) and practical engineering margin for gate driver. Next, the influence of the turn-ON and turn-OFF gate control delay times on the maximum junction temperature for different SiC device sizes is investigated. A minimum SiC device size can be identified, which offers a maximum junction temperature less than 150 °C while operating within the optimal range of gate delay times from the previous step. Finally, Section IV concludes this article.

II. Power Loss Models

The objective of this section is to develop a generalized power loss model for Si/SiC hybrid switches with total power loss and junction temperature as outputs and SiC device size as a continuous input variable. The schematic of the Si/SiC hybrid switch consisting of a high-current Si IGBT as the main switch and a low-current SiC MOSFET as the auxiliary switch is shown in Fig. 1. The paralleling structure of the Si/SiC hybrid switch combines the conduction advantages of Si IGBT and SiC MOSFET because most of the load current flows through the SiC MOSFET at a low current level and through the Si IGBT at a high current level, thus offering a reduced conduction loss.

Gate control signal patterns for the hybrid switches have been previously studied to reduce the switching losses of the hybrid switch, as shown in Fig. 2.

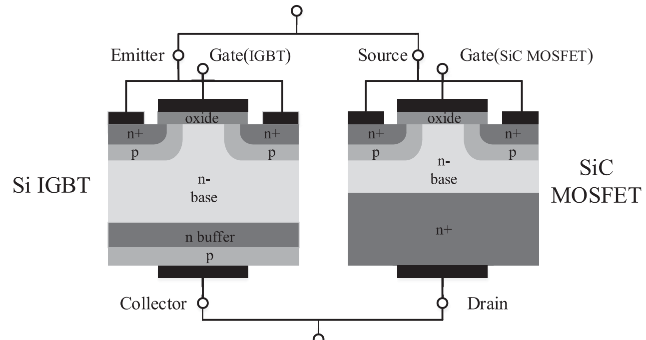


Fig. 1. Schematic of a hybrid switch made of paralleled Si IGBT and SiC MOSFET.

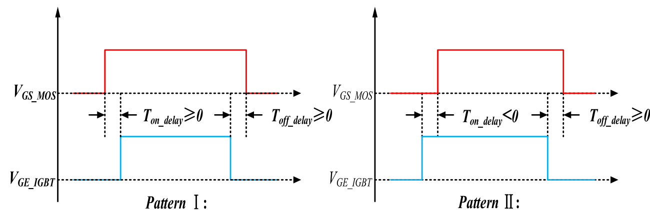


Fig. 2. Two gate control signal patterns for the hybrid switch. The SiC MOSFET leads the Si IGBT at turn-ON in Pattern I, while it lags in Pattern II.

These two gate control patterns of the Si/SiC hybrid switch were widely adopted in previous studies. They can enable the ZVS-ON operation of the SiC MOSFET or the main IGBT, and the ZVS-OFF operation of the main IGBT. The turn-ON and turn-OFF gate signal delay times between the IGBT and the SiC MOSFET of an hybrid switch are defined as $T_{\text{on_delay}}$ and $T_{\text{off_delay}}$, respectively. When $T_{\text{on_delay}}$ has a positive value, the IGBT realizes ZVS turn-ON operation, while the SiC MOSFET turns ON under a hard-switching condition. When $T_{\text{on_delay}}$ has a negative value, the MOSFET realizes ZVS turn-ON operation, while the IGBT turns ON under a hard-switching condition. Thus, it is generally preferred to have a positive $T_{\text{on_delay}}$ value because the hard turn-ON switching loss of the SiC MOSFET is smaller than the IGBT. For $T_{\text{off_delay}}$, we only use a positive value to ensure the IGBT always turns OFF before the SiC MOSFET and realizes a ZVS turn-OFF operation. This way we can reduce the large turn-OFF switching loss of the IGBT caused by its tail current.

The conduction and switching losses as well as the cost of the SiC MOSFET are strongly dependent on its chip size. Under certain gate control patterns, the SiC MOSFET may undergo hard-switching while conducting the entire load current and thus incur a large power loss despite its inherent high switching speed. This may result in a considerably elevated junction temperature compared to that of the main IGBT. The over temperature concern is more severe for a small SiC chip due to its larger on resistance and higher thermal resistance. In order to simultaneously achieve safe and efficient operation and cost reduction (small SiC chip size) of the hybrid switch, we need to develop a generalized power loss model for Si/SiC hybrid switches with total power loss and junction temperature as outputs and SiC device size as a continuous input variable.

A. Conduction Loss

Under the conduction state, the current flows through the auxiliary SiC MOSFET and/or the main IGBT depending on the current level. A critical forward current is as follows:

$$I_{\text{MOS_knee}} = \frac{V_{\text{knee}}}{R_{ds}} \tag{1}$$

where V_{knee}, $I_{\text{MOS_knee}}$, and R_{ds} are the knee voltage of the IGBT, the critical forward current, and the on resistance of the SiC MOSFET, respectively. When the overall forward current of the hybrid switch is too small to result in a forward voltage less than V_{knee}, only the SiC MOSFET conducts. Once $I_{\text{MOS_knee}}$ is surpassed, both devices jointly undertake the conduction current. R_{ds} is inversely proportional to the chip area A [20], which can be expressed as

$$R_{ds}(A) = \frac{A_{\text{ref}}}{A} \cdot R_{ds_\text{ref}} \tag{2}$$

where R_{ds_ref} and A_{ref} are the reference on resistance and chip area of the SiC MOSFET, respectively. With a straight-line approximation for the output characteristics of the IGBT, an equivalent asymptote with an intercept of V_{knee} and a slope of the reciprocal of R_{ce} is established. The current distribution between the SiC MOSFET and the IGBT can be derived as

$$I_{\text{MOS}}(A) = \frac{R_{ce}}{R_{ce} + R_{ds}(A)} I_F + \frac{V_{\text{knee}}}{R_{ce} + R_{ds}(A)} \tag{3}$$

$$I_{\text{IGBT}}(A) = \frac{R_{ds}}{R_{ce} + R_{ds}(A)} I_F - \frac{V_{\text{knee}}}{R_{ce} + R_{ds}(A)} \tag{4}$$

where R_{ce} is the slope resistance of the IGBT, and I_F is the total forward current of the hybrid switch. Considering the temperature coefficient of the ON-state characteristics of the IGBT and SiC MOSFET, V_{knee} and R_{ce} of the IGBT, and R_{ds} of the SiC MOSFET are functions of the junction temperature [21], respectively, as given by

$$R_{ds}(A, T_{j_\text{MOS}}) = R_{ds}(A, 25\,^\circ\text{C}) + T_{CR_\text{MOS}} \cdot (T_{j_\text{MOS}} - 25\,^\circ\text{C}) \tag{5}$$

$$R_{ce}(T_{j_\text{IGBT}}) = R_{ce}(25\,^\circ\text{C}) + T_{CR_\text{IGBT}} \cdot (T_{j_\text{IGBT}} - 25^\circ\,\text{C}) \tag{6}$$

$$V_{\text{knee}}(T_{j_\text{IGBT}}) = V_{\text{knee}}(25\,^\circ\text{C}) + T_{CV_\text{IGBT}} \cdot (T_{j_\text{IGBT}} - 25\,^\circ\text{C}) \tag{7}$$

where T_{j_MOS} and T_{j_IGBT} are the junction temperatures of the SiC MOSFET and the IGBT, respectively. T_{CV_IGBT} and T_{CR_IGBT} are the temperature coefficients of the IGBT's knee voltage and equivalent ON-state resistance, respectively. T_{CR_MOS} is the temperature coefficient of the SiC MOSFET's ON-state resistance. The temperature coefficient of the ON-state characteristic can be calculated from 25 °C, and the hot values from the datasheets of the IGBT and SiC MOSFET, e.g., for T_{CR_MOS}, applies:

$$T_{CR_\text{MOS}} = \frac{R_{ds}(150\,^\circ\text{C}) - R_{ds}(25\,^\circ\text{C})}{150\,^\circ\text{C} - 25\,^\circ\text{C}}. \tag{8}$$

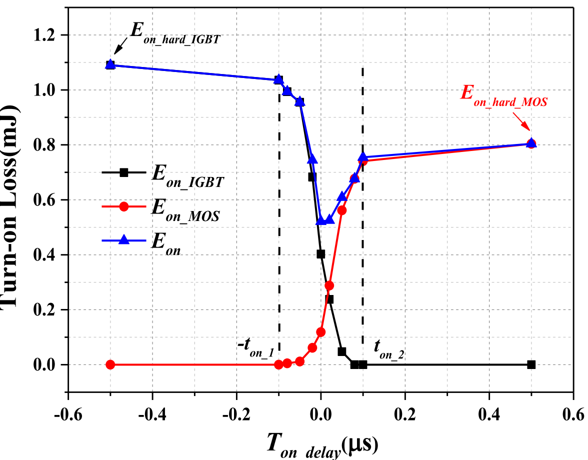


Fig. 3. Turn-ON switching losses of the Si/SiC hybrid switch as a function of the turn-ON delay time between the Si IGBT and SiC MOSFET $T_{\text{on_delay}}$.

Consequently, the conduction losses of the two internal devices of the hybrid switch are the function of the SiC MOSFET's chip area and its own junction temperature, which can be expressed as follows:

$$E_{\text{cond_MOS}}(A, I_F, T_{j_\text{MOS}}) = \begin{cases} I_{\text{MOS}}^2 \cdot R_{ds}(A, T_j); & I_F < I_{\text{knee}} \\ (M_{Rce} \cdot I_F + M_{Vnee})^2 \cdot R_{ds}(A, T_j); & I_F \geq I_{\text{knee}} \end{cases} \tag{9}$$

$$E_{\text{cond_IGBT}}(A, I_F, T_{j_\text{IGBT}}) = \begin{cases} 0; & I_F < I_{\text{knee}} \\ (M_{Rds} \cdot I_F - M_{Vnee}) \cdot [V_{\text{knee}} + (M_{Rds} \cdot I_F - M_{Vnee}) \cdot R_{ce}]; & I_F \geq I_{\text{knee}} \end{cases} \tag{10}$$

where M_{Rce}, M_{Rds}, and M_{Vnee} are expressed as

$$M_{Rds}(A, T_j) = \frac{R_{ds}(A, T_j)}{R_{ce} + R_{ds}(A, T_j)}$$

$$M_{Rce}(A, T_j) = \frac{R_{ce}}{R_{ce} + R_{ds}(A, T_j)}$$

$$M_{Vnee}(A, T_j) = \frac{V_{\text{knee}}}{R_{ce} + R_{ds}(A, T_j)}$$

B. Turn-On Switching Loss

Fig. 3 shows the exemplar measured turn-ON switching loss of the hybrid switch at various turn-ON delay times in a double-pulse-clamped inductive load circuit with a dc-link voltage of 600 V and a load current of 25 A at room temperature. The tested hybrid switch is consisted of the CREE 1200 V/12.5 A SiC MOSFET (C2M0160120D) and Infineon 1200 V/25 A Si IGBT (IGW25N120H3). The freewheeling diode is 1200 V/24 A SiC Schottky Diode (C4D15120D). The $E_{\text{on_hard_MOS}}$ and $E_{\text{on_hard_IGBT}}$ are the hard-switching turn-ON losses of the SiC MOSFET and IGBT, respectively. The total turn-ON switching loss of the hybrid switch is the sum of the two internal devices'

TABLE I
PARAMETERS OF POWER LOSS MODEL

Parameters	value
a_{I_MOS}	2.1
b_{V_MOS}	1.13
c_{I_MOS}	1.3
d_{V_MOS}	0.75
a_{I_IGBT}	1.67
b_{V_IGBT}	1.24
c_{I_IGBT}	0.86
d_{V_IGBT}	0.68
M_{on}	-0.0147
N_{on}	1.078
M_{off}	-0.023
N_{off}	1.057

turn-ON loss and shown as

$$E_{\text{on}}(T_{\text{on_delay}}) = E_{\text{on_MOS}}(T_{\text{on_delay}}) + E_{\text{on_IGBT}}(T_{\text{on_delay}}) \tag{11}$$

where E_{on}, $E_{\text{on_MOS}}$, and $E_{\text{on_IGBT}}$ are the total turn-ON switching losses of the entire hybrid switch, the SiC MOSFET, and the IGBT, respectively.

First, we will consider that the switching process is solely undertaken by either device (the IGBT or the SiC MOSFET) when an absolute magnitude of the gate turn-ON delay time is sufficiently large, say either within the interval $(-\infty, -t_{on_1})$ or $(t_{on_2}, +\infty)$. In this case, almost all the switching loss of the hybrid switch is attributable to the one subject to the hard-switching because the other one undertakes a ZVS. The forward current I_F, the dc-link voltage V_{dc}, and the junction temperatures of the devices all have the impact on the hard-switching turn-ON loss of the SiC MOSFET and the IGBT in their switching processes. In [21], the non-linear approximation method was presented for the switching loss based on the specified operating point and scaling it to the desired or actual operation point. An empirical formula giving the hard-switching turn-ON loss of the SiC MOSFET based on the non-linear approximation is given as

$$\begin{aligned} &E_{\text{on_hard_MOS}}(I_F, T_j) \\ &\quad = E_{\text{on_MOS_ref}}\left(\frac{I_F}{I_{\text{ref}}}\right)^{c_{I_\text{MOS}}}\left(\frac{V_{\text{DC}}}{V_{\text{ref}}}\right)^{d_{V_\text{MOS}}} \\ &\qquad \times (1 + T_{CS_\text{on_MOS}}(T_{j_\text{MOS}} - T_{j_\text{ref}})) \end{aligned} \tag{12}$$

where $E_{\text{on_MOS_ref}}$, I_{ref}, V_{ref}, and T_{j_ref} are the references of the turn-ON loss, the forward current, the dc- link voltage, and the junction temperature of the SiC MOSFET, respectively, obtained at specific operating conditions according to the datasheet. c_{I_MOS} and d_{V_MOS} are the exponent coefficients of the correction factors for the hard turn-ON switching loss of SiC MOSFET on load current and dc voltage, respectively. These parameters are empirically determined correction coefficients. $T_{cs_\text{on_MOS}}$ is the temperature coefficient for the SiC MOSFET, which can be extracted from the manufacture's datasheet. Their values are shown in Table I. A similar formula giving the hard-switching turn-ON loss of the IGBT can be found as

$$\begin{aligned} &E_{\text{on_hard_IGBT}}(I_F, T_j) \\ &\quad = E_{\text{on_IGBT_ref}}\left(\frac{I_F}{I_{\text{ref}}}\right)^{c_{I_\text{IGBT}}}\left(\frac{V_{\text{DC}}}{V_{\text{ref}}}\right)^{d_{V_\text{IGBT}}} \\ &\qquad \times (1 + T_{CS_\text{on_IGBT}}(T_{j_\text{IGBT}} - T_{j_\text{ref}})). \end{aligned} \tag{13}$$

Similar to the conduction losses, the hard-switching turn-ON losses are adapted with the chip area. The hard-switching turn-ON loss of the SiC MOSFET can be approximated with a linear model of the chip area [20] at given V_{dc} as

$$\begin{aligned} &E_{\text{on_hard_MOS}}(A, I_F, T_{j_\text{MOS}}) \\ &\quad = (M_{\text{on}}A + N_{\text{on}})E_{\text{on_MOS_ref}}\left(\frac{I_F}{I_{\text{ref}}}\right)^{c_{I_\text{MOS}}}\left(\frac{V_{\text{DC}}}{V_{\text{ref}}}\right)^{d_{V_\text{MOS}}} \\ &\qquad \times (1 + T_{CS_\text{on_MOS}}(T_{j_\text{MOS}} - T_{j_\text{ref}})) \end{aligned} \tag{14}$$

where M_{on} and N_{on} are the coefficients of the linear approximation of the dependency of the SiC MOSFET's switching losses on its chip area. Their values can be extracted from the series different current rating SiC MOSFETs. The gate resistance R_g and gate drive voltage V_g also have influence on the switching device's power loss. A typical gate resistance and gate drive voltage of IGBTs or MOSFETs are selected and kept constant in most cases of power converters. This article focuses on the discussion of complicated multi-variable input problem and multiobjective optimization, including $T_{\text{on_delay}}$, $T_{\text{off_delay}}$, SiC MOSFET chip size, dc voltage, load current, and junction temperatures. Therefore, the influence of gate resistance and gate drive voltage of the SiC MOSFET is not discussed in order to simplify the analysis of the loss model. Their values are considered as the same with the datasheet recommended.

Second, we will derive the switching ON loss that is jointly attributable to both devices when the gate turn-ON delay time is between $[-t_{on_1}, t_{on_2}]$. The SiC MOSFET's switching ON loss increases with the gate turn-ON delay time from $-t_{on_1}$ to t_{on_2}, while the IGBT's switching ON loss decreases. A local minimal value of the total switching ON loss of the hybrid switch results in zero delay time. This is because the current rise (*di*/*dt*) of the IGBT and the SiC MOSFET has overlap, leading to a higher *di*/*dt* of the hybrid switch than other two cases at the small magnitude of the gate turn-ON delay time. The switching ON loss of the SiC MOSFET and the IGBT during this turn-ON delay time interval can be expressed using the second-order polynomial functions of $T_{\text{on_delay}}$, which appear as follows:

$$\begin{aligned} E_{on_\text{MOS}}(A, T_{\text{on_delay}}) &= E_{\text{on_hard_MOS}}(A) \\ &\quad \times [a_1 T_{\text{on_delay}}^2 + b_1 T_{\text{on_delay}} + c_1] \end{aligned} \tag{15}$$

$$\begin{aligned} E_{\text{on_IGBT}}(T_{\text{on_delay}}) &= E_{\text{on_hard_IGBT}} \\ &\quad \times [a_2 T_{\text{on_delay}}^2 + b_2 T_{\text{on_delay}} + c_2] \end{aligned} \tag{16}$$

where the parameters can be expressed as

$$a_1 = \frac{1}{(t_{on_1}+t_{on_2})^2} \qquad a_2 = \frac{1}{(t_{on_1}+t_{on_2})^2}$$
$$b_1 = 2t_{on_1}a_1 \quad ; \quad b_2 = -2t_{on_2}a_2$$
$$c_1 = t_{on_1}^2 a_1 \qquad c_2 = t_{on_2}^2 a_2.$$

Therefore, the turn-ON switching losses of the hybrid switch at varying SiC MOSFET's chip areas can be expressed as

$$E_{\text{on_MOS}}(A, T_{\text{on_delay}}) = \begin{cases} 0, & T_{\text{on_delay}} \in (-\infty, -t_{\text{on_1}}) \\ (M_{\text{on}}A + N_{\text{on}})E_{\text{on_hard_MOS}} \\ \times (a_1 T_{\text{on_delay}}^2 + b_1 T_{\text{on_delay}} + c_1), & T_{\text{on_delay}} \in [-t_{\text{on_1}}, t_{\text{on_2}}] \\ (M_{\text{on}}A + N_{\text{on}})E_{\text{on_hard_MOS}}, & T_{\text{on_delay}} \in (t_{\text{on_2}}, +\infty) \end{cases} \quad (17)$$

$$E_{\text{on_IGBT}}(T_{\text{on_delay}}) = \begin{cases} E_{\text{on_hard_IGBT}}, & T_{\text{on_delay}} \in (-\infty, -t_{\text{on_1}}) \\ E_{\text{on_hard_IGBT}}(a_2 T_{\text{on_delay}}^2 \\ + b_2 T_{\text{on_delay}} + c_2), & T_{\text{on_delay}} \in [-t_{\text{on_1}}, t_{\text{on_2}}] \\ 0, & T_{\text{on_delay}} \in (-\infty, -t_{\text{on_1}}). \end{cases} \quad (18)$$

C. Turn-Off Switching Loss

Based on the above analysis for the turn-ON transition, the following equations for calculating the turn-OFF losses can be derived in a similar fashion. To reduce the typically large turn-OFF loss of the IGBT due to its tail current, a ZVS IGBT turn-OFF prior to the SiC MOSFET is preferred, as shown in Fig. 2. The total turn-OFF loss of the hybrid switch is expressed as

$$E_{\text{off}}(T_{\text{off_delay}}) = E_{\text{off_MOS}}(T_{\text{off_delay}}) + E_{\text{off_IGBT}}(T_{\text{off_delay}}) \quad (19)$$

where E_{s_off} is the total turn-OFF switching loss of the hybrid switch, and $E_{\text{off_MOS}}$ and $E_{\text{off_IGBT}}$ are the turn-OFF switching loss of the SiC MOSFET and IGBT, respectively. The total turn-OFF switching loss of the SiC MOSFET consists of the hard turn-OFF switching loss and the additional conduction loss during the short gate turn-OFF delay time, which can be expressed as

$$E_{\text{off_MOS}}(T_{\text{off_delay}}) = E_{\text{off_hard_MOS}} + \Delta E_{\text{cond_MOS}}(T_{\text{off_delay}}) \quad (20)$$

where $E_{\text{off_hard_MOS}}$ is the hard turn-OFF switching loss and $\Delta E_{\text{cond_MOS}}$ is the additional conduction loss. Similar to the hard turn-ON switching loss of the SiC MOSFET, the turn-OFF switching loss of the SiC MOSFET can be given as

$$E_{\text{off_hard_MOS}}(A, I_F, T_j)(M_{\text{off}}A + N_{\text{off}}) \times E_{\text{off_MOS_ref}}\left(\frac{I_F}{I_{\text{ref}}}\right)^{a_{I_\text{MOS}}}\left(\frac{V_{\text{DC}}}{V_{\text{ref}}}\right)^{b_{V_\text{MOS}}} \times [1 + T_{CS_\text{off_MOS}}(T_{j_\text{MOS}} - T_{j_\text{ref}})] \quad (21)$$

where M_{off} and N_{off} are the coefficients of the linear approximation. Since the SiC MOSFET conducts 100% forward current during the gate turn-OFF delay time, the additional conduction loss $\Delta E_{\text{cond_MOS}}$ could be modeled as a linear function of the gate turn-OFF delay time $T_{\text{off_delay}}$, which is expressed as

$$\Delta E_{\text{cond_MOS}}(A, T_{\text{off_delay}}) = \left[I_F^2 \cdot R_{ds}(A)\right] T_{\text{off_delay}} \quad (22)$$

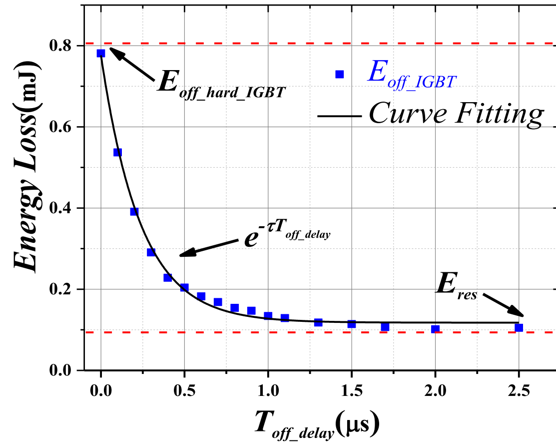


Fig. 4. IGBT turn-OFF switching loss as a function of the turn-OFF delay time between the Si IGBT and SiC MOSFET $T_{\text{off_delay}}$.

The additional conduction loss is also strongly affected by the SiC MOSFET's chip area because the ON-state resistance of the SiC MOSFET is inversely proportional to its chip area.

The IGBT is turned OFF without undertaking high voltage since the SiC MOSFET is still conducted when using the gate control patterns, as shown in Fig. 2. The large amount of stored charge in N-base region of the IGBT decreases exponentially due to the minority carrier recombination during the gate turn-OFF delay time [8]. Fig. 4 shows the typical dependency of the IGBT's turn-OFF switching loss on its gate signal's turn-OFF delay time.

The turn-OFF switching loss of the IGBT can be modeled as

$$E_{off_IGBT}(T_{off_delay}) = (E_{off_hard_IGBT} - E_{res})e^{-\tau \cdot T_{off_delay}} + E_{res} \quad (23)$$

where E_{res} is the residual turn-OFF switching loss of the IGBT, and τ is the exponential time constant for the dependency of the IGBT's switching OFF loss on the gate turn-OFF delay time. $E_{\text{off_hard_IGBT}}$ is the hard turn-OFF switching loss of the IGBT at a certain forward current.

The E_{res} is caused by which the IGBT has to undertake the dc-link voltage and remove the remaining plasma when the SiC MOSFET is hard switching OFF [22]. The magnitude of E_{res} is mainly influenced by the dc-link voltage. When the gate turn-OFF delay time between the IGBT and the SiC MOSFET is long enough, the magnitude of E_{res} is almost constant at the certain dc-link voltage. When the gate turn-OFF delay time is zero or negative, the IGBT is hard switching OFF. Similar to the hard turn-ON switching loss of the IGBT, the hard turn-OFF switching loss of the IGBT can be given as

$$E_{\text{off_hard_IGBT}}(I_{\text{IGBT}}, T_j) = E_{\text{off_hard_IGBT_ref}}\left(\frac{I_{\text{IGBT}}}{I_{\text{ref}}}\right)^{a_{I_IGBT}}\left(\frac{V_{\text{DC}}}{V_{\text{ref}}}\right)^{b_{V_\text{IGBT}}} \times [1 + T_{CS_\text{off_IGBT}}(T_{j_\text{IGBT}} - T_{j_\text{ref}})]. \quad (24)$$

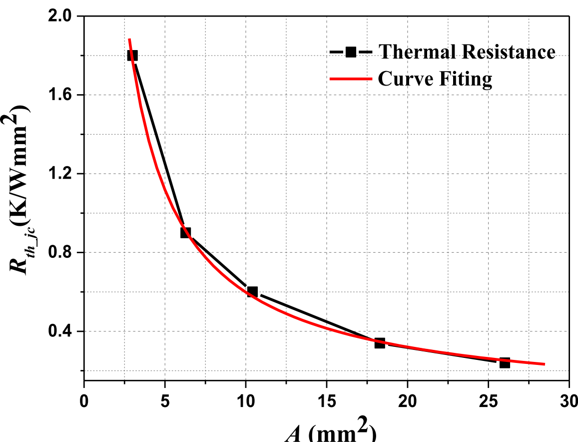


Fig. 5. SiC MOSFET thermal resistance as a function of its chip size (from Wolfspeed datasheets).

In this article, the Wolfspeed TO-247 package C2M series SiC MOSFET and the Infineon Si IGBT: IGW25N120H3 are used to extract parameters in the power loss model. The values of the coefficients in the power loss model are shown in Table I.

Therefore, neglecting the load current ripple, the total power loss of the SiC MOSFET and the IGBT in the dc–dc buck converter could be expressed as

$$P_{\text{loss_MOS}}(A, T_{\text{on_delay}}, T_{\text{off_delay}}) = (D - f_{sw}T_{\text{off_delay}})E_{\text{cond_MOS}} + f_{sw}(E_{\text{off_MOS}} + E_{\text{on_MOS}}) \quad (25)$$

$$P_{\text{loss_IGBT}}(A, T_{\text{on_delay}}, T_{off\text{_delay}}) = (D - f_{sw}T_{\text{off_delay}})E_{\text{cond_IGBT}} + f_{sw}(E_{\text{on_IGBT}} + E_{\text{off_IGBT}}) \quad (26)$$

where D is the duty cycle of the dc–dc buck converter and the f_{sw} is the switching frequency. Equations (25) and (26) show that the power losses of the SiC MOSFET and IGBT are functions of the gate control delay times and the internal SiC MOSFET's chip area. As the junction temperature of the SiC MOSFET and IGBT is dependent on their power loss, their junction temperatures are strongly affected by SiC MOSFET's chip area too.

D. Thermal Resistance Model

The thermal resistance of the SiC MOSFET is determined by its chip area and the package. The Wolfspeed TO-247 package C2M series SiC MOSFET's typical dependency between the chip area and the thermal resistance from junction to case is shown in Fig. 5.

Using a curve-fitting method, the chip-area-based thermal resistance can be modeled as

$$R_{th_jc}(A) = M_{Rth} \cdot \frac{K}{W \cdot mm^2} \cdot (\lambda_A \cdot A)^{-N_{Rth}} \quad (27)$$

where $M_{R\text{th}}$ and $N_{R\text{th}}$ are curve-fitting parameters. Since A is the active chip area of the SiC MOSFET, its thermal resistance is related to its total chip areas. Therefore, λ_A is the coefficient between the active chip area and the total chip area, which is about 1.2 in this experiment. In the steady-state operation, the relationship of the SiC MOSFET's average junction temperature and its power loss is expressed as

$$T_j = T_c + R_{th_jc} \cdot P_{\text{loss_MOS}} \quad (28)$$

where T_c is the case temperature of the SiC MOSFET. Based on (28), the dependency of the hybrid switch's junction temperatures on the varying SiC MOSFET chip area can be estimated.

TABLE II
Si/SiC Hybrid Switch Case Studies

Type	Si IGBT	SiC MOSFET	Chip Area(mm^2)	I_{IGBT}/I_{MOS}
HyS-1	IGW25N120H Chip Area: 25mm^2	C2M0280120D	2.85	4.1
HyS-2		C2M0160120D	6.29	2
HyS-3		C2M0080120D	10.42	1

III. Experimental Model Validation

The objective of this section is to experimentally validate the proposed power loss model through both double pulse testing and dc–dc buck converters. In this article, three hybrid switches (each with a different SiC chip size) are composed for behavior characterization. An Infineon 1200 V/25 A Si IGBT (IGW25N120H3) is selected as the main IGBT in these three hybrid switches, while three Wolfspeed SiC MOSFETs as an auxiliary part are used as shown in Table II. The electrical and thermal parameters for modeling are extracted from corresponding manufacture datasheet of discrete-packaged devices and bare dies. The IGBT's chip area is 25 mm^2. The IGBT is rated at 25 A under 100 °C of the case temperature, while three SiC MOSFETs are rated at 6 A, 12.5 A, and 24 A, respectively, under the same case temperature. The chip areas pertaining to them are 2.85 mm^2, 6.29 mm^2, and 10.42 mm^2, respectively.

A. Conduction and Switching Losses

The forward conduction (output characteristic) curves for the three hybrid switches under both 25 and 150 °C case temperatures are shown in Fig. 6(a) and (b), respectively. The solid and dotted lines are denoting the measured and modeling forward output characteristics, respectively. A large discrepancy could be evidenced around the intercept of V_{knee} because the exponential function of actual IGBT output characteristic was neglected by the approximation. A good match for the rest of the output characteristics can be observed that account for the variation of chip areas of the auxiliary SiC MOSFET and case temperature differences.

To validate the switching loss model of the hybrid switch, the three hybrid switches were characterized with a double pulse test at 600 V dc voltage and 25 A load current at room temperature (25 °C). The gate resistance and gate drive voltage of the SiC MOSFET are 2.5 Ω and +20 V/−5 V, and the IGBT are 22 Ω and +15 V/−5 V, which are the same with their datasheet recommended. Fig. 7 compares the measured and modeled minimal total turn-ON loss of the three hybrid switches (each with a different SiC chip size) under an optimum gate turn-ON delay time.

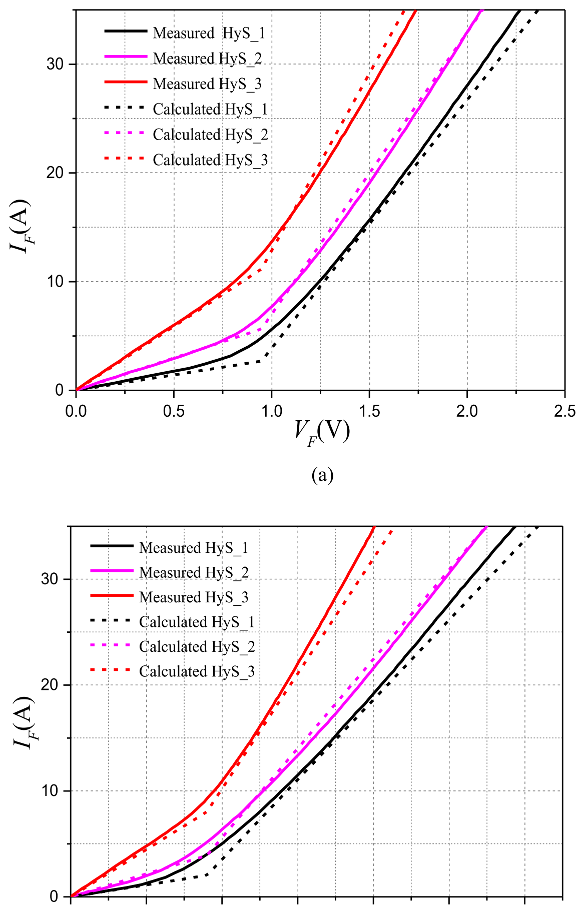


Fig. 6. Comparison of measured and modeled forward I–V characteristics of three hybrid switches at (a) 25 °C and (b) 150 °C.

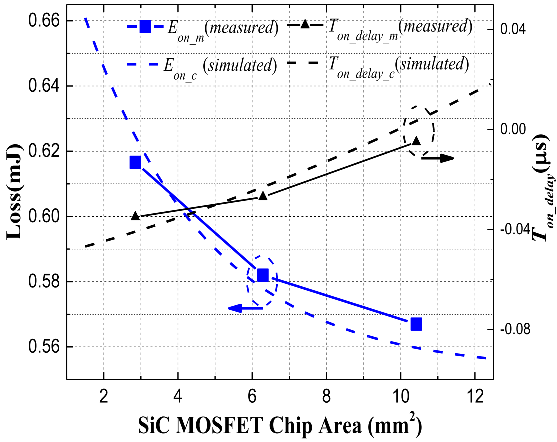


Fig. 7. Comparison of the measured and simulated minimum turn-ON switching loss and optimized $T_{\text{on_delay}}$.

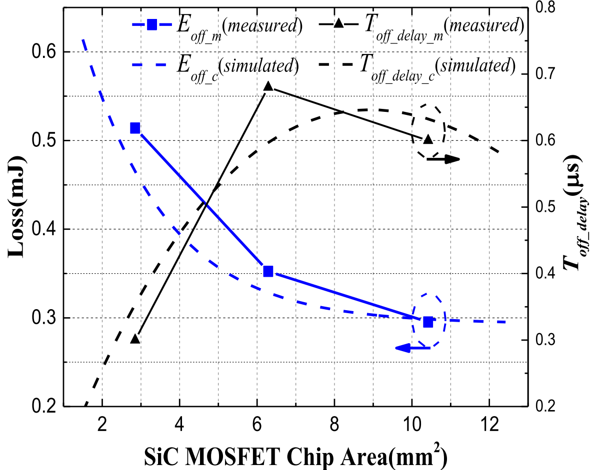


Fig. 8. Comparison of the measured and simulated minimum turn-OFF switching loss and optimized $T_{\text{off_delay}}$.

$T_{\text{on_delay_}m}$ and $T_{\text{on_delay_}c}$ are the corresponding optimal gate turn-ON delay time for the measured and calculated cases, respectively. The minimum turn-ON losses of the Si/SiC hybrid switches decreases significantly with increasing SiC MOSFET chip area. This is because the turn-ON speed of the hybrid switch during the turn-ON process is slightly increased with the increase of the SiC MOSFET chip size.

Fig. 8 compares the measured and calculated minimal total turn-OFF losses of the three hybrid switches under an optimum gate turn-OFF delay time. Note that the total turn-OFF loss for the SiC MOSFET also includes its conduction loss during the turn-OFF delay time period. $T_{\text{off_delay_}m}$ and $T_{\text{off_delay_}c}$ are the corresponding measured optimal gate turn-OFF delay time and calculated optimal gate turn-OFF delay time, respectively. The total turn-OFF loss of the three hybrid switches decreases with increasing SiC MOSFET chip area because of two factors. First, the SiC MOSFET's additional conduction loss ΔE_{c_off} during the turn-OFF delay decreases with increasing chip size. Second, IGBT's share of the load current decreases with the increase of the SiC MOSFET chip size inducing the turn-OFF loss $E_{\text{off_IGBT}}$ to be decreased with the increasing of SiC MOSFET chip size.

B. DC–DC Buck Converter Case Study

In order to investigate the hybrid switch performance at different SiC chip size in an actual power electronic application, we build a dc–dc buck converter using the three hybrid switches. The impact of the SiC MOSFET's chip size on the efficiency and thermal behaviors is studied.

The switching frequency, input voltage, and output voltage of the dc–dc buck converter is 20 kHz, 600 V, and 300 V, respectively. A 30% ripple current level is achieved with a 1-mH filter inductor. The CREE 1200 V/24 A C4D15120D Silicon Carbide Schottky Diode is used as the low side freewheeling diode in the buck converter. The conversion efficiency of the hybrid switch converter is measured by the power analyzer ZIMMER LMG640 and the case temperatures of both devices are measured by an infrared camera of FLIR A655sc, as shown in Fig. 9. The *RC* network is used to estimate the junction temperatures of the hybrid switch. In the steady state, the simplified *RC* thermal equivalent circuit of the hybrid switch is shown in Fig. 10, where T_a is the ambient temperature, and $R_{th(c-a)}$ is the device case to ambient thermal resistance, which is determined by the cooling

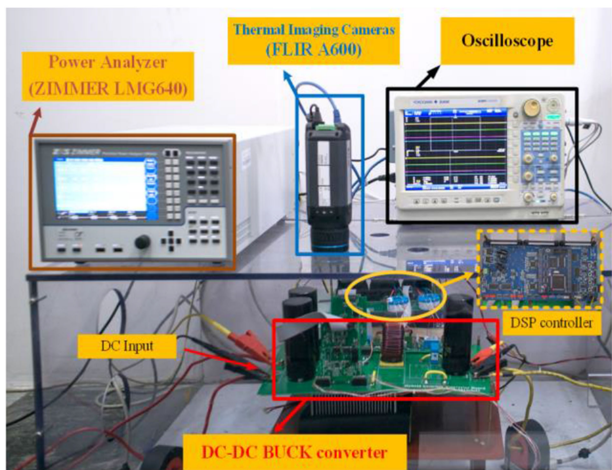


Fig. 9. Prototype of the hybrid switch dc–dc converter.

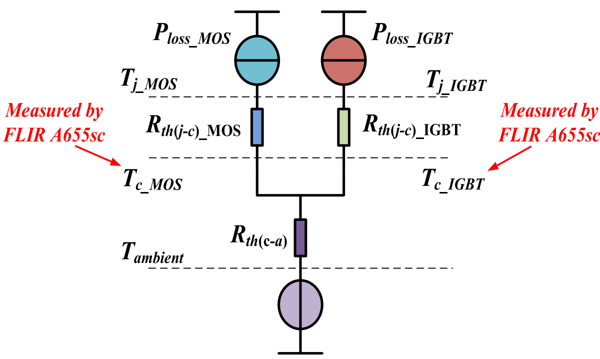


Fig. 10. Simplified thermal equivalent circuit diagram of the hybrid switch.

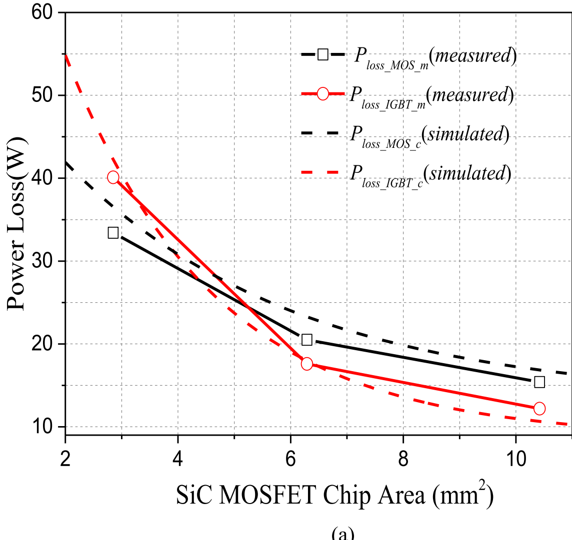
strategy adopted by the converter. In order to calculate the power loss and junction temperatures of the hybrid switch in converter applications, $R_{th(c-a)}$ should be known.

If we first estimated the junction temperatures of the hybrid switch using (28) based on the measured power loss and case temperatures, $R_{th(c-a)}$ can be estimated as

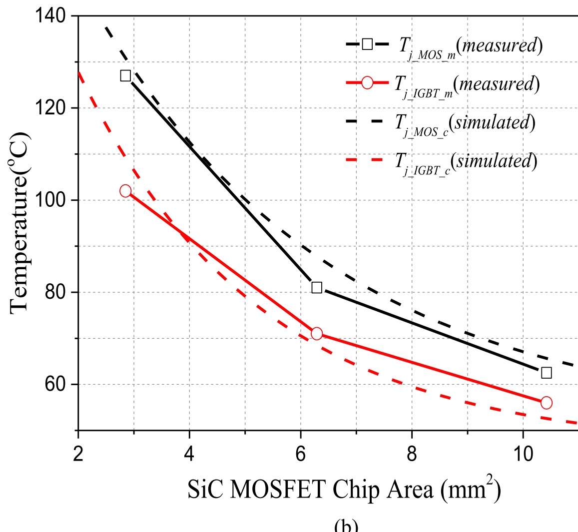
$$R_{th(c-a)} = \frac{T_j - T_a}{P_{\text{loss}}} - R_{th(j-c)} \tag{29}$$

In this experiment, the estimated $R_{th(c-a)}$ is about 1.6 K/W.

By applying the optimal gate turn-ON and turn-OFF delay times as shown in Figs. 7 and 8, the measured efficiencies of the buck converter under a 7.5-kW output power for the three types of hybrid switches are 97.53% ($A = 2.85$ mm^2), 98.093% ($A = 6.29$ mm^2), and 98.233% ($A = 10.42$ mm^2), respectively. The efficiency improves with the increase of the SiC MOSFET's chip size. The power losses and junction temperatures with respect to the three hybrid switches are shown in Fig. 11(a) and (b), respectively. The solid and dotted lines denote the measured and calculated results, respectively. $P_{\text{loss_MOS_}m}$ and $P_{\text{loss_IGBT_}m}$ are the measured power loss of the SiC MOSFET and IGBT, respectively, which are obtained by the integral of the product of measured voltage and current waveforms over a duty cycle in the steady state. The junction temperatures ($T_{j\text{_MOS_}m}$ and $T_{j\text{_IGBT_}m}$) of the SiC MOSFET and IGBT are estimated based on the power losses and case temperatures, respectively. $P_{\text{loss_MOS_}c}$ and $P_{\text{loss_IGBT_}c}$ are calculated power loss based on the power loss model, and $T_{j\text{_MOS_}c}$ and $T_{j\text{_IGBT_}c}$ are the calculated junction temperatures based on the calculated power loss.



(a)



(b)

Fig. 11. Comparison of the measured and modeled junction temperature and power loss of the hybrid switch under steady-state operation of the dc–dc buck converter. (a) Power loss. (b) Junction temperature.

When the SiC MOSFET chip area is 2.85 mm^2, the power loss of the IGBT is higher than that of the SiC MOSFET. It is because the turn-OFF switching loss and the conduction loss of the IGBT are large at the small chip area SiC MOSFET condition. Though the power loss of the IGBT is larger than the SiC MOSFET, IGBT's junction temperature is still lower than that of the SiC MOSFET due to the small thermal resistance of the IGBT. When the SiC MOSFET's chip area increases from 2.85 to 6.29 mm^2, the estimated junction temperature of the SiC MOSFET decreases from 127 to 82 °C, and the IGBT decreases from 102 to 71 °C. The corresponding power loss of the SiC MOSFET decreases

from 33.4 to 22.5 W, and the power loss of the IGBT decreases from 40.1 to 18.6 W. The junction temperatures of the hybrid switch's two internal devices are dramatically decreased when the SiC MOSFET's chip area increases from 2.85 to 6.29 mm^2. However, the improvement is step down when the SiC MOSFET's chip area increases from 6.29 to 10.42 mm^2. The estimated junction temperature of the SiC MOSFET decreases from 82 to 64.5 °C, and the IGBT decreases from 71 to 57 °C, when the SiC MOSFET's chip area increases from 6.29 to 10.42 mm^2. The corresponding power loss of the SiC MOSFET and IGBT only decreases by 5 W and 4.4 W, respectively. The small difference between the measured and simulated results indicates the validation of the power loss model.

IV. Device Sizing Optimization Methodology

The objective of this section is to develop a methodology to minimize SiC device size while optimizing total IGBT/MOSFET power loss and ensuring maximum junction temperature still below a specified value. Here, we select an IGBT with the full current rating of the hybrid switch since the cost of the IGBT is relatively insignificant. A small SiC MOSFET device size will lower the switch cost, but result in an overheated SiC chip and/or high total loss for the hybrid switch. Furthermore, the gate control delay times also affect the total power loss and junction temperature of the hybrid switch. This is a very complex multivariable optimization problem which involves not only SiC die size but also its gate control delay times. Therefore, we propose a methodology using the aforementioned loss model to minimize SiC device size while optimizing total power loss and ensuring maximum junction temperature still below 150 °C, as shown in Fig. 12. The methodology is divided into three main steps to clearly illustrate the process of selecting the optimal SiC chip area. In the first step, the power losses and junction temperatures of the hybrid switch at different $T_{\text{on_delay}}$, $T_{\text{off_delay}}$, and different SiC MOSFET chip areas are calculated. In the second step, the common optimal $T_{\text{on_delay}}$ and $T_{\text{off_delay}}$ ranges at different SiC MOSFET chip size are identified based on the calculated power loss from the first step. In the third step, the minimum SiC MOSFET chip size is identified according to a criteria with a maximum junction temperature less than 150 °C while operating within the optimal delay time ranges identified from the second step.

In this experiment, the Infineon 1200 V/25 A Si IGBT (IGW25N120H3) is selected as the main IGBT. The interval of the $T_{\text{on_delay}}$ and $T_{\text{off_delay}}$ is set as $T_{\text{on_delay}} \in [-0.25\ \mu\text{s}, 0.25\ \mu\text{s}]$, $T_{\text{off_delay}} \in [0\ \mu\text{s}, 2\ \mu\text{s}]$. The duty cycle, dc voltage, and forward current of the hybrid switch are set as 50%, 600 V, and 25 A, respectively. The different case temperatures represent the different cooling condition of the hybrid switch based buck converter. For example, $T_c = 50$ °C represents the converter using a bulky cooling system to keep the hybrid switch at low under a low-case-temperature condition. And $T_c = 100$ °C represents the converter using a lighter cooling system. Considering the worst operation conditions of the SiC MOSFET in the real applications, the case temperature of the two devices is set 100 °C.

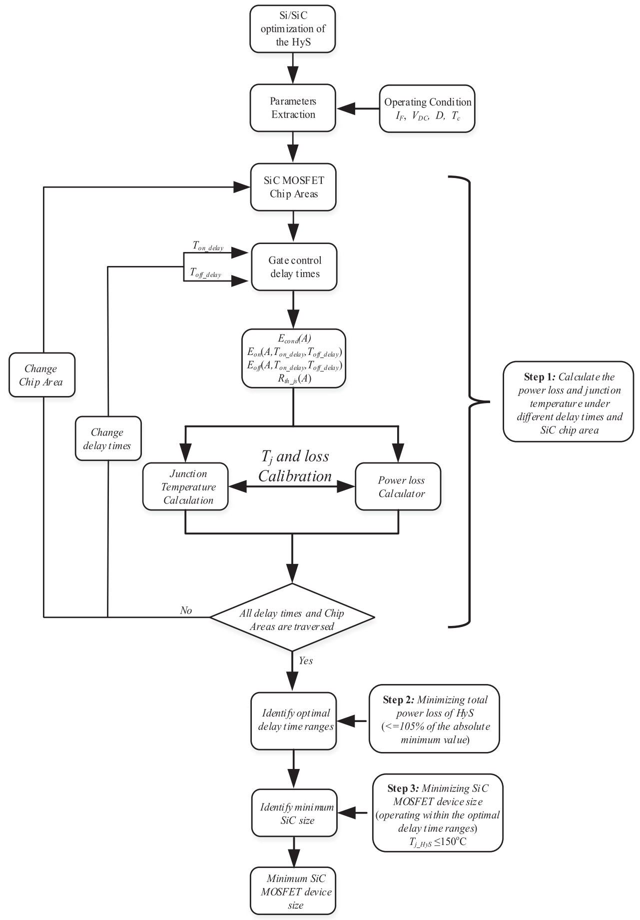


Fig. 12. Methodology for optimizing SiC device size of Si/SiC hybrid switch.

In the first step, the power losses and junction temperatures of the hybrid switch at different delay times and different SiC MOSFET chip area are calculated. $T_{\text{on_delay}}$, $T_{\text{off_delay}}$, and SiC MOSFET chip area are the main parameters that strongly affect the power losses and junction temperatures of the hybrid switch. At the given $T_{\text{on_delay}}$, $T_{\text{off_delay}}$, and SiC MOSFET chip area, the power losses and junction temperature of the hybrid switch can be calculated based on the power loss model. As shown in Fig. 12, a three-layer loop is used to calculate the power losses and junction temperatures of the hybrid switch at different SiC MOSFET chip areas and different delay times (including $T_{\text{on_delay}}$ and $T_{\text{off_delay}}$). Because the power loss and junction temperature of the device are coupled, in order to obtain the precise power loss and junction temperature of the hybrid switch, the power loss and junction temperature can be obtained in an iterative manner. In the first iteration, the power loss is calculated based on the case temperature, and then a new and more precise junction temperature can be obtained using this calculated power loss, then the new power loss can be calculated based on this new junction temperature. After several iterations, the final power loss value and junction temperature will be reached.

Based on this method, Fig. 13 shows the total power loss of the hybrid switch at different SiC MOSFET chip areas and different gate control delay times. The *x*-axis and *y*-axis represent

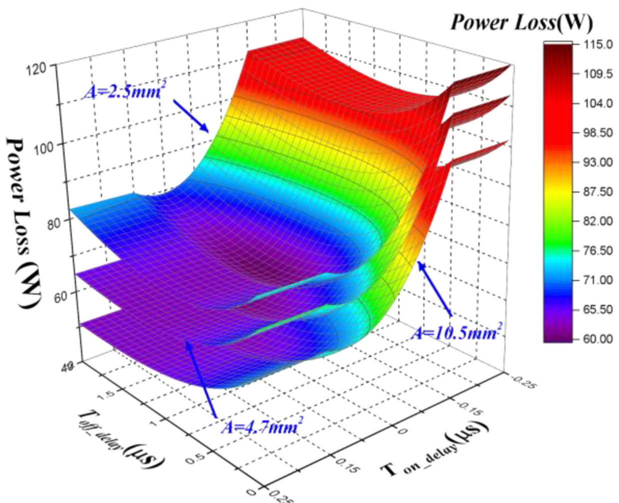


Fig. 13. Calculated power loss of a hybrid switch at different gate control delay times and SiC MOSFET chip areas.

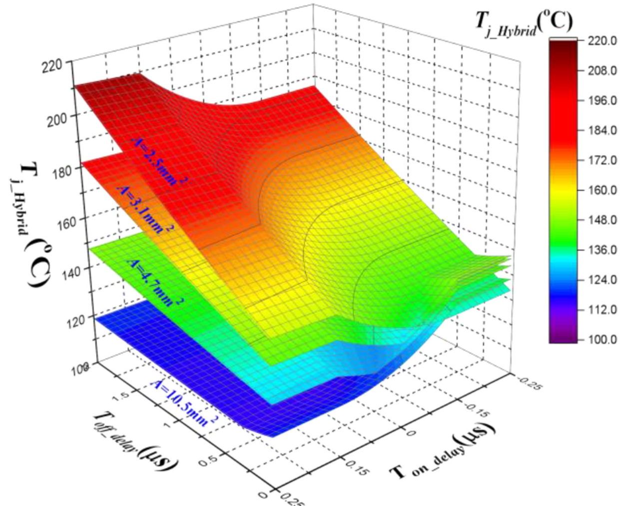


Fig. 14. Junction temperature of hybrid switch at different gate control delay times and SiC MOSFET chip areas.

$T_{\mathrm{on_delay}}$ and $T_{\mathrm{off_delay}}$, respectively. In addition, the z-axis is the total power loss of the hybrid switch. In Fig. 13, three SiC MOSFET chip areas within a wide range are chosen to show the overall power loss distribution of the hybrid switch as a function of SiC MOSFET chip area.

Generally, the total power loss of the hybrid switch is increased with the decrease of the SiC MOSFET chip size because the large chip size SiC MOSFET has smaller conduction and switching losses. The effects of the gate control delay times on the total power loss of the hybrid switch are more complicated than that of the SiC MOSFET chip size. The hybrid switch's total power loss under positive gate turn-ON delay time is obviously smaller than that under negative gate turn-ON delay time because the hard turn-ON switching loss of the SiC MOSFET is smaller than that of the IGBT. The hybrid switch's total power loss decreases first and then increases with the increase of the gate turn-OFF delay time. It is because although the IGBT's turn-OFF loss is decreased with the increase of the gate turn-OFF delay time, the SiC MOSFET's additional conduction loss is increased with the gate turn-OFF delay time. When the gate delay times are appropriate, the total power loss of the hybrid switch can be minimized, as shown in Fig. 13.

Similarly, in Fig. 14, we choose several different SiC MOSFET areas within a wide range to show the dependency of the hybrid switch's junction temperature distribution on the SiC MOSFET chip area. The x-axis and y-axis represent $T_{\mathrm{on_delay}}$ and $T_{\mathrm{off_delay}}$, respectively. In addition, the z-axis is the maximum junction temperature of the hybrid switch.

The maximum junction temperature of the hybrid switch is dramatically decreased with the increase of the SiC MOSFET chip size, as shown in Fig. 14. This is because of the smaller total power loss and larger thermal resistance of the SiC MOSFET under the larger SiC MOSFET chip size. The gate control delay times strongly affect the hybrid switch's maximum junction temperature too. When the gate turn-ON and turn-OFF delay times are large, the junction temperature of the hybrid switch is large because the small chip size SiC MOSFET undertakes the

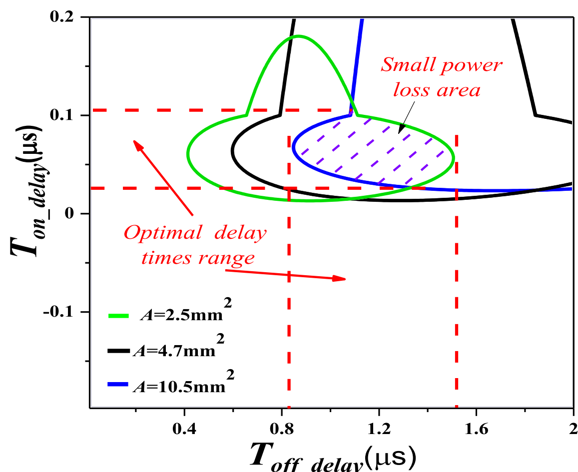


Fig. 15. Optimal range of gate control delay times of the hybrid switch for a total power loss within 5% of the minimum value ($<=$ 105% of the absolute minimum value).

hard turn-ON switching loss and large additional conduction loss. The maximum junction temperature of the hybrid switch may be higher than the 150 °C with the decrease of the SiC MOSFET under some specific gate delay time range.

In the second step, the optimal gate control delay times to achieve the minimum total power loss of the hybrid switch at different SiC MOSFET chip size are identified based on the calculated power loss from the first step. From the practical application consideration, the optimal gate control delay times to achieve the minimum total power loss should be within a range to provide some engineering margin for hybrid-switch-based converter design. It is because the cooling conditions, driver solutions, and system stray inductance in the actual hybrid-switch-based converter applications may be different to the simulation conditions. Therefore, as shown in Fig. 15, the optimal common gate control delay time range can be identified for the hybrid switch to achieve the minimum total power loss (within a margin

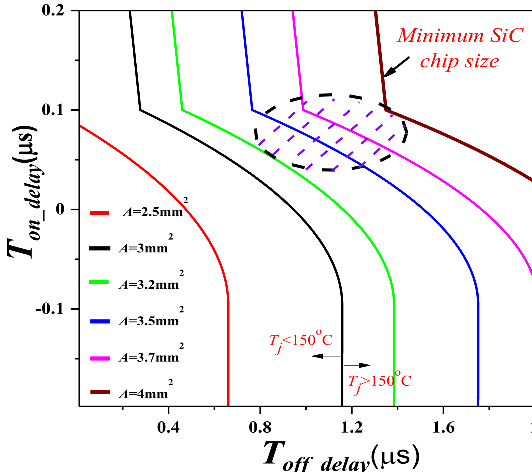


Fig. 16. Minimum SiC MOSFET chip size optimization (reducing the SiC chip size as small as possible while ensuring the optimal delay time range below 150 °C).

of 5%) at different SiC MOSFET chip sizes. The small overlap area of the gate turn-ON and turn-OFF delay times offers the minimal total power loss of the hybrid switch under different SiC MOSFET chip sizes.

In the third step, the junction temperature of the hybrid switch when operating within the optimal gate control delay time range identified from the previous step is studied, and the minimized SiC chip size is identified, which offers a maximum junction temperature less than 150 °C while operating within the optimal range of gate delay times from the previous step. Fig. 16 shows the corresponding $T_{\mathrm{on_delay}}$ and $T_{\mathrm{off_delay}}$ distribution when the maximum junction temperature of the hybrid switch is equal to 150 °C under different SiC MOSFET chip size.

When the gate delay times are in the left of the lines, the maximum junction temperature of the hybrid switch is below 150 °C, otherwise is higher than 150 °C. When the SiC MOSFET chip size is very small such as 2.5 mm^2, the optimal gate delay times range (identified from the previous step) is out of the safe junction temperature operation range. This is because the high junction temperature of the SiC MOSFET is caused by its large power loss and thermal resistance. With the increase of the SiC chip size, the optimal gate delay time ranges are gradually included within the safe operation delay time range. The minimum SiC MOSFET chip size can be identified which offers a maximum junction temperature less than 150 °C while operating within the optimal delay time ranges. In this experiment, the minimum SiC MOSFET chip size is about 4 mm^2, as shown in Fig. 16, and the corresponding current rating is about 9 A.

V. Conclusion

In this article, a generalized power loss model for the Si/SiC hybrid switches with total power loss and junction temperature as outputs and SiC device size as a continuous input variable is proposed, and experimentally validated through both simple double pulse testing and a dc–dc buck converter case study. The influence of the turn-ON and turn-OFF gate control delay times between the internal IGBT and SiC MOSFET on the total power loss and maximum junction temperature of the hybrid switch in the double pulse test and dc–dc buck converter is extensively investigated by simulations and experimental studies.

Based on the power loss model, a methodology to minimize the internal SiC MOSFET's size while optimizing the total power loss of hybrid switch and ensuring its maximum junction temperature still below 150 °C is developed. It consists two main steps. In the first step, the turn-ON and turn-OFF delay times are optimized to a narrow range, which provides a minimum total power loss (within a margin of 5%) within a wide range of the SiC MOSFET chip size and offers some engineering margin for hybrid switch gate driver design too in actual applications. In the next step, a minimum SiC device size can be identified, which offers a maximum junction temperature less than 150 °C while operating within the optimal range of gate delay times from the previous step. Using this method, the optimizing SiC MOSFET device sizing can be obtained to achieve the optimized cost-effectiveness of the hybrid switch in converter applications.

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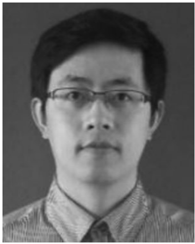

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