Parallel-Converter System Grid Current Switching Ripples Reduction Using a Simple Decentralized Interleaving PWM Approach

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***Abstract*—A simple decentralized interleaving PWM approach is proposed for parallel grid-tied converters, in order to achieve significant reduction of switching current ripples at the point of common couplings (PCC). First, the remote PCC voltage phase angle information is calculated through only the local measurement of a distribution generation (DG) unit converter and the estimation of the corresponding feeder voltage drops. With simple interpolations, the discretized PCC voltage angle information at a DG local controller is used as a novel synchronizer to effectively identify the carrier angle of DG units at the exact time instant of the PCC voltage phase angle zero crossing. Then, the relative digital carrier phase angles of parallel DG units are adaptively adjusted in a high-resolution manner until they are properly interleaved. It has been validated that the proposed modulation approach is effective under adverse situations with mismatched feeder impedances, processor crystal oscillator frequency deviations, and notable grid voltage frequency/magnitude disturbances.**

***Index Terms*—Adaptive carrier, interleaving pulsewidth modulation (PWM), parallel grid-tied converters, power quality, switching harmonic.**

I. Introduction

AN INCREASING number of grid-tied pulsewidth modulation (PWM) interfacing converters have been integrated into modern power systems for many applications including active-front end of variable frequency drive, distribution generation (DG), grid-interactive energy storage, and power conditionings in [1] and [2]. With high penetration level of power electronic converters, the control of grid-tied converter becomes more challenging due to a few major issues such as control loops interaction, protection interferences, and the power quality problems.

Among various types of grid-tied converter control objectives, the converter current tracking performance has always attracted extensive attention. In general, the current control approaches can be classified into a few types according to the control bandwidth and effective frequency ranges. First, the proportional and resonant (PR) controller [3] in the stationary reference frame has been well studied to replace the conventional PI regulator in the rotating reference frame. To improve grid-tied converter output current fundamental component tracking accuracy even with low-switching frequencies, an improved PR current regulator [4] was developed where the impulse invariance method is adopted to replace the conventional Tustin transformation for the digital implementation. In addition, the sampling and PWM processing delays are further compensated using an interpolation approach [5]. On the other hand, to reduce the intermediate frequency range resonance of grid-tied converter output filters, various active damping methods including virtual impedance based approach in [6] and [7], the multiloop cascaded control approach [8], and the model-based predictive control with inherent active damping capability [9]–[11] have been extensively studied. For high-frequency switching ripples of converters above closed-loop control bandwidth, they are mainly compensated through properly designed passive output filters instead of using any active approaches in [12] and [13].

However, for cost-effective high power converters with relatively low switching frequency but small output filter, the switching ripples can be quite obvious [14]. When multiple high power converters with the same control and circuitry parameters are placed together, such as the case of a centralized solar power or wind power station, the sum of the switching ripples flowing into the main grid can be further aggregated in [15] and [16], leading to serious power-quality problems.

Alternatively, if a centralized controller is adopted to synchronize the digital carriers of all parallel converters, it is possible to actively control the displacement among parallel converter digital carriers to obtain a few favorable features. For instance, the common mode voltage reduction or even elimination can be realized via adaptively modulating dual converters with opposite dynamic common mode voltage polarity in [17] and [18]. In addition, it has been well understood that the dominated switching ripples of parallel converter can be cancelled using

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interleaving PWM approaches in [19] and [20]. Note that the circulating current among parallel converters may be amplified when the carriers of converters are shifted for switching ripples reduction in [21] and [22]. To address this problem, either matching transformer or the separated dc voltage rails can be considered to cutoff the path for zero sequence current flow [23]. Furthermore, to reduce the cost of the system, coupled inductor or common mode inductor in [24] and [25] to increase the impedance of the zero sequence equivalent circuit has also been considered as an alternative solution. In more recent years, an interesting hierarchical PWM modulation architecture and a global synchronized modulation approach were proposed in [26] and [27]. The key idea of this modulation approach category is that the carrier for each converter module is implemented at the power module local processor. At the same time, local processors are all synchronized with a main controller using either high- or low-bandwidth communication systems. Then, both the switching ripple current and the common mode current of the system can be reduced via using interleaving PWM approach. However, once communication failures appear, the performance of these interleaving modulation approaches cannot be guaranteed.

To address the limitation of centralized interleaving PWM approaches for parallel grid-tied converter switching ripple reduction, a decentralized PWM method is developed using the point of common couplings (PCC) voltage phase angle as a robust synchronizer. First, the PCC voltage phase angle is calculated by obtaining the voltage drops on the feeder impedance and the voltage phase angle at the point of connection (PoC). Then, for each converter, the digital carrier angle at the exact time instant of the estimated PCC voltage phase angle zero crossing is captured through a simple linear interpolation process. Afterwards, an online carrier shifting approach is adopted to dynamically adjust digital carrier angles of parallel converters, without involving any communications between their local processors. By using this fully decentralized modulation approach for parallel converters, an accurate interleaving PWM can be obtained for the reduction of switching current ripples at PCC, even under the case of uncertain crystal oscillator deviations at local controllers or grid voltage variations.

II. Critical Review of Conventional Approaches

A. Conventional Decentralized Control

Fig. 1 shows a simplified diagram of grid-tied system with two parallel converters. They are connected to the common ac bus and each converter is regulated independently without any communication. It is seen that the total harmonic distortion (THD) of DG output current $I_{L(a),DG1}$ and $I_{L(a),DG2}$ are mainly fixed to 22.5% in the entire simulation process due to nontrivial switching ripples. However, as the crystal oscillator frequency of two converters has -10 PPM and $+10$ PPM deviation, the actual carrier frequency of the corresponding converter is 0.99999 and 1.00001 kHz, respectively. Even with slight deviations, switching ripples of the sum of DG currents $I_{\mathrm{sum}(a)}$ is slowly time-varying. Accordingly, it is seen that the THD of the sum of DG currents $I_{\mathrm{sum}(a)}$ is only 4.96% at the beginning of the simulation due to the opposite carrier interleaving angles between two converters, while the grid current THD increases to peak value at 22.5% when the carrier interleaving angles become almost the same at 25 s.

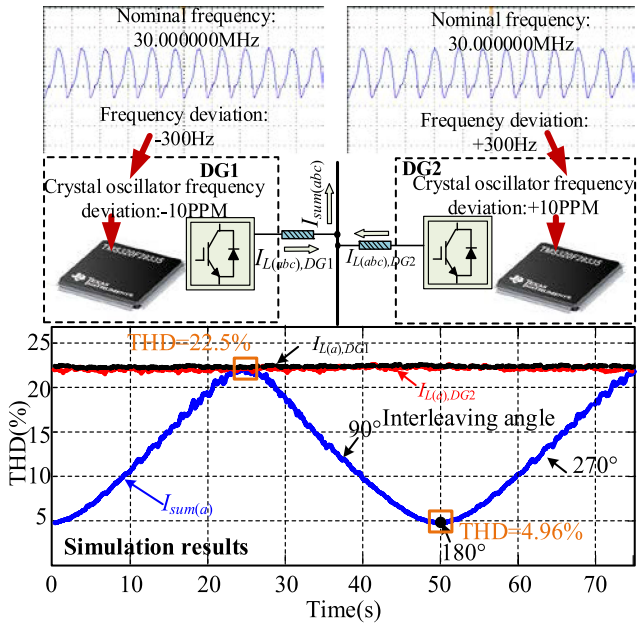

Fig. 1. Time-varying output current THD profile when power converter processor crystal oscillator frequency deviation exists.

B. Centralized Control

In order to overcome the crystal oscillator frequency deviation problems in the abovementioned fully decentralized parallel converters-based system, a well-accepted approach is to use centralized controller for all PWM gating signals generation and transmission, as shown in Fig. 2. The power circuit is shown in the top half of the diagram, where three converters are connected to the common ac bus (PCC) with their respective feeders (L_F and R_F). In addition, each interfacing converter has an output choke (L_f and R_f). For parallel grid-tied converter-based system, there is usually a capacitor bank (C_g) at PCC to further absorb the high frequency switching harmonics from converter bridges. In order to focus on the performance of DG current regulation, the dc rail of each converter is directly connected to a battery bank to stabilize dc rail voltage.

The control diagram of the system is shown in the bottom of Fig. 2. First, the PCC voltage angle (θ_{PCC}) is extracted for grid synchronization of parallel converters using a PLL. Then, for each converter, the instantaneous reference current ($I^{\mathrm{ref}}_{(\alpha\beta)}$) in the two-axis stationary reference frame is determined according to the corresponding real and reactive power references (P^{ref} and Q^{ref}). Afterwards, a current regulator ($G_{cur}(s)$) is adopted to ensure a rapid tracking of grid current and the output of the current regulator is the reference voltage (V^{ref}) for PWM modulation processing. In order to obtain a proper switching ripple mitigation performance, the carrier phase angles (φ_{Car}) of parallel converters are interleaved.

It is necessary to note that this system has two types of angles. The first one is the angle of PCC voltage (θ_{PCC}), which varies

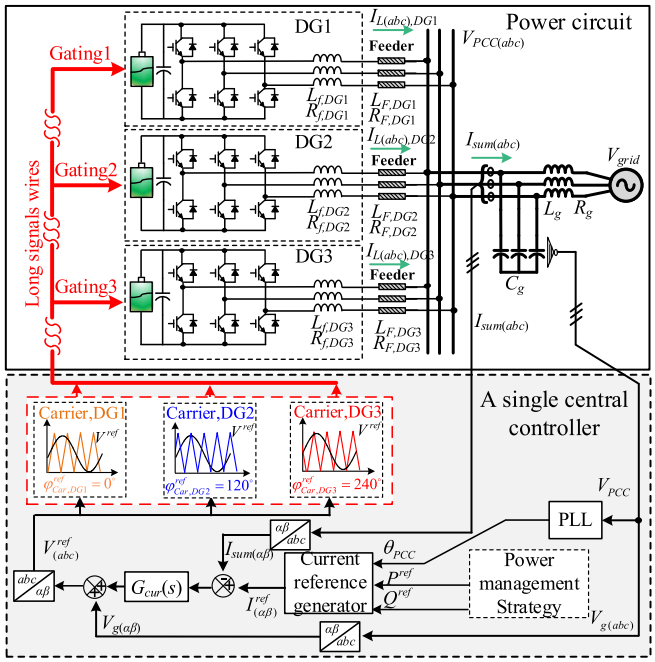

Fig. 2. Diagram of multiple grid-tied converters with a single central controller.

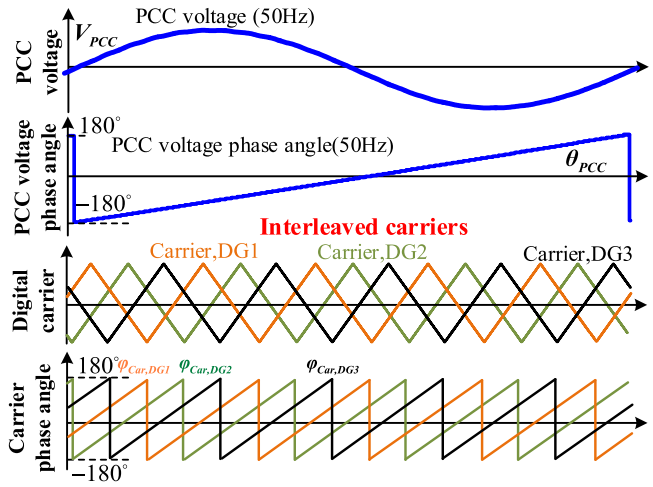

Fig. 3. Illustration of PCC voltage and digital carrier phase angles.

periodically at mainly fixed 50 Hz frequency. The second one is the angle of digital carrier (φ_{Car}). When the digital carrier works in "count up and count down" mode [28], a complete process is defined as a digital carrier cycle and the corresponding angle φ_{Car} varies from -180° to 180°. Their differences are further illustrated in Fig. 3.

The synchronized gating signals, as shown in Fig. 2, need to be sent from the central controller to each converter power circuit via long signals wires, such as in the case of a solar power station with distributed solar inverters. This long signal wiring configuration suffers from high costs, rich noises, and low reliability. In addition to the centralized control to achieve interleaving PWM, there are also efforts of realizing global synchronous PWM via the assistance of low bandwidth communications between multiple digital signal processors (DSPs) of parallel converters. In [27], an interesting master–slave control approach is proposed where one DSP acts as a global synchronous unit to send synchronous pulses and shifting angles information to other DSP chips in a periodical manner. Accordingly, satisfactory interleaving PWM performance is obtained. However, this method still needs communications between converter processors and the THD of the grid current at the synchronous pulses generation time period may be slightly affected.

III. Proposed Decentralized Control Approach

In order to overcome the limitations of conventional centralized approaches as mentioned previously, a decentralized interleaving PWM approach is proposed in this section.

A. System Configuration and Overall Control Architecture

The diagram of a three-converter based grid-tied system with fully decentralized control and modulation approaches is shown in Fig. 4. In general, the power circuit configuration is similar to that in Fig. 2. As the centralized control and communications are abandoned in this proposed method, only the local processor of DG3 is shown in the left part of Fig. 4.

First, the real power reference, reactive power reference, DG output current, PoC voltage, dc link voltage, and carrier phase angle of this DG3 are oversampled at a relatively high rate at fixed 20 kHz as $P^{\mathrm{ref}}(k)$, $Q^{\mathrm{ref}}(k)$, $I_{L(abc)}(k)$, $V_{PoC(abc)}(k)$, $V_{\mathrm{dc}}(k)$, and $\varphi_{\mathrm{Car}}(k)$, where k denotes the sampled value at the kth interval. In addition, a digital PLL using second-order generalized integrator (SOGI) is adopted to obtain the PoC voltage phase angle as $\theta_{PoC}(k)$. The reference output current of the DG unit is expressed as $I^{\mathrm{ref}}_{(\alpha\beta)}(k)$ and a well understood PR $G_{cur}(z)$ is adopted to regulate the DG output current $I_{L(\alpha\beta)}(k)$ as

$$\begin{cases} V^{\mathrm{ref}}_{(\alpha\beta)}(k) = G_{cur}(z)\cdot(I^{\mathrm{ref}}_{(\alpha\beta)}(k) - I_{L(\alpha\beta)}(k)) + V_{PoC(\alpha\beta)}(k) \\ G_{cur}(z) = k_{p\_cur} + \dfrac{2\cdot k_{i\_cur}\cdot T_s\cdot \ln(z)}{\ln^2(z)+(T_s\cdot\omega_0)^2} \end{cases} \tag{1}$$

where $V^{\mathrm{ref}}_{(\alpha\beta)}(k)$ is the reference voltage in the two-axis stationary reference frame for PWM modulation processing, k_{p_cur} is the proportional gain, k_{i_cur} is the resonant controller gain, ω_0 is the fundamental angular frequency, and T_s is the sampling period of the system. In this article, as low switching frequency converter is selected for case study, the impulse invariance method transformation is adopted to obtain the discretized format of the current regulator $G_{cur}(z)$.

In addition, the local processor of each converter consists of a grid and carrier angle detection block and a dynamic carrier frequency adjustment block. The grid and carrier angle detection block is mainly responsible for calculating the angles of PCC voltage via PoC voltage measurement and the estimation of voltage drops on the DG feeders. Then, the digital carrier angle at the exact time instant of PCC voltage phase angle zero crossing is estimated using a linear interpolation approach. In addition, this block provides carrier angle at the exact time of PCC voltage angle zero crossing to the dynamic carrier frequency adjustment process. The details are introduced in the following two subsections.

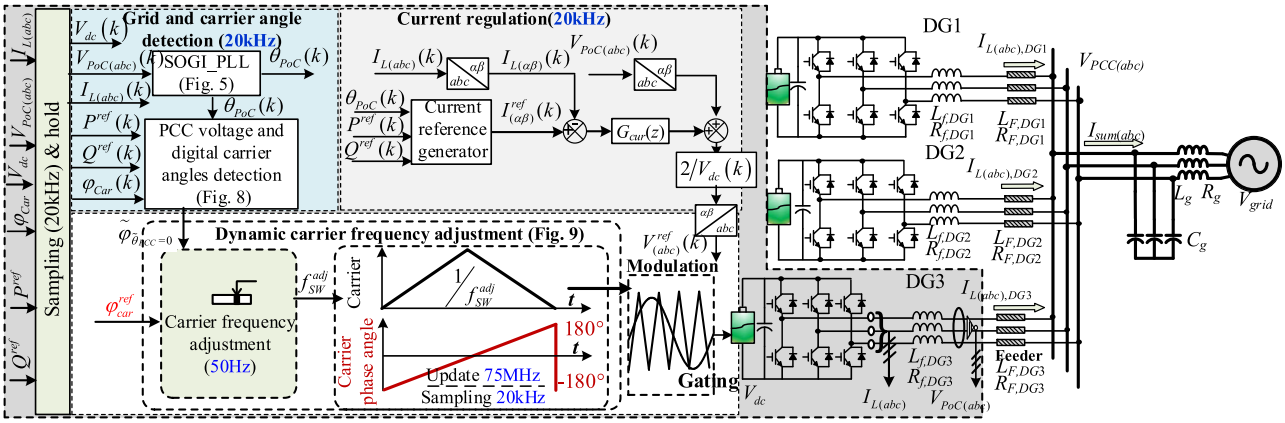

Fig. 4. Overall diagram of grid-tied converter using the proposed decentralized PWM modulation approach.

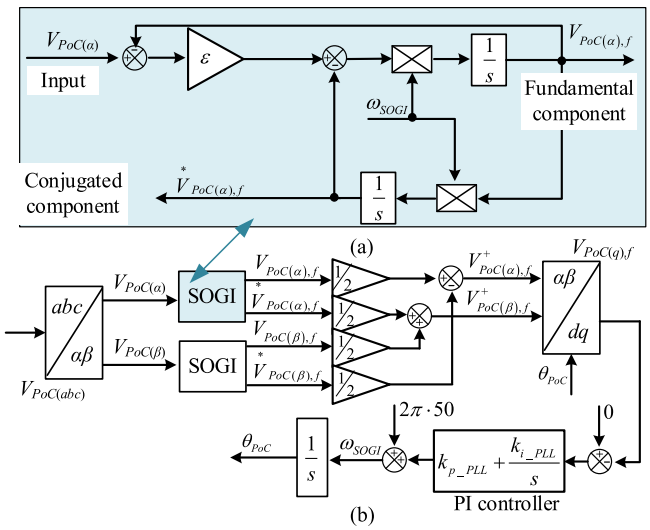

Fig. 5. Diagram of SOGI based PLL for PoC phase angle detection. (a) SOGI. (B) SOGI-PLL.

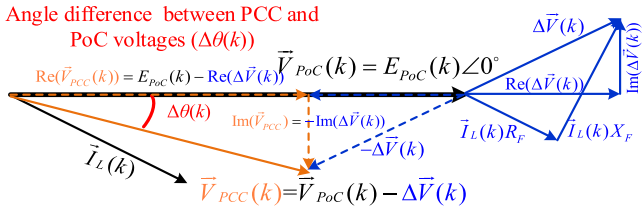

Fig. 6. Voltage/current phasor diagram of grid-tied converter.

B. PCC Voltage and Digital Carrier Phase Angles Detection

Once the PCC voltage angle information is accurately detected in a real-time manner by all converter local processors, it can be used as an inherent synchronizer or digital time based on the system. For the proposed decentralized system with only local measurement, the PCC voltage angle information detection can be achieved by following two steps.

First, as mentioned earlier, the PoC voltage $V_{PoC(abc)}(k)$ is sampled at fixed 20 kHz rate and a second-order generalized integrator-based phase-locked-loop (SOGI-PLL) is adopted to obtain the instantaneous angle information of PoC as $\theta_{PoC}(k)$. The detailed diagram and the expression of the SOGI-PLL are shown in Fig. 5 and (2)–(4), respectively

$$V_{PoC(\alpha),f} = \frac{\varepsilon\omega_{SOGI}s}{s^2+\varepsilon\omega_{SOGI}s+(\omega_{SOGI})^2}V_{PoC(\alpha)} \tag{2}$$

$$\overset{*}{V}_{PoC(\alpha),f} = \frac{\varepsilon(\omega_{SOGI})^2}{s^2+\varepsilon\omega_{SOGI}s+(\omega_{SOGI})^2}V_{PoC(\alpha)} \tag{3}$$

$$\begin{cases}\omega_{SOGI} = 100\pi - V_{PoC(q),f}\cdot\left(k_{p\_PLL}+\frac{k_{i\_PLL}}{s}\right)\\ \theta_{PoC} = \frac{1}{s}\cdot\omega_{SOGI}\end{cases} \tag{4}$$

where ω_{SOGI} is the center angular frequency of SOGI, ε is the damping coefficient of PLL, $V_{PoC(\alpha),f}$ is the fundamental frequency component of $V_{PoC(\alpha)}$, $\overset{*}{V}_{PoC(\alpha),f}$ is the conjugated component of $V_{PoC(\alpha),f}$, and $V_{PoC(q),f}(k)$ is the q-axis components of $V_{PoC,f}(k)$. k_{P_PLL} and k_{i_PLL} are the coefficient of PI controller in PLL.

Meanwhile, the difference $\Delta\theta(k)$ between PCC voltage and PoC voltage phase angles are determined according to the phasor diagram, as shown in Fig. 6, where the phasor of PoC voltage $\vec{V}_{PoC}(k) = E_{PoC}(k)\angle 0^\circ$ is align to the horizontal direction, $\vec{I}_L(k)$ is the DG output current, $\Delta\vec{V}(k)$ denotes the voltage drops on the feeder of the converter, and R_F, X_F are the feeder resistance and reactance, respectively.

The relationship of the phasor diagram in Fig. 6 can be further descripted by the following equations as:

$$\begin{cases}P^{\text{ref}}(k) - j\cdot Q^{\text{ref}}(k) = \overrightarrow{I}_L(k)\cdot\overrightarrow{V}_{PoC}(k)\\ \Delta\overrightarrow{V}(k) = \overrightarrow{I}_L(k)\cdot(R_F+jX_F)\\ \overrightarrow{V}_{PCC}(k) = \overrightarrow{V}_{PoC}(k) - \Delta\overrightarrow{V}(k).\end{cases} \tag{5}$$

Note that it is assumed the power tracking is accurate at the steady-state operation. Accordingly, the reference real and reactive power $P^{\text{ref}}(k)$ and $Q^{\text{ref}}(k)$ is adopted to replace the actual output power in the power flow analysis.

With the equation in (5) and when the feeder impedance is pre-determined, the angle difference $\Delta\theta(k)$ between PCC and

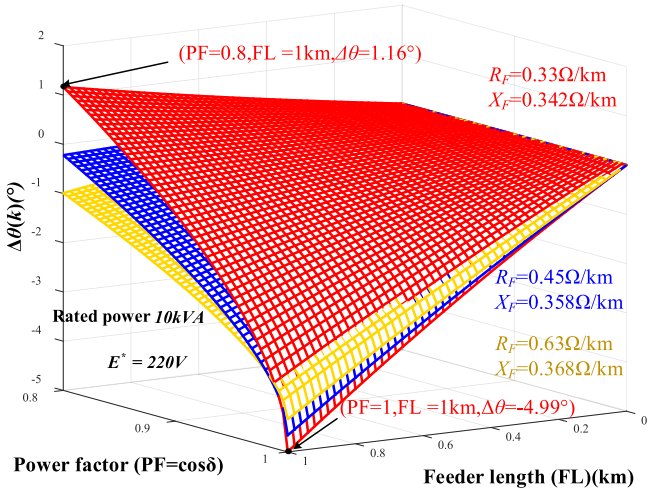

Fig. 7. Voltage angle difference $\Delta\theta(k)$ versus feeder length and converter PF.

PoC voltages can be easily derived in (6) as

$$\Delta\theta(k) = \tan^{-1}\left[\frac{\mathrm{Im}(\overrightarrow{V}_{PCC}(k))}{\mathrm{Re}(\overrightarrow{V}_{PCC}(k))}\right] = \tan^{-1}\left[\frac{Q^{\mathrm{ref}}(k)R_F - P^{\mathrm{ref}}(k)X_F}{E^2{}_{PoC}(k) - P^{\mathrm{ref}}(k)R_F - Q^{\mathrm{ref}}(k)X_F}\right]. \quad (6)$$

Then, the estimated PCC voltage phase angle $\tilde{\theta}_{PCC}(k)$ is given as

$$\tilde{\theta}_{PCC}(k) = \theta_{PoC}(k) + \Delta\theta(k). \quad (7)$$

For a three-phase converter operating at 10 kVA/400 V rated power, the variations of angle difference $\Delta\theta(k)$ are presented in Fig. 7 considering the variations of different converter power factor (PF) and feeder length (FL). It can be clearly seen that for a system with feeder parameters as $R_F = 0.33\,\Omega/\mathrm{km}$ and $X_F = 0.342\,\Omega/\mathrm{km}$, the angle difference can be up to -4.99° degree when the converter PF is at 1.0 and feeder length is 1.0 km. This further confirms that the feeder voltage drops must be taken into consideration during the detection of PCC voltage angle.

It is also necessary to note that even when the system is oversampled at a relatively high rate at 20 kHz, it is not possible to directly get the exact time instant of PCC voltage angle zero crossing by using only the discretized data. Alternatively, a threshold is added and when the absolute value of $\tilde{\theta}_{PCC}(k)$ is fall into this range, a PCC voltage angle zero crossing flag is set up. For this system with 20 kHz sampling frequency, the grid voltage with 50 Hz fundamental frequency is measured 400 times in a fundamental cycle. That means the detected grid voltage angle difference $(\Delta\theta_{PCC})$ between adjacent sampling points is around

$$\Delta\theta_{PCC} = \frac{360^\circ}{f_{\mathrm{sampling}}/f_0} = 0.9^\circ \quad (8)$$

where f_{sampling} is the sampling frequency, f_0 is the fundamental grid frequency. Then, the upper and lower threshold difference can be set to be equal to the angle difference as $[-0.45^\circ, 0.45^\circ]$ during the system steady-state operation. This

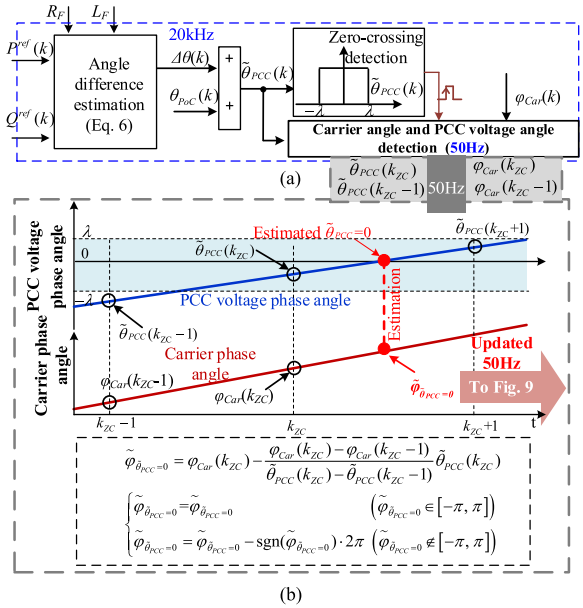

Fig. 8. PCC voltage phase angle zero crossing detection and relative carrier phase angle detection. (a) PCC voltage zero crossing trigger. (b) Carrier phase angle estimation.

means the detected discrete grid voltage phase angle can always fall into this range once in every fundamental cycle, to trigger the carrier angle and PCC voltage angle detection. However, considering that the detected grid voltage phase angle may have some jittering or nonlinearity due to the presence of grid voltage disturbances or the sudden change of DG output power, we have set a wider threshold as $[-0.90^\circ, 0.90^\circ]$.

It is known that a digital triangle carrier is represented by the carrier phase angle (φ_{Car}). When the PCC voltage angle zero crossing triggers the digital carrier phase angle acquiring, φ_{Car} at the beginning of the sampled period $(k = k_{ZC})$ is captured as $\varphi_{\mathrm{Car}}(k_{ZC})$. However, as these values are sampled in a fixed rate at 20 kHz and PCC voltage angle zero crossing trigger is enabled by tolerant band at 0.9 degree, the φ_{Car} at the exact time instant of PCC voltage angle zero crossing cannot be directly obtained. Further considering that the PCC voltage angle–time relationship has good linear property at around zero crossing regions as shown in Fig. 8(b), it is feasible to use a simple linear interpolation to estimate the φ_{Car} at the exact time instant of PCC voltage angle zero crossing as $\tilde{\varphi}_{\tilde{\theta}_{PCC}=0}$

$$\tilde{\varphi}_{\tilde{\theta}_{PCC}=0} = \varphi_{\mathrm{Car}}(k_{ZC}) - \frac{\varphi_{\mathrm{Car}}(k_{ZC}) - \varphi_{\mathrm{Car}}(k_{ZC}-1)}{\tilde{\theta}_{PCC}(k_{ZC}) - \tilde{\theta}_{PCC}(k_{ZC}-1)}\tilde{\theta}_{PCC}(k_{ZC})$$

$$\tilde{\varphi}_{\tilde{\theta}_{PCC}=0} = \begin{cases} \tilde{\varphi}_{\tilde{\theta}_{PCC}=0} & \left(\tilde{\varphi}_{\tilde{\theta}_{PCC}=0} \in [-\pi,\ \pi]\right) \\ \tilde{\varphi}_{\tilde{\theta}_{PCC}=0} - \mathrm{sgn}(\tilde{\varphi}_{\tilde{\theta}_{PCC}=0}) \cdot 2\pi & \left(\tilde{\varphi}_{\tilde{\theta}_{PCC}=0} \notin [-\pi,\ \pi]\right) \end{cases} \quad (9)$$

where sgn is sign function. The output of sgn is 1 when the input is positive number, otherwise it is -1.

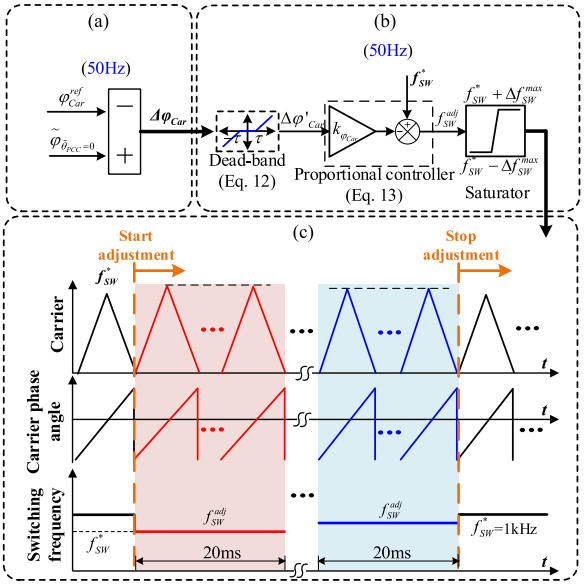

Fig. 9. Illustration of the dynamic carrier adjustment process. (a) Carrier angle difference calculation. (b) Carrier frequency adjustment. (c) Dynamic carrier adjustment.

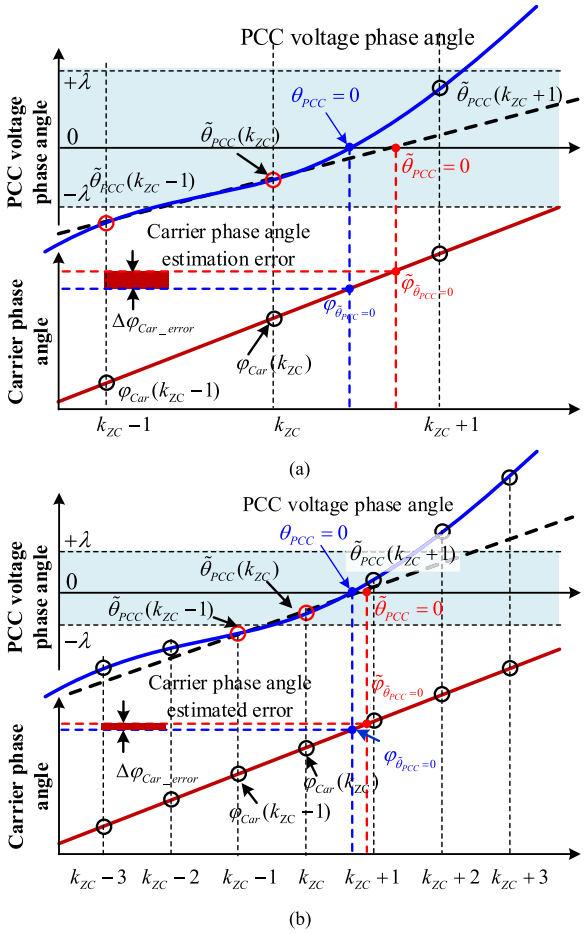

Fig. 10. Performance of extracted PCC voltage phase angle zero crossing detection. (a) Low sampling frequency. (b) High sampling frequency.

C. Adaptive Carrier Adjustment

When the instantaneous angle of digital carrier at the time instant of PCC voltage phase angle zero crossing is estimated, it can be dynamically adjusted until the parallel-converter system achieves proper interleaving PWM regulation. For a system with N parallel connected DG units, the serial number (SN) of DG unit is usually predetermined before the grid integration operation. Then, the reference carrier angle of a DG unit with series number $k(\varphi^{\text{ref}}_{\text{Car},DGk})$ is simply determined as

$$\varphi^{\text{ref}}_{\text{Car},DGk} = \frac{360^\circ \cdot (k-1)}{N}. \tag{10}$$

The detailed demonstration of the proposed carrier angle shifting algorithm is shown in Fig. 9. First, the difference between reference carrier angle $\varphi^{\text{ref}}_{\text{Car}}$ and the actual carrier angle at the time instant of PCC voltage angle zero crossing $\tilde{\varphi}_{\tilde{\theta}_{PCC}=0}$ is defined as

$$\Delta\varphi_{\text{Car}} = \tilde{\varphi}_{\tilde{\theta}_{PCC}=0} - \varphi^{\text{ref}}_{\text{Car}}. \tag{11}$$

To avoid the switching action jittering during the steady-state operating of the system, this angle difference passes through a dead-band as

$$\begin{cases} \Delta\varphi'_{\text{Car}} = 0 & (\Delta\varphi_{\text{Car}} \in [-\tau, \tau]) \\ \Delta\varphi'_{\text{Car}} = \Delta\varphi_{\text{Car}} & (\Delta\varphi_{\text{Car}} \notin [-\tau, \tau]) \end{cases} \tag{12}$$

where τ is the threshold. Then, a simple proportional regulator is adopted to dynamically adjust the switching frequency of the DG unit in the next fundamental cycle as

$$f^{adj}_{SW} = f^{*}_{SW} - k_{\varphi_{\text{Car}}} \cdot \Delta\varphi'_{\text{Car}} \tag{13}$$

where $k_{\varphi_{\text{Car}}}$ is the proportional gain of the carrier frequency regulator, f^{*}_{SW} is the nominal switching frequency, and f^{adj}_{SW} is the adaptive reference carrier frequency. Similarly, to avoid the dramatic change of the converter switching frequency, a saturator as $[f^{*}_{SW} - \Delta f^{\max}_{SW},\ f^{*}_{SW} + \Delta f^{\max}_{SW}]$ is placed at the output of the regulator in Fig. 9. With the abovementioned dynamic switching frequency adjustment approach, the relative phase angles of parallel DG units' carriers can be slowly tuned until they are properly interleaved.

D. Impact of Grid Disturbance and Feeder Impedance Uncertainty

From the previous discussion, it can be seen that the accuracy of PCC voltage phase angle zero crossing detection is affected by a few factors, such as measurement noises, analog to digital converter accuracy, feeder impedance estimation. Among them, the disturbances from the main grid and the uncertainty of feeder impedance usually have the most influential impacts. In the following of this subsection, these two factors are analyzed.

First, the accuracy of carrier angle estimation is less affected by low sampling frequency during the system steady-state operation, as both the digital carrier phase angle and estimated PCC voltage phase angle change linearly versus time. However, when the grid voltage has transient disturbances, using a relatively high sampling frequency could definitely help to improve the accuracy of the PCC voltage phase angle detection.

TABLE I
PARAMETERS OF THE EXPERIMENTAL SYSTEM

Circuitry parameters	Value
DG rated power	10kVA
Rated voltage (V_{PCC})	RMS:50V/50Hz
DC link voltage (V_{dc})	200V
Output filter inductance (L_f)	1.5mH
Grid capacitance (C_g)	120μF
Feeder impedance (R_F and L_F)	$R_{F,DG1} = 0.1\Omega$ $L_{F,DG1} = 0.15$mH $R_{F,DG2} = 0.1\Omega$ $L_{F,DG2} = 0.3$mH $R_{F,DG3} = 0.2\Omega$ $L_{F,DG3} = 0.15$mH
IGBT dead-time	3μs
Control parameters	**Value**
Digital counter frequency f_{clock}	75MHz
Sampling frequency $f_{sampling}$	20kHz
Nominal switching frequency f_{SW}^{*}	1kHz
$\tilde{\theta}_{PCC}$ zero-crossing threshold $[-\lambda, \lambda]$	$[-0.9^{\circ}, 0.9^{\circ}]$
k_{p_cur}	2V/A
k_{i_cur}	10V/(A · s)
ω_0	100πrad/s
ω_{SOGI}	100πrad/s
SOGI damping coefficient ε	2
k_{p_PLL}	180rad/(V · s)
k_{i_PLL}	3200rad/(V · s^2)
$\Delta\varphi_{Car}$ dead-band $[-\tau, \tau]$	$[-3.6^{\circ}, 3.6^{\circ}]$

To validate the above discussion, the diagram of digital carrier angle detection with different sampling frequencies is shown in Fig. 10, where the PCC voltage phase angle is a nonlinear curve due to disturbances. The proposed method utilizes the estimated PCC voltage phase angle $[\tilde{\theta}_{PCC}(k_{ZC}-1)$ and $\tilde{\theta}_{PCC}(k_{ZC})]$ and the measured carrier angle $(\varphi_{\mathrm{Car}}(k_{ZC}-1)$ and $\varphi_{\mathrm{Car}}(k_{ZC}))$ at $k_{ZC}-1$th and k_{ZC}th sampling points to estimate carrier angle $(\tilde{\varphi}_{\tilde{\theta}_{PCC}=0})$ at the exact time of PCC voltage phase angle zero crossing $(\tilde{\theta}_{PCC}=0)$. It can be clearly seen from Fig. 10(b) that the error of carrier angle estimation $(\Delta\varphi_{\mathrm{Car\_error}})$ becomes smaller with higher sampling frequency. Considering the primary application of the proposed approach is parallel grid-tied high power converters, where relatively low switching frequency but high sampling frequency is already available. In this case, it can be concluded that the performance of the system can be less affected by the grid disturbances.

On the other hand, the accuracy of feeder voltage drop calculation is more relevant to the detection of feeder impedance. This can be realized through offline approach by using the information from the variation of PQ flow in [29] and [30], the online method using the noncharacteristic harmonic ripple injection [31 and 32], and the hybrid approach [33]. As indicated in the previous study [29]–[33], the error of feeder impedance estimation is typically less than 10%.

For a DG unit with the parameters as shown in Table I; and with 10% and 20% feeder impedance detection errors, the difference between the estimated PCC voltage phase angle $\tilde{\theta}_{PCC}$ and the real PCC voltage phase angle θ_{PCC} are shown in Fig. 11(a), the difference between the carrier phase angle $\tilde{\varphi}_{\tilde{\theta}_{PCC}=0}$ and the reference carrier angle $\varphi_{\mathrm{Car}}^{\mathrm{ref}}$ is shown in Fig. 11(b). It can be easily seen that the error of phase angle increases when the DG unit is delivering more real power to the grid. Specifically, for the DG with 10% feeder impedance error, the error of estimated PCC voltage phase angle is no more than 0.04° even when the DG unit works at rated output real power condition.

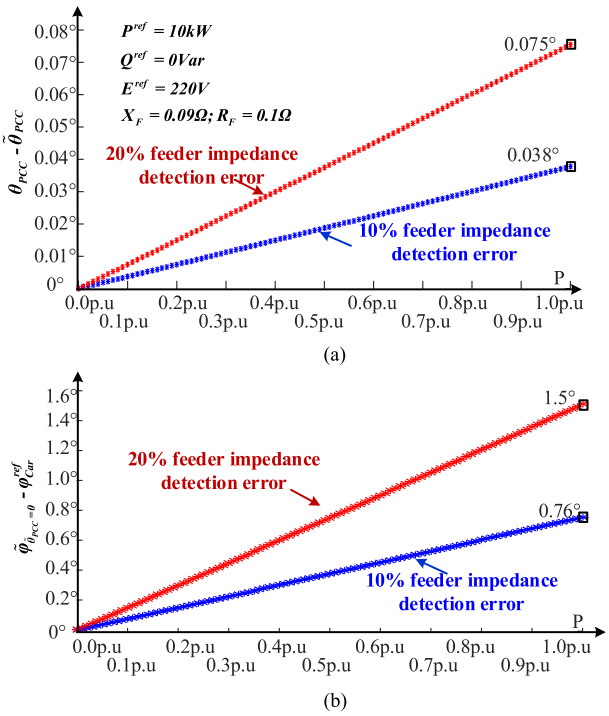

Fig. 11. PCC angle and carrier angle difference under the case of different converter output power.

IV. VERIFICATION RESULTS

Experimental results are obtained from a scale-down laboratory test-rig with three DGs at the same rated power. The configuration of the system can be seen from Fig. 12. In this test-rig, the three-phase main grid is emulated by a programmable source. Each three-phase converter is controlled by a DSP+FPGA-based processor, where a DSP TMS320F28335 from Texas Instruments are adopted to carry out the closed-loop control algorithm and an FPGA EP4CE10E22A7 from Altera is mainly responsible for generating the adaptive carrier and the gating signals. In order to demonstrate the practical situation of high power converters, three converters are controlled with low nominal switching frequency f_{SW} at 1 kHz but moderate sampling frequency f_{sampling} at 20 kHz is adopted. In addition, the internal control variables are displayed by using a high-speed digital to analog converter (DAC) AD5348BRU at 20 kHz refreshing rate. The detailed key circuitry and control parameters are shown in Table I.

First, the dynamic performance of the system from identical digital carriers to interleaved carriers is shown in Fig. 13, where the sum of the DG currents $(I_{\mathrm{sum}(a)})$ and the PCC voltage $(V_{PCC(a)})$ are shown in Fig. 13(a) and (b), respectively. It is seen

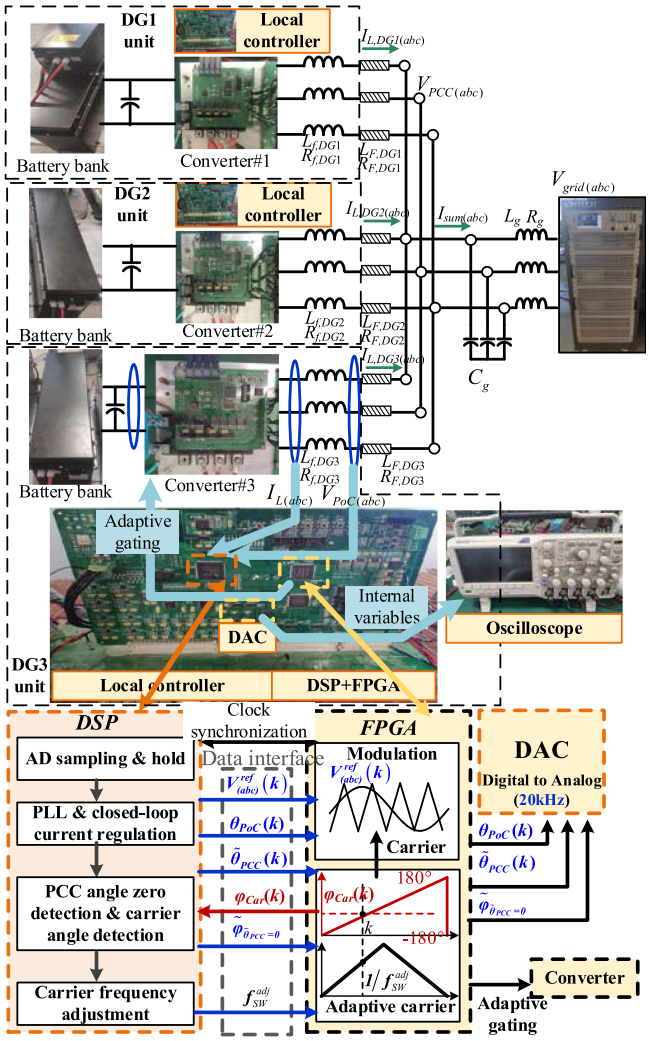

Fig. 12. Illustration of the experimental system and the role of controller.

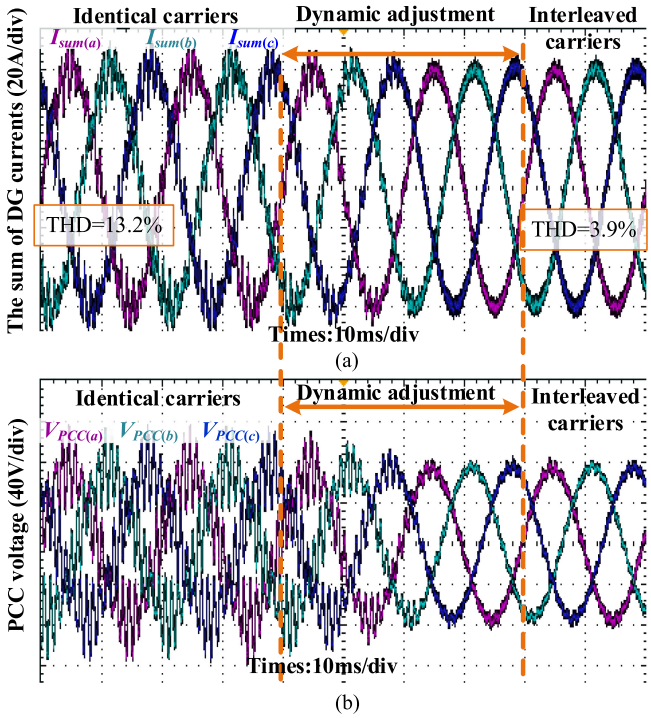

Fig. 13. Dynamic performance of DG output currents and PCC voltage from identical and interleaving carrier operation. (a) Dynamic performance of the sum of DG currents. (b) Dynamic performance of PCC voltage.

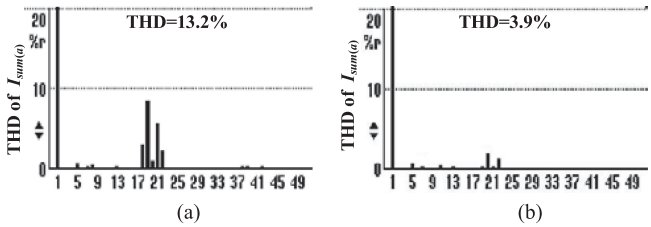

Fig. 14. Comparative $I_{\mathrm{sum}(a)}$ harmonic spectra. (a) Identical carrier control. (b) Interleaved carrier control.

from Fig. 13(a) that $I_{\mathrm{sum}(a)}$ has significant switching ripples when DG carriers are controlled to be identical but it becomes highly smooth and sinusoidal when the proposed interleaving PWM approach is applied to the parallel DG units. Meanwhile, as the switching ripple current at PCC is mitigated using the proposed decentralized interleaving PWM approach, it is seen from Fig. 13(b) that PCC voltage ripples are also suppressed in the end of the process.

In order to obtain a better understanding of the proposed approach, the harmonic spectra of $I_{\mathrm{sum}(a)}$ are shown in Fig. 14, where it is noticed that $I_{\mathrm{sum}(a)}$ has 13.2% THD and the dominated harmonic components are mainly at 19th and 21st order harmonic frequencies when using the modulation approach with identical carriers. As expected, the THD of $I_{\mathrm{sum}(a)}$ significantly reduces to only 3.9% by using the proposed interleaving PWM approach.

It is necessary to note that demonstrating digital carriers at very high refreshing rate in a real time manner is difficult. Alternatively, the carrier angles $\tilde{\varphi}_{\tilde{\theta}_{PCC}=0}$ of DG units at the time instant of each PCC voltage phase angle zero crossing are captured, as shown in Fig. 15. The demonstrated signals in Fig. 15 are produced by the DACs with 20 kHz refreshing rate. From this figure, it is clearly seen that the carrier angles are almost identical at the beginning of the experiment. When the interleaving PWM control is activated, the carrier angles rapidly drift away and they become proper interleaved in around two fundamental cycles after the starting of the proposed modulation.

The detailed performances of three DG units in different modulation modes are shown in Figs. 16 and 17. First, Fig. 16 shows the performance of the system when the identical carriers are adopted for all DG units. It is seen from Fig. 16(a) that both the PCC voltage and PoC voltages of DG units have significant switching ripples. In addition, the output currents $(I_{L(a)})$ of DG units and the sum of the output currents $(I_{\mathrm{sum}(a)})$ are shown in Fig. 16(b), where it is seen that all DG units have rich switching ripple components with similar phase angle, and accordingly, the sum of the DG output currents is also highly distorted. Finally, the output voltages of three DG units are presented in Fig. 16(c). As seen, the central locations of DG unit voltage pulses are

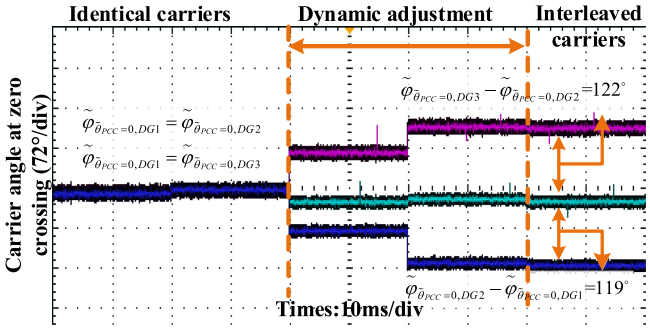

Fig. 15. Dynamic performance of carrier angle $\tilde{\varphi}_{\tilde{\theta}_{PCC}=0}$.

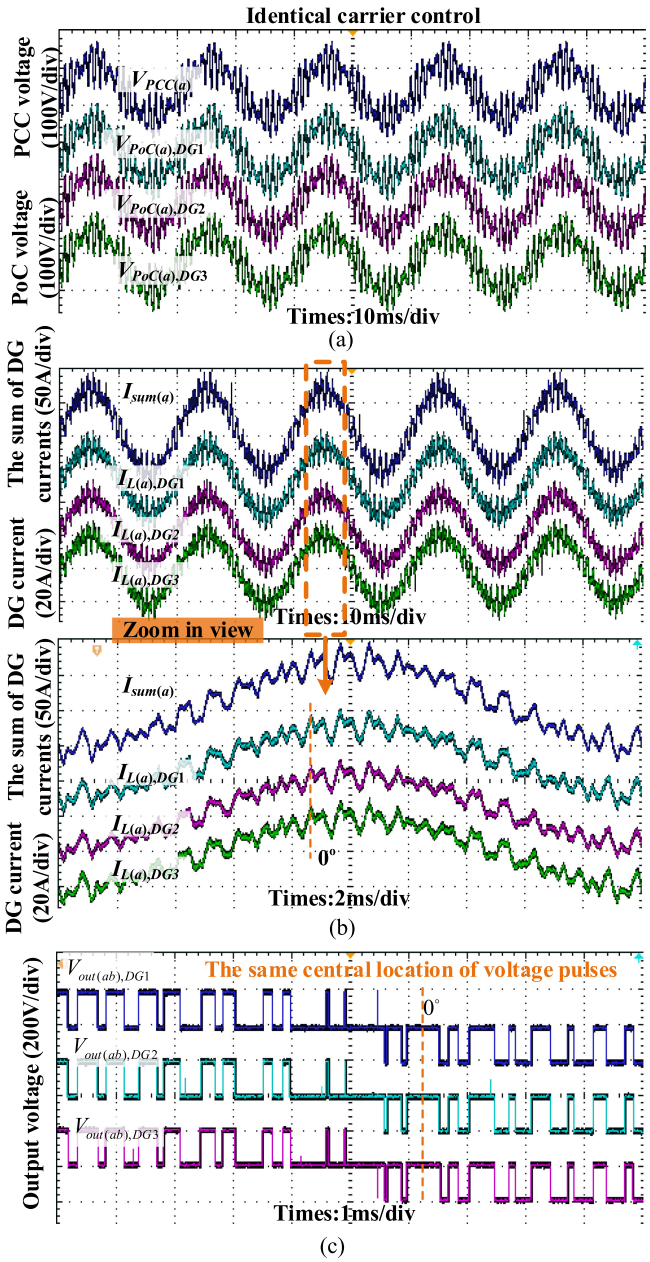

Fig. 16. Performance of the system with identical carriers. (a) Voltage performance. (b) Current performance. (c) Output voltage performance.

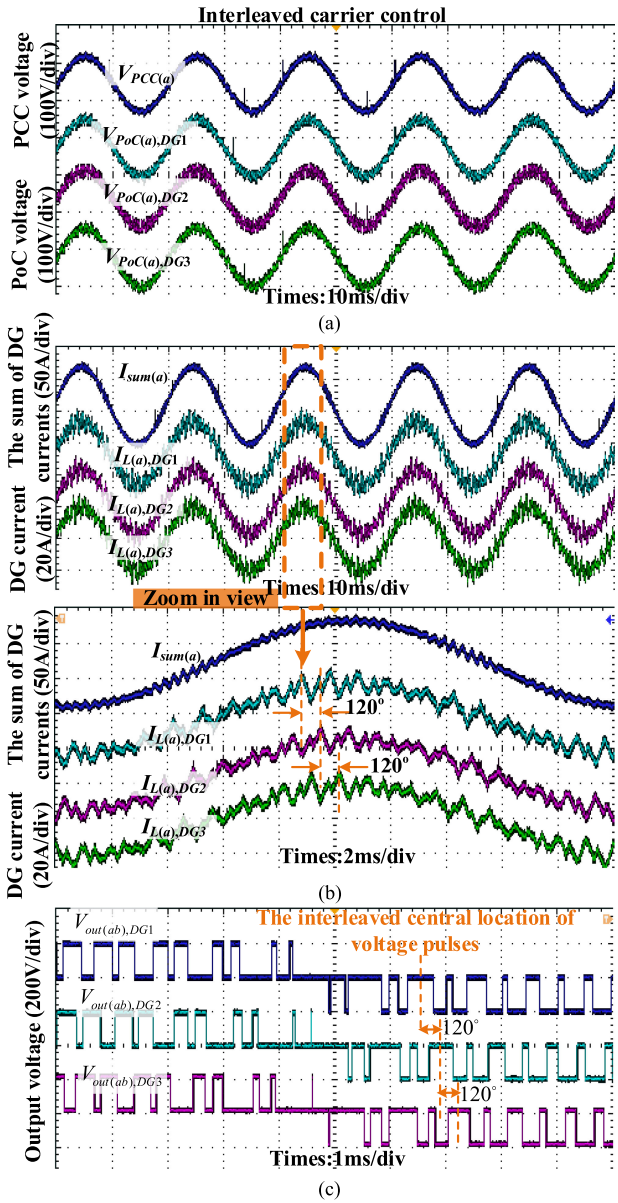

Fig. 17. Performance of the system with interleaved carriers. (a) Voltage performance. (b) Current performance. (c) Output voltage performance.

almost the same, indicating an identical carrier for all DG units in this operation condition.

Similarly, the comparative performance of the system using the proposed interleaving PWM control is obtained in Fig. 17. In this case, due to the cancellation of dominated DG output current switching ripples at PCC, it is seen from Fig. 17(a) and (b) that the PCC voltage, PoC voltages of three DG units, and the sum of the DG output currents $I_{\mathrm{sum}(a)}$ all become highly smooth and sinusoidal. Nevertheless, the ripples of the DG unit output currents ($I_{L(a),DG1}$, $I_{L(a),DG2}$, and $I_{L(a),DG3}$), as shown in Fig. 17(b) are similar to the counterparts in Fig. 16(b). This further demonstrates that the interleaving PWM control mainly reduces the sum of the output current ripples at PCC, while the output current of each DG is roughly unchanged. Finally, it can

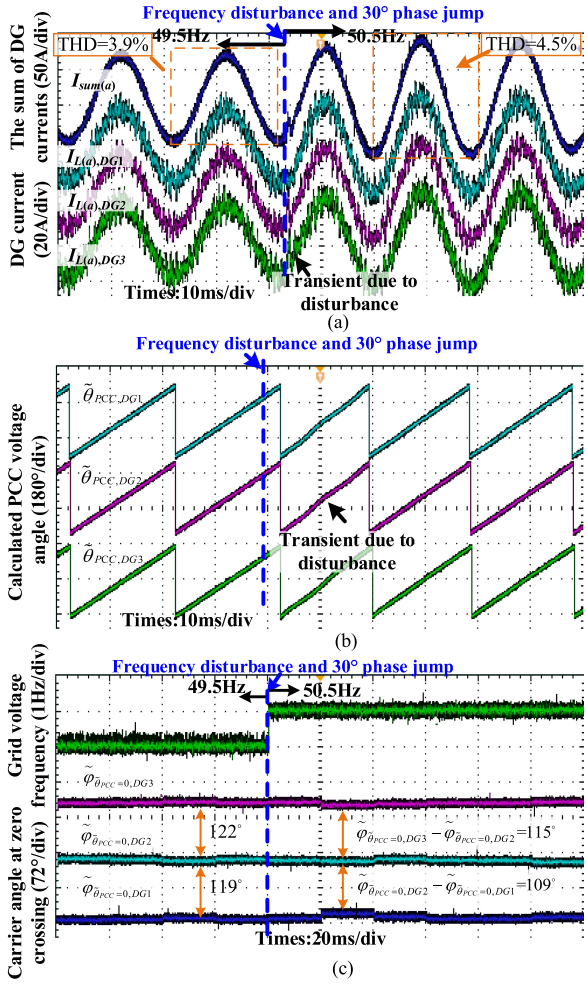

Fig. 18. Performance of the system with grid voltage frequency jump from 49.5 to 50.5 Hz and 30° phase jump. (a) Current performance under disturbance. (b) Calculated PCC voltage phase angle from three DGs. (c) Relative carrier phase angle relationships.

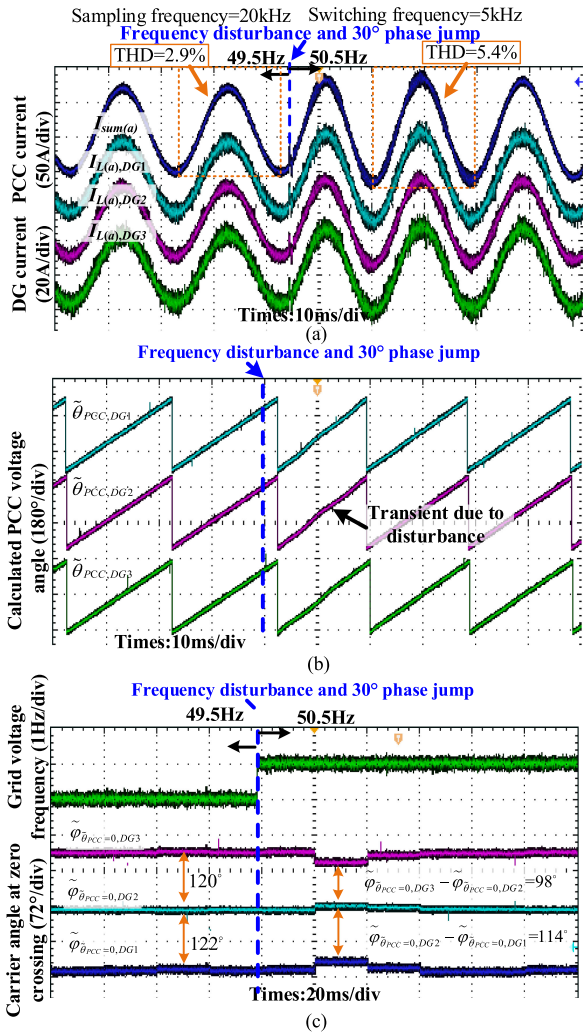

Fig. 19. Performance of the system with 5 kHz switching frequency and fixed 20 kHz sampling frequency. (a) Current performance under disturbance. (b) Calculated PCC voltage phase angle from three DGs. (c) Relative carrier phase angle relationships.

be further noticed from Fig. 17(c) that the central locations of DG unit voltage pulses have notable displacement, due to the implementation of the proposed interleaving PWM approach.

The performance of the system during grid voltage disturbances is also investigated. In this test, the grid voltage frequency has a sudden jump from 49.to 50.5 Hz. In addition, the grid voltage phase angle has 30° jump in order to emulate an adverse situation. First, the response of the sum of the output currents $(I_{\mathrm{sum}(a)})$ and DG unit output currents $(I_{L(a)})$ are shown in Fig. 18(a), where it is seen that all currents have minor disturbance at the beginning of the grid voltage disturbance. Accordingly, the THD of $I_{\mathrm{sum}(a)}$ increases from 3.9% (before the grid disturbance) to 4.5% (for one cycle after the disturbance).

During this grid voltage disturbance, the estimated PCC voltage phase angles from three DG units are all presented in Fig. 18(b). Note that 10% feeder impedance estimation errors are considered for the calculation of PCC voltage phase angle. It is clearly seen that the three DG units have similar estimated PCC voltage phase angles in the entire process. This means the grid voltage disturbances only have minor impact of the phase angle estimation.

In addition, the carrier angles $\tilde{\varphi}_{\tilde{\theta}_{PCC}=0}$ at each estimated PCC voltage phase angle zero crossing are obtained as shown in Fig. 18(c), where it is seen that the carrier angle differences are fixed to around 120° at the steady-state but it has minor fluctuations to around 115° and 109°, respectively, at the beginning of the transient.

The primary application of the proposed approach is the high power parallel grid-tied converters with relatively low switching frequency. However, it is necessary to note that the proposed approach can be applied to medium power rating converters with higher switching frequency in a similar manner. To validate this, another test with 5 kHz switching frequency but fixed 20 kHz sampling frequency is carried out as shown from Fig. 19(a)–(c). In this test, the grid also has a disturbance and it is also seen that the sum of the output currents changes from 2.9% THD at the steady-state to 5.4% THD during the transient. Similarly, it is seen that the estimated PCC voltage phase angle

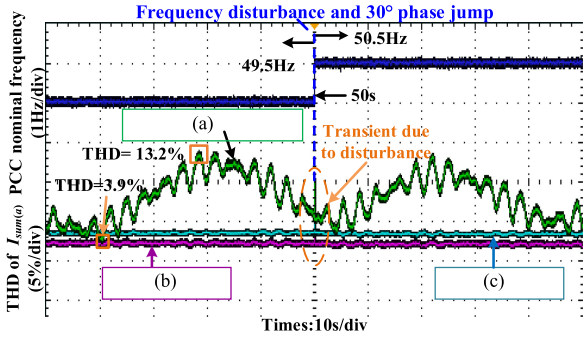

Fig. 20. Long time-scale grid current THD performance. (a) Fluctuating THD. (b) THD = 3.9% (c) THD = 5.6%.

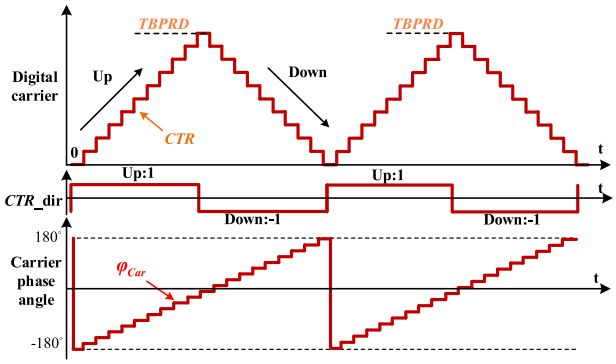

Fig. 21. Diagram of digital carrier and carrier angle.

and the carrier angle displacement feature notices disturbances during the transient. From the above comparative discussion in Figs. 18 and 19, it can be simply concluded that relatively high sampling/switching ratio is preferred for the implementation of the proposed method. However, the approach has certain tolerance to grid voltage disturbance even with relatively low sampling/switching ratio at five.

Finally, the long time scale performances of the system using different modulation approaches are compared in Fig. 20. In this test, the grid voltage frequency is fixed to 49.5 Hz at the beginning but it increases to 50.5 Hz and with additional 30° phase jump at 50 s, as shown in the top of the Fig. 20. It is clearly seen that THD profile using independent regulation of each converter has a slow fluctuation of THD ranging from 3.9% to 13.2%. This is mainly caused by unknown crystal oscillator frequency deviation at each converter local processor. On the other hand, when the proposed method is adopted but the PoC voltage is assumed to be the same as the PCC voltage, it is seen that the THD profile is mainly fixed to 5.6%. Finally, when the feeder voltage drops are considered in the detection of PCC voltage phase angle zero crossing, the THD of the sum of the DG currents further reduces to only 3.9% by using the proposed modulation approach. It is interesting to find that the sudden changes of grid voltage frequency and phase angle have no obvious impact to the long time-scale THD performance, regardless of the modulation approach being adopted.

V. Conclusion

A decentralized modulation approach is developed to realize the switching ripple current mitigation of parallel high power grid-tied DG units. The PCC voltage phase angle is estimated via an oversampled DG unit PoC voltage and proper estimation of feeder voltage drops. Then, PCC voltage phase angle is utilized as an inherent synchronizer to identify the digital carrier angle information of each DG unit. Afterwards, a simple carrier angle adjustment approach is adopted to dynamically change each converter carrier frequency until proper interleaved carriers are achieved. By using this proposed method, an interleaving PWM modulation of parallel grid-tied converters can be easily achieved without any additional hardware costs or communications.

Comprehensive analysis and experiments have been carried out to validate the sensitivity of the proposed approach to various factors including grid voltage disturbance, feeder impedance estimation errors, and the variable sampling/switching ratios. It is suggested that the proposed approach is more suitable for parallel-connected high power converters where the scenario of low switching frequency and oversampling of voltage and current is already available.

Appendix

In this article, the digital carrier is represented by the carrier angle φ_{Car}. For a repetitive "up-and-down" digital carrier, as shown in Fig. 21, it represented by a few registers [28]: 1) TBPRD is the period register. For a 75 MHz digital counter, TBPRD is determined as $\mathrm{TBPRD} = (75\ \mathrm{MHz}/2 \cdot f_{sw})$; 2) CTR is the carrier register at the present time instant and it is always in between 0 to TBPRD; 3) CTR_dir is the carrier direction register. When the digital counter is up mode, CTR_dir is 1. Otherwise, CTR_dir is -1.

Then, the carrier angle and the digital carrier registers relationship can be easily given as:

$$\varphi_{\mathrm{Car}} = 180^{\circ} \cdot \left(\frac{\mathrm{CTR} \cdot \mathrm{CTR\_dir}}{\mathrm{TBPRD}} - 1 \right) \tag{A1}$$

$$\begin{cases} \mathrm{CTR\_dir} = -\mathrm{sgn}(\varphi_{\mathrm{Car}}) \\ \mathrm{TBPRD} = f_{\mathrm{clock}} / \left(2 \cdot f_{SW}\right) \\ \mathrm{CTR} = \mathrm{TBPRD} \cdot \left(1 - \mathrm{sgn}(\varphi_{\mathrm{Car}}) \cdot \frac{\varphi_{\mathrm{Car}}}{180^{\circ}}\right). \end{cases} \tag{A2}$$

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